

Active Electrodes for Wearable EEG Acquisition: Review and Electronics Design Methodology

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Abstract—Active Electrodes (AE), i.e. electrodes with built-in readout circuitry, are increasingly being implemented in wearable healthcare and lifestyle applications due to AE’s robustness to environmental interference. An AE locally amplifies and buffers μ V-level EEG signals before driving any cabling. The low output impedance of an AE mitigates cable motion artifacts thus enabling the use of high-impedance dry electrodes for greater user comfort. However, developing a wearable EEG system, with medical grade signal quality on noise, electrode offset tolerance, common-mode rejection ratio (CMRR), input impedance and power dissipation, remains a challenging task. This paper reviews state-of-the-art bio-amplifier architectures and low-power analog circuits design techniques intended for wearable EEG acquisition, with a special focus on AE system interfaced with dry electrodes.

Index Terms—Active electrode, instrumentation amplifier (IA), electroencephalography (EEG), dry electrodes, common-mode rejection ratio (CMRR), brain-computer interface (BCI)

I. INTRODUCTION

Recent advances in biomedical technologies, integrated circuits (ICs), sensors and data analysis techniques have accelerated the development of wearable technology for Tele-health applications. Today, miniature and low-power medical sensors can be easily integrated into various accessories that continuously sense, process and transfer people’s physiological information during their daily life activities. By reducing the need for manual intervention and by lowering the cost, these medical devices are being widely used in personal healthcare and home diagnostics, such as wellness and health monitoring, home rehabilitation, and the early detection of brain disorders [1][2].

Electroencephalography (EEG) is one of the most important methods to monitor the electrical behaviors of the brain and to evaluate brain disorders. In recent years, the growing need for continuous and comfortable brain activities monitoring have promoted the development of wearable EEG devices for both clinical and non-clinical applications [3]-[5], from deep sleep monitoring, epileptic seizure detection, mental state analysis, to

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gaming, sports, and military use. However, a remaining issue of standard EEG devices is their dependence on gel electrodes, e.g. wet electrodes, which can improve reliability and signal integrity at the expense of inconvenience and discomfort. Moreover, gel will eventually dry out, resulting in degraded recording quality and the need for electrode replacement. These drawbacks prevent wet electrodes being used for long-term and continuous EEG monitoring, especially when a large number of electrodes are placed on scalp.

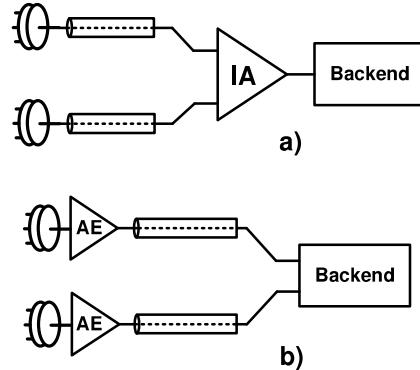


Fig. 1. Simplified block diagram of a) a conventional EEG readout with an instrumentation amplifier (IA); b) active electrode (AE) based EEG readout.

Dry electrodes solve this problem by eliminating the need for gel, which in turn enables a faster setup time and greater user comfort, but the tradeoff is electrode-skin impedance. Typical dry-electrode impedance falls into a range from a few hundreds of $k\Omega$ to a few tens of $M\Omega$ [6] (see details in section II), leading to a significant increase in the noise and interference picked up from the environment.

An electrode with a co-integrated amplifier (Fig. 1), i.e. an *Active Electrode* (AE), reduces noise pickup by minimizing the routing between the electrode and the amplifier. Furthermore, the amplifier’s low output impedance mitigates cable motion artifacts, thus eliminating the use of shielded cables for low cost [7]. On the other hand, an AE based system typically require more wires (e.g. power supply and reference) compared to a conventional EEG readout circuitry, especially when additional functions (e.g. impedance measurement) are integrated in AEs.

This paper reviews and compares the design methodologies of AE-based EEG systems, from electrode-tissue interface (in section II) to the succeeding readout circuitry (in section IV and V), particularly focusing on the specifications (in section III) and design methodologies of the instrumentation amplifier (IA) that forms the core of an AE. Several examples of AE systems are presented (in section VI) to demonstrate appropriate circuits

design techniques can improve overall system performance for high-quality EEG measurement.

II. ELECTRODE-TISSUE INTERFACE

Biopotential electrodes convert ionic physiological signals to electrical signals. As the first component of signal acquisition chain, the characteristics of electrode-tissue interface can be a system performance limiting factor. Practical concerns for electrodes are materials, polarization voltage, electrode-tissue impedance (Fig. 2), and user comfort.

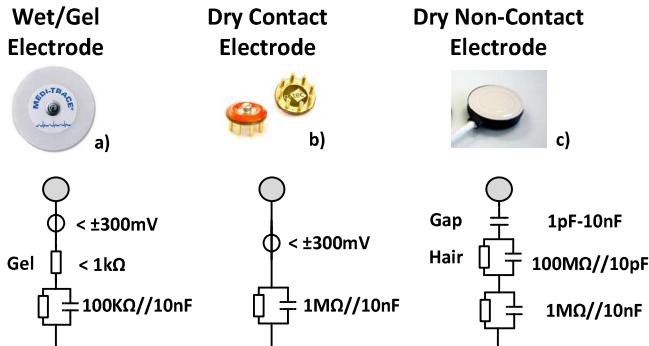


Fig. 2. Equivalent electrical models of different electrode-tissue interfaces. a) Ag/AgCl electrode, b) g.tec's dry electrode, c) QUASAR's capacitive electrode

The concepts and materials of biopotential electrodes highly depend on their applications.

Body surface electrodes for wearables can be grouped into the following categories [8]: metal-plate electrodes (long-term), disposable foam-pad electrodes (low cost), metallic suction electrodes (no strap), floating electrodes (minimize motion artifacts), flexible electrode (comfortable), and internal needle electrode (subdermal). For wearable scalp EEG measurement, flexible metal/polymer electrodes with pins sliding through hair are the most popular form factors for high-quality scalp contact.

Regarding to the electrode materials, gold (Au), platinum, silver chloride (AgCl) and sintered Ag/AgCl are common used. Gold and platinum electrodes are expensive, but are robust and easy to maintain. As polarizable electrodes (capacitive), gold electrodes provide a good signal quality at frequencies above 0.1Hz (not suitable for DC recordings). AgCl and Ag/AgCl electrodes also provide good signals, with lowest polarization voltage of 220mV and low baseline drift of 0.13mV at 25°C. Being non-polarizable (resistive), Ag/AgCl electrodes can be used for DC recordings. Tin or stainless steel is possible but less desired for high-quality EEG recording, because they may suffer from diverse degrees of polarization, baseline drift, low-frequency noise, and high resistance [9].

Electrodes impedance also heavily depends on the electrode materials and concepts. Generally, non-invasive body surface electrodes can be divided into three categories: wet, dry contact and dry non-contact. Typical wet electrodes with Ag/AgCl and hydrogel ensure an easy conversion between ionic current and electron current, resulting in low electrode impedance up to a few kΩ. Dry contact electrodes eliminate the use of gel, at the cost a higher impedance ranging from several hundreds of kΩ [10] up to a few tens of MΩ [11]. Dry non-contact electrodes isolate the electrode and skin by capacitive coupling, but this

leads to even higher electrode impedance and more susceptible to motion artifact. The impedance of dry non-contact electrodes mainly depend on garment hair, the distance of air gap and the surface area of electrodes. In recent years, some new electrode concepts were proposed to reduce the electrode impedance, such as quasi-dry electrodes [12], a concept between “wet” and “dry” electrodes, hydrate the local scalp area by releasing a small amount of moisturizing solution from the electrode reservoir, and achieve impedance in the order of a few tens of kΩ.

Polarization voltage, or half-cell potential, develops across the electrolyte-electrode interface because of the unbalanced distribution of anions and cations [13], while electrode offset is the differential polarization voltage between electrodes, and it depends on the electrochemical unbalance of two electrodes, i.e. materials, temperature and the ion concentration of body fluid, Ag/AgCl electrodes are widely used due to its low polarization.

Regarding to user comfort, dry electrodes implemented with conductive rigid metal pins can penetrate the hair and provide long-term EEG recording but at the cost of discomfort and pain. Silver-coated polymer bristles [14], dry foam electrodes [15], polymer electrodes made of polydimethylsiloxane (PDMS) [16] or polyurethane [17], and comb-shaped polymer electrodes [18] can provide soft contact to the skin while still providing low electrode impedance in the order of 20kΩ to 500kΩ, being promising alternatives for wearable EEG applications.

III. PERFORMANCE CRITERIA OF AE READOUT CIRCUITRY

AE-based wearable EEG systems should be designed to meet the following requirements compliant with medical standards, which impose constraints on the electrical performance of an AE system in terms of its noise, input impedance, electrode offset tolerance, common-mode rejection ratio (CMRR), power dissipation etc. (Table I). The following sections will discuss major specifications and challenges in detail (Fig. 3).

TABLE I: EEG MEDICAL STANDARDS AND PROPOSED SPECIFICATIONS FOR WEARABLE EEG APPLICATIONS

	IEC60601* [19]	IFCN** [20]	Target specifications
Applications	Clinical EEG	Clinical EEG	Wearable EEG
Input voltage range	0.5mV _{pp}	--	1mV _{pp}
Input referred noise (per channel)	6μV _{pp}	0.5μV _{rms} (0.5-100Hz)	1μV _{rms} (0.5-100Hz)
Bandwidth	0.5-50Hz	0.16-70Hz	0.5-100Hz
Electrode offset	±300mV	--	±300mV
Input impedance @50/60 Hz	--	>100MΩ	>100MΩ
CMRR @50/60 Hz	--	110dB	80dB
Power dissipation (per channel)	--	--	100μW
Safe DC current	50uA	--	50uA
Number of wires	--	--	Minimal

*IEC60601: standards for the safety and effectiveness of medical electrical equipment published by the International Electrotechnical Commission.

**IFCN: standards of International Federation of Clinical Neurophysiology.

A. Power Dissipation

Battery size and capacity would be the major determinants of

a wearable system's size. Therefore, the power dissipation of an EEG system is an important design parameter. For example, to realize a 24-hour continuous operation with a typical 3.6V coin cell lithium battery [21], the system must consume an average supply current of less than 5mA.

B. Noise

According to the IEC standard [19], an EEG system should exhibit the maximum input-referred noise of $6\mu\text{V}_{\text{pp}}$ to detect μV -level EEG signals. This nominal peak-to-peak noise can be converted to the root mean square (rms) noise by dividing a factor of 6.6 [22], resulting in an integrated noise of $0.91\mu\text{V}_{\text{rms}}$. As a result, state-of-the-art bio-amplifiers usually target for an input-referred noise of $<1\mu\text{V}_{\text{rms}}$ in a 0.5Hz to 100Hz bandwidth. Furthermore, their $1/f$ noise is typically mitigated by dynamic circuit techniques (see section V.B).

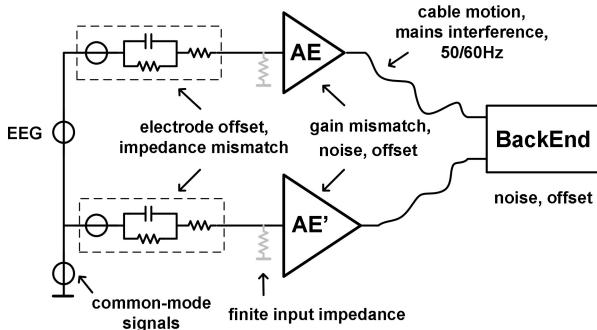


Fig. 3. Illustration of major aggressors of one-channel AE-based readout.

C. Electrode Offset Tolerance

Electrode offset can be as large as a few 100mVs, which can saturate an AE or significantly reduce its dynamic range. Based on the IEC standard [19], a scalp EEG system should be able to accommodate up to $\pm 300\text{mV}$ of electrode offset.

D. Input Impedance

The voltage divider, formed by electrode-tissue impedance (ETI) and the AE's input impedance, reduces the AE's gain. To minimize such a gain attenuation, AEs should have a high input impedance of $>100\text{M}\Omega$ at 50/60Hz [20]. This is especially the case with dry electrodes, whose ETI can be up to a few $\text{M}\Omega$. Moreover, the ETI mismatch between two AEs can lead to a limited systematic CMRR of 50dB-80dB, even if the AEs are perfectly matched.

E. Common Mode Rejection Ratio (CMRR)

To reject common-mode interference, e.g. 50/60Hz from the mains, an amplifier with 110dB CMRR is preferred for clinical applications, otherwise the input common-mode signals will be converted into differential errors, polluting the output visibility and reducing amplifier's output dynamic range. For wearable EEG systems, the CMRR is typically limited by the mismatch of dry electrodes and the finite input impedance of the amplifier, thus the CMRR requirements on amplifiers or AEs are relaxed.

F. Number of Connecting Wires

An often overlooked feature in an AE system is the number of connecting wires. In practice, each AE will be connected to a

backend signal processor via a cable consisting of multiple conductors for power supply and data transport. Minimizing the number of conductors is important to reduce system cost and complexity, especially when tens of AEs are needed in a multi-channel EEG system, or when polygraphic recordings are required for AEs.

IV. AE AMPLIFIER ARCHITECTURES

In an AE-based EEG system, the choice of either a buffer or an *instrumentation amplifier (IA)* is an important architectural decision. This is because the selected architecture has a major impact on the system specifications, e.g. input dynamic range, power budget, noise performance, cabling requirements, etc. This section will discuss the advantages and disadvantages of both architectures.

A. Analog Buffers

An analog buffer, i.e. a voltage follower, is the most popular architecture as an AE because of balanced analog performance, e.g. high input impedance, low output impedance and low gain variation. Furthermore, a buffer only requires 3 wires (V_{dd} , V_{ss} and V_{out}) connected to a backend processor. Novel buffers have been invented towards higher input impedance and fewer wires. In [23], ultra-high input impedance ($60\text{fF}/5\text{T}\Omega$) is achieved via using an impedance bootstrapping technique. In [24], an output current driver enables the buffer's analog output to be shared with negative supply via a single wire, at the cost of $\frac{1}{2}$ output dynamic range (Fig. 4a). A similar principle is presented in [25], where the analog output is combined with the buffer's positive supply; however, to maintain a large output dynamic range, the buffer is powered by a 5V supply voltage (Fig. 4b).

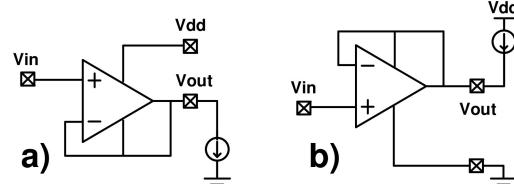


Fig. 4. Two-wire analog buffers, a) current sink driver; b) current source driver.

An analog buffer also facilitates the use of active shielding [26], a well-known technique to reduce the interference coupled to the inner lead wire. Active shielding is realized by driving a shield mesh wrapped around the inner lead wire to insulate biopotential signals from the external interference. The driving signal which is fed back to the shield mesh should be the same as input biopotential signal but in a low-impedance manner. An analog buffer is an ideal solution for low-power active shielding, because its low-impedance output can drive the shield mesh directly.

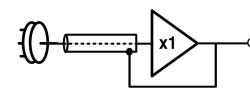


Fig. 5. Active shielding realized by an analog buffer.

B. Inverting Amplifiers

Bio-amplifiers with resistive feedback are rarely used due to the system constraints on noise and component area. However,

AC-coupled inverting amplifiers with capacitive feedback [27] address both issues, thus being widely used in wearable and implantable medical instruments [28][29]. An AE built with a capacitively coupled inverting amplifier [30] is shown in Fig. 6. This AE exhibits balanced analog performance, e.g. low noise of $0.8\mu V_{rms}$, rail-to-rail electrode offset tolerance, low power dissipation of $20\mu W$. To realize a cutoff frequency $<0.5Hz$, a large resistor of a few tens of $G\Omega$ is required. To avoid the need for an external component, an on-chip pseudo-resistor [27] was implemented (see Section III.C), at the cost of nonlinearity and inaccuracy of the resistance.

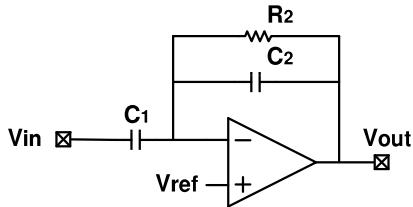


Fig. 6. Capacitively coupled inverting amplifier used as an AE.

The power of a capacitively coupled inverting amplifier can be further reduced by optimizing its core amplifier [31]-[33]. Apart from the general guidelines of low-power amplifiers (see Section V.A), a state-of-the-art bio-amplifier [34] achieves low noise of $0.34\mu V_{rms}$ with only $1.17\mu W$ power, corresponding to a noise-efficiency-factor (NEF) of 1.74. Such a power-efficient design is realized by combining a localized low supply voltage of $0.6V$ together with an inverter-based current reuse technique (see Section V.A).

A remaining challenge of a capacitively coupled amplifier is its parameter tradeoff between input impedance and noise [35], both are related to the input coupling capacitor C_1 .

C. Non-Inverting Amplifiers

Non-inverting amplifiers have higher input impedance than inverting amplifiers, so AEs implemented with non-inverting amplifiers using resistive feedback (Fig. 7a) were proposed in [36][37]. The input resistor (R_1) is a primary noise contributor, and so it is typically in the order of a few $k\Omega$. However, such a low resistance then increases the amplifier's load and power dissipation.

Alternatively, non-inverting amplifiers can utilize capacitive feedback [38] (Fig. 7b) to mitigate resistor noise. This amplifier architecture can tolerate $\pm 300mV$ electrode offset because their DC gain are always unity regardless of AC gain. The residual offset can be compensated with the help of a so-called DC servo loop (DSL), which tracks and attempts to null the output offset by negative feedback (see Section V.C)

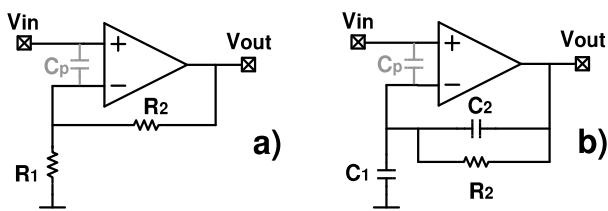


Fig. 7. Non-inverting amplifier, a) resistive feedback; b) capacitive feedback.

D. DC-Coupled Amplifiers

The AC-coupled amplifiers described above not only reject electrode offset, but also block very low frequency signals and induce distortion. AC-coupled amplifiers can therefore not be used to measure slow cortical potentials (SCP) [39], where extremely low frequency ($<1Hz$) surface voltage is monitored for various cognitive tasks (e.g., language) and sensory-motor tasks (e.g., motor preparation and expectation) [40].

A DC-coupled amplifier (Fig. 8) would preserve these low frequency signals, but its gain would be limited by a large dynamic range ($>90dB$) determined by electrode offset and μV EEG signals. In addition, A high-resolution ADC (>16 bit) is typically required to meet the noise specifications [41], leading to significant power dissipation in a multi-channel system [42].

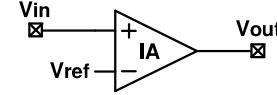


Fig. 8. A general DC-coupled amplifier used as an AE.

A DC-coupled amplifier can be realized with many different architectures, e.g. current balancing amplifiers [43][44], current feedback amplifiers [45][46], three-opamp amplifiers [47], and capacitively coupled chopper amplifiers [35][48]. In case DC measurement is not mandatory, a DC-coupled amplifier can be easily converted into an AC-coupled amplifier by adding a DC servo loop (DSL) (see section V.C).

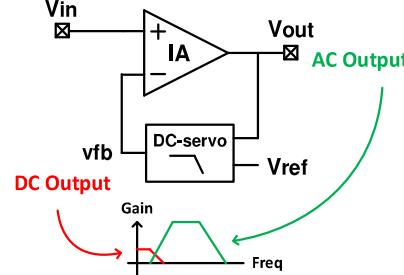


Fig. 9. “Functionally” DC-coupled amplifier with voltage-based feedback.

An alternative DC-coupled amplifier, namely “functionally” DC-coupled amplifier [49][50], can combine the advantages of both AC-coupled and DC-coupled amplifiers, i.e. very large electrode offsets tolerance ($\pm 350mV$) at low power ($<1\mu W$) while still remaining DC-coupled. This is accomplished by utilizing a DC-servo loop based on voltage-to-voltage feedback (Fig. 9), which tracks the offset at the amplifier's output and cancels it by driving the inverting input of the amplifier. As a result, the AC-coupled EEG signals are available at the amplifier's output, while the DC and extremely low frequency signals are available at the output of the DC-servo loop with unity gain. A “functionally” DC-coupled AE can then be made by combining both AC and DC outputs. The reconstructed transfer function is nearly identical to that of a true DC-coupled AE, as the two channels' normalized gain plots have their -3dB points at one frequency (Fig. 10).

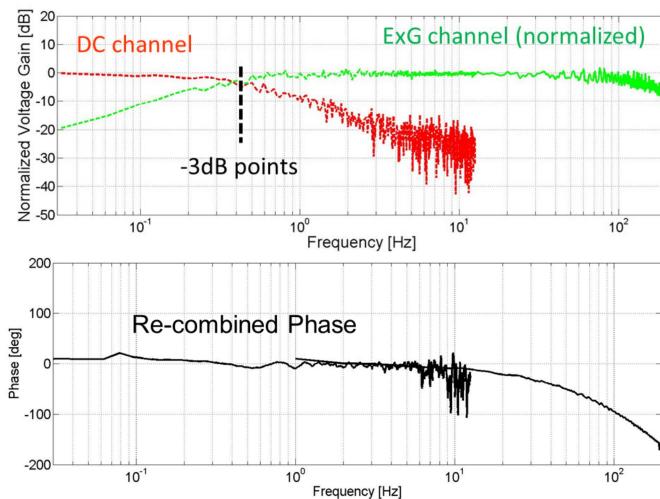


Fig. 10. Normalized gain and phase versus frequency of DC and ExG channels, exhibiting their complementary transfer-function characteristics at -3dB point.

Although the DC servo loops can also be implemented with a voltage-to-current feedback [35][43][48], however, this suffers from a performance tradeoff between electrode offset tolerance and power (see section V.C), which limits the offset tolerance to roughly 50mV.

V. CIRCUIT DESIGN TECHNIQUES

Although numerous amplifier architectures have been used as AEs, they all involve various performance tradeoffs and so no ideal architecture has yet emerged. Zooming in from system level to circuit level, this section reviews various circuit design techniques to improve the AE-specific specifications listed in section III.

A. Power Reduction

At the system level, a major drawback of a buffer-based AE system is its low noise-to-power efficiency. A low-noise buffer is power hungry, and it only performs impedance conversion without providing any voltage gain. As a result, the next stage (Fig. 3) has to overcome the same challenges of noise and electrode offset tolerance, reducing system's power efficiency. Alternatively, to improve the noise-to-power efficiency, an AE can be implemented as an instrumentation amplifier, of which the voltage gain relaxes the noise requirement of the succeeding stage [30]. However, using two amplifiers (as one EEG channel) poses a different challenge in terms of CMRR degradation due to their gain mismatch.

At the circuit level, the AE's noise specification drives the overall power budget. A conventional amplifier has to increase the amount of power to reduce the thermal noise. However, novel circuit techniques can achieve the same target with low power. Current reuse [33], e.g. by using an inverter-based input transistors consisting of series-connected NMOS and PMOS (Fig. 11), doubles the input transconductance without adding any tail current, but at the expense of $\frac{1}{2}$ input dynamic range. State-of-the-art capacitively coupled bio-amplifiers employing similar techniques achieve low noise-efficient factors (NEFs) of 1.74 [34] and 2.1 [51] by further reducing the supply voltage of the first stage (Fig. 11). Both designs exploit the fact that the amplifier's inputs (v_n , v_p) are at virtual ground and so the core

amplifier A1 only needs to have a small input dynamic range.

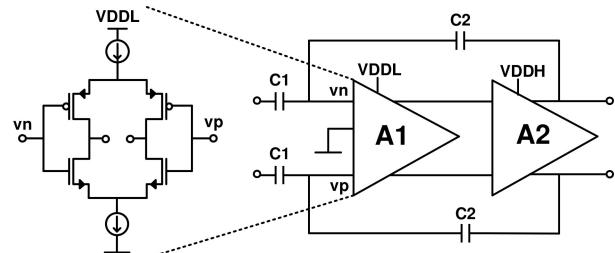


Fig. 11. AC-coupled capacitively coupled IA, where a low supply (VDDL) and current reuse technique are implemented in the first stage A1.

B. Noise Reduction

Apart from thermal noise, $1/f$ noise (flicker noise) is usually the dominant noise source of a bio-amplifier because the noise bandwidth can be a few kHz. Conventionally, $1/f$ noise can be reduced by enlarging the size of the input transistors, but using extremely large transistors not only takes up more space but also reduces input impedance by adding parasitic capacitances.

Alternatively, dynamic circuit techniques can mitigate the amplifier's $1/f$ noise and intrinsic offset in a power- and area-efficient manner. Two well-known dynamic techniques include auto-zeroing (AZ) and chopping (Fig. 12) [52]. AZ operates in two phases. Noise and offset are sampled and stored in the first phase, and so they will be compensated in the second phase. Drawback of AZ is that high frequency noise is folded back and distributed over the bandwidth of $f_s/2$ (Fig. 13a). Chopping operates continuously by periodically swapping the amplifier's inputs, which modulates the $1/f$ noise and offset to a chopping frequency f_c , thus no noise folding exists (Fig. 13b).

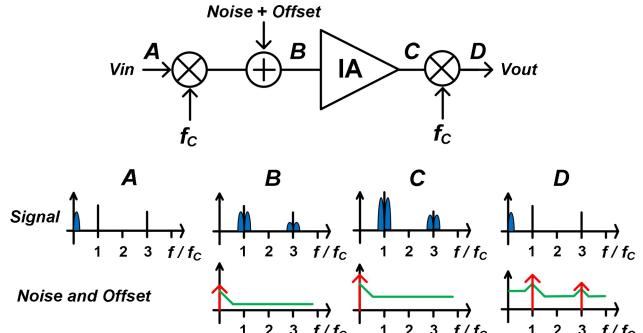


Fig. 12. Chopper modulation to reduce the IA's $1/f$ noise and intrinsic offset.

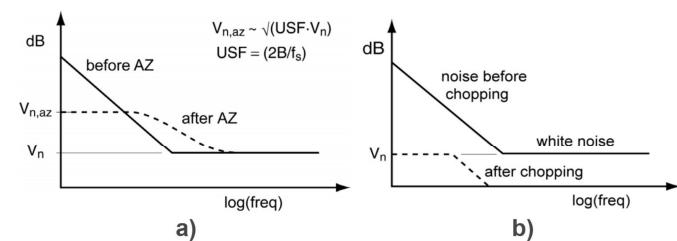


Fig. 13. Illustration of the noise spectrum of a) auto-zeroing; b) chopping.

Choppers have been implemented at different locations of an amplifier. For example, in a capacitively coupled amplifier, an input chopper can be placed before the input coupling capacitor [35][48] (Fig. 14a). However, this chopper scheme effectively realizes a DC-coupled amplifier, which has a limited electrode offset tolerance of only a few tens of mV. In addition, the input

impedance of the chopper amplifier is reduced to the equivalent of a switched-capacitor resistor formed by $2/f_{\text{chop}}C_1$.

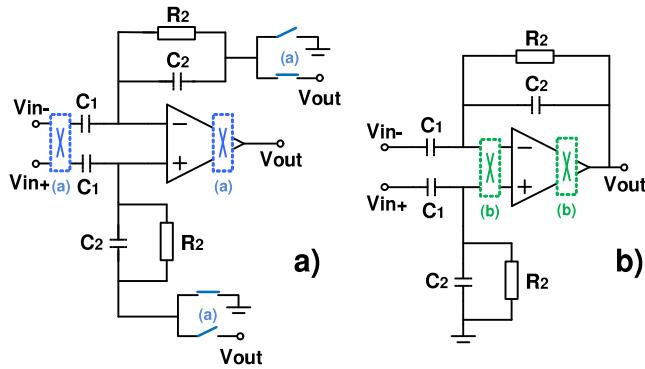


Fig. 14. Capacitively coupled amplifier with alternative chopping schemes, a) chopping before the input capacitors; b) chopping at the virtual ground.

On the other hand, the input chopper can be placed inside the feedback loop [30][54], i.e. at the amplifier's virtual ground (Fig. 14b). This chopper scheme ensures rail-to-rail electrode offset tolerance, but it suffers from $1/f^2$ noise (Fig. 15) due to chopper-induced current noise at a high impedance node [55].

The $1/f^2$ noise has been observed in other chopper amplifier architectures, such as a non-inverting chopper amplifier [38], inverting chopper amplifiers [30][56], and a chopper amplifier equipped with an external floating high-pass filter (HPF) [44]. The common problem of these amplifiers is that chopping was always performed at very high-impedance node (in $\text{G}\Omega$ range).

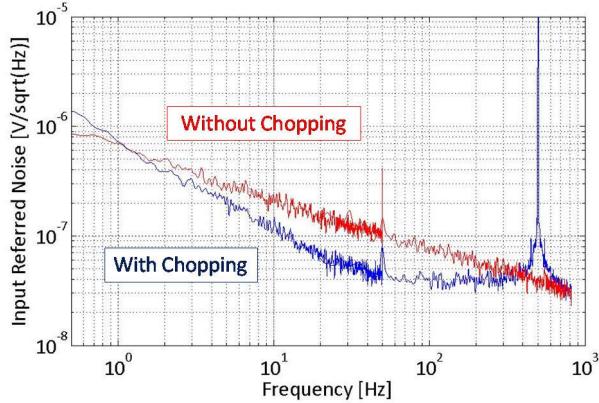


Fig. 15. Measured $1/f^2$ noise of chopping scheme b) depicted in Fig. 14.

Although the $1/f^2$ noise can be reduced by carefully sizing the input chopper switches and by selecting the optimum chopping frequency [55], a simpler solution is to implement the chopping at a relatively low impedance node (in $\text{M}\Omega$ range) [43][49].

C. Electrode Offset Compensation

AC-coupling via capacitor is the most obvious way to enable electrode offset rejection. However, large capacitors of at least a few tens of pF hinder area efficiency. A DC-servo loop (DSL), i.e. a feedback loop with low-pass filter ($<0.5\text{Hz}$) characteristic, can compensate electrode offset as well. A DC-servo loop can be implemented via either a current feedback (Fig. 16a), or a voltage feedback (Fig. 16b).

In current feedback DSLs [35][43][48], the maximum offset tolerance is usually limited ($<50\text{mV}$), it subjects to the amount of compensation currents (I_{dc}) and power. While reducing the

amplifier's input transconductance (i.e. V-I converter in Fig. 16a) would enlarge the offset tolerance, this would compromise the gain and noise.

Voltage feedback DSLs [49][50] can tolerate electrode offset of at least $\pm 300\text{mV}$ while only consuming μV power. However, the noise contribution of the DSL must be minimized since it is directly connected to the amplifier's input.

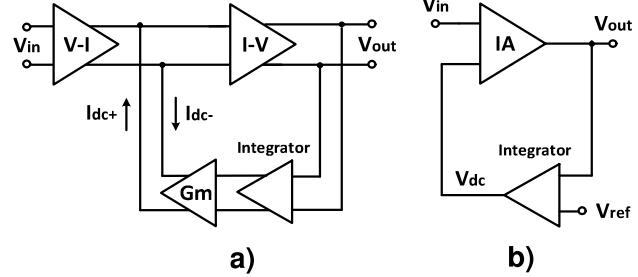


Fig. 16. Generic IA with DSLs, a) current feedback; b) voltage feedback.

A common challenge of a DSL is to implement a sub-Hertz cutoff frequency. State-of-the-art amplifiers emulate an on-chip $\text{G}\Omega$ -range resistor as follows (Fig. 17): a pseudo-resistor [27], a switched-capacitor (SC) resistor [35], and a switched-resistor resistor [57].

A pseudo-resistor exhibits a very large resistance up to tens of $\text{G}\Omega$, determined by the leakage current of a subthreshold metal-oxide-semiconductor field-effect transistor (MOSFET) and a parasitic lateral bipolar junction transistor (BJT) [27]. As a result, a pseudo resistor is area efficient but highly nonlinear due to the variation of process, voltage, and temperature (PVT). In [31], a new pseudo-resistor structure bootstraps its gate bias voltage (Fig. 17a) to improve linearity within a voltage swing of $\pm 0.25\text{V}$.

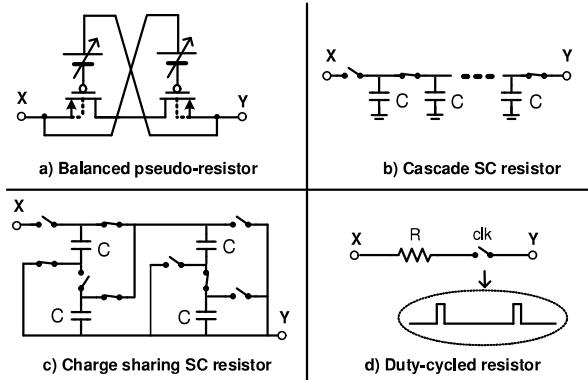


Fig. 17. Different implementations of a $\text{G}\Omega$ -level on-chip resistor.

On the other hand, implementing a large switched-capacitor (SC) resistor ($>50\text{G}\Omega$) is not easy because of the constraints of switching frequency and sampling capacitor. In [35], a cascade SC resistor (Fig. 17b) is implemented by a cascade of multiple small capacitors that are sampled in alternating phases. In [54], another SC resistor, utilizing a series-to-parallel charge sharing scheme (Fig. 17c), improves its resistance by $\times 10$ to maximum $150\text{G}\Omega$.

In [57], a duty-cycled resistor (Fig. 17d) consists a reference resistor and a switch which is closed only for a short duration per clock cycle. Ideally, any resistor value beyond R_{ref} can be realized by adjusting the duty cycle of the switching clock.

Apart from implementing huge resistors, a DSL can also be

made by using large (external) capacitors. For instance, a gm-C integrator was proposed in [43], where a low transconductance is combined with an external capacitor ($1\mu\text{F}$) to implement a sub-Hertz cutoff frequency in low power. The use of external capacitor also ensures a low-impedance chopping facilitating the reduction of $1/f^2$ noise.

In case large external passive components are not desired, a digitally-assisted DSL may work [58][59] (Fig. 18). Low-pass filtering function is realized in digital domain, taking benefits from area- and power-efficiency, and reconfigurable flexibility. Moreover, in digitally-assisted DSL, the DC signal is directly available at DSL's output as a digital output.

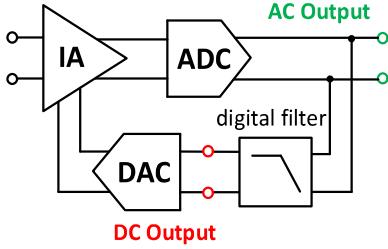


Fig. 18. “Functionally” DC-coupled AE with a digitally-assisted filter.

A DSL can also be implemented with calibration for coarse offset compensation, where a digital-to-analog converter (DAC) periodically compensates electrode offset with digital codes as input. The digital codes controlling the DAC can be generated differently. In [60], a coarse offset compensation was presented, where the amplifier’s output baseline is regulated between two predefined threshold voltages by using a current steer DAC to avoid hard clipping. In [30], the input offset of the amplifier is mostly compensated by a foreground calibration. The current steering DAC, controlled by successive approximation register (SAR) logics, calibrates the offset from 220mV to 20mV in 7 clock cycles. In general, calibrating the offset has the advantage of being low power, since it is only active before the signal acquisition. However, electrode offset is not purely static, the foreground calibration suffers from offset drift.

D. Input Impedance Boosting

AEs require a maximum input impedance to reduce input signal division and the CMRR degradation. At the system level, non-inverting amplifiers would be the first option. At the circuit level, impedance bootstrapping techniques can further increase the input impedance, and this is essential for a non-contact EEG recording [23]. Impedance bootstrapping can be realized in two formats, i.e. current feedback and voltage feedback (Fig. 19), both rely on a proper amount of positive feedback.

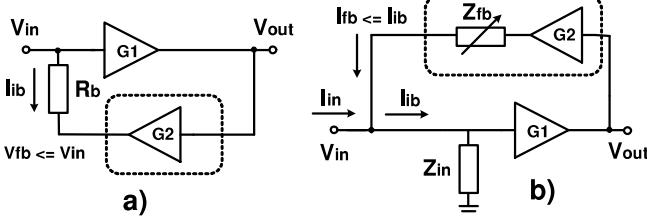


Fig. 19. Impedance boosting via: a) voltage feedback; b) current feedback.

In [23], output signal is fed back to bootstrap the amplifier’s lead bias resistor (Fig. 19a), such a voltage feedback bootstraps the input impedance to infinitely large (if $G_1G_2=1$). In [30][48],

input current is provided by a positive feedback loop (Fig. 19b), ideally also bootstraps the input impedance to infinitely large (if $I_{fb}=I_{ib}$). In both cases, the amount of positive feedback, either current or voltage, must be carefully controlled to maintain the loop stability and maximize the input impedance when parasitic components exist [30] (Fig. 20).

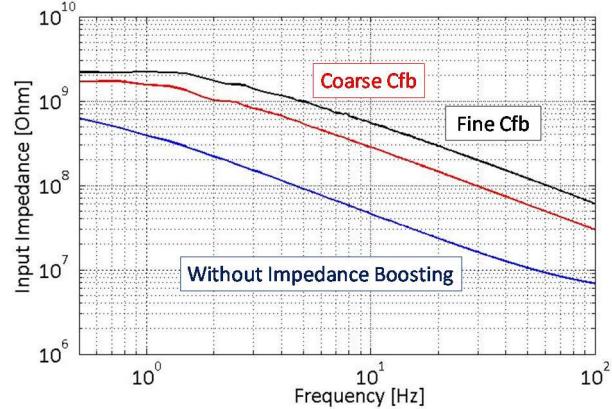


Fig. 20. Measured input impedance of an active electrode [30], the input impedance is increased by tuning the amount of positive feedback (via C_{fb}).

Feedforward technique is another option for input impedance boosting of a chopper amplifier (Fig. 21). In [57][61], a pair of auxiliary buffers pre-charge the input coupling capacitors at the beginning of each chopping phase (clk3 and clk4), maintaining high input impedance. After pre-charging, buffers are removed from signal path and the input choppers starts operating in the rest chopping phase (clk1 and clk2). The feedforward technique reduces average DC current of the signal path and thus boosts the input impedance to $300\text{M}\Omega$ for a wide signal bandwidth of 1Hz-5kHz [57].

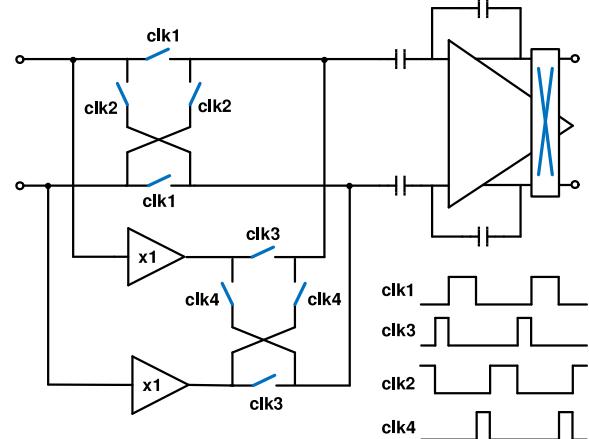


Fig. 21. Capacitively coupled chopper amplifier utilizes two auxiliary buffers and pre-charging clock scheme for input impedance boosting [57].

E. CMRR Enhancement

There are two mechanisms that limit the practical CMRR of an AE-specific EEG system: the mismatch of electrode-tissue impedance (ETI) and the gain mismatch of two AEs. The ETI mismatch can be moderated by maximizing the AEs’ input impedance, while chopping between AEs for CMRR boosting is not practical since AEs are mounted on separated boards. Therefore, the mismatch of AEs typically limits the CMRR to $<60\text{dB}$ (with amplifiers) and $<90\text{dB}$ (with buffers). Trimming the gain of each AE is also possible but can be expensive due to

the need of extra test infrastructure. Other circuit techniques to improve the CMRR are: common-mode feedback (CMFB) and common-mode feedforward (CMFF). A common advantage of both techniques is that the noise generated from both circuits is common-mode noise to the AEs, and thus can be suppressed differentially.

Common-Mode Feedback (CMFB)

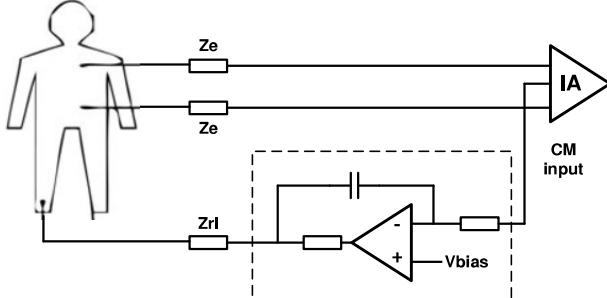


Fig. 22. Driven-Right-Leg (DRL) circuit.

The most well-known CMFB circuit is the Driven-Right-Leg (DRL) (Fig. 22) [62], where the common-mode (CM) output voltage is tracked and fed back to the subject through a third electrode, i.e. the bias electrode. The DRL improves CMRR by reducing the common-mode input impedance to the amplifier, resulting in less pickup of common mode input signals from the human body educating. Since the electrode-tissue impedance (Z_e , Z_{rl}) are also in the feedback loop, the DRL therefore improves the CMRR limited by both electrode mismatch and the AEs' mismatch. However, an integrator capacitor of several nF and a current limiting resistor of a few 100k Ω are needed for stability and safety [26], respectively. When dry electrodes are used, it becomes more difficult to achieve the loop stability, especially when both electrode offset and electrode impedance mismatch exist.

The common-mode signal can be fed back to the AEs input, instead of the subject (Fig. 23), thus the ill-defined electrode impedance is excluded from the feedback loop. In [30], such a CMFB circuit utilizes a summing amplifier for the output CM signal extraction, and the common-mode signal of the AEs are fed back to the non-inverting inputs of the AEs. As a result, the CMRR between a pair of AEs was improved by 30dB at 50Hz.

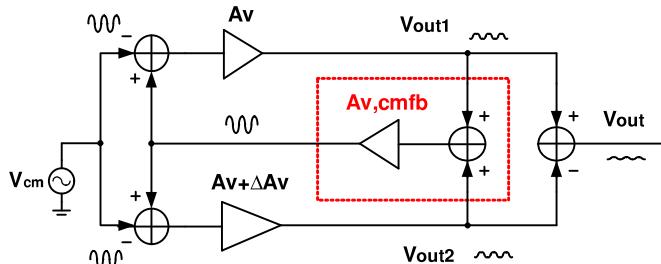


Fig. 23. CMFB technique for CMRR improvement of two AEs.

The CMFB can also be realized in digital domain. In [63], a digitally-assisted CMFB performs the common-mode signal extraction in the digital processor for better area efficiency and flexibility. However, both ADC and digital data transmission induce latency, which reduces the phase margin of the loop and thus degrades the loop stability. To overcome this problem, the common-mode signal extraction can be performed in a narrow bandwidth [64][65], where only 50/60Hz CM interferences are fed back to the subject for stability.

Common-Mode Feedforward (CMFF)

The CMFF technique is based on the compensation of the common-mode signal precisely at the input of each AE before amplification, which reduces the actual common mode signal swing seen by the AEs. Compared with the CMFB technique, the CMFF advances in terms of simplicity and stability.

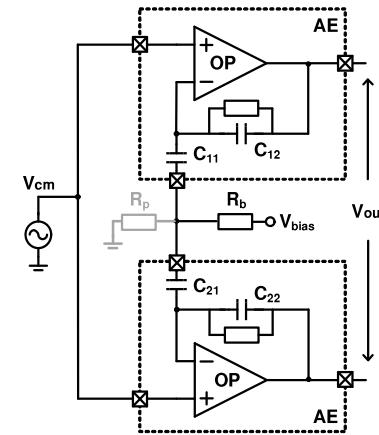


Fig. 24. CMFF scheme (via R_b and V_{bias}) for the CMRR improvement of two non-inverting AEs [38].

The CMFF can be integrated into a non-inverting amplifier with a resistive feedback [37] or a capacitive feedback (Fig. 24) [38]. In both cases, the CMFF is realized by connecting the AEs' reference inputs together to null the common mode input current. For example, in capacitive feedback AEs (Fig. 24), the reference input nodes of two operational (OP) amplifiers are capacitively connected to a well-defined DC voltage (V_{bias}) via a large bias resistor ($R_b=100M\Omega$). The reference node, i.e. the CMFF node, becomes an averaging node of all input signals. As a result, no common-mode current will flow through input capacitors C_{11} and C_{21} , improving the CMRR of a pair of AEs by 28dB (Fig. 25).

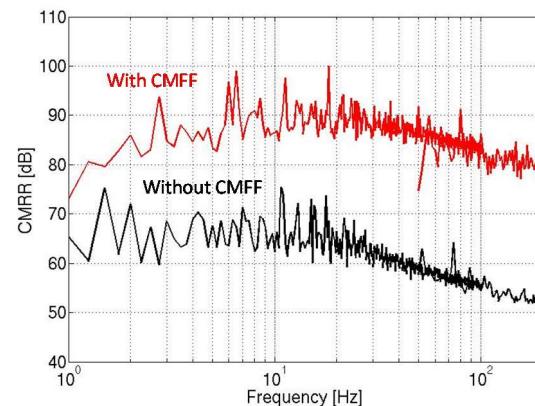


Fig. 25. Measured CMRR of two AEs depicted in Fig. 24.

A more generic CMFF scheme, which can be used in any AE architecture, has been proposed in [49], where an analog buffer forwards the input common-mode signal to the negative inputs of all the AEs via a g_m -C filter (Fig. 26). The CMRR of two AEs has been improved by 60dB without considering their electrode impedance mismatch. This CMFF scheme is also applicable to other AE architectures, where the buffer would simply drive the negative (reference) input of the AEs. Another nice feature of this generic CMFF scheme is the suppression of interferences and cable motion, since the buffer has a very low impedance.

TABLE II: PERFORMANCE SUMMARY OF AE-BASED SYSTEMS.

	TBioCAS'11 [30]	TBE'06 [68]	TBioCAS'14 [66]	EMBC'09 [36]	JSSC'14 [38]	JSSC'15 [49]
AE voltage gain	3, 10, 100	100	10	11	11, 51, 101	140, 700, 1200
Supply voltage	1.8V	5V	3V	3.3V	1.8V	1.8V
Input referred noise (per channel)	1.2 μ Vrms (0.5-100Hz)	7.49 μ Vrms (1-1kHz)	0.56 μ Vrms (0.5-100Hz)	2.4 μ Vrms (0.5-100Hz)	1.75 μ Vrms (0.5-100Hz)	0.65 μ Vrms (0.5-100Hz)
Electrode offset tolerance	Rail-to-rail	\pm 250mV	--	Rail-to-rail	\pm 250mV	\pm 350mV
DC-coupling feature	AC-coupling	AC-coupling	AC-coupling	AC-coupling	AC-coupling	"Functionally" DC-coupling
Input impedance	100M Ω @50Hz	1T Ω @DC	100M Ω @50Hz	--	400M Ω @50Hz	100M Ω @50Hz
CMRR @50Hz	82dB (with CMFB)	78dB	64dB	90dB	84dB (with CMFF)	102dB (with CMFF)
AFE power consumption (per channel)	20 μ W (AE only)	7.5mW (AE only)	360 μ W (AE only)	600 μ W incl. ADC	82 μ W incl. ADC	105 μ W incl. ADC
ADC	no	no	no	16 bits	12 bits	12 bits
Number of wires	4	2	4	--	6	5

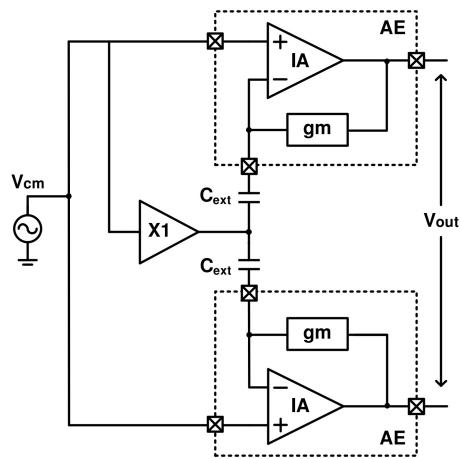


Fig. 26. Generic CMFF scheme via an analog buffer for CMRR improvement of two AC-coupled AEs.

F. Reducing the Number of Wires

An AE generally requires multiple connecting wires, such as power, analog/digital output, clock, data, CMFF/CMFB, reset, etc. On the other hand, there is a growing trend to extend AE's functions from EEG recording only towards multi-parameter monitoring for comprehensive analysis of brain activities. Examples include electrode impedance tomography (EIT) [66], functional near-infrared spectroscopy (fNIRS) [67]. However, adding new functions to an AE increases the number of wires

Similar to the 2-wire buffer AEs, combining the AE's analog output with power supply (or ground) through a current source (or sink) driver also reduces the number of wires [66][67]. This approach is generally applicable to any type of AE. However, the loss of $1/2$ dynamic range makes it not suitable for AEs with low supply voltages.

Combining the digital I/O signals of an AE is an alternative solution to reduce the number of wires. In [69], a single-wire self-coded pulse-width-modulation (PWM) was proposed, it merges the digital input with clock into a PWM signal.

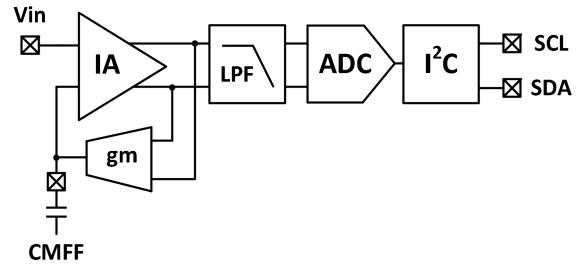


Fig. 27. Digital active electrode (DAE) with fully-integrated analog signal processor and digital interface.

AEs with all digital I/O signals is another promising solution. This can be realized by co-integrating a local ADC and a digital interface on an AE, known as a *digital active electrode (DAE)* [49] (Fig. 27). A DAE based system utilizes a built-in 2-wire I²C interface connecting the AEs to a backend microcontroller in a daisy chain. Each DAE interfaces with other modules via a 5-wire bus, including the digital I/O signals, power supplies and the common CMFF input. The I²C bus not only encompasses the complexity of integration but also enables the modularity of DAEs.

VI. CONCLUSION

Active electrodes enable scalp EEG measurement with dry electrodes for improved user comfort and long-term monitoring but also induces design challenges of low-power recording and medical grade signal quality.

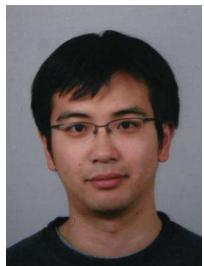
The parametric design methodologies of active-electrode specific EEG systems were explained. These key specifications can be met and enhanced via both architecture selection and circuits design techniques.

Table II summarizes and compares the overall performance of recently published AE systems. In these systems, the digital active electrode [49] achieves the most balanced performance while including the most functions. Comparatively, other AE systems either consume mW power [68], or have diminished analog performance, in terms of 64dB CMRR [62], >2 μ Vrms input noise [32][64], and 6 connecting wires [34].

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