

A MULTI-LEVEL INVERTER FOR GRID CONNECTED PV APPLICATION WITH EXTENDED INPUT VOLTAGE RANGE

PROJECT REPORT

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ABSTRACT

Owing to low cost, small size and low weight, transformer-less inverters became prominent in single-phase grid connected photo-voltaic systems. Key issues pertaining to these inverters include suppression of common mode leakage current and improvement of conversion efficiency. Achieving higher efficiency in single-phase grid-connected photo-voltaic systems depends on the number of stages involved in feeding power to the grid, predominantly, if the photovoltaic (PV) array voltage is less than peak value of the grid voltage.

In this project, an integrated dc-dc converter based grid-connected transformer-less PV inverter is proposed which is aimed at maintaining a high efficiency even if the PV array voltage falls below the peak value of grid voltage (efficient operation at an extended input voltage range). This helps in injecting more power to the grid even while operating under low PV voltage conditions. The variation of inverter output voltage depending on the photovoltaic (PV) array voltage is controlled by a single switch. The proposed topology has features such as no double stage conversion so that overall system efficiency is improved, Multi-levels in the inverter output voltage when the dc-dc converter is active thereby reduces the distortion of the grid current and Minimized CM leakage current which is suitable for grid-connected transformer-less PV systems.

A complete description of the operating principle and analysis of the proposed inverter are presented. Detailed simulation studies are carried out in MATLAB/Simulink environment to verify the analysis. Experimental results for a scaled down laboratory prototype are included as a proof-of-concept to validate the claims. The obtained results clearly validate the performance of the proposed inverter and its practical application in grid-connected PV systems.

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CHAPTER – 1

INTRODUCTION

1.1 GRID CONNECTED PV SYSTEMS

Grid-connected photovoltaic systems are composed of PV arrays connected to the grid through a power conditioning unit and are designed to operate in parallel with the electric utility grid. These Grid Connected PV Systems have solar panels that provide some or even most of their power needs during the day time, while still being connected to the local electrical grid network during the night time.

Solar powered PV systems can sometimes produce more electricity than is actually needed or consumed, especially during the long hot summer months. This extra or surplus electricity is either stored in batteries or as in most grid connected PV systems, fed directly back into the electrical grid network.

In other words, homes and buildings that use a grid connected PV system can use a portion or all of their energy needs with solar energy, and still use power from the normal electrical mains grid during the night or on cloudy dull and rainy days, giving the best of both worlds. Then in grid connected PV systems, electricity flows to and from the mains grid according to sunlight conditions and the actual electrical demand at that time.

In grid-connected photo-voltaic (PV) systems, the energy yield and payback time are greatly dependent on the initial cost and efficiency of the inverter. Other important factors in single-phase grid-feeding inverters are its weight and size. Therefore, the use of transformer-less single-phase grid-feeding inverters with high conversion efficiency is desirable.

1.2 PV SYSTEM CHARACTERISTICS AND IMPACTS

Today's grid-connected residential and commercial systems typically have the following characteristics and associated impacts:

- The PV system and the inverter are connected to the grid in parallel with the load.
 - The load is served whenever the grid is available.
 - Energy produced by the PV system decreases the apparent load. Energy produced in excess of the load flows into the distribution system.

- The PV system has no storage and cannot serve the load in the absence of the grid.
 - The PV system produces power at unity power factor and utility supplies all Volt Ampere reactive power.
- The inverter meets the requirements of IEEE 1547-2005.
- There is no direct communication or control between the utility and the inverter.
 - If the inverter senses that utility service has fallen outside set boundaries for voltage and/or frequency or utility service is interrupted, the inverter will disconnect from the utility until normal conditions resume. The load remains connected to the utility.
- For residential and small-commercial systems, the grid interconnection is typically net-metered at a flat rate.
- The price of energy is constant throughout the day and there is no demand charge.
 - When excess energy is produced, the meter spins backwards.
 - Energy is bought and sold at the same price.
 - Over the course of a month or a year, if energy produced exceeds energy used, the utility will not pay for the excess above the amount used.
 - If the grid is not available, grid-tied PV inverters (without energy storage and load transfer capability) cannot serve the load, even when sunlight is present and the PV modules are able to produce power.
- For large-scale commercial systems, rate structures are more complex.
- Time-of-use rates often apply, with cost of energy being higher during periods of peak demand.
 - Demand charges may apply with a significant portion of the utility bill derived from the highest power requirement (kW) measured over a 15 to 30 minute interval during the monthly billing period.
 - A charge for VARS (reactive power) may apply.
 - Net metering is less common, and some systems are not permitted to deliver any power back to the utility. In this case, the load must always exceed the energy generated by the solar system.

- Other systems have dual meters and power is purchased by the utility at a lower rate than the rate charged for power supplied by the utility to the customer.

1.3 IMPLICATIONS FOR UTILITY OPERATIONS

There are utility concerns that high penetration of inverter-based solar energy systems along with other distributed generation sources on distribution lines will contribute to instabilities and possibly unsafe operations due to one or several of the following design and operational characteristics:

- Because PV energy production does not always coincide with the times when it is most economical for utilities to use it, it can negatively impact utility operating economics.
 - No power is available in the hours immediately after sunset when demand for power may be high. Thus, the utility must increase peak power generation during these hours.
 - Conversely, utility demand is low in the early morning hours (sunrise to ~ 9 am). Power from solar systems during these hours results in a lower load for the utility, decreasing the need for economical 24-hr base load power, and increasing the need for more expensive intermediate and peaking power during the rest of the day.
- From the utility perspective, net-metered, flat rate customers, especially those whose net demand approaches zero, do not pay a fair share of their costs.
 - If energy generated equals energy used, then energy-related charges (the dominant part of most residential and small commercial bills) will approach zero.
 - Without a demand (kW) charge or significant interconnection charge, customers will pay little for the benefits of being connected to the grid.
- Power production from an individual PV system may increase or decrease rapidly due to cloud passages.
 - In most cases, the rate of change of the collective output from PV systems will be moderated by the geographic dispersal of the systems. However, in a case where the service area is relatively small and rapid weather changes can occur, measurements 6 conducted by Tucson Electric Power show that a rapidly-

passing cloud bank can essentially eliminate all solar generation across Tucson in less than 5 minutes.

- The introduction of significant amounts of rapidly-changing intermittent power in a utility system can affect the controls on and increase the need for spinning reserve.
- If a utility experiences sagging voltage under high demand conditions, IEEE 1547 requires that inverters disconnect. However, since the loads are not automatically disconnected, the utility will see an increase in demand, potentially aggravating the cause of the voltage sag and leading to a blackout (decreased utility system reliability).
- The addition of large numbers of inverters has been shown to increase the probability of islanding, during which inverters continue to supply local loads after a utility fault.² Other impacts to the utility include:
 - Inverters are limited in their ability to introduce extremely high levels of short circuit current, but the addition of large systems or many small systems can sum to significant short circuit currents and possibly cause equipment malfunction or damage.
 - Utility protection relays are designed to detect a fault, e.g. an arc to ground created by a tree branch falling across a line. The relays briefly disconnect from the fault to allow the fault to clear, and then reconnect to provide continuing service. If islanding detection fails and inverters remain on-line:
 - The inverters may be damaged by the reconnect.
 - The inverters may continue to supply current which could maintain the fault, causing the utility protection relays to lock open. Utility technicians must then be dispatched to reset the relays, and customers may be left without power for a significant time.
 - When technicians are dispatched, if the inverters are still on-line, the safety of the technicians is threatened because of power being supplied to the load side of disconnects and downed power lines.
- Frequency regulation may be impacted when distributed generation from PV systems becomes greater than local conventional generation. The effect on frequency regulation has not yet been observed, but is dependent upon the characteristics of the loads and the load-to-generation ratio.

- Phase-to-neutral over voltage may develop with load/generation imbalance or with phase to neutral faults. This condition will likely be worsened with high penetrations of PV distributed systems with no dis-patchability or interactive controls. Single phase systems installed disproportionately on a single phase may cause severely unbalanced networks leading to damage to controls or transformers.
- Inverters using pulse-width-modulation schemes to regulate their outputs typically do not add to lower number harmonics, however the higher frequencies associated with the power electronics do inject higher order harmonics.
- The levels of higher order harmonics from inverters that would interfere with the distribution equipment have not been fully characterized and need to be studied to determine if there is a possible effect on safety and equipment ratings. However, if required, mitigating the impact by filtering is generally simple, but will impact cost and performance
- Inverter-generated pulses associated with impedance detection for anti-islanding also accumulate in high penetration scenarios and may cause out-of-spec utility voltage profiles.

1.4 LITERATURE SURVEY

1. DC/AC converter to convert direct electric voltage into alternating voltage or into alternating current

Authors: *H. Schmidt, C. Siedle, and J. Ketterer*

Patent: *US Patent US7 046 534 B2, May 16, 2006*

Inference: A full-bridge inverter along with a ac bypass (FB-ACBP) is discussed in which is called as Highly Efficient and Reliable Inverter Concept (HERIC) topology. A fluctuating CM voltage could be observed since the freewheeling path potential is not clamped. However, the ground leakage current is minimized to an acceptable level.

2. Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into an alternating current voltage

Authors: *M. Victor, F. Greizer, S. Bremicker, and U. Hübler*

Patent: *US Patent US7 411 802 B2, August 12, 2008*

Inference: SMA Solar Technology Ag. suggested the use of a H5 topology.

3. An Optimized Transformer-less Photovoltaic Grid-Connected Inverter

Authors: *H. Xiao, S. Xie, Y. Chen, and R. Huang*

Patent: *IEEE Trans. on Ind. Electron., vol. 58, no. 5, pp. 1887–1895, May 2011.*

Inference: H5 topology is further improved by an additional switch which is used to eliminate the CM current.

4. A survey and extension of high efficiency grid connected transformer-less solar inverters with focus on leakage current characteristics

Authors: *Z. Ozkan and A. M. Hava*

Patent: *Energy Conv. Cong. and Expo. (ECCE), 2012 IEEE, Sept 2012, pp. 3453–3460*

Inference: Midpoint coupled H6 topology offers reduced switching losses. Based on this topology several midpoint coupled grid-feeding transformer-less topologies are presented.

5. Highly Efficient Single Phase Transformer-less Inverters for Grid-Connected Photovoltaic Systems

Authors: *S. V. Araujo, P. Zacharias, and R. Mallwitz*

Patent: *IEEE Trans. on Ind. Electron., vol. 57, no. 9, pp. 3118–3128, Sept 2010*

Inference: A single-phase transformer-less inverter is proposed which is composed of two step-down converters. A high level of efficiency and reliability is achieved by using only four semiconductor devices.

6. High-Efficiency MOSFET Inverter with H6-Type Configuration for Photovoltaic Nonisolated AC-Module Applications

Authors: *W. Yu, J. S. J. Lai, H. Qian, and C. Hutchens*

Patent: *IEEE Trans. on Power Electron., vol. 26, no. 4, pp. 1253–1260, April 2011.*

Inference: High efficiency of the inverter is achieved by naturally keeping the body diodes of the switches inactive.

7. Improved single-phase transformer-less inverter with high power density and high efficiency for grid-connected photovoltaic systems

Authors: *Y. W. Cho, W. J. Cha, J. M. Kwon, and B. H. Kwon*

Patent: *IET Renewable Power Gen., vol. 10, no. 2, pp. 166–174, 2016.*

Inference: It suggested a highly efficient and power dense inverter. It consists of a dual-parallel-buck inverter and two auxiliary circuits are provided for zero-current switching turn-off of the diodes, thus improving the system efficiency.

8. Efficient Transformerless MOSFET Inverter for a Grid-Tied Photovoltaic System

Authors: *M. Islam and S. Mekhilef*

Patent: *IEEE Trans. on Power Electron., vol. 31, no. 9, pp. 6305–6316, Sept 2016.*

Inference: The use of super-junction MOSFETs and SiC diodes enables a high inverter efficiency. In renewable power generation systems (like solar), the input dc voltage of the converter may vary greatly. For example, the output dc voltage of a solar panel changes with different temperature conditions.

9. Z-source inverter

Authors: *F. Z. Peng*

Patent: *IEEE Transactions on Industry Applications, vol. 39, no. 2, pp. 504–510, Mar 2003.*

Inference: A single-stage circuit is employed when the input voltage is above the critical level and a step-up converter is used when the PV array voltage falls below it. This topology however, requires a higher input voltage (almost double compared to previous topologies), due to its similarity with half bridge inverter. Single-stage topologies such as the Z-source inverter, quasi – Z source inverter or the split source inverter eliminate the additional dc-dc converter by utilizing a passive boosting stage.

10. Modulation for Three Phase Transformer-less Z-Source Inverter to Reduce Leakage Currents in Photovoltaic Systems

Authors: *F. Bradaschia, M. C. Cavalcanti, P. E. P. Ferraz, F. A. S. Neves, E. C. dos Santos, and J. H. G. M. da Silva*

Patent: *IEEE Transactions on Industrial Electronics, vol. 58, no. 12, pp. 5385–5395, Dec 2011.*

Inference: With conventional modulation techniques, they are not suitable for transformer-less inverter operation on account of having a variable common mode voltage, and consequently, a high leakage current

11. Transformer-less Photovoltaic Inverter Based on Interleaving High-Frequency Legs Having Bidirectional Capability

Authors: *C. Liu, Y. Wang, J. Cui, Y. Zhi, M. Liu, and G. Cai*

Patent: *IEEE Transactions on Power Electronics, vol. 31, no. 2, pp. 1131–1142, Feb 2016.*

Inference: The capacitors and inductors for the single-phase Z-source topologies have to be rated for twice the dc-link voltage and the rated current due to its inherent design structure

12. H5-HERIC Based Transformer-less Multilevel Inverter for Single-Phase Grid Connected PV Systems.

Authors: *G. Vazquez, P.R. Martinez-Rodriguez, J.M. Sosa, G. Escobar, M.A. Juarez and A. A. Valdez.*

Patent: *IEEE 2015*

Inference: Input Voltage is split by using a bidirectional switch. Thereby reducing the flow of leakage current.

13. Improved Single Phase Transformer-less Inverter with high power density and high efficiency for grid connected photo voltaic systems.

Authors: *Yong-Won Cho, Woo-Jun Cha, Jung-Min Kwon, Bong-Hwan Kwon.*

Patent: *IET Renewable power generation 2015*

Inference: High power density is achieved. High switching frequency reduces the filter inductor capacity.

14. Efficient Transformer-less MOSFET Inverter for Grid-Tied Photovoltaic System

Authors: *Monirul Islam, Saad Mekhilef.*

Patent: *IEEE 2015*

Inference: MOSFET switch is used. Clamping the common mode voltage. As the output power increases the efficiency decreases.

15. Technical Information on Capacitive Leakage Currents

Authors: *Ableitstrom*

Patent: *SMA technical information*

Inference: Parasitic capacitance occurs due to

- Film of water on the glass.
- Grounded Support Frame.
- Roof Surface Area.

1.5 EXISTING PROBLEMS

Topologies based on H5 and H6 are proposed to eliminate the leakage current of the grid-tied PV application. These inverters consist of five and six power switches respectively and some diodes for disconnecting the dc side from the grid. These topologies are more costly than the

FB inverter, because they use extra switches and diodes. Another disadvantage of these topologies is lower efficiency due to the current that circulates through three power switches at the same time.

Several high efficient new H5 and H6 transformer-less inverters are proposed to achieve lightweight and also lower cost. They have the capability of reactive power injection to the grid. The leakage current is high in these topologies, which is the main disadvantage of them and doesn't suit for the application when the PV array voltage falls below the peak value of grid voltage.

1.5 PROPOSED SOLUTION

The design of the inverter should be aimed towards higher efficiency (for a wide PV voltage range) and low CM leakage current. In order to simultaneously address these challenges, a novel topology is proposed, which contains a dc-dc converter that is energized only when the PV array voltage drops below the critical voltage.

The proposed topology has the following features:

- 1) No double stage conversion - Improves the efficiency of the overall system.
- 2) Multi-levels in the inverter output voltage when the dc-dc converter is active - Reduces the distortion of the grid current.
- 3) Minimized CM leakage current - Suitable for grid-connected transformer-less PV systems

1.6 ORGANIZATION OF THE PROJECT

Chapter 1 is an overview on the grid connected PV system while the following chapters aim to provide a much detailed insight. Chapter 2 introduces the solar panel while Chapter 3 explains the PIC microcontroller and the program code for pulse generation. Followed by which Chapter 4 draws up on the MOSFET switch. The design of the driver and the power supply circuit are illustrated in Chapter 5. Consecutively, Chapter 6 discusses the project working and modulation strategy employed. Simulation results and data gathered from the analysis are provided in Chapter 7. Chapter 8 shows the implementation of the hardware. Chapter 9 concludes the report. Last but not least, the references are cited in Chapter 10.

CHAPTER – 2

SOLAR PHOTOVOLTAIC SYSTEM

2.1 HISTORY

While experimenting in his father's laboratory, 19-year-old Alexandre Edmond Becquerel created the world's first photovoltaic cell and thereby discovered the photovoltaic effect. In his experiment, carried out in 1839, Becquerel placed two platinum electrodes in a container with silver chloride in an acidic solution. When illuminated voltage and current were generated over the electrodes and Becquerel found that the strength of the current changed with illumination. Because of this work, the photovoltaic effect has also been known as the "Becquerel effect". The next significant photovoltaic development arose from the interest in the photoconductive effect in selenium after Willoughby Smith found that selenium shows photoconductivity in 1873. In 1877 William Grylls Adams and his student Richard Evans Day observed the photovoltaic effect in solidified selenium by illuminating a junction between selenium and platinum. This was the first demonstration of the photovoltaic effect in an all solid-state system, proving that electricity could be produced from light without moving parts. In 1884 the first rooftop solar array was installed in New York, demonstrating an efficiency of almost 1%. The solar array used selenium solar cells invented the year before by an American inventor Charles Fritts, demonstrating that meaningful power could be extracted from solar cells. The invention impressed Werner von Siemens who stated: "The direct conversion of light into electricity has been shown for the first time". At this early stage of solar cell history optimism gripped the inventors. Fritts optimistically predicted that "we may ere long see the photoelectric plate competing with [coal-fired electrical-generating plants]". The first fossil-fueled power plants had only been built three years before Fritts announced his intentions by Thomas Edison. At the time the technology seemed poised to gain importance in a world discovering the wonders of electricity. James Clerk Maxwell praised the study of photoelectricity as "a very valuable contribution to science." But neither Maxwell nor Siemens had a clue as to how the phenomenon of photoelectricity worked. Maxwell wondered, "Is the radiation the immediate cause or does it act by producing some change in the chemical state?" Siemens urged a "thorough investigation to determine upon what the electromotive light-action of [the] selenium depends."

In subsequent years, the physical understanding of the phenomenon was improved with contributions from the likes of Heinrich Hertz who investigated ultraviolet light photoconductivity and discovered the photoelectric effect. In 1905 Albert Einstein publishes a paper explaining the photoelectric effect on a quantum basis later earning him a Nobel prize in physics.

The progress towards practical solar cells proved slow despite the breakthroughs in understanding. Bruno Lange, a German scientist whose 1931 solar panel resembled Fritts's design, predicted that, "in the not distant future, huge plants will employ thousands of these plates to transform sunlight into electric power...that can compete with hydroelectric and steam-driven generators in running factories and lighting homes." But Lange's solar cell worked no better than Fritts's.

The birth of the modern solar cell occurred along with that of the silicon transistor. Two scientists, Calvin Fuller and Gerald Pearson of the famous **Bell Laboratories**, led the pioneering effort that took the **silicon transistor** from theory to working device. During their work, they made silicon containing a small concentration of gallium making the silicon p-doped. When a rod of the material was dipped into a hot lithium bath the portion of the silicon immersed in the lithium became n-doped. Where the positively and negatively doped silicon met, a permanent electrical field developed. This is the **p-n junction**, the heart of the transistor and solar cell, where all electronic activity occurs. Illuminating the junction by lamplight an ammeter connected to the sample recorded a significant electrical current

2.2 POWER FROM A SOLAR CELL

To understand and measure how much power is produced from a solar cell, the **characteristic curve** of a solar cell is an important concept to understand. The characteristic curve show the current and voltage (IV) characteristics of a solar cell or module giving a detailed description of its solar energy conversion ability and efficiency, see figure 2.1. This characteristics curve is most often called an **IV-curve** and is basically a graphical representation of the operation of the solar cell or module summarizing the relationship between the current and voltage at the existing conditions of irradiance and temperature. **IV curves** provide the information required to configure a solar system so that it can operate as close to its optimal **peak power point** as possible.

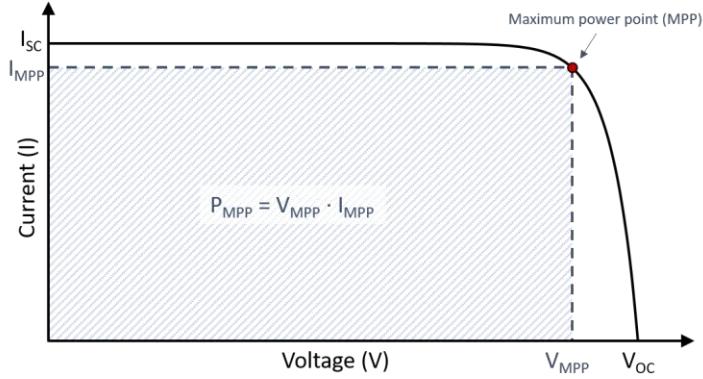


Fig.2.1

It is easy to measure two of the characteristic values of the IV curve, namely the **open circuit voltage (V_{oc})** and the **short circuit current (I_{sc})** with a simple multi-meter. The open circuit voltage of the solar cell is the maximum voltage that the solar cell will supply, while the short circuit current of a solar cell is the maximum current the solar cell will produce. The issue with the two states, I_{SC} and V_{OC} , is that the most interesting aspect of a solar cell is not the current flow with no potential drop, nor the potential drop with no current flow, but the product of these two; the power. When either the potential drop or the current flow is zero, the power, being the product of the two, will be zero. Therefore, a more interesting aspect is the **maximum power** the solar cell can produce.

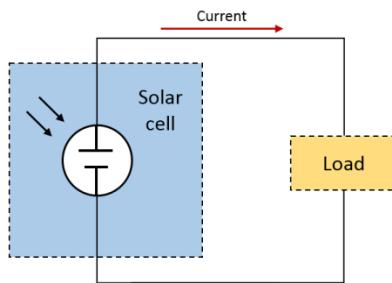


Fig.2.2

By increasing the **resistive load** on a solar cell continuously from zero (short circuit) to a very high value (equivalent to open circuit) one can determine the **maximum power point**, see figure 2.2. Plotting the power as a function of the voltage results in the blue curve, see figure 2.3, where the maximum power point (P_{MPP}) is the peak point of the power curve. The power is the product of the voltage and the current.

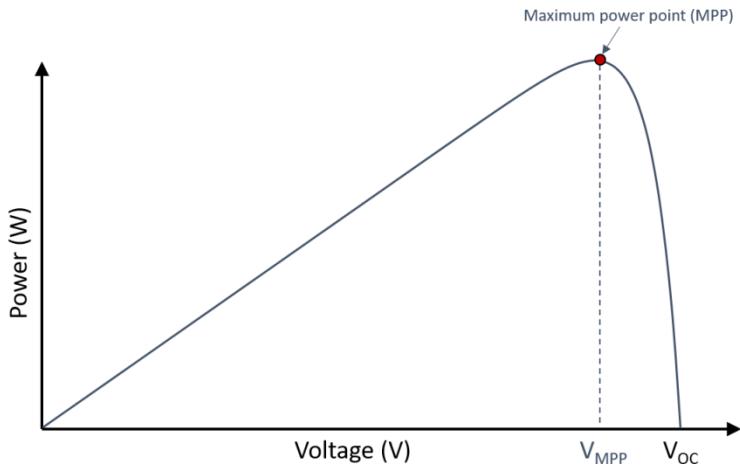


Fig.2.3

2.3 SERIES AND PARALLEL CONNECTIONS

When we use solar cells we typically connect more than one solar cell together to increase the power produced. When we make these connections it is important to understand how the current and voltage adds together depending on the connection. There are two ways to connect solar cells, **parallel and series connections**.

Parallel connection

In a parallel connection **all cells are forced to have the same voltage, while the currents are added up.**

$$V = V_1 = V_2 = \dots = V_n \quad V = V_1 = V_2 = \dots = V_n \quad I = I_1 + I_2 + \dots + I_n$$

Figure 2.4 shows a module of solar cells connected in parallel. On the left you can see the characteristic curves of modules consisting of three, two, and one cell.

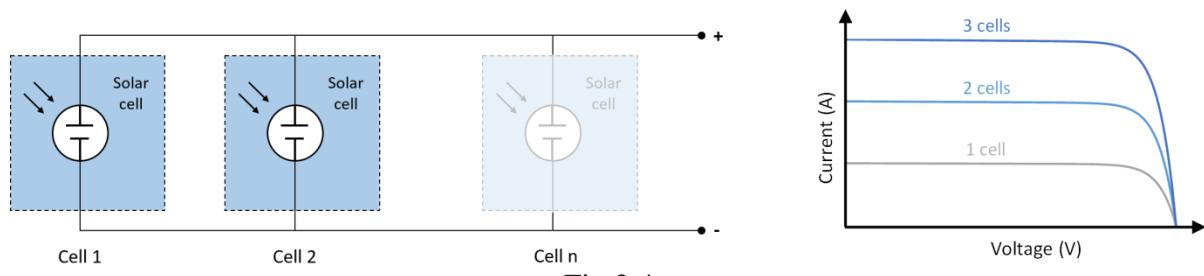


Fig.2.4

Series connection

When cells are connected in **series** the **current for each cell will be the same, while the voltages are summed.**

$$I=I_1=I_2=\dots=I_n \quad V=V_1+V_2+\dots+V_n$$

In figure 2.5, you can see a module with serially connected solar cells and a characteristic curve for three, two, and one connected cells.

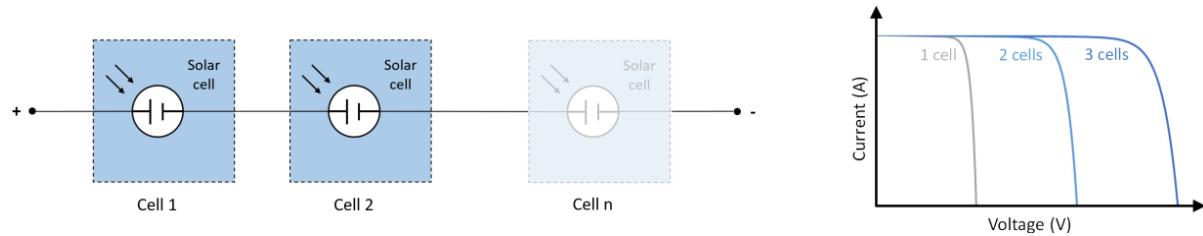


Fig.2.5

We typically see series connections of cells in modules since this ensures **higher voltages**. If we try to imagine a solar cell module consisting of 100 cells each having a voltage of 0.6 V and a current of 4 A, we can connect all cells in either parallel or serial connection. In the case of a parallel connection the module voltage would be 0.6 V and the current 400 A. In the case of a serial connection the voltage would be 60 V and 4 A. In either case the power is the same, however, the **transport losses would be significantly different**. If we consider Ohm's law and the power law, we see that the power lost to a wire scales with the current squared. Therefore we would need extremely thick cables if we were to transport high current at low voltages. Conversely high voltages and low currents give much lower transmission losses **high voltages and low currents give much lower transmission losses** and thinner cables are required.

2.4 SHADOW EFFECTS

It is important to consider what happens when one or more solar cells in such connections are in **shadow**.

In figure 2.6 you can see how a shaded cell in a module affects the overall module performance. To draw this plot it is assumed that the shaded cell is 90% shaded. From earlier

we know that the **open circuit voltage** of a shaded cell only changes slightly, while the **short circuit current will drop** with around 90%. The overall IV curve for a module decays with roughly the amount of current loss from the one shaded cell. Thus the overall power loss of the module corresponds to the shaded area. This means that a parallel connection is nicely behaved in partial shading losing only the shaded area.

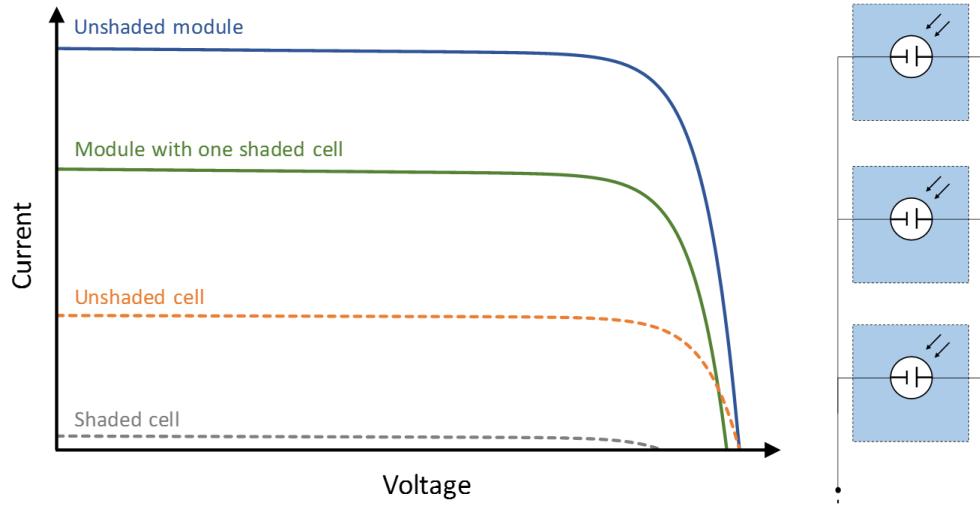


Fig.2.6

While the parallel connection is relatively good-natured when it comes to partial shading, the same cannot be said for a series connection, as can be seen from figure 2.7. With one shaded cell in the series connection the two other cells must push their current through the shaded cell. This causes a negative voltage over the shaded cell. The current is limited by the shaded cell and therefore the overall current of the module is limited. As can be seen from figure two, this effect reduces the power output from the module with a single shaded cell significantly.

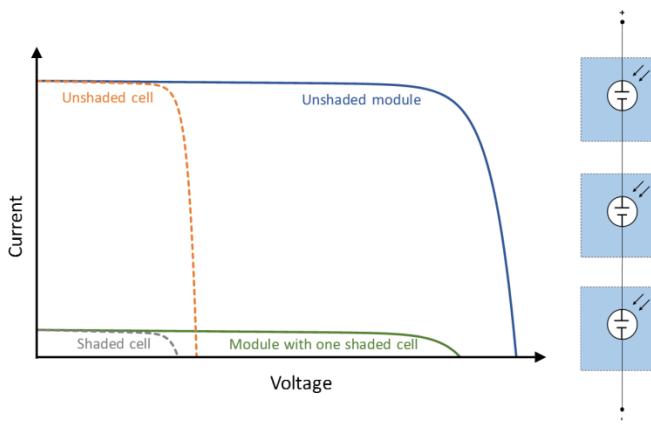


Fig.2.7

A solution to the problem with series connection is to employ a **bypass diode over the shaded cell**, see figure 2.8. Bypass diodes allow current to pass shaded cells and thereby reduce the voltage losses through the module. When a module becomes shaded its bypass diode begins to conduct current through itself. With the bypass diode the current is no longer limited by the shaded cell, and the impact on the overall IV curve is greatly reduced, see figure 2.9.

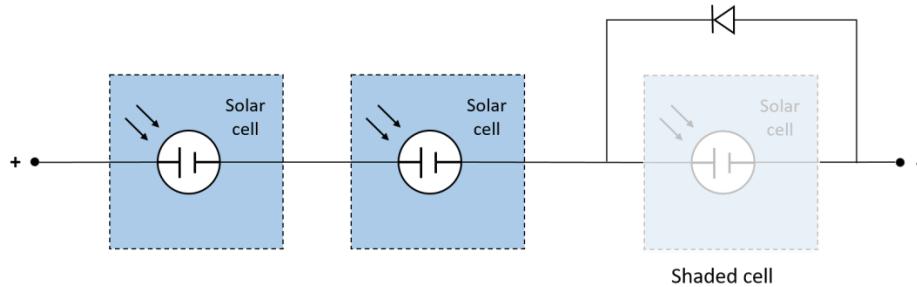


Fig.2.8

Bypass diodes also serve another purpose, namely the prevention of hotspots. In modules with one shaded cell and no bypass diode, there will be a massive heating of the shaded cell caused by the other cells. The usage of bypass diodes alleviates this problem.

In real solar modules bypass diodes are not employed for each cell. The reason is that the diodes would have to be incorporated into the encapsulation if the solution should be practical. Instead bypass diodes are employed for strings of cells (e.g. 12, 18, or 24 cells). It is therefore important that modules are not mounted in places were partial shading is expected during the day.

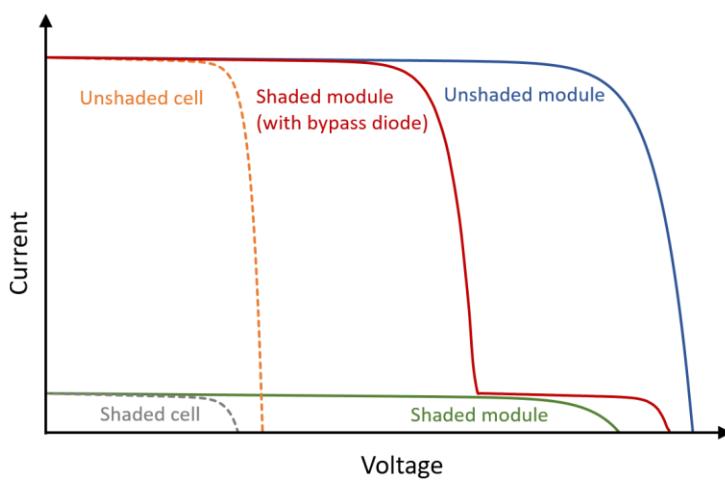


Fig.2.9

2.5 SILICON SOLAR CELLS WORKING

To understand how a silicon solar cell collects light we must look at the photocurrent generation at different depths of the cell. Figure 2.10 shows a schematic representation of a silicon solar cell with four different photon absorption events.

- **Absorption in the space charge region (photon 1).** Photon 1 is absorbed within the space charge region. The field prevailing in the space charge region separates the generated electron-hole pair and drives the two charge carriers in different directions. The hole must travel a relatively long way through the base to the plus contact, however, as it is in the p-region during this movement, the probability of a recombination is small. Therefore, almost all generated electron-hole pairs generated in the space charge region can be used for the photocurrent.
- **Absorption within the diffusion length (photon 2).** Photon 2 is absorbed deep in the solar cell, but within the diffusion length for the electron. The generated electron is not situated in an electrical field but diffuses somewhat randomly throughout the crystal. If, by chance, it arrives at the edge of the space charge region it is drawn to the n-side by the prevailing field where it can flow to the contact. As the electron was generated within the diffusion length, the probability that it reaches the space charge region is relatively high.
- **Absorption in the emitter (photon 3).** Photon 3 is absorbed in the highly doped emitter. Because of the high degree of doping, the diffusion length is extremely small. Therefore, the probability for the generated hole to recombine before reaching the space charge region is high. The highly doped upper edge of the emitter is occasionally referred to as the dead layer in order to emphasize that this is where the highest recombination probability is situated.
- **Absorption outside the diffusion length (photon 4).** Photon 4 is absorbed helplessly deep inside the lower region of the solar cell. Although the electron diffuses through the p-base, it recombines with a hole before it can reach the space charge region. Thus, although an electron-hole pair is formed due to light absorption, no contribution to the photocurrent is made. The diffusion length is depending on the crystal quality and therefore highly pure silicon crystals are needed for solar cells, so that absorbed infrared light rays can be used deep in the cell.

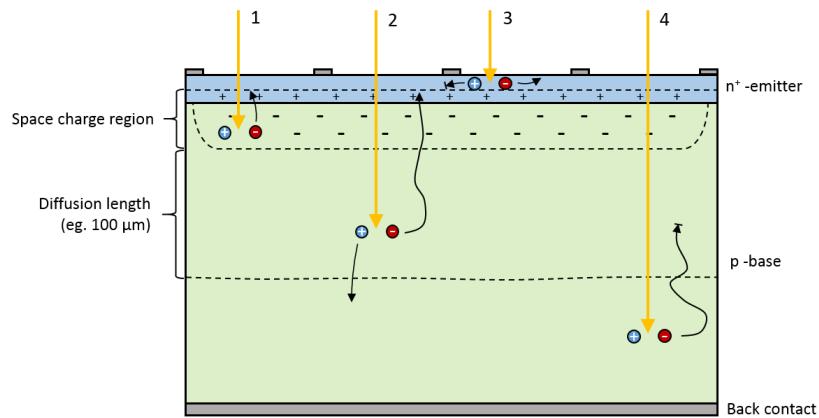


Fig.2.10

CHAPTER – 3

PIC CONTROLLER

3.1 INTRODUCTION

In this project the hardware is implemented using the Pic- Microcontroller “Pic 16F88”. The advantages of the Pic- microcontroller is that the instruction set of this controller are fewer than the usual microcontroller. Unlike Conventional processors, which are generally complex, instruction set computer (CISC) type, Pic microcontroller is a RISC processor.

The advantages of RISC processor against CISC processor are:

1. RISC instructions are simpler and consequently operate faster.
2. A RISC processor takes a single cycle for each instruction, while CISC processor requires multiple clocks per instruction (typically, at least three cycles of throughput execution time for the simplest instruction and 12 to 24 clock cycles for more complex instruction), which makes decoding a tough task.
3. The control unit in a CISC is always implemented by a micro-code, which is much slower than the hardware implemented in RISC.

The idea of using the Pic microcontroller is because:

1. To employ the frequently used instructions as the instruction set while using a few instructions to achieve the same function performed by a much more complex instruction in a CISC.
2. The RISC itself has a large number of general purpose registers, largely reduced the frequency of the most time-consuming memory access.
3. In terms of clock rate, the RISC with its much simpler circuits can have a higher clock rate that again increases the performance of a processor.

Overall the RISC processor can provide processing power more than three times of a CISC processor in a particular field of application.

3.2 FEATURES OF PIC

Low-Power Features:

- Power-Managed modes:
 - Primary Run: RC oscillator, 76 μ A, 1 MHz, 2V
 - RC_RUN: 7 μ A, 31.25 kHz, 2V
 - SEC_RUN: 9 μ A, 32 kHz, 2V - Sleep: 0.1 μ A, 2V
- Timer1 Oscillator: 1.8 μ A, 32 kHz, 2V
- Watchdog Timer: 2.2 μ A, 2V
- Two-Speed Oscillator Start-up

Oscillators:

- Three Crystal modes: LP, XT, HS: up to 20 MHz
- Two External RC modes
- One External Clock mode: - ECIO: up to 20 MHz
- Internal oscillator block: - 8 user selectable frequencies: 31 kHz, 125 kHz, 250 kHz, 500 kHz, 1 MHz, 2 MHz, 4 MHz, 8 MHz

Peripheral Features:

- Capture, Compare, PWM (CCP) module:
 - Capture is 16-bit, max. resolution is 12.5 ns
 - Compare is 16-bit, max. resolution is 200 ns
 - PWM max. resolution is 10-bit
- 10-bit, 7-channel Analog-to-Digital Converter
- Synchronous Serial Port (SSP) with SPI (Master/Slave) and I²C™ (Slave)
- Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART/SCI) with 9-bit address detection: - RS-232 operation using internal oscillator (no external crystal required)
- Dual Analog Comparator module: -
- Programmable on-chip voltage reference
- Programmable input multiplexing from device inputs and internal voltage reference –
- Comparator outputs are externally accessible Pin Diagram

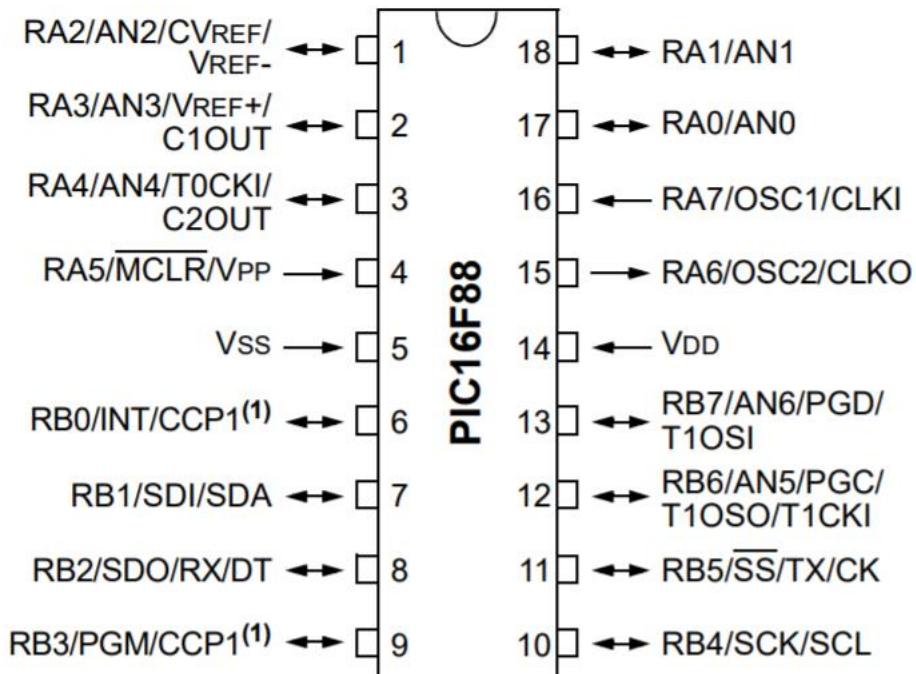
Special Microcontroller Features:

- 100,000 erase/write cycles Enhanced Flash program memory typical
- 1,000,000 typical erase/write cycles EEPROM data memory typical
- EEPROM Data Retention: > 40 years
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Processor read/write access to program memory
- Low-Voltage Programming
- In-Circuit Debugging via two pins
- Extended Watchdog Timer (WDT): - Programmable period from 1 ms to 268s
- Wide operating voltage range: 2.0V to 5.5V

3.3 PIN DIAGRAM

Pin Diagram

18-Pin PDIP, SOIC



Note 1: The CCP1 pin is determined by the CCPMX bit in Configuration Word 1 register.

Device	Program Memory		Data Memory		I/O Pins	10-bit A/D (ch)	CCP (PWM)	AUSART	Comparators	SSP	Timers 8/16-bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)							
PIC16F87	7168	4096	368	256	16	N/A	1	Y	2	Y	2/1
PIC16F88	7168	4096	368	256	16	1	1	Y	2	Y	2/1

Fig.3.1

3.4 DEVICE OVERVIEW

AVAILABLE MEMORY IN PIC16F87/88 DEVICES

Device	Program Flash	Data Memory	Data EEPROM
PIC16F87/88	4K x 14	368 x 8	256 x 8

There are 16 I/O pins that are user configurable on a pin-to-pin basis. Some pins are multiplexed with other device functions. These functions include:

- External Interrupt
- Change on PORTB Interrupt
- Timer0 Clock Input
- Low-Power Timer1 Clock/Oscillator
- Capture/Compare/PWM
- 10-bit, 7-channel A/D Converter
- SPI/I²C™
- Two Analog Comparators
- AUSART
- MCLR (RA5) can be configured as an input

Block diagram

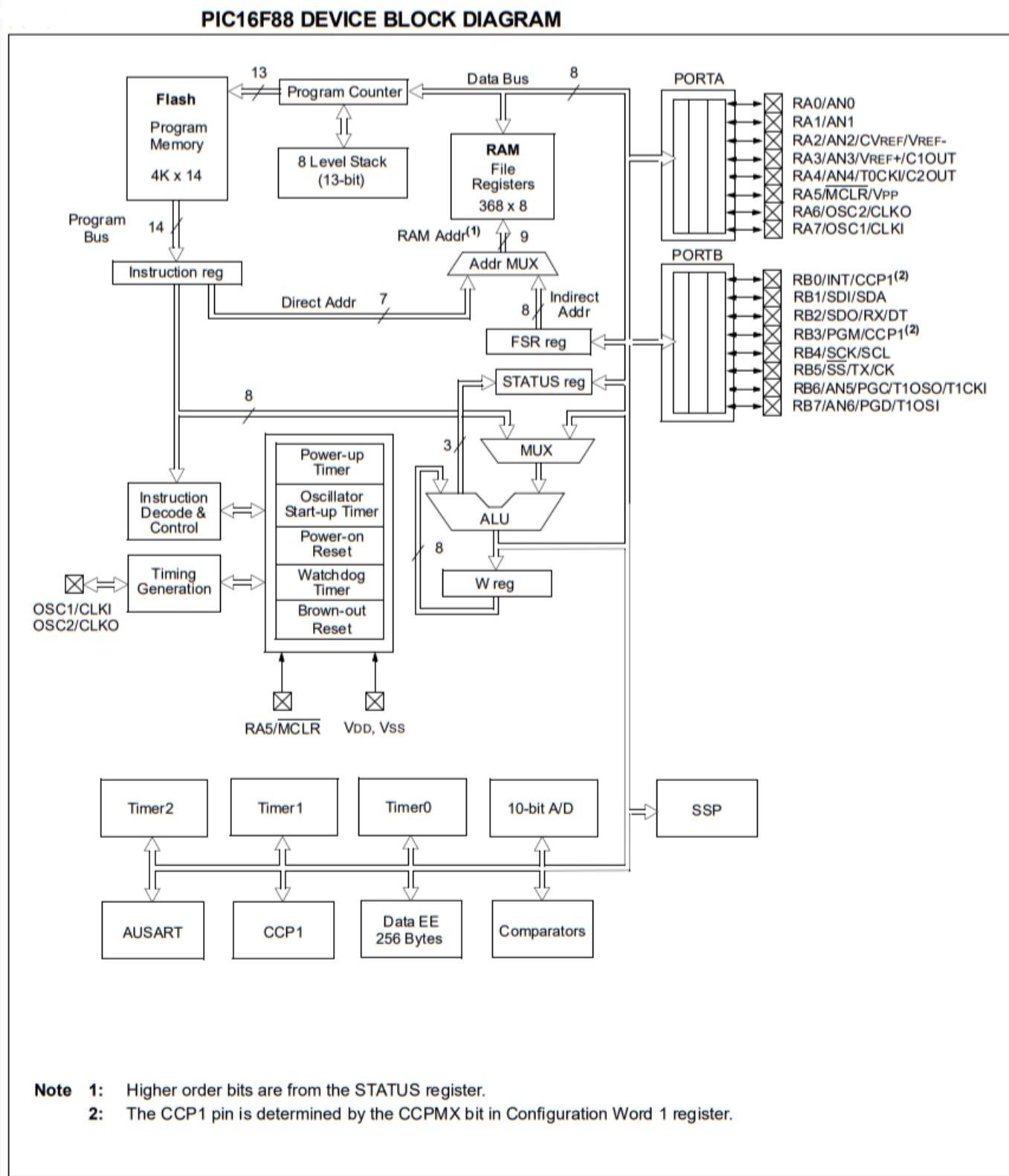


Fig.3.2

3.5 PIN-OUT DESCRIPTION

PIC16F87/88 PINOUT DESCRIPTION

Pin Name	PDIP/ SOIC Pin#	SSOP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
RA0/AN0	17	19	23	I/O	TTL	PORTA is a bidirectional I/O port.
RA0				I	Analog	Bidirectional I/O pin.
AN0						Analog input channel 0.
RA1/AN1	18	20	24	I/O	TTL	Bidirectional I/O pin.
RA1				I	Analog	Analog input channel 1.
AN1						
RA2/AN2/CVREF/VREF-	1	1	26	I/O	TTL	Bidirectional I/O pin.
RA2				I	Analog	Analog input channel 2.
AN2				O		Comparator VREF output.
CVREF				I	Analog	A/D reference voltage (Low) input.
VREF-(4)						
RA3/AN3/VREF+/C1OUT	2	2	27	I/O	TTL	Bidirectional I/O pin.
RA3				I	Analog	Analog input channel 3.
AN3				I	Analog	A/D reference voltage (High) input.
VREF+(4)				O		
C1OUT						Comparator 1 output.
RA4/AN4/T0CKI/C2OUT	3	3	28	I/O	ST	Bidirectional I/O pin.
RA4				I	Analog	Analog input channel 4.
AN4(4)				I		Clock input to the TMR0 timer/counter.
T0CKI				O	ST	Comparator 2 output.
C2OUT						
RA5/MCLR/VPP	4	4	1	I	ST	Input pin.
RA5				I	ST	Master Clear (Reset). Input/programming voltage input. This pin is an active-low Reset to the device.
MCLR				P	-	Programming voltage input.
VPP						
RA6/OSC2/CLKO	15	17	20	I/O	ST	Bidirectional I/O pin.
RA6				O	-	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
OSC2				O	-	In RC mode, this pin outputs CLKO signal which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
CLKO						
RA7/OSC1/CLKI	16	18	21	I/O	ST	Bidirectional I/O pin.
RA7				I	ST/CMOS ⁽³⁾	Oscillator crystal input.
OSC1				I	-	External clock source input.
CLKI						

Legend: I = Input O = Output I/O = Input/Output P = Power
 - = Not used TTL = TTL Input ST = Schmitt Trigger Input

- Note 1:** This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.
4: PIC16F88 devices only.
5: The CCP1 pin is determined by the CCPMX bit in Configuration Word 1 register.

PIC16F87/88 PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP/ SOIC Pin#	SSOP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
RB0/INT/CCP1 ⁽⁵⁾ RB0 INT CCP1	6	7	7	I/O I I/O	TTL ST ⁽¹⁾ ST	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. Bidirectional I/O pin. External interrupt pin. Capture input, Compare output, PWM output.
RB1/SDI/SDA RB1 SDI SDA	7	8	8	I/O I I/O	TTL ST ST	Bidirectional I/O pin. SPI data in. I ² C™ data.
RB2/SDO/RX/DT RB2 SDO RX DT	8	9	9	I/O O I I/O	TTL ST	Bidirectional I/O pin. SPI data out. AUSART asynchronous receive. AUSART synchronous detect.
RB3/PGM/CCP1 ⁽⁵⁾ RB3 PGM CCP1	9	10	10	I/O I/O I	TTL ST ST	Bidirectional I/O pin. Low-Voltage ICSP™ Programming enable pin. Capture input, Compare output, PWM output.
RB4/SCK/SCL RB4 SCK SCL	10	11	12	I/O I/O I	TTL ST ST	Bidirectional I/O pin. Interrupt-on-change pin. Synchronous serial clock input/output for SPI. Synchronous serial clock Input for I ² C.
RB5/SS/TX/CK RB5 SS TX CK	11	12	13	I/O I O I/O	TTL TTL	Bidirectional I/O pin. Interrupt-on-change pin. Slave select for SPI in Slave mode. AUSART asynchronous transmit. AUSART synchronous clock.
RB6/AN5/PGC/T1OSO/ T1CKI RB6 AN5 ⁽⁴⁾ PGC T1OSO T1CKI	12	13	15	I/O I I/O O I	TTL ST ⁽²⁾ ST ST	Bidirectional I/O pin. Interrupt-on-change pin. Analog input channel 5. In-Circuit Debugger and programming clock pin. Timer1 oscillator output. Timer1 external clock input.
RB7/AN6/PGD/T1OSI RB7 AN6 ⁽⁴⁾ PGD T1OSI	13	14	16	I/O I I I	TTL ST ⁽²⁾ ST	Bidirectional I/O pin. Interrupt-on-change pin. Analog input channel 6. In-Circuit Debugger and ICSP programming data pin. Timer1 oscillator input.
VSS	5	5, 6	3, 5	P	—	Ground reference for logic and I/O pins.
VDD	14	15, 16	17, 19	P	—	Positive supply for logic and I/O pins.

Legend: I = Input O = Output I/O = Input/Output P = Power
 — = Not used TTL = TTL Input ST = Schmitt Trigger Input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

4: PIC16F88 devices only.

5: The CCP1 pin is determined by the CCPMX bit in Configuration Word 1 register.

Tab.3.1

3.6 SUMMARY

This chapter deals with design and specification of PIC microcontroller. The ports and pin description are also discussed and also some features with some advantages are also discussed in this chapter. The code for this PIC micro-controller can be found in the appendix.

CHAPTER – 4

MOSFET

4.1 INTRODUCTION

Power MOSFET is a type of MOSFET which is specially meant to handle high levels of power. These exhibit high switching speed and can work much better in comparison with other normal MOSFETs in the case of low voltage levels. However its operating principle is similar to that of any other general MOSFET. Power MOSFETs which are most widely used are n-channel Enhancement-mode or p-channel Enhancement-mode or n-channel Depletion-mode in nature.

Further, there are a wide variety of power MOSFET structures like Vertical Diffused MOS (VDMOS) or Double-Diffused MOS or DMOS, UMOS or Trench-MOS, VMOS, etc. Figure4.1 show an n-substrate VDMOS made of n-substrate and an n-epitaxial layer into which p and n+ regions are embedded into using double diffusion process.

Here the channel is formed in a p-type region when the gate-to-source voltage is made positive. Most importantly, here, the Source (S) terminal is placed over the Drain (D) terminal forming a vertical structure. As a result, in VDMOS the current flows beneath the gate area vertically between the source and the drain terminals through numerous n+ sources conducting in-parallel. As a result, the resistance offered by the device during its ON state $R_{DS(ON)}$ is much lower than that in the case of normal MOSFETs which enable them to handle high currents. This resistance of the device is seen to double as the current increments by about 6% (Figure 4.2a). On the other hand $R_{DS(ON)}$ is highly influenced by the junction temperature T_J (Figure 4.2b) and is seen to be positive in nature.

Similar to this we can even have a p-substrate **power MOSFET** provided we replace n-type materials with p-type and then reverse the polarities of the voltages applied. However they exhibit a much higher $R_{DS(ON)}$ in comparison with n-substrate devices as they employ holes as their majority charge carriers instead of electrons. Nevertheless, these are preferred to be used as buck converters.

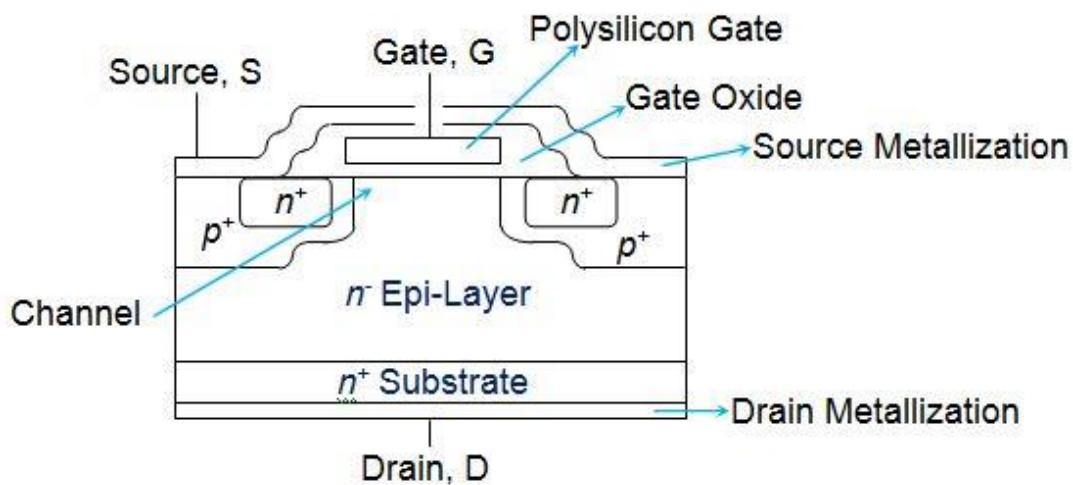


Fig.4.1

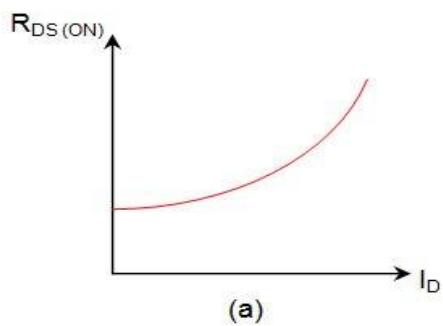


Fig.4.2(a)

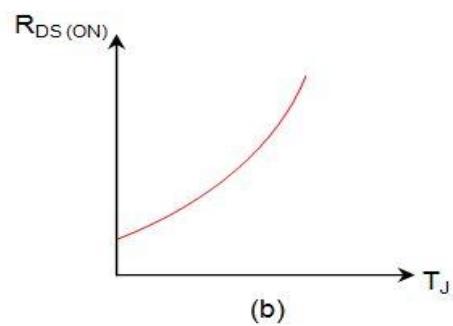


Fig.4.2(b)

Although the structures of the normal MOSFETs and the power MOSFETs are seen to be different, the basic principle behind their working remains unaltered. That is, in both of them the formation of conduction channel is the same which is nothing but the suitable bias applied at the gate terminal resulting in an inversion layer.

4.2 OPERATING PRINCIPLE OF MOSFET

Power MOSFET is a minority carrier device. So, conduction takes place only by the electrons. Therefore, the conduction cannot take place through the MOSFET from the drain to source due to the presence of P-layer in between. But this is possible by Inversion layer creation.

The operation of MOSFET divides into two parts

1. Formation of the depletion layer
2. Creation of Inversion Layer

1) Formation of the depletion layer

By connecting a positive voltage to the drain with respect to the source and the gate is positive with respect to the body, the MOSFET works as forward biased. The p-layer has a large number of holes and few electrons. The holes are the majority charge carrier and electrons are minority charge carrier. Due to the positive voltage applied between the gate and the body, these electrons are attracted towards the gate and gather below the oxide layer and produce the depletion layer.

2) Creation of Inversion Layer

The number of electrons below the oxide layer will greater than the number of holes if the positive gate voltage increases further. Hence, n-type of sub-layer form below the oxide layer. This process is known as the creation of the inversion layer. The process of generation of an inversion layer due to the extremely applied gate voltage is known as the field effect. This inversion layer is also known as the induced layer.

The resistance of induced layer depends on the magnitude of the gate to body voltage. Higher the gate voltage lesser the resistance. The resistance decreases with an increase in the gate to body voltage. But after a certain level, the resistance is not decreased even increasing the gate to body voltage. If the maximum specified value of the gate voltage exceeds then the oxide layer will breakdown.

4.3 CHARACTERISTICS MOSFET

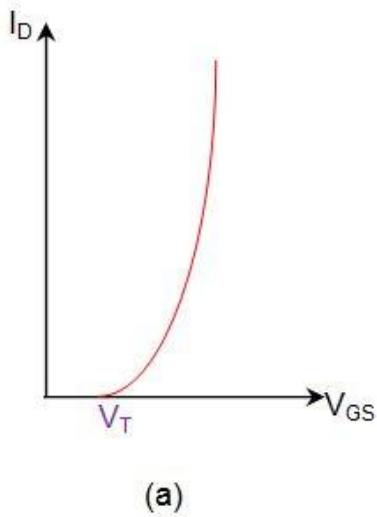
It is a graph of drain current I_d versus drain to source voltage V_{DS} for different values of the gate to source voltage V_{GS} . It has three regions; saturation, cut-off, and ohmic region. In the application where the MOSFET used as a switch, the device works in the cut-off region and ohmic region when turned OFF and ON respectively. The operation in the saturation region avoided reducing the power dissipation in the on-state.

When the gate-source voltage is less than the threshold voltage, the MOSFET is in the cut-off state. To avoid breakdown the drain to source breakdown voltage should be greater than the applied voltage. The avalanche breakdown takes place.

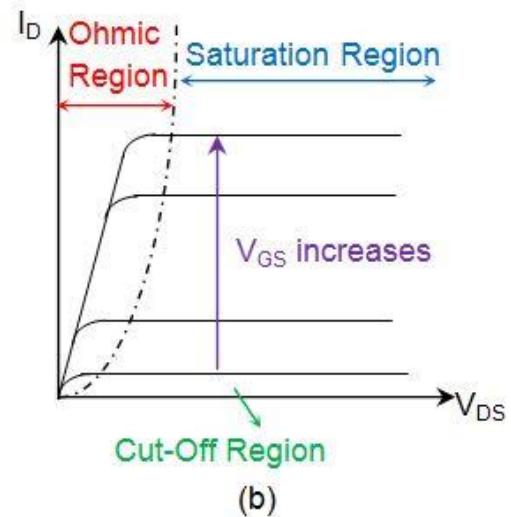
The power MOSFET goes into the ohmic region when a larger positive gate to source voltage apply and the drain to source voltage is small. In this region, the power dissipation is low.

In the saturation region, the drain current is almost independent of the drain to source voltage. It is only dependent on the gate to source voltage. The gate voltage is greater than the threshold voltage. The drain current increase with the increase in the gate to source voltage.

As a result, the nature of transfer characteristics (Figure 4.3(a)) and the output characteristics (Figure 4.3(b)) exhibited by either of them are almost identical to each other.



(a)



(b)

Fig4.3(a) Input characteristics

Fig4.3(b)Output characteristics

Further, it is to be noted that in the case of power MOSFETs which are based on vertical structure, the doping and the thickness of the epitaxial layer decide the voltage rating while the channel width decides its current rating. This is the reason because of which they can sustain high blocking voltage and high current, making them suitable for low power switching applications. However even lateral-structure based MOSFETs exist which behaves better in comparison with vertical-structure based designs especially in saturated operating region, enabling their use in high-end audio amplifiers. Another **advantage of power MOSFET** is the fact that they can be paralleled as their forward voltage drop increases with

an increase in the temperature which in turn assures equal current distribution amongst all of its components. **Power MOSFETs** are extensively used as a part of power supplies, DC-DC converters and low-voltage motor controllers.

4.4 USING THE MOSFET AS A SWITCH

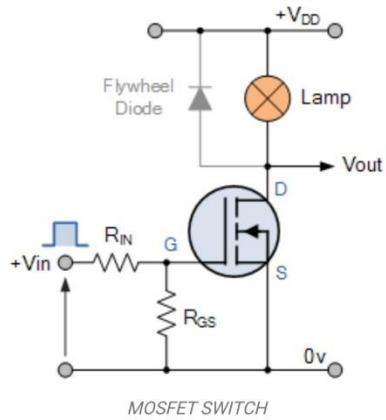


Fig.4.4 MOSFET SWITCH

In this circuit arrangement an enhanced mode and N-channel MOSFET is being used to switch a sample lamp ON and OFF. The positive gate voltage is applied to the base of the transistor and the lamp is ON ($V_{GS}=+v$) or at zero voltage level the device turns off ($V_{GS}=0$). If the resistive load of the lamp was to be replaced by an inductive load and connected to the relay or diode which is protect to the load. In the above circuit, it is a very simple circuit for switching a resistive load such as lamp or LED.

But when using MOSFET to switch either inductive load or capacitive load protection is required to contain the MOSFET device. We are not giving the protection the MOSFET device is damage. For the MOSFET to operate as an analog switching device, it needs to be switched between its cutoff region where $V_{GS}=0$ and saturation region where $V_{GS}=+v$. MOSFET is also a transistor. We abbreviate it as Metal Oxide Silicon Field Effect Transistor. It will have P-channel and N-channel. It consists of a source, gate and drain. Here we connected a resistive load of 24Ω in series with an ammeter, and a voltage meter connected across the MOSFET. In the transistor the current flow in the gate is in positive direction and

source goes to ground. In BJT's, the current flow is base-to-emitter circuit. But in MOSFET there is no current flow because there is a capacitor at the beginning of the gate, it just requires only voltage. We will know this by doing the simulation process with switching ON/OFF. When the switch is ON there is no current flow in the circuit, when we take a resistance of 24Ω and 0.29 of ammeter voltage then we find negligible voltage drop across the source because there is +0.21V across MOSFET.

Resistance between drain and source is called RDS. Because of RDS, the voltage drop appears while current flow in circuit. RDS varies depending on the type of MOSFET (it could be 0.001, 0.005, and 0.05 depending on the voltage type).

Finally, we will conclude that, the transistor requires current whereas MOSFET require voltage. The driving requirement for the MOSFET is much better, much simpler as compared to a BJT.

4.5 FEATURES OF POWER MOSFETS

Power MOSFET has lower switching losses but its on-resistance and conduction losses are more. MOSFET is a voltage-controlled device. MOSFET has positive temperature co-efficient for resistance. This makes parallel operation of MOSFET easy. If a MOSFET shares increased current initially, it heats up faster its resistance rises and this increased resistance causes this current to shift to other devices in parallel. In MOSFET secondary break down does not occur, because it has positive temperature co-efficient. Power MOSFETS in higher voltage ratings have more conduction losses

IRF 840- POWER MOSFET:

- 1) Dynamic dv/dt Rating
- 2) Repetitive Avalanche Rated
- 3) Fast switching
- 4) Ease of paralleling
- 5) Simple Drive requirements

4.6 MERITS, DEMERITS AND APPLICATION

MERITS:

1. The GATE driving circuit of MOSFET is simple.
2. It can operate at the high switching frequency.
3. It has better thermal stability because the temperature coefficient of MOSFET is positive.
4. Easy to turn ON and OFF.
5. On-state resistance is low.
6. The second breakdown does not take place.

DEMERITS:

1. The on-state voltage across the MOSFET is very high. So, on-state power dissipation is high.
2. It has the asymmetric blocking capacity. They can block a high forward voltage but they cannot block high reverse voltage. Therefore, we need to connect a diode to protect the MOSFET.

APPLICATIONS:

1. Uninterrupted Power Supplies (UPS)
2. Switch Mode Power Supplies (SMPS)
3. High-frequency inverter
4. Motor control application
5. Display driver
6. In power amplifier
7. Industrial applications
8. Relay driver

CHAPTER – 5

DRIVER CIRCUIT AND POWER SUPPLY CIRCUIT

5.1 DRIVER CIRCUIT

A Power MOSFET is a voltage-controlled device that is used as a switching element in power supply circuits and motor drives, amongst other systems. The *gate* is the electrically isolated control terminal for each device. The other terminals of a MOSFET are source and drain, and for an IGBT they are called collector and emitter. To operate a MOSFET/IGBT, typically a voltage has to be applied to the gate that is relative to the source/emitter of the device. Dedicated drivers are used to apply voltage and provide drive current to the gate of the power device. This article discusses what these gate drivers are, why they are required, and how their fundamental parameters, such as timing, drive strength, and isolation, are defined.

5.2 OPTOCOUPLE ISOLATOR

There are many situations where signals and data need to be transferred from one subsystem to another within a piece of electronics equipment, or from one piece of equipment to another, without making a direct electrical connection. Often this is because the source and destination are (or may be at times) at very different voltage levels, like a microprocessor which is operating from 5V DC but being used to control a triac which is switching 240V AC. In such situations the link between the two must be an isolated one, to protect the microprocessor from over voltage damage.

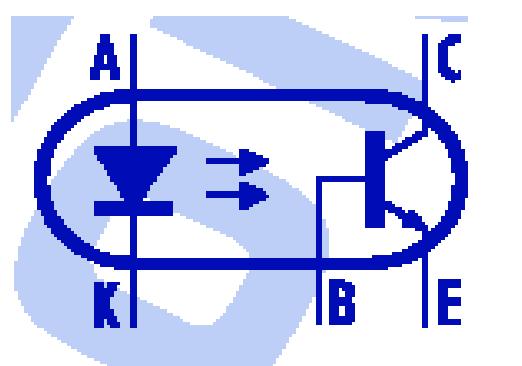


Fig.5.1

Relays can of course provide this kind of isolation, but even small relays tend to be fairly bulky compared with ICs and many of today's other miniature circuit components. Because they're electro-mechanical, relays are also not as reliable and only capable of relatively low speed operation. Where small size, higher speed and greater reliability are important, a much better alternative is to use an opto-coupler. These use a beam of light to transmit the signals or data across an electrical barrier, and achieve excellent isolation.

5.3 PROPOSED DRIVER

In contrast to bipolar transistor, MOSFETs do not require constant power input, as long as they are not being switched on or off. The isolated gate-electrode of the MOSFET forms a capacitor (gate capacitor), which must be charged or discharged each time the MOSFET is switched on or off. As a transistor requires a particular gate voltage in order to switch on, the gate capacitor must be charged to at least the required gate voltage for the transistor to be switched on. Similarly, to switch the transistor off, this charge must be dissipated, i.e. the gate capacitor must be discharged.

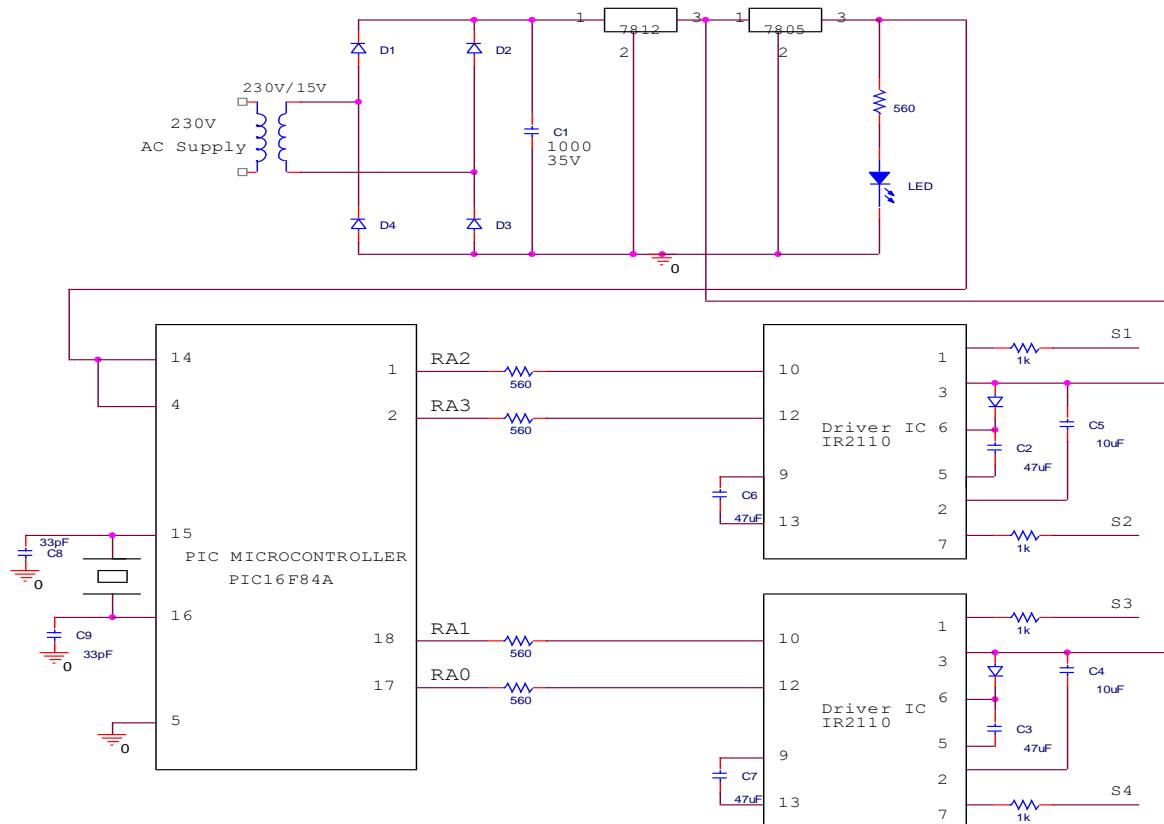


Fig.5.2

When a transistor is switched on or off, it does not immediately switch from a non-conducting to a conducting state; and may transiently support both a high voltage and conduct a high current. Consequently, when gate current is applied to a transistor to cause it to switch, a certain amount of heat is generated which can, in some cases, be enough to destroy the transistor. Therefore, it is necessary to keep the switching time as short as possible, so as to minimize switching loss. Typical switching times are in the range of microseconds. The switching time of a transistor is inversely proportional to the amount of current used to charge the gate. Therefore, switching currents are often required in the range of several hundred milli-amperes, or even in the range of amperes. For typical gate voltages of approximately 10-15V, several watts of power may be required to drive the switch. When large currents are switched at high frequencies, e.g. in DC to DC converters or large electric motors, multiple transistors are sometimes provided in parallel, so as to provide sufficiently high switching currents and switching power.

The switching signal for a transistor is usually generated by a logic circuit or a microcontroller, which provides an output signal that typically is limited to a few milli-amperes of current. Consequently, a transistor which is directly driven by such a signal would switch very slowly, with correspondingly high power loss. During switching, the gate capacitor of the transistor may draw current so quickly that it causes a current overdraw in the logic circuit or microcontroller, causing overheating which leads to permanent damage or even complete destruction of the chip. To prevent this from happening, a gate driver is provided between the microcontroller output signal and the power transistor.

5.4 POWER SUPPLY CIRCUIT

Power supply is a device that transfers electric power from a source to a load using electronic circuits. Typical application of the power supplies is to convert utility's AC input power to regulated voltage required for electronic equipment.

BASIC FUNCTIONAL UNITS:

Most electronic circuits need a DC supply such as a battery to power them. Since the mains supply is AC it has to be converted to DC to be useful in electronics. This is what a power supply does.

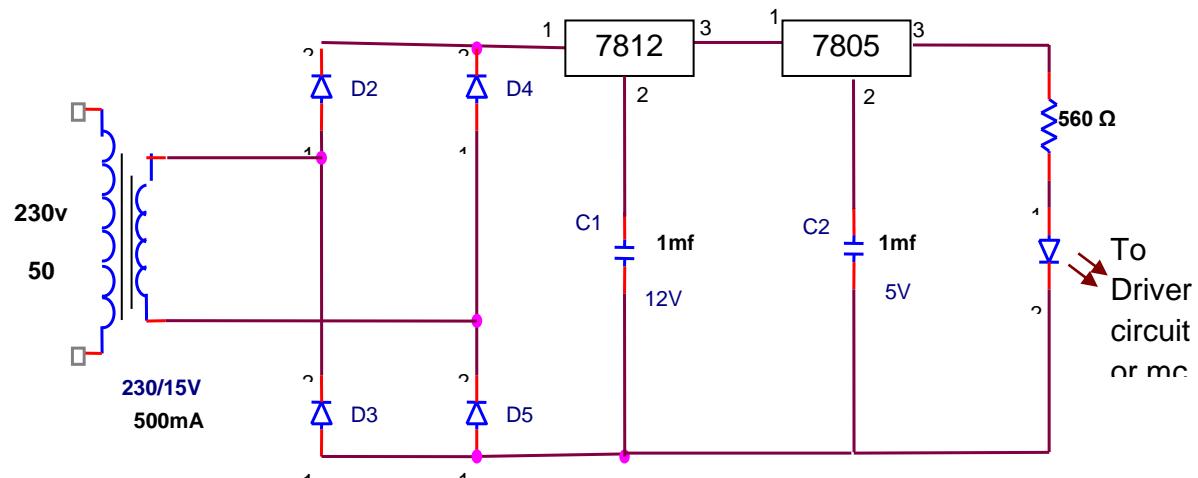


Fig 5.3: Power circuit

First the AC mains supply passes through an isolating switch and safety fuse before it enters the power supply unit.

In most cases the high voltage mains supply is too high for the electronic circuitry. It is therefore stepped down to a lower value by means of a Transformer. The mains voltage can be stepped up where high DC voltages are required.

From the transformer the AC voltage is fed to a rectifier circuit consisting of one or more diodes. The rectifier converts AC voltage to DC voltage. This DC is not steady as from a battery. It is pulsating. The pulsations are smoothed out by passing them through a smoothing circuit called a filter. In its simplest form the filter is a capacitor and resistor.

Any remaining small variations can, if necessary, be removed by a regulator circuit which gives out a very steady voltage. This regulator also removes any variations in the DC voltage

output caused by the AC mains voltage changing in value. Regulators are available in the form of Integrated Circuits with only three connections.

Each of the blocks is described in more detail below:

- Transformer - steps down high voltage AC mains to low voltage AC.
- Rectifier - converts AC to DC, but the DC output is varying.
- Smoothing - smooths the DC from varying greatly to a small ripple.
- Regulator - eliminates ripple by setting DC output to a fixed voltage.

TRANSFORMER:

A TRANSFORMER is a device that transfers electrical energy from one circuit to another by electromagnetic induction (transformer action). The electrical energy is always transferred without a change in frequency, but may involve changes in magnitudes of voltage and current. Because a transformer works on the principle of electromagnetic induction, it must be used with an input source voltage that varies in amplitude. There are many types of power that fit this description; for ease of explanation and understanding, transformer action will be explained using an AC voltage as the input source. The centertap transformer is used in the power supply unit. A center-tapped transformer and two diodes can form a full-wave rectifier that allows both half-cycles of the AC waveform to contribute to the direct current, making it smoother than a half-wave rectifier.

A **center tap** is a wire that is connected to a point half way along one of the windings of a transformer , inductor or a resistor. Center taps are sometimes used on inductors for the coupling of signals, although most tapping are not at the center but usually near one end. In the case of resistors, tapping is usually done only with potentiometers, and center tapping is just a special case of normal operation of these devices.

RECTIFIER:

Rectification is the conversion of alternating current (AC) to direct current (DC). This almost always involves the use of some device that only allows one-way flow of electrons. As we have seen, this is exactly what a semiconductor diode does. The simplest type of rectifier circuit is the half-wave rectifier, so called because it only allows one half of an AC waveform to pass through to the load:

FILTER:

This DC is not steady from a rectifier. It is pulsating. The pulsations are smoothed out by passing them through a smoothing circuit called a filter. In its simplest form the filter is a capacitor and resistor.

CHAPTER – 6

PROPOSED TOPOLOGY AND MODULATION STRATEGY

6.1 HERIC INVERTER

A Highly Efficient and Reliable Inverter Concept (HERIC) is designed by adding two extra switches connected across the AC output side in a full bridge inverter. Each pair of the diagonal switches is operated at high switching frequency during one half of the grid voltage. Fig.6.1 shows the circuit diagram of the HERIC topology. Similar to the H5 topology there are four operating modes available for the HERIC topology. They are:

- Mode 1: Active Conduction mode in positive half period
- Mode 2: Freewheeling mode in positive half period
- Mode 3: Active Conduction mode in negative half period
- Mode 4: Freewheeling mode in negative half period

In the Active Conduction modes by the switching pair action of semiconductor devices S1 to S4, the power is supplied to the utility grid. In the freewheeling mode, the switch S5 is turned ON during the positive half period and hence the current freewheels through the switch S5 and the anti-parallel diode of the switch S6. Similarly in the negative half period of the freewheeling mode, the switch S6 is turned ON and the output current freewheels through the anti-parallel diode of the switch S5 and the switch S6.

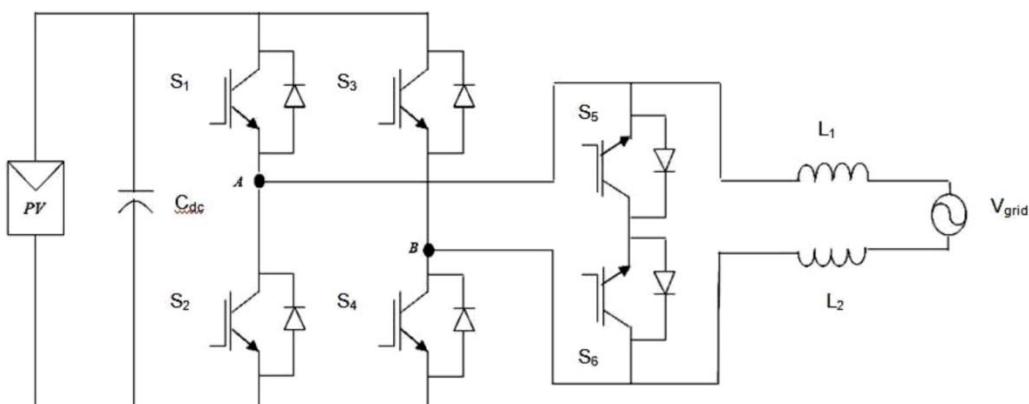


Fig.6.1

Thus AC voltage decoupling is accomplished by shorting the AC side of the inverter during zero voltage states. Fig.6.2 illustrates the PWM firing schemes for the HERIC topology for switches S1 to S6. The effect of this decoupling has a major advantage that this prevents the output current to flow through the diodes of the full H-bridge. This topology maintains the voltage across the PV panel to be floating in nature and hence achieve a constant common mode voltage.

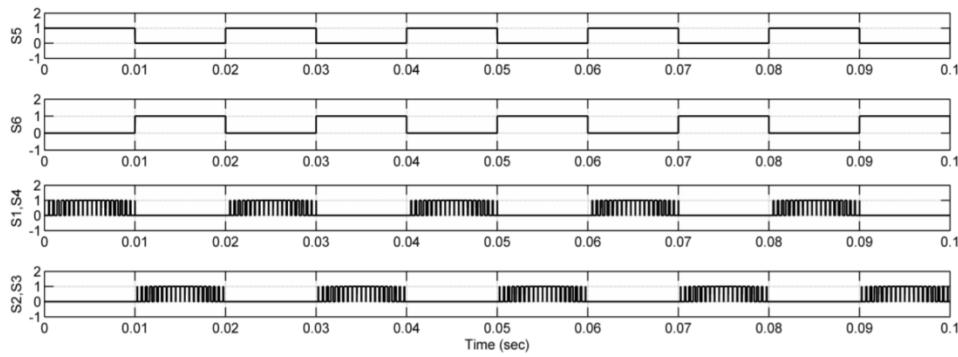


Fig.6.2

The efficiency of the inverter is substantially increased, without affecting the common mode behaviour of the whole system. Since there is no common mode voltage generated, the leakage current through the parasitic capacitance would be very small. Fig.6.3 illustrates the common mode leakage current for HERIC topology. The HERIC topology has been developed to exhibit inherently very high conversion efficiency over a wide working range compared to other topologies. The operation of the bidirectional switch with the grid frequency reduces switching losses than other topologies.

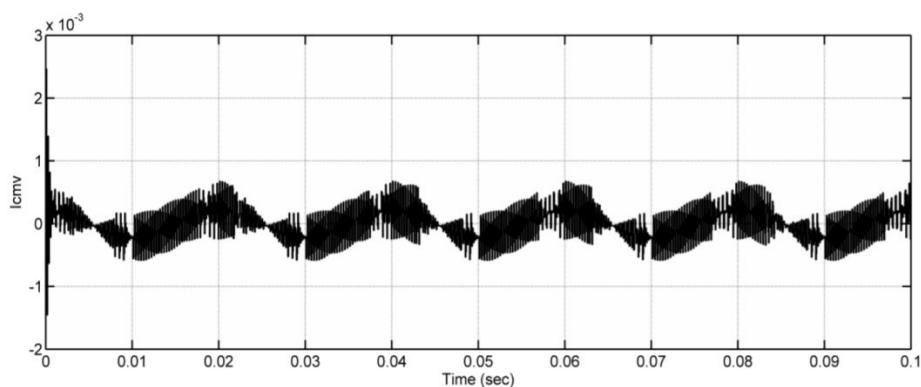


Fig.6.3

6.2 PROPOSED INVERTER TOPOLOGY

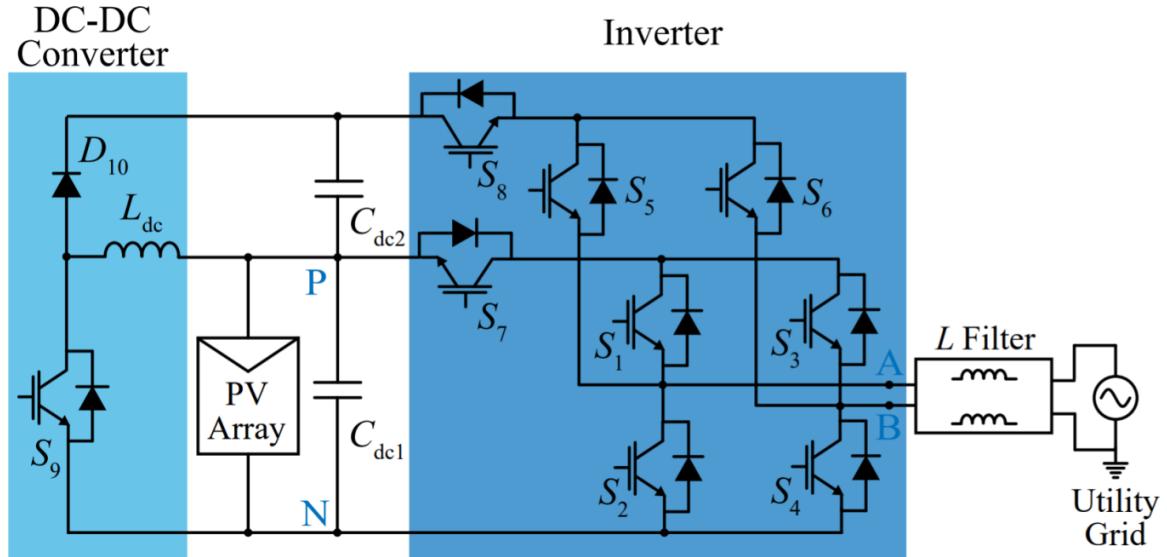


Fig.6.4

The proposed inverter topology is depicted in Fig. 6.4. It incorporates a HERIC inverter configuration (S1-S6) with two additional semiconductor switches (S7 and S8) respectively. The circuit is designed to work in two distinct modes of operation namely three-level mode and five-level mode. When the PV array output voltage is greater than the peak grid voltage, S7 is kept on and S8 is kept off. This enables the circuit to operate as a HERIC inverter using switches S1-S6. The dc-dc converter (consisting of S9, Ldc and D10) remains off during this mode. This enables the three-level mode of operation, similar to a HERIC inverter. In case the PV array output voltage falls below the peak grid voltage, the dc-dc converter is energized. This leads to a transfer of power from the PV to the second dc-link capacitor Cdc2 such that total dc-link voltage ($V_{dc1} + V_{dc2}$) becomes more than the peak grid voltage. This mode of operation gives a five-level inverter voltage output which shows the multilevel operation of the proposed circuit while operating under low PV voltage conditions. The voltage across Cdc2 is V_{dc2} and is used by the inverter only when the instantaneous grid voltage is more than the PV array voltage (V_{dc1}), as shown in Fig.6.5 During the period when the instantaneous grid voltage is less than the PV voltage, V_{dc1} , power is directly used from PV. Therefore, the dc-dc converter only processes a fraction of the total PV power. Most of the power flows directly from PV to the inverter, thereby leading to higher efficiency even at low PV voltage as compared to the use of dc-dc boost converter in cascade with conventional inverters. This concept is represented using block diagram as shown in Fig.6.6. The conventional structure is shown in Fig.6.6(a) and the partial power processing structure is shown in Fig.6.6(b).

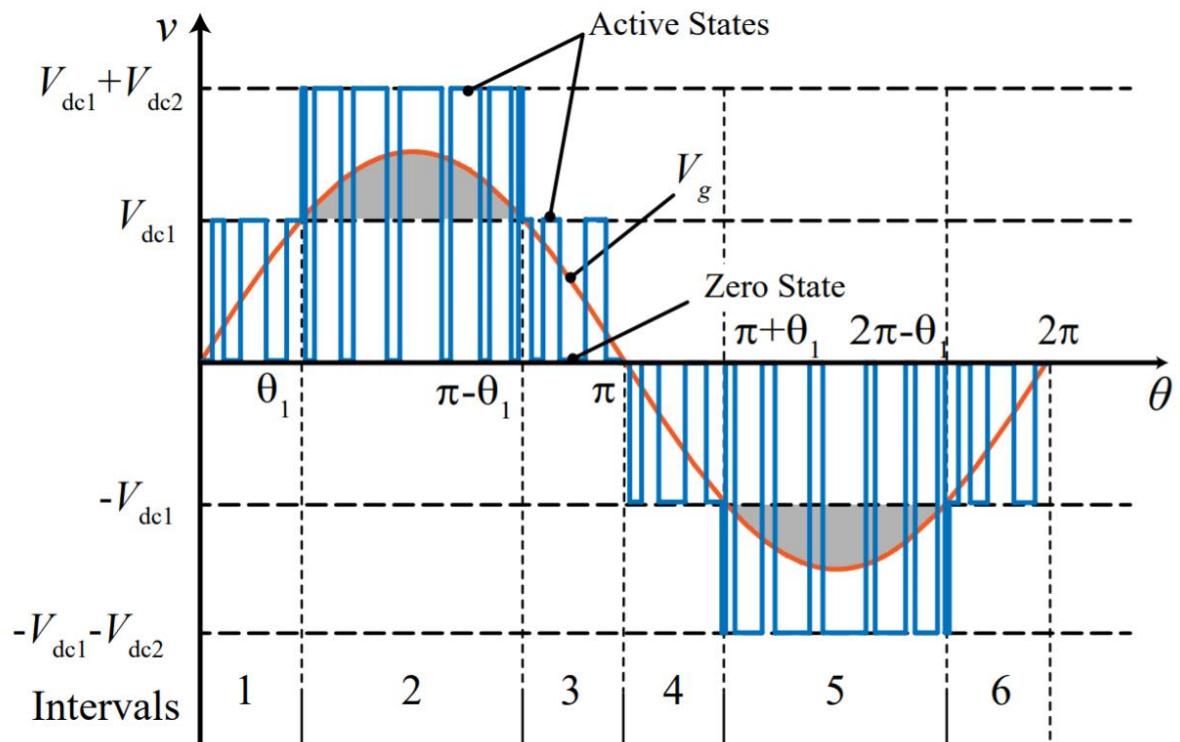


Fig.6.5

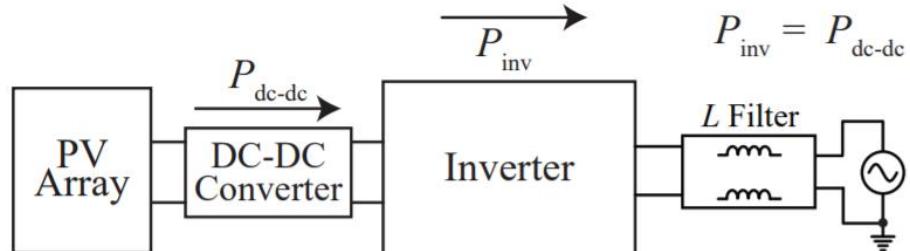


Fig.6.6(a)

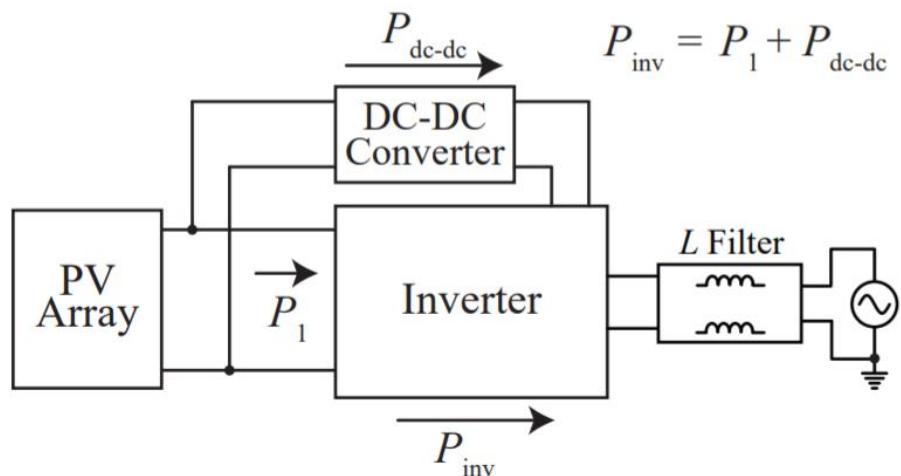


Fig.6.6(b)

6.3 OPERATION

There are three states of operation, they are:

- 3-level mode of operation
- 5-level mode of operation
- Zero state of operation

6.3.1 THREE-LEVEL MODE OF OPERATION

- ***POSITIVE HALF CYCLE (Mode 1 and 3)***

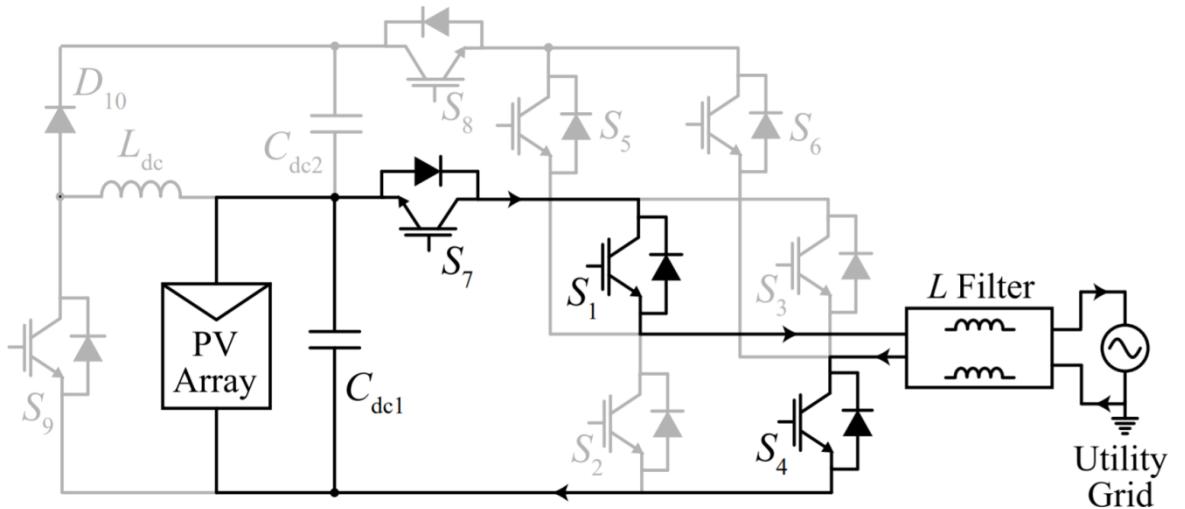


Fig.6.7

In this interval, the inverter output voltage is realized using an active (V_{dc1}) state and a zero state. The active state is achieved by turning on the devices S_1 , S_4 and S_7 . The path for the flow of current in this state is shown in Fig.6.7. In order to achieve the zero state S_5 and S_6 are turned on and the grid current freewheels through the devices (S_5 , D_6 or S_6 , D_5) as shown in Fig.6.11. The dc-dc converter remains non-energized. During this interval, S_5 and S_7 are continuously kept on, thereby avoiding switching loss in these devices.

In general, S_1 , S_4 , S_7 are turned on.

$$V_o = V_{dc1}$$

- **NEGATIVE HALF CYCLE (Mode 4 and 6)**

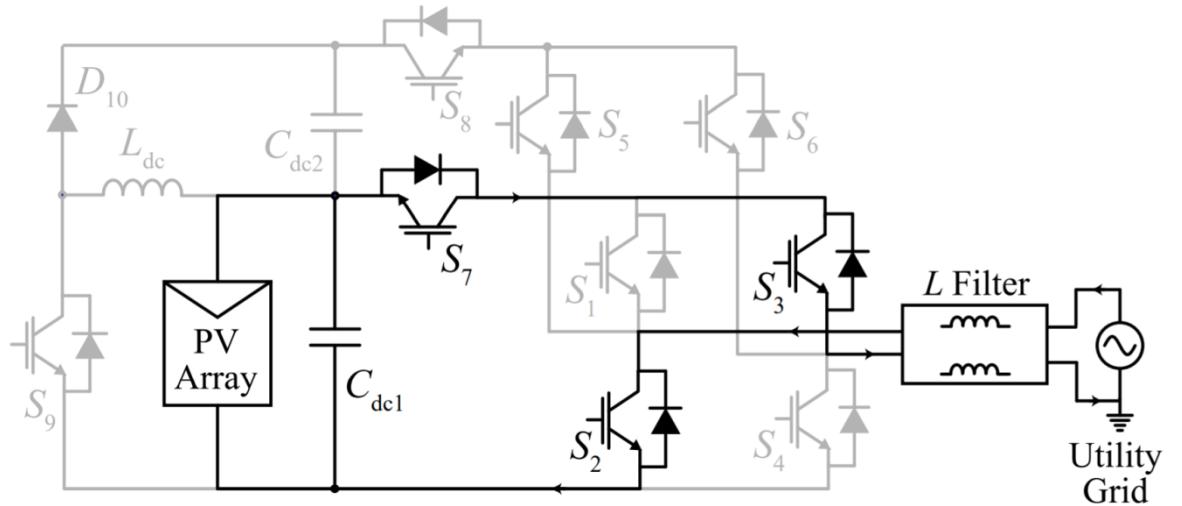


Fig.6.8

In this interval, the reference signal lies between zero and $-V_{dc1}$. The zero state is realized as shown in Fig.6.11. For the active state $-V_{dc1}$, S_2 , S_3 and S_7 are turned on, as shown in Fig.6.8. The dc-dc converter remains off in this mode.

In general, S_2 , S_3 , S_7 are turned on.

$$V_o = - (V_{dc1})$$

6.3.2 FIVE LEVEL MODE OF OPERATION

- **POSITIVE HALF CYCLE (Mode 2)**

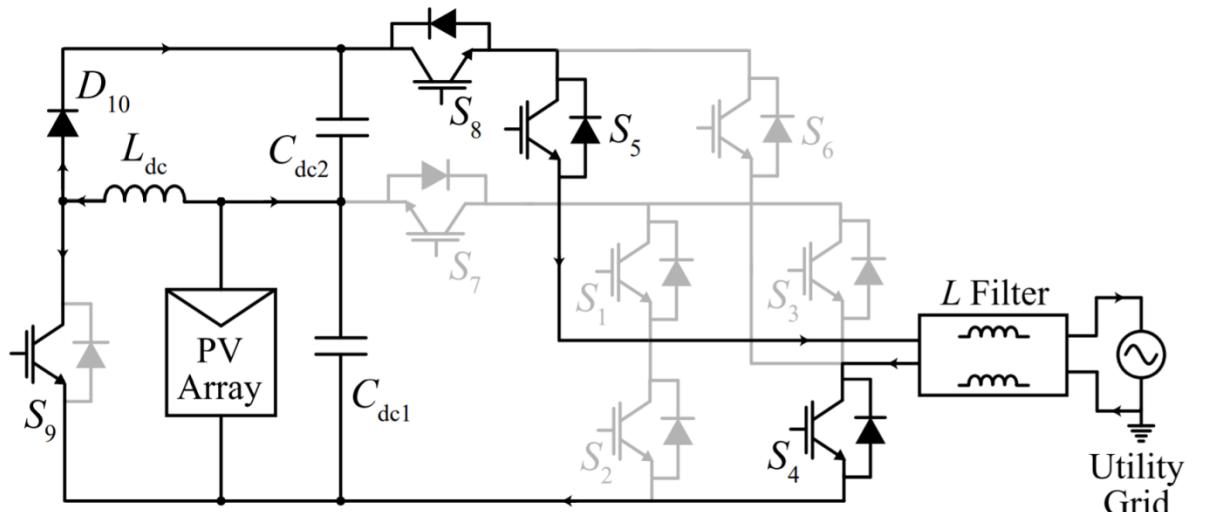


Fig.6.9

During this interval, the inverter output voltage lies between the zero state and the active state ($V_{dc1} + V_{dc2}$). Zero state is realized by turning on S_5 and S_6 as shown in Fig.6.11. To realize the active state of $V_{dc1} + V_{dc2}$, switches S_4 , S_5 and S_8 are turned on, as shown in Fig.6.9. Since the capacitor C_{dc2} is used, the voltage across it is maintained by the boost converter (S_9 , D_{10} , L_{dc}).

In general, S_4 , S_5 , S_8 are turned on.

$$V_o = (V_{dc1} + V_{dc2}).$$

- **NEGATIVE HALF CYCLE (Mode 5)**

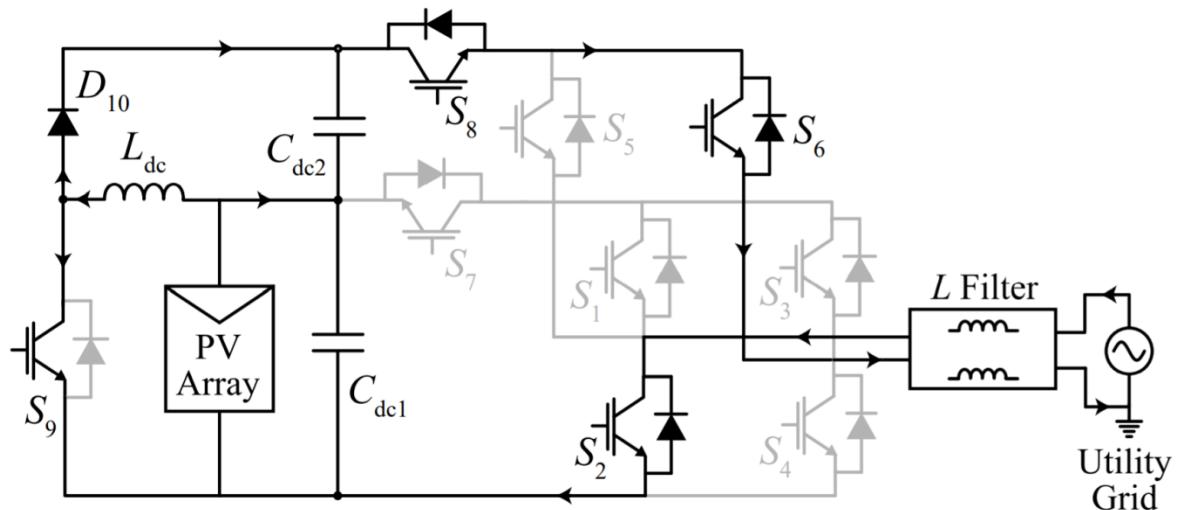


Fig.6.10.

In this mode, an active state ($-V_{dc1} - V_{dc2}$) and a zero state are used. The active state is realized by turning on the switches S_2 , S_6 and S_8 , as shown in Fig.6.10. The dc-dc converter maintains voltage across C_{dc2} during this mode.

In general, S_2 , S_6 , S_8 are turned on.

$$V_o = -(V_{dc1} + V_{dc2}).$$

6.3.3 ZERO STATE OF OPERATION

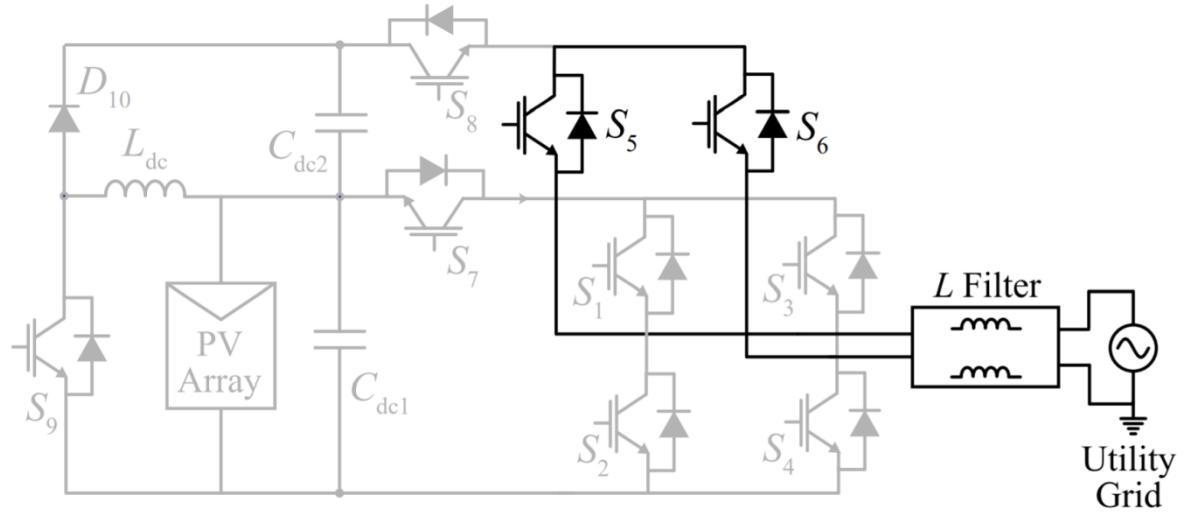


Fig.6.11

In order to achieve the zero state S5 and S6 are turned on and the grid current freewheels through the devices (S5, D6 or S6, D5) as shown in Fig.6.11

6.4 SWITCHING CONFIGURATION

MODES	S1	S2	S3	S4	S5	S6	S7	S8	
1	I	I	0	0	I	0	0	I	0
2	0	0	0	I	I	0	0	I	
3	I	0	0	I	0	0	I	0	
4	0	I	I	0	0	0	I	0	
5	0	I	0	0	0	I	0	I	
6	0	I	I	0	0	0	I	0	

Tab.6.1.

6.5. MODULATION STRATEGY

The modulation strategy is based on the Phase Opposition Disposition (POD) sinusoidal PWM technique as shown in Fig. 5. Carriers C1 and C3 have peak values of ($V_{dc1} + V_{dc2}$) and ($-V_{dc1} - V_{dc2}$), whereas the peak value of C2 and C4 are V_{dc1} and $-V_{dc1}$, respectively. C2 is compared with a sinusoidal reference in the positive half cycle during Modes 1 and 3 to generate switching signals for S1, S4 and S7 whereas C1 is compared with the reference signal in Mode 2 to generate the switching signal for S8. The switching signals for S5 and S6 are complementary of S2 and S4, respectively. Similarly, during the negative half cycle C4 is compared with the reference signal during Modes 4 and 6 to generate switching signals for S2, S3 and S7. C3 is compared with the reference signal in Mode 5 to generate switching signal for S8. This strategy enables a multilevel (five level) operation of the inverter. It should be noted that, this modulation strategy ensures a low leakage current in the PV system, which is imperative for grid-connected applications. The CM voltage (u_{cm}) is given by

$$u_{cm} = \frac{u_{AN} + u_{BN}}{2}$$

where,

u_{AN} is the voltage between Node A and Node N

u_{BN} is the voltage between Node B and Node N

as shown in Fig.6.4.

The CM voltages for each state is derived and provided in Fig.6.12.

It is concluded that since the CM voltages for both the states are an interval are equal, there would not be any high frequency oscillations in the CM voltage. This would suppress the flow of leakage current

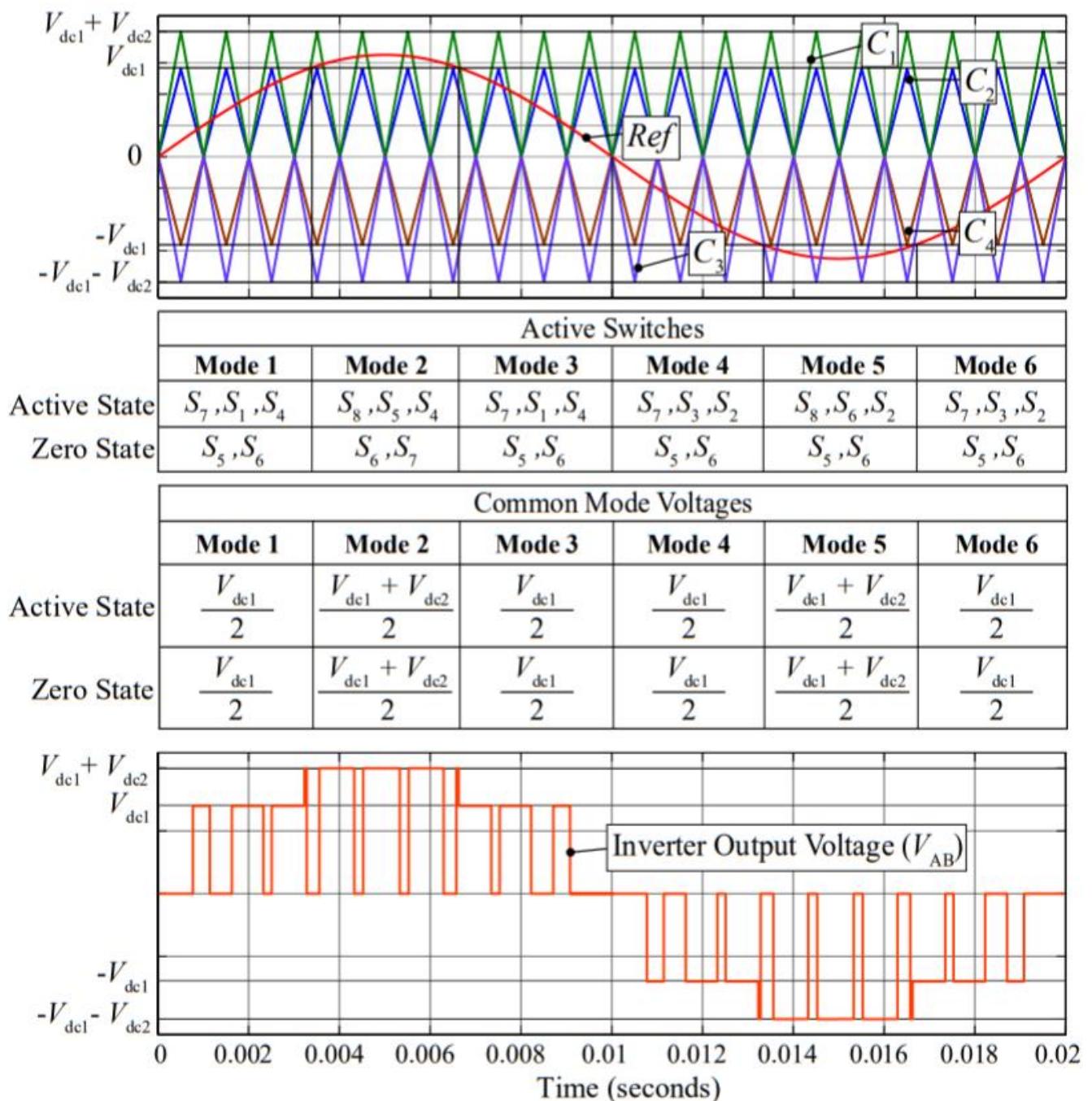


Fig.6.12

6.6 CONCLUSION

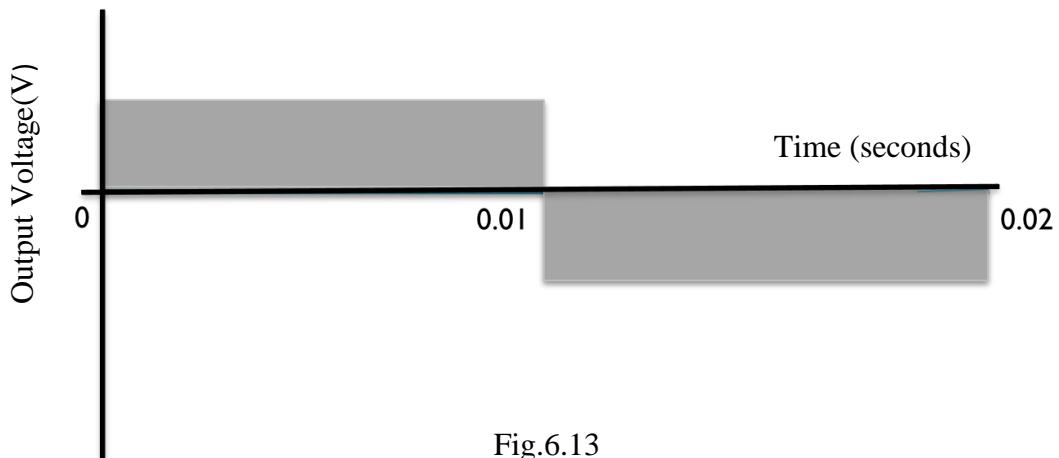


Fig.6.13

Three level output operates in modes 1 and 3 during positive cycles which is for the time period of 0.01 seconds in case of a 50 Hz system and operates in mode 4 and 6 during negative cycle for the time period between 0.01 and 0.02 in case of a 50Hz system forming the three level output.

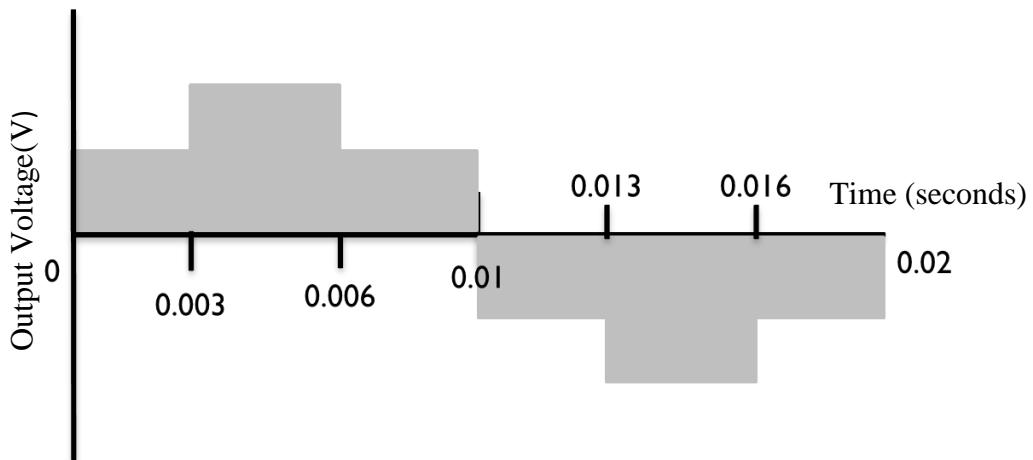


Fig.6.14

Five level output operates in mode 1 for the time period between 0 and 0.003, mode 2 for the time period between 0.003 and 0.006, mode 3 for the time period between 0.006 and 0.01 during positive cycles which is for the time period of 0.01 seconds in case of a 50 Hz system and operates in mode 4 for the time period between 0.01 and 0.013, mode 5 for the time period between 0.013 and 0.016, mode 6 for the time period between 0.016 and 0.02 during negative cycle for the time period between 0.01 and 0.02 in case of a 50Hz system forming the Five level output.

CHAPTER – 7

SIMULATION RESULTS

7.1 OVERALL CIRCUIT

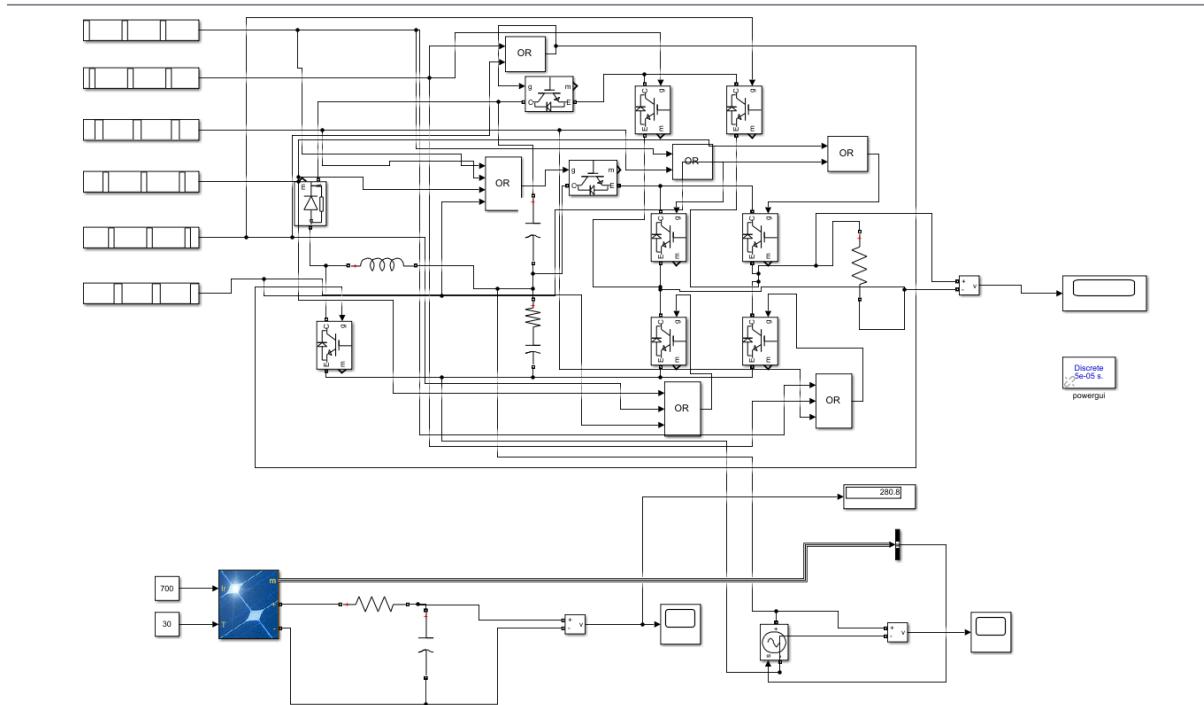


Fig. 7.1

7.2 INPUT VOLTAGE

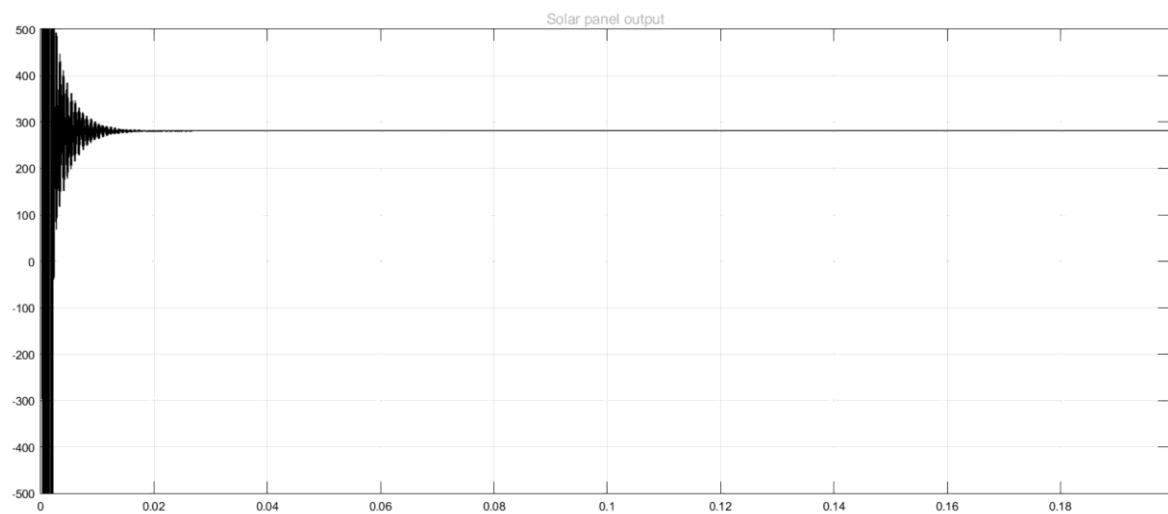


Fig. 7.2

7.3PULSE PATTERN

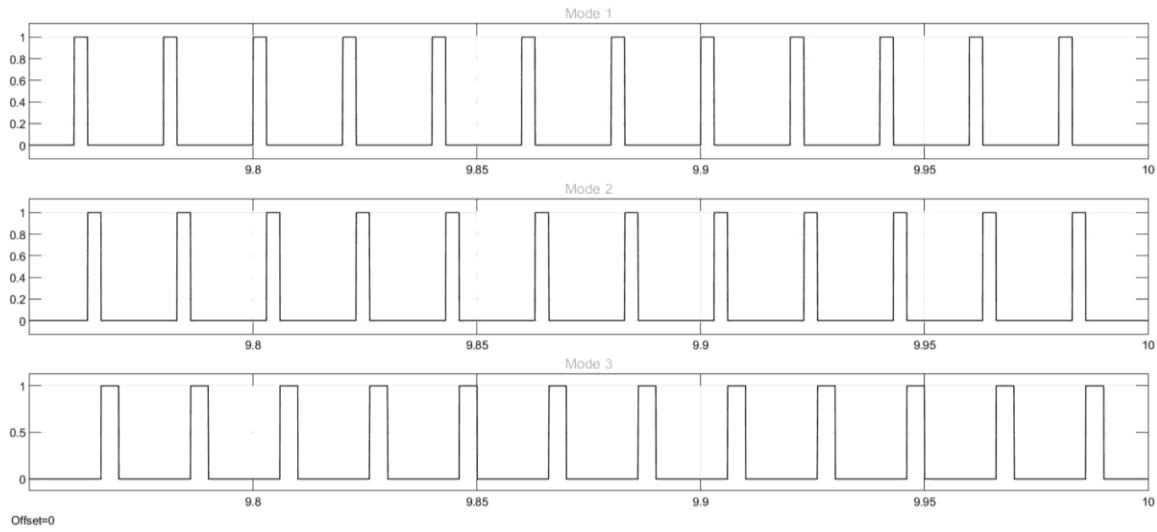


Fig.7.3.1

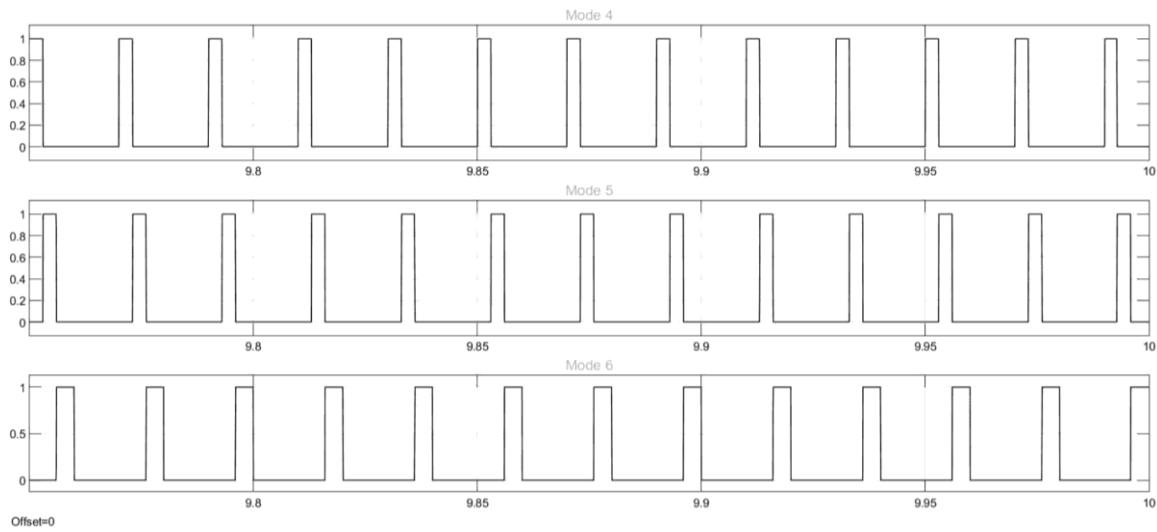


Fig.7.3.2

7.4 THREE LEVEL OUTPUT

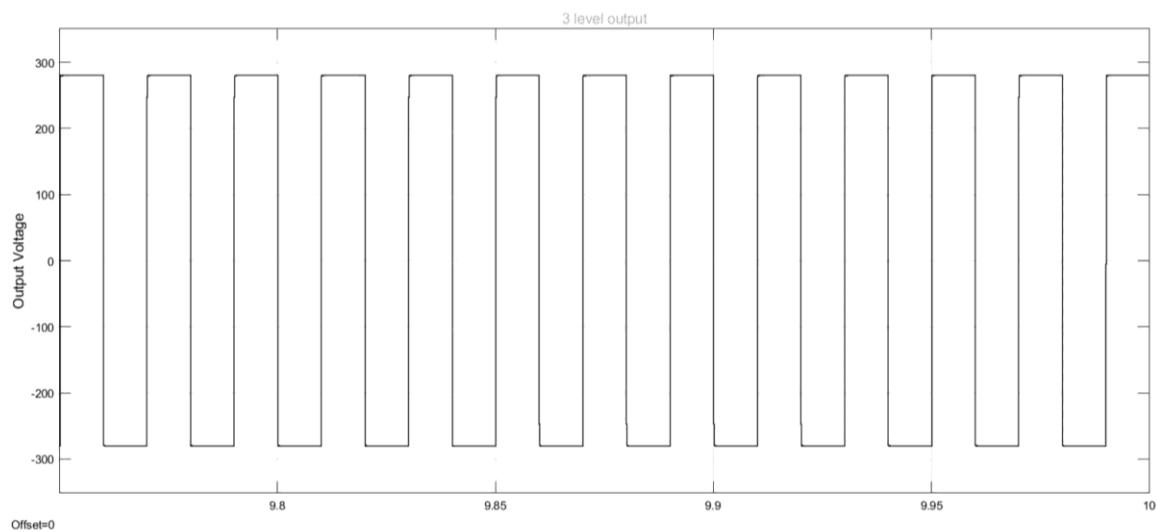


Fig.7.4

7.5 FIVE LEVEL OUTPUT

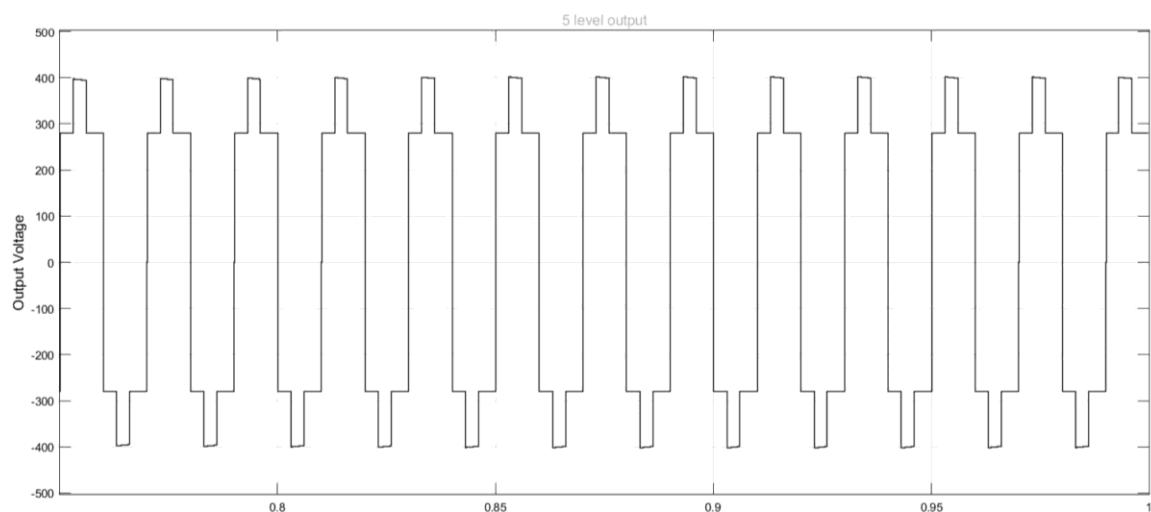


Fig.7.5

7.6 SIMULATION BY SPWM

7.6.1 OVERALL CIRCUIT

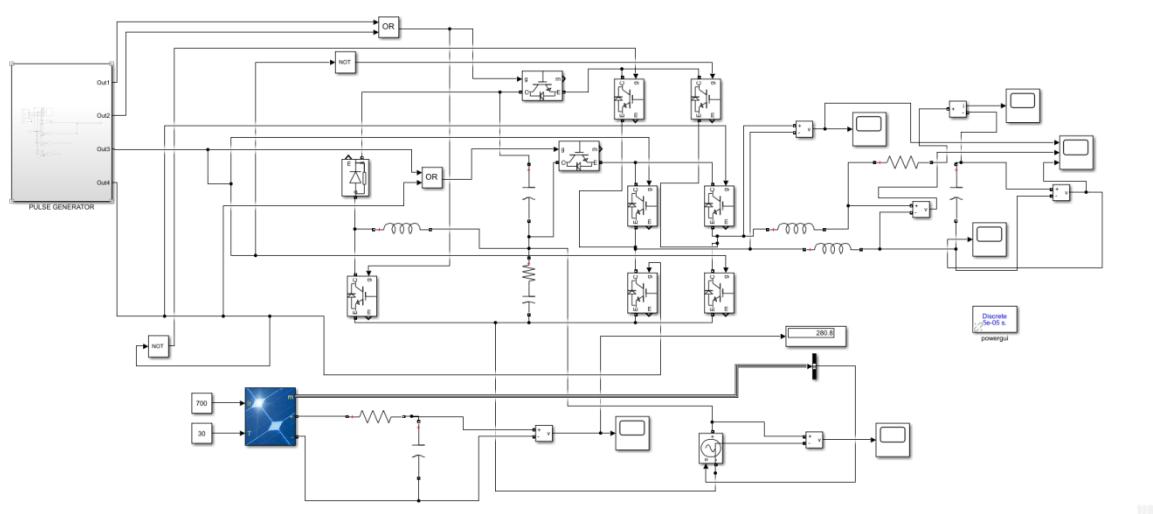


Fig.7.6.1

7.6.2 INPUT VOLTAGE

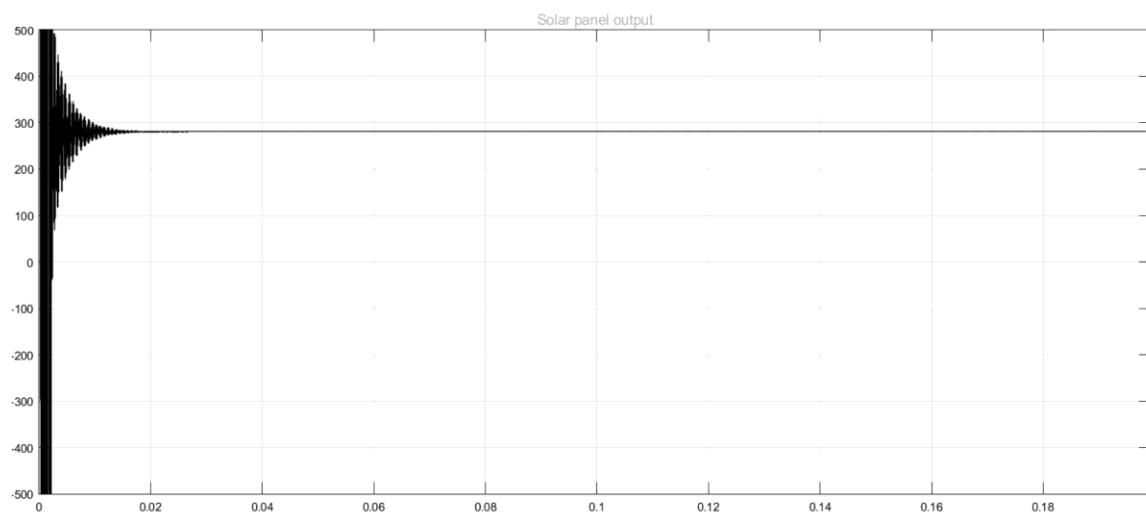


Fig.7.6.2

7.6.3 PULSE GENERATION

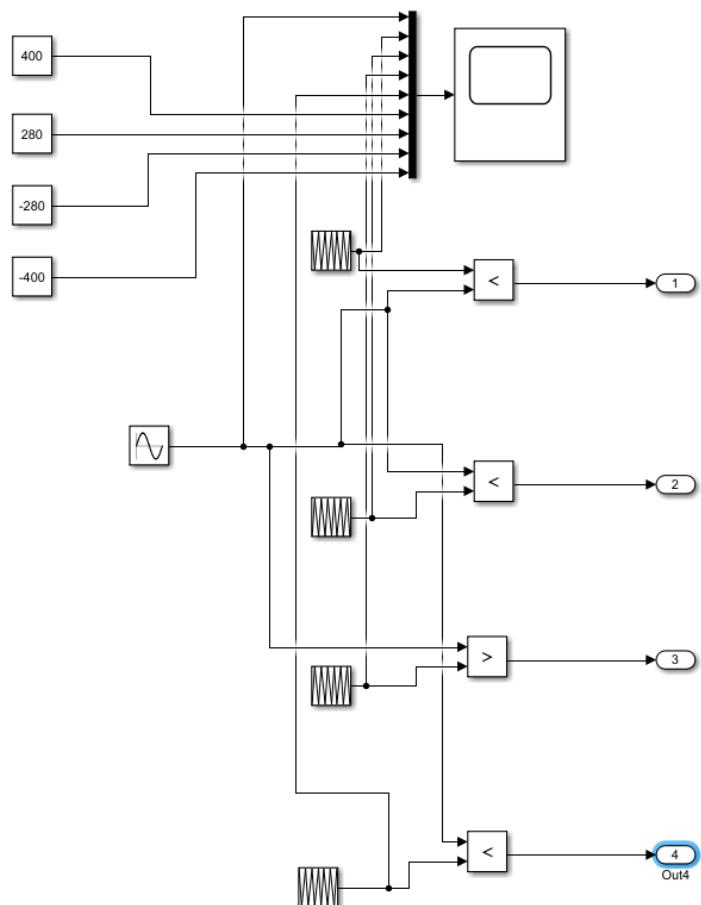


Fig.7.6.3

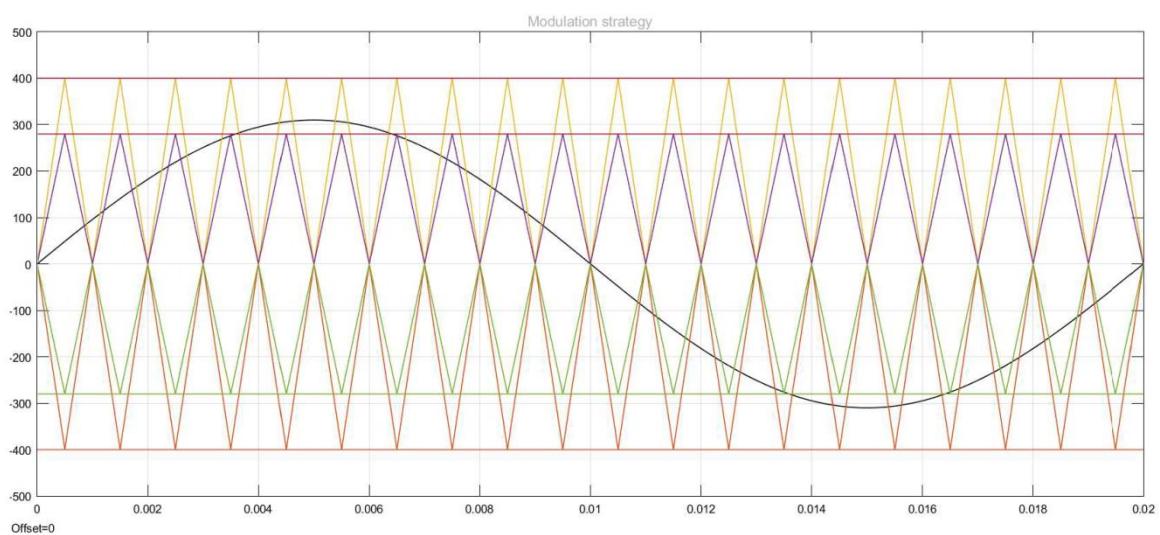


Fig.7.6.4

7.6.4 THREE LEVEL OUTPUT

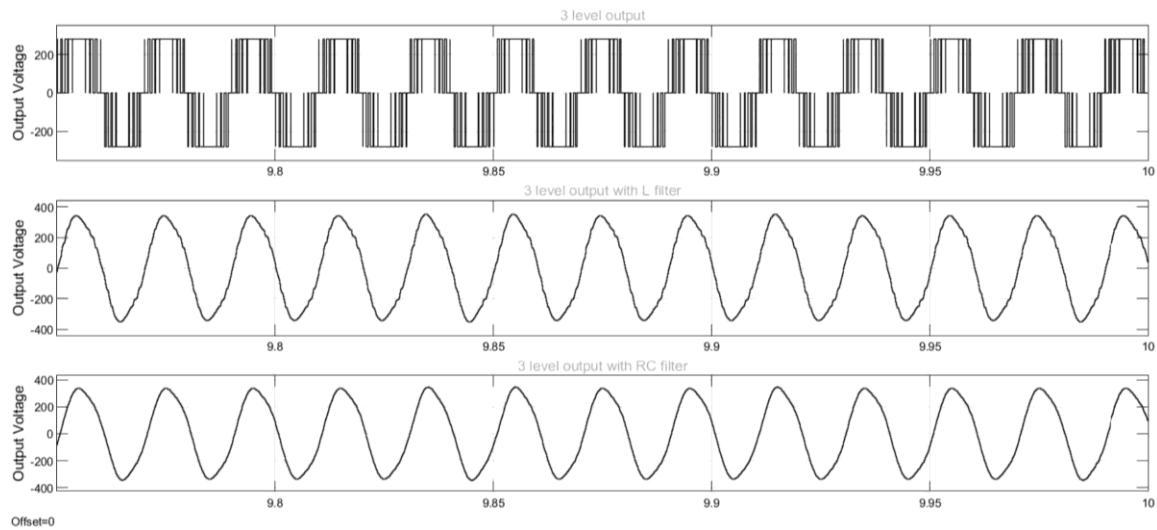


Fig.7.6.5

7.6.5 FIVE LEVEL OUTPUT

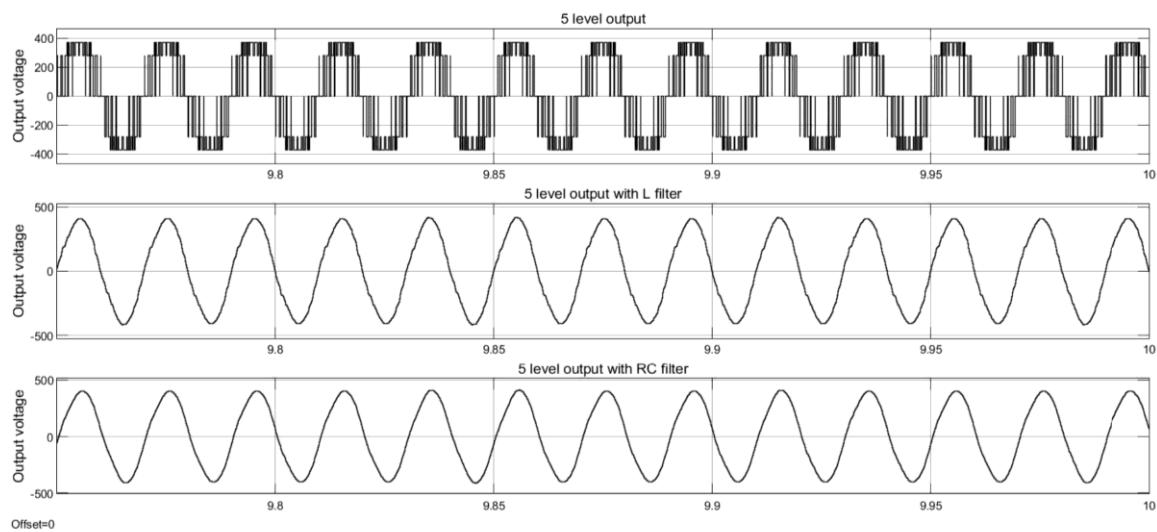
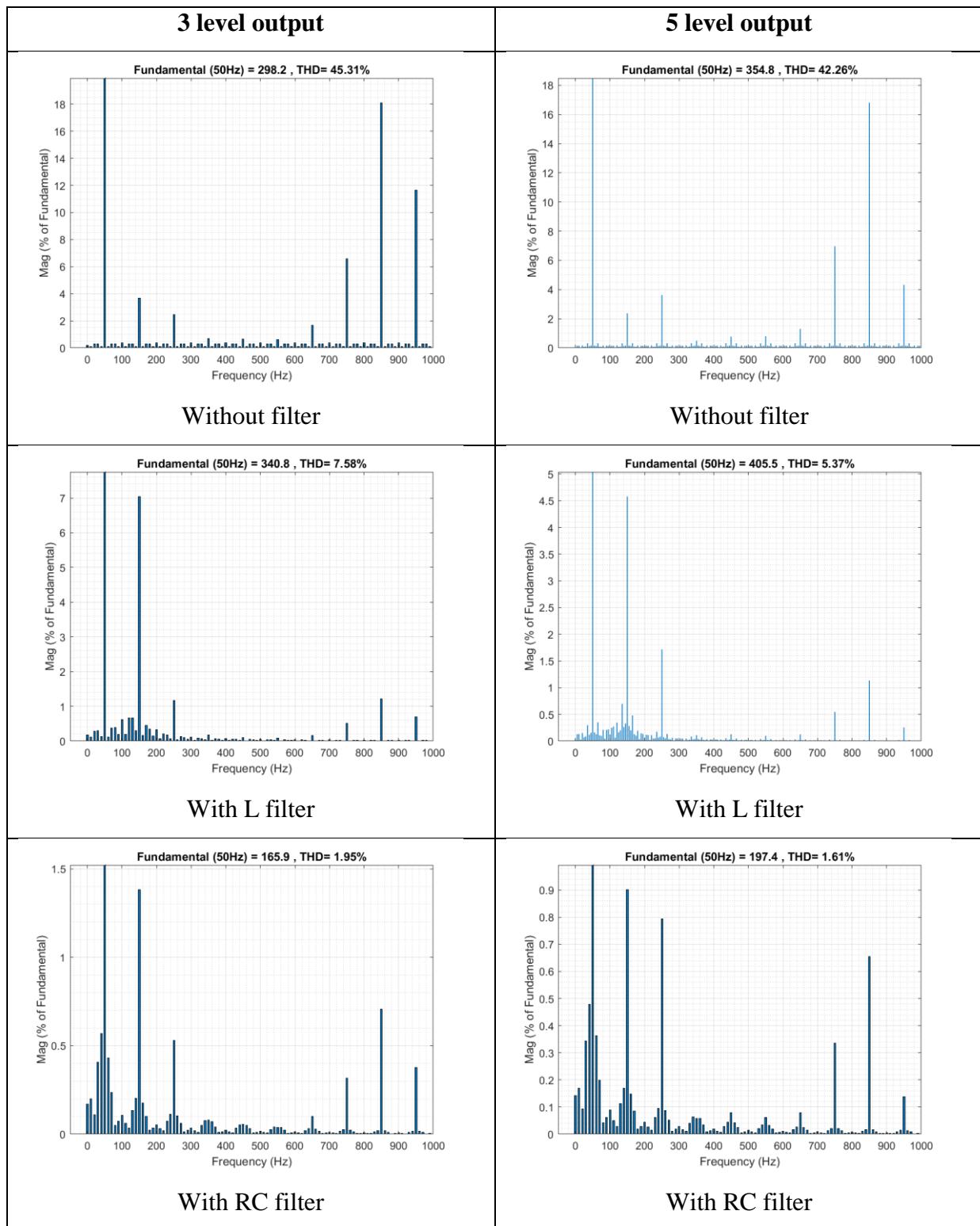


Fig.7.6.6

7.6.6 THD ANALYSIS



7.7 SUMMARY

All the simulation results of the proposed system are explained in this chapter. These simulation results are achieved through MATLAB Simulink tool. From these waveforms, the characteristics of the system are studied.

Input voltage(DC)	280 V
Output voltage(AC) 3-level mode of operation	280 V
Output voltage(AC) 5-level mode of operation	400 V
Extended DC- DC converter voltage	120 V

Tab.7.1

CHAPTER - 8

HARDWARE IMPLEMENTATION

8.1 OVERVIEW OF KIT

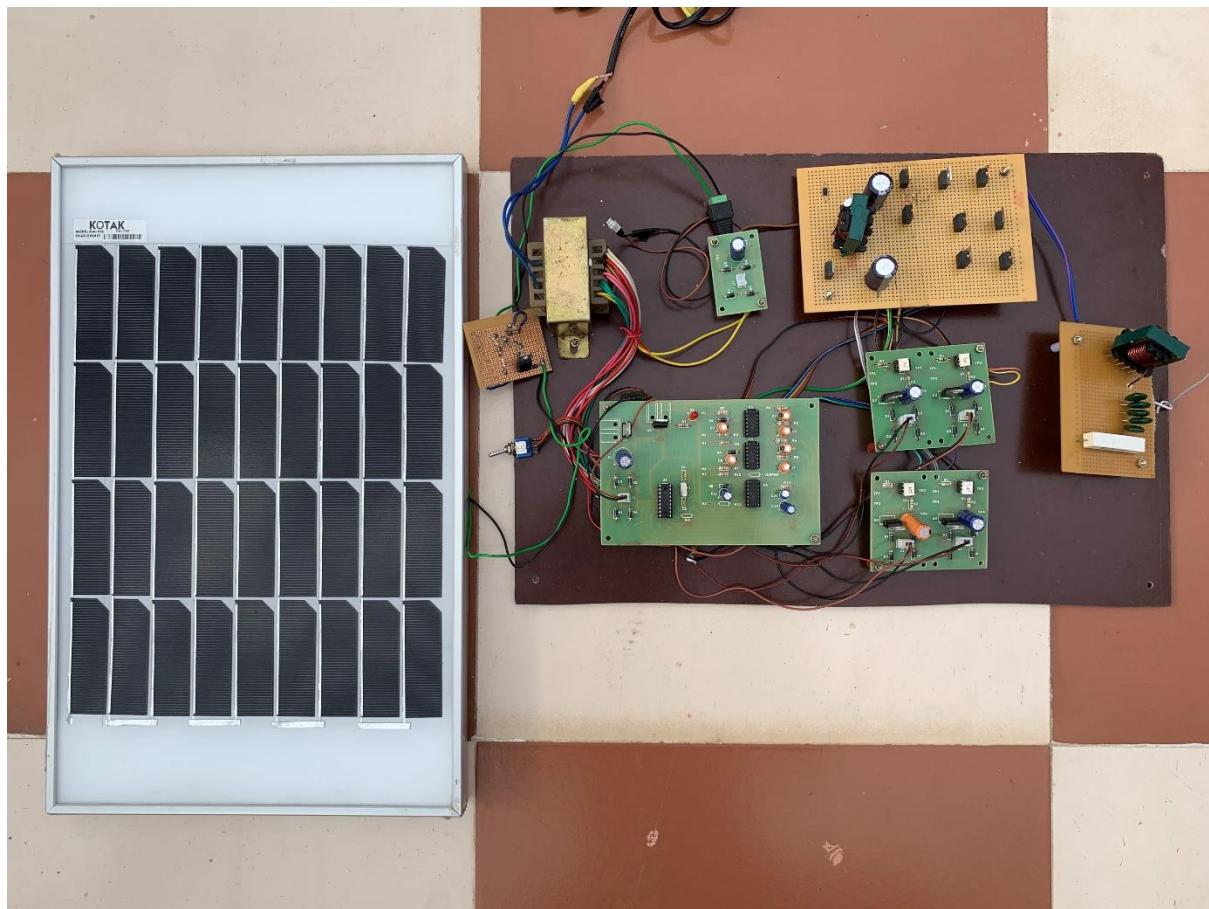


Fig.8.1

8.2 GATE PULSES



Fig.8.2 Switch 1

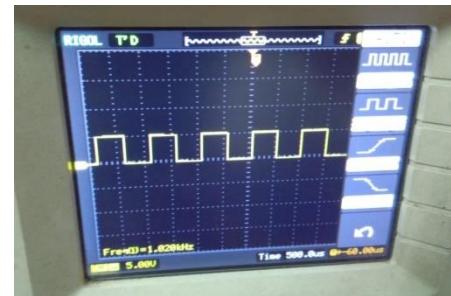


Fig.8.3 Switch 2

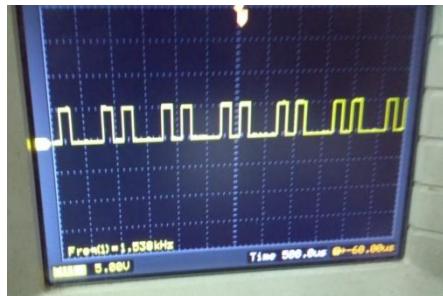


Fig.8.4 Switch 3

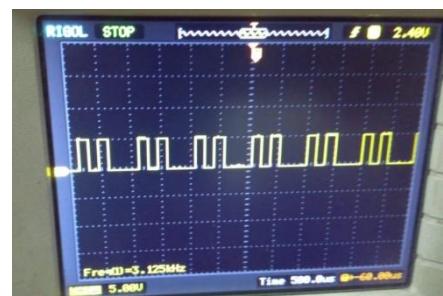


Fig.8.5 Switch 4



Fig.8.6 Switch 5

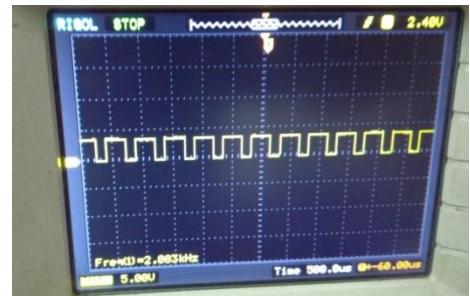


Fig.8.7 Switch 6

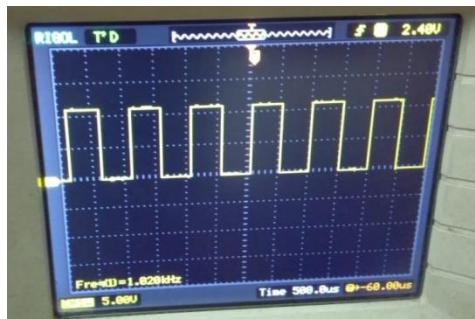


Fig.8.8 Switch 7

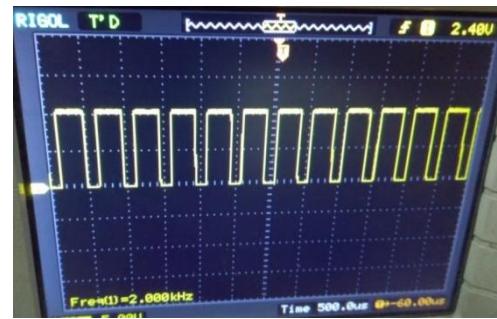


Fig.8.9 Switch 8 &9

8.3 OUTPUT WAVEFORM

8.3.1 THREE LEVEL OUTPUT WAVEFORM



Fig.8.10

8.3.2 FIVE LEVEL OUTPUT WAVEFORM



Fig.8.11

8.3.3 THREE LEVEL OUTPUT WAVEFORM WITH FILTER



Fig.8.12

8.3.4 FIVE LEVEL OUTPUT WAVEFORM WITH FILTER



Fig.8.13

8.4 COMPONENT SPECIFICATIONS

Diode	Uf4007, 1A,1000V
MOSFET	IRF830,8A,500V
Input filter capacitor	1000UF,35V
INPUT Inductor	3mH
Filter inductor L_f	1 mH
Filter capacitor C_f	400 nF
Load resistor	500 OHM
Input voltage	13.6 DC
Switching frequency	1KHZ
Output voltage	30V

Tab.8.1

8.5 OUTPUT COMPARISON

Mode	Input voltage	3-level output (voltage)	DC-DC extended (voltage)	5-level output (voltage)
Simulation	280	280	120	400
Hardware	15	20	14	30

Tab.8.2

CHAPTER – 9

CONCLUSION

An integrated dc-dc converter based transformer-less PV inverter with a wide input voltage range is presented in this project. The proposed inverter topology incorporates a HERIC inverter configuration (S1 to S6) with two additional semiconductor switches (S7 and S8) respectively of which switch is used to control the output voltage level depending on the PV array voltage. The circuit is designed to work in two distinct modes of operation namely three-level mode and five-level mode. In normal mode of operation the expected three level output voltage (280 V AC) is achieved and during the period when the PV array output voltage falls below the peak grid voltage, the switch which is responsible for five level mode of operation is turned ON and the required five level output voltage(400 V AC) is achieved.

The main characteristics of the proposed inverter are summarized as follows:

1. Higher efficiency even at low solar radiations, since there is no double stage conversion of power.
2. Multi-levels in the inverter output voltage is achieved when the dc-dc converter is energized, which improves the quality of the grid current.

From the results derived it can be concluded that the proposed inverter topology is suitable for grid-connected transformer-less single-phase PV applications especially for wide variations in solar PV voltage.

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APPENDIX

PIC16F88 CODE:

```
del equ 3ch
del1 equ 3dh
del2 equ 3eh

org 000h
bsf STATUS,5
movlw 00h
movwf TRISB
    movlw 03h
movwf TRISA
movlw 00h
movwf ANSEL
bcf STATUS,5

start: btfss porta,1
        goto two

        movlw 49h
        movwf PORTB
        call delay

        movlw 98h
        movwf PORTB
        call delay

        movlw 49h
        movwf PORTB
        call delay

        movlw 46h
        movwf PORTB
        call delay

        movlw 0a2h
        movwf PORTB
        call delay

        movlw 46h
        movwf PORTB
        call delay
        goto start

two:   movlw 49h
        movwf PORTB
```

```
call delay
call delay

    movlw 00h
    movwf PORTB
    call delay

    movlw 46h
    movwf PORTB
    call delay
    call delay

    movlw 00h
    movwf PORTB
    call delay

    goto start

delay:
    movlw 05h
    movwf del2
loop1: movlw 34h
    movwf del
loop:   decfsz del, 1
        Goto loop
        decfsz del2, 1
        Goto loop1
Return
```