Homework 1

Computer Organization and Architecture
CSCI 361, Fall 2014

Due: September 19, 2014 in class

Instructions: Complete the problems enumerated below. Answers must typed and neatly formatted. You will submit a printed hardcopy of your work at the **beginning** of class on the specified due date. Be sure to include your name and email address on your submission.

Processor	Clock Rate	CPI
P1	3.0 GHz	1.5
P2	2.5 GHz	1.0
P3	4.0 GHz	2.2

Problem 1.5a [5 points]: Which processor has the highest performance expressed in instructions per second?

Problem 1.5b [5 points]: If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

Problem 1.5c [10 points]: We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction.

Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D).

	Instr. Class CPI				Clock Rate
	A	**B**	**C**	**D**	
P1	1	2	3	3	2.5 GHz
P2	2	2	2	2	3.0 GHz

You are given a program with a dynamic instruction count of 1.0E6 instructions divided into class as follows:

- 10% class A,
- 20% class B,
- 50% class C, and
- 20% class D.

Problem 1.6a [10 points] What is the global CPI for each implementation?

Problem 1.6b [10 points] Find the clock cycles required in both cases.

The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power.

The Core i5 Ivy Bridge, released in 2012, has a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

Problem 1.8.1 [5 points] For each processor find the average capacitive loads.

Problem 1.8.2 [5 points] Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.

Problem 1.8.3 [10 points] If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? (Note: power is defined as the product of voltage and current.)

The results of the SPEC CPU2006 bzip2 benchmark running on an AMD Barcelona has an instruction count of 2.389E12, an execution time of 750 s, and a reference time of 9650 s.

Problem 1.11.1 [5 points] Find the CPI if the clock cycle time is 0.333 ns.

Problem 1.11.2 [5 points] Find the SPECratio.

Problem 1.11.4 [5 points] Find the increase in CPU time if the number of instructions of the benchmark is increased by 10% and the CPI is increased by 5%.

Problem 1.11.6 [10 points] Suppose that we are developing a new version of the AMD Barcelona processor with a 4 GHz clock rate. We have added some additional instructions to the instruction set in such a way that the number of instructions has been reduced by 15%. The execution time is reduced to 700 s and the new SPECratio is 13.7. Find the new CPI.

Another pitfall cited in Section 1.10 is expecting to improve the overall performance of a computer by improving only one aspect of the computer. Consider a computer running a program that requires 250 s, with 70 s spent executing FP instructions, 85 s executed L/S instructions, and 40 s spent executing branch instructions.

Problem 1.13.1 [5 points] By how much is the total time reduced if the time for FP operations is reduced by 20%?

Problem 1.13.2 [5 points] By how much is the time for INT operations reduced if the total time is reduced by 20%?

Problem 1.13.3 [5 points] Can the total time can be reduced by 20% by reducing only the time for branch instructions?
