Digitaltechnik

Contents

MSB - Most significant bit
LSB - Least significant bit

$x\%1$ - drop decimal value from x.
2^n - number of possible states with n bits.

Resistance of a wire

ρ - resistivity of the metal (Ωm)
l - length of the wire
A - cross sectional area of the wire
$R = \frac{\rho l}{A}$

Modern electronics uses 0.8V as high.

Floating Voltage - when a pin / contact is not connected by a “normal” (lower than that of air) resistance to V_DD / circuit ground. Essentially the same as any conductive surface in the room, on which a very weak 50Hz signal is usually seen due to induction from all the EM sources in the room.

Why digital instead of analog? Error correction.

Schaltfunktionen

Schaltfunktion - $Y = f(X_0, X_1, X_2, ..., X_{N-1})$ - Nimmt mehrere Bits als Input und produziert eine einzige Bit als Ausgang.

Alle Schaltfunktionen lassen sich als einer Wahrheitstabelle darstellen mit mindestens $N + 1$ Spalten und 2^N Zeilen, wo N ist der Nummer von Inputs.

NOT'ing a gate usually means the resistor just needs to be moved before the transistors (essentially appending a NOT gate).

OR - Disjunction

AND - Conjunction - The resistor after the output point is needed to prevent a short circuit when both inputs are high.

Antivalenz (XOR) - High if only one of the inputs is high.

XNOR - High if both inputs are the same, gate symbol is a =.

CMOS (Complementary Metal Oxide Semiconductor) Technology

Transistor - Trans-Resistor (changable resistor)
MOS Transistor - Electronic component with contacts **S** ource, **D** rain und **G** ate. Charge carriers flow from S to D. They are always controlled through a voltage between Gate and Source (unlike a current with BJT) and is therefore more efficient for very low / high power applications. They are also easier to etch in ICs and are therefore predominantly used in logic circuits.

Although very high pull up resistors vastly reduce power loss when using a single MOS transistor, such large resistances are difficult to fabricate in ICs. CMOS uses a PMOS instead which has practically ∞ resistance when "open".

$|V_{GS}| < |V_{th}|, R_{SD} \to \infty$ - The transistor is off
$|V_{GS}| > |V_{th}|, R_{SD} \to 0$ - The transistor is on

N-Type (NMOS) - Threshold voltage is positive. Negative electrons flow from S to D (Hence D is connected to the positive terminal in a circuit)
P-Type (PMOS) - Threshold voltage is negative. Positive Holes flow from S to D. Circle at the gate in symbol.

- CMOS Gatter müssen aus genau so vielen NMOS und PMOS Transistoren bestehen
- Bei m Eingängen gibt es m NMOS und m PMOS transistoren

The V_D of an "off" MOS transistor is floating (undefined) unless it is pulled up / down.

A CMOS gate can be split into two networks / Pfads:

	Pull-up	Pull-down
MOS Type	PMOS	NMOS
NAND	Parallel	Series
NOR	Series	Parallel

These can be converted between one another by breaking the circuit into parallel / series blocks until each block contains one transistor, then switching the type of transistor and connecting them again in the opposite manner (parallel ⇔ series). V_DD becomes the output and the output becomes ground.

Switching Delays

- t_{pHL}, t_{pLH} - Propogation delay - Time taken between a 50% change in the input voltage leading to a 50% change in the output
- $t_{tHL}(t_{\text{fall}}), t_{tLH}(t_{\text{rise}})$ - Time between the output rising / falling between 10% and 90% voltage

$t_d = \frac{t_{pHL}+t_{pLH}}{2}$ - Average switching time, easier to work with in practice

Boolean Algebra

The following properties apply to an expresion only containing AND / OR gates:
- Commutative, order does not matter
- Associative, grouping / order of (the same) operations is irrelevant
- Distributive, $A \wedge (B \vee C) = (A \wedge B) \vee (A \wedge C)$

Some not so obvious axioms of boolena algebra:
- $A \vee (A \wedge B) = A = A \wedge (A \vee B)$ - consider the effect on the whole circuit when the outer variable is high / low
- $(A \wedge B) \vee (\neg A \wedge B) = (A \vee B) \wedge (\neg A \vee B) = B$ - Neighbourhood law

Order of Operations

1. Brackets
2. Negation
3. AND, NAND, OR, NOR
4. XOR, XNOR

An expression with missing brackets is ambiguous and invalid.

De Morgan's Laws

$$\neg(A \wedge B \wedge C \wedge ...) \equiv \neg A \vee \neg B \vee \neg C \vee ...$$
$$\neg(A \vee B \vee C \vee ...) \equiv \neg A \wedge \neg B \wedge \neg C \wedge ...$$

The conversion between the pull up and pull down expression in a CMOS circuit uses De Morgan's laws:

$$\mathbf{Y_{pd}} = \overline{((A \cdot (B + C) \cdot D) + F + (G \cdot H)) \cdot E}$$
$$\mathbf{Y_{pu}} = ((\overline{A} + (\overline{B} \cdot \overline{C}) + \overline{D}) \cdot \overline{F} \cdot (\overline{G} + \overline{H})) + \overline{E}$$

Universal Gates

Any logic circuit can be expressed using only NAND / NOR gates. This is very advantageous as all gates in the circuit would have the same timing properties, reducing costs and errors.

To convert a logical expression into NAND / NOR, double negation + De Morgan's laws can be used, for example:

$$A \wedge B \equiv ?$$
$$\neg\neg A \wedge B \equiv \neg\neg A \vee \neg B$$
$$\neg A \text{ NOR } \neg B \equiv (A \text{ NOR } A) \text{ NOR } (B \text{ NOR } B)$$

Min / Maxterms

For n variables there are 2^n possible min / maxterms:
- Minterm: Expression that outputs 1 for **one** specific combination of inputs, if we want 1 only when A low, B High, minterm: $\neg A \wedge B$
- Maxterm: Expression that outputs 0 for **one** specific combination of inputs, if we want 0 only when

Let us consider we want expressions that output high / low only when $A = 0, B = 1$:
- Minterm: $\neg A \wedge B$, high only in this case
- Maxterm: $A \vee \neg B$, low only in this case

Normal Forms

A way of expressing a boolean expression that can easily be determined from the desired truth table (and then simplified using boolean algebra / Karnaugh diagrams). After constructing either a list of minterms for each 1 in the output, or list of maxterms for each 0:
- Disjunctive Normal Form - Minterms (ANDed variables) joined using disjunctions (OR)
- Conjunctive Normal Form - Maxterms (ORed negations) joined using conjunctions (AND)

Both result in the same output.

Karnaugh Diagrams

Used to visually and systematically simplify boolean expressions instead of through often complicated boolean algebra manipulation. Furthermore, race conditions (hazards) can be easier identified using this method.

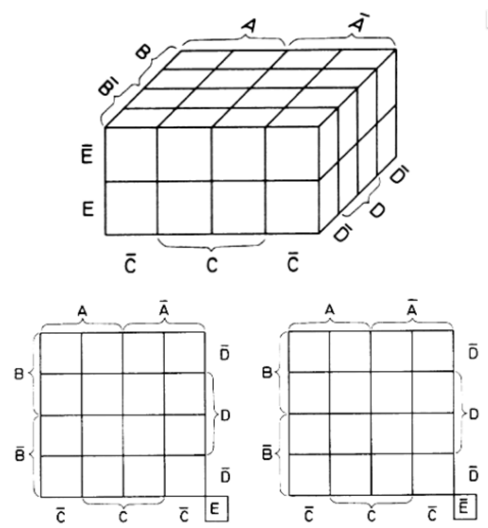
They are analogous to a truth table but represented as a matrix with 2^n elements, where n is the number of inputs.

Simply a methodical way of using the neighbour simplification rule: $(\neg A \wedge \neg B) \vee (A \wedge \neg B) = \neg B$

Don't care - Combinations of inputs for which the output doesn't matter, for example additional unneeded numbers in a boolean counting system. Marked with an X in a Karnaugh Diagram. The X's can be treated as 1s or 0s when creating packets if it reduces the amount of packets (and therefore joining gates) in the simplified expression.

Method

- Construct a matrix with 2^n elements, where each side of the matrix representsthe two states of a variable. One of each pair of variables facing opposite one another must be "split" so the neighbour rule can still be applied (See examples).
- Each element contains a 1 for each minterm (DNF) and the rest 0, or 0 for each maxterm (in this case the element headers are negated when allocating) and the rest as 1. *Don't Care* conditions can be written as X when the output for a specific combination doesn't matter.
- Create packets (also known as blocks) using the largest possible rectangle with 1s / 0s (may include Xs as they fit best). The packets must contain 2^n cells!
- Packets may overlap, "pacman" over the border and pass through layers, but not take non rectangle shapes (for example an L shape) or be diagonal. It is better to err on the side of caution and choose less packets, which may be possible to simplify later through linear algebra.
- They must capture the entire state of the diagram - Either all the 1s or all the 0s. Xs of course don't all need to be included.
- Each packet represents a minterm (if it contains 1s) or maxterm (contains 0s), which can then be simplified to the variable(s) which remain constant in the packet ADDed / ORed together (depending on if min or maxterm).
- The result of each packet can then be combined as the DNF / KNF.
- **IMPORTANT**: When combining results of the packets, they must all represent the same type (min or maxterm). If it's easier to formulate different types of packets, min and maxterms can of course be converted between another.



Static hazards - When the same variable is used in a parent logic gate, changes in the variable can lead to delayed “notches” in the parent’s output due to time delays. These can be recognized in Karnaugh diagrams: where two packets are orthogonally next to each other but do not overlap. They can be directly fixed by introducing an extra packet two join the place of the hazard - this results in more gates overall but avoids the hazard.

Number Systems

Base (Radix) - b-adischen Reiehen like in analysis, negative indices of the base for defining decimals

Hexadecimal - Uses digits $0 - 9$ and $A - F$ for 16 possible digits in total. Used to represent binary numbers in a more compact format by splitting a binary number into groups of 4 digits

Octal - Radix 8, can be converted from binary using groups of 3 binary digits.

Converting Decimal to Radix R

1. Perform whole number division of the decimal D by the Radix R: $\frac{D}{R} = Q_0 + r_0$, the remainder is the first digit in the target radix
2. Divide the result of the previous whole-number division Q_0 by the radix R again, this remainder is now the second digit in the target radix and so on
3. Continue until Q_i reaches 0

Converting $0 \leq D_{10} < 1$ to Radix R

This is the same process but the decimal is multiplied by the radix R and the resulting product is used in the next multipliciation. The current digit is the floor of TODO: Coefficients?, starting with the most significant bit.

Only possible for a finite number of decimal digits.

Signed Binary Numbers

- Signing bit
- 1s complement
- 2s complement: Advantageous for performing arithmetic with signed numbers as the sign remains accurate

2s Complement

TODO: Screenshot from script (Konstruktion von 2er-Komplementen) How it can be converted back into decimal, either convert to positive then calculate or use first bit (sign) as $-(2)^n$ and the others as positive binary digits

Fractional numbers still have $\pm 2^0$ as the signing bit, converted in the same way. In the case of a whole + fractional number only the first bit is a signing bit

IMPORTANT: Do not forget signing bit for positive numbers

Binary Arithmetic

Addition of two binary numbers, with maximum n digits has at most $n + 1$ bits in the result. TODO: Addition of 4x1s = Carry over 1 two places

Binary subtraction can be written as the addition of 2s complement numbers

Encoding

Tetraden / Nibble - groups of 4 bits

Many different ways to encode 10 numbers, each has their advantages / disadvantages. Gray / O'Brien useful for counting TODO: Why?

Parity Bit

Additional bit representing if the number of 1s in a word / block is odd / even TODO: Double check

An extra word can be sent with the purpose of checking and also correcting previous words

Datapath Circuits

Multiplexer

Outputs one selected bit from several inputs using a binary selection signal. Circuit is a selection of minterms $(\neg S_0 \wedge \neg S_1 \wedge D_0) \vee (\neg S_0 \wedge S_1 \wedge D_1) \vee (S_0 \wedge \neg S_1 \wedge D_2) \vee (S_0 \wedge S_1 \wedge D_3)$

Demultiplexer

Inverse of a multiplexer, selects at which output a signal is outputed. Same Circuit but ORed with Y

Code Translator (Umsetzer)

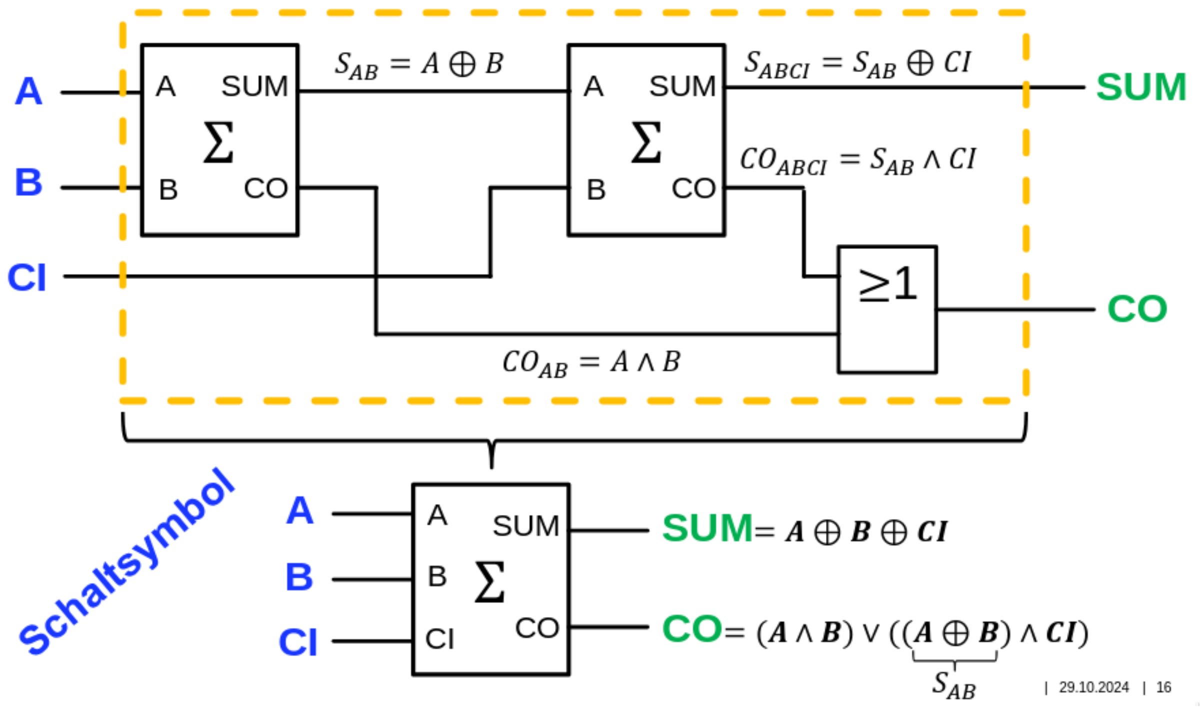
Converts between number encoding. Create KNF -> Karnaugh diagram for each output and the set of inputs, TODO: Clarify

Half Adder

Outputs the sum of two binary digits and the remainder (Carry Out CO) to be passed to an adjacent full-adder one place value higher. Symbol has $\sum$ on it.

Full Adder

3 inputs: A, B and Carry In (CI) for a lower CO bit. Simply a combination of two half adders plus an OR gate taking in CI and CO of the internal half adder.



TODO: Series (with multiplexer and clock signal?) vs parallel adder

Parallel Adder
TODO: Add example and (dis)advantages

Ripple Carry
Advantage: Easy to expand and combine Disadvantage: Carry bits take time to ripple up the place values

Carry-Look-Ahead Adder
Advantages of both combined, TODO: Some kind of recursive equation

Subtraction
XOR Gates handle two's complement signing bits well

Multiplication
Sum of shifted partial products: $(a + b) \cdot c = a \cdot c + b \cdot c$, x2 = shift one to the left, x0.5: shift 1 bit to the right

Booth's Multiplication Algorithm for 2s Complement numbers will not be examined.

Sequential Circuits

Sequential circuits depend not only on the inputs but also the previous state. TODO: formal definition TODO: Mention how logic tables are used with previous states -> state n+1

SR-Latch
TODO: Diagrams of both variants TODO: Draw / find state diagram, describe pin functionality Q2 is simply $\neg Q1$

Clock-controlled Latch
Just like SR but the S and R pins only take effect when the clock is high. TODO: Symbol, Circuit and state diagrams TODO: is this called edge triggered?

D-Latch