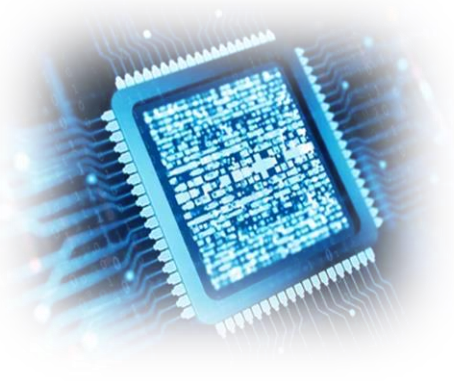


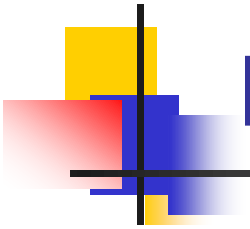
MICROPROCESSOR SYSTEMS

BLG212E

Burak Berk Üstündağ CRN: 11450
Gökhan İnce / Ayşe Yılmazer CRN: 11446

İTÜ Bilgisayar ve Bilişim Fakültesi

Week 14: I/O techniques and Interfacing in Microprocessor Systems



Microprocessor based system Design

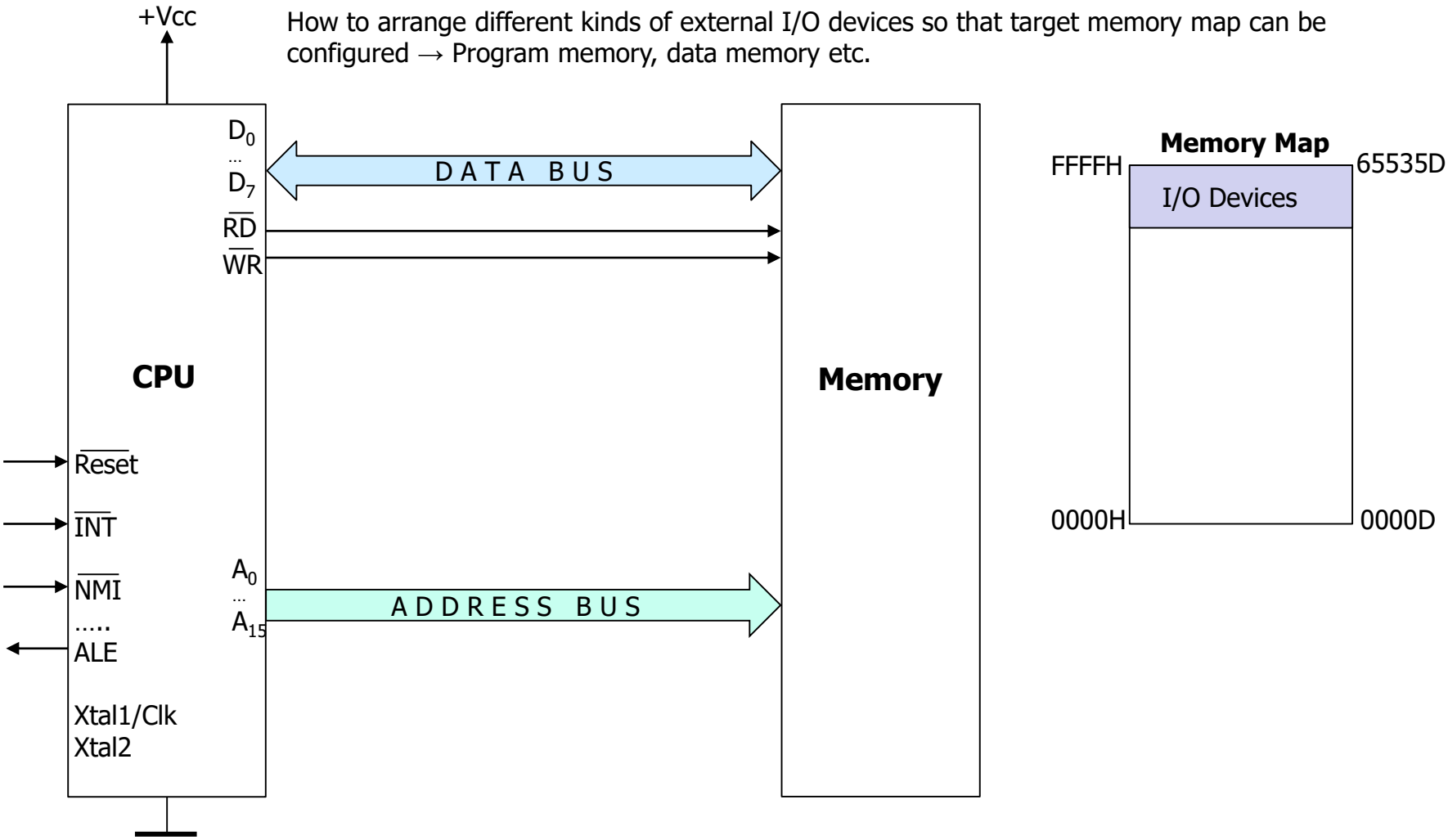
- External I/O interfacing
- Typical external I/O components
- Cache Management
- Direct Memory Access

http://www.ninova.itu.edu.tr/EgitimDetay.aspx?eId=30

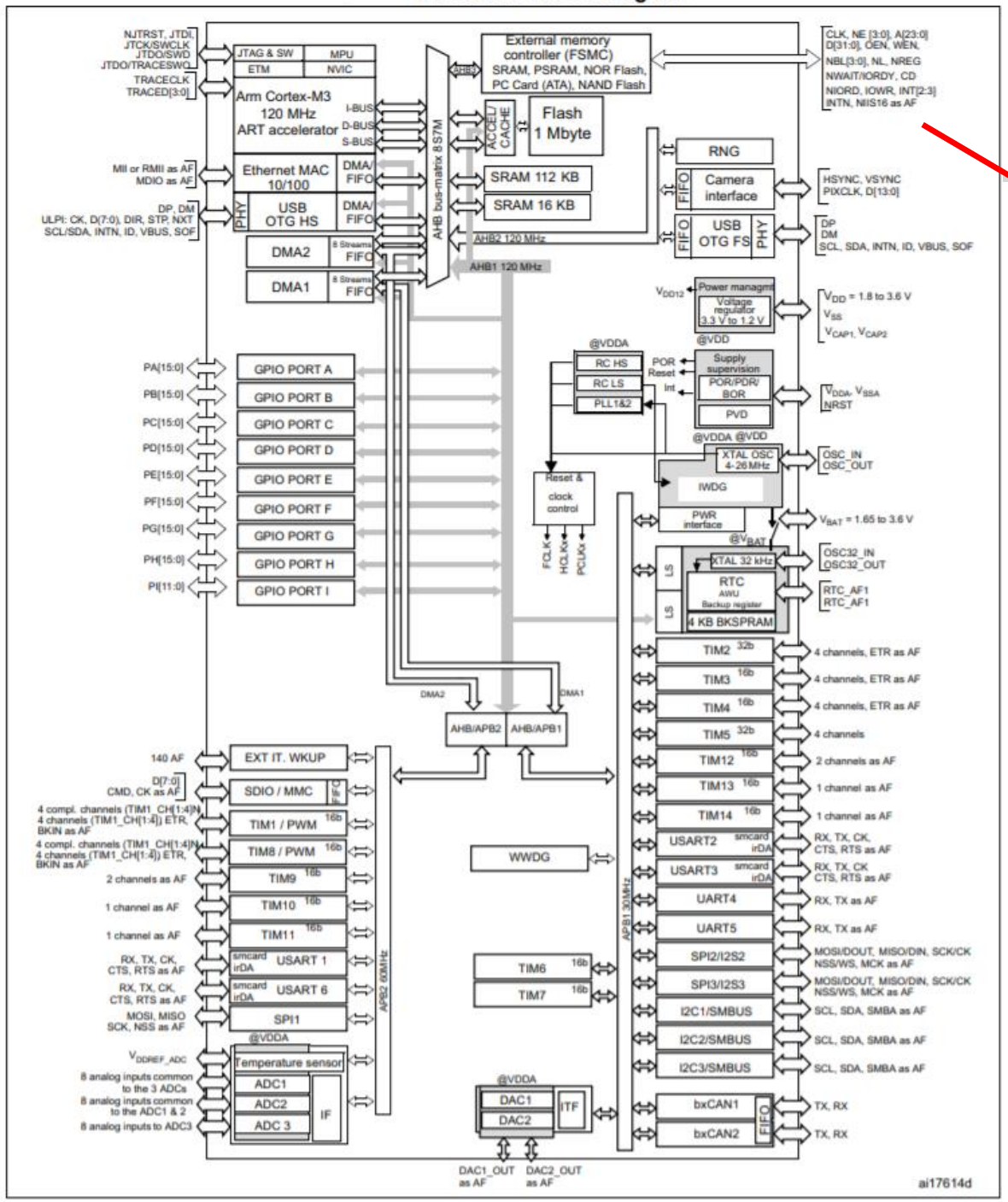
External I/O Operations

CPU: 64K Addressing Capability, 8Bits, Reset Vector (POR): 0000H

Problem:
How to arrange different kinds of external I/O devices so that target memory map can be configured → Program memory, data memory etc.



STM32F20x block diagram



CLK, NE [3:0], A[23:0]
D[31:0], OEN, WEN,
NBL[3:0], NL, NREG
NWAIT/IORDY, CD
NIORD, IOWR, INT[2:3]
INTN, NIIS16 as AF

Non-configurable I/O example

CPU: 64K Addressing Capability, 8Bits, Reset Vector (POR): 0000H, 32K EPROM, 16K SRAM, 8K EEPROM

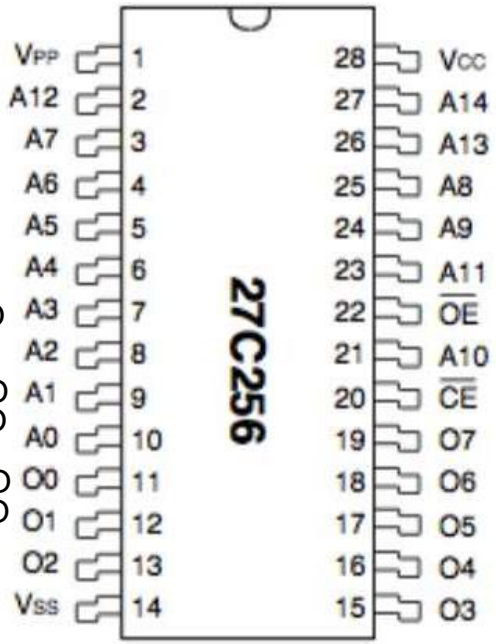
8 Keys, 4 Relays and 4 LEDs will be interfaced to the system

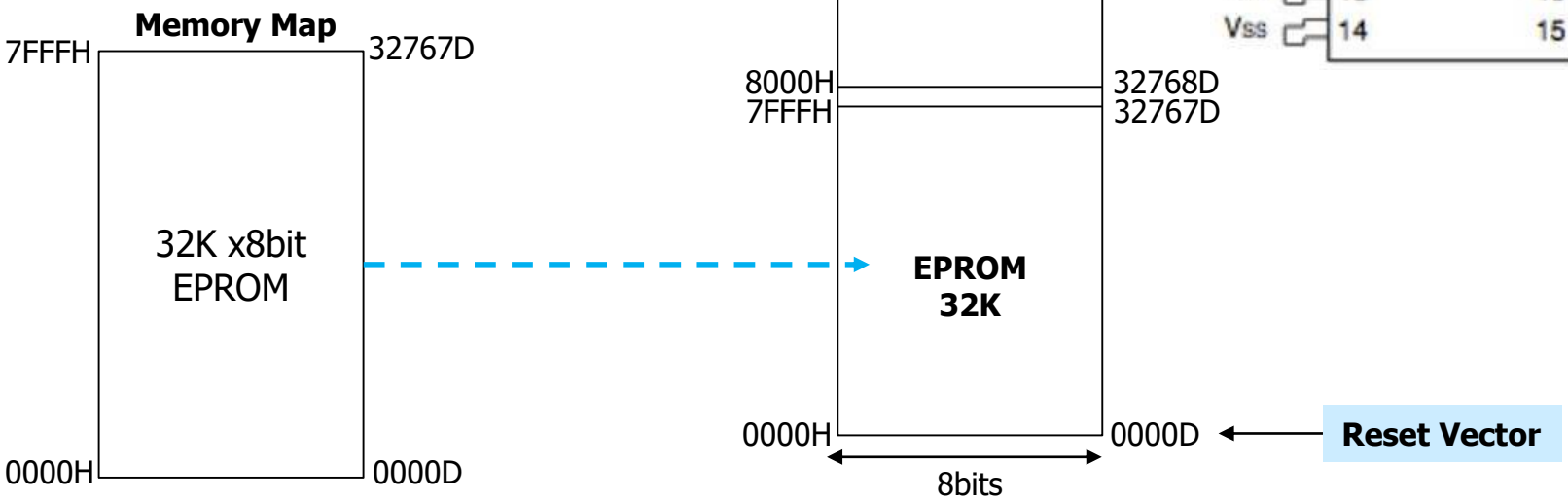
1- 32K EPROM : 32x8kbit → 27C256: P, $\overline{OE}$, $\overline{CE}$

2- 27C→O_0...O_7 , Generic code: 27C256

3- x256→ M=256kbit=256x1024 bit
Since 27C refers 8 bits I/O,
Address bus size= $\log_2$ (256x1024/8)=8+10-3=15
Address lines→ A0..A14

4- a 74HC573 for 8 button input
a 74HC573 for 4 LED outputs and 4 Relay outputs





Memory Map

CPU: 64K Addressing Capability, 8Bits, Reset Vector (POR): 0000H, 32K EPROM, 16K SRAM, 8K EEPROM, 8 bit Input, 8bit Output

1- 16K SRAM : 16x8kbit → 62C128: $\overline{WE}$, $\overline{OE}$, $\overline{CE}$

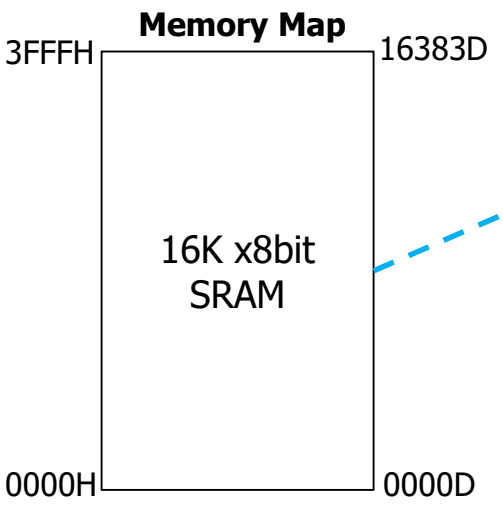
2- 62C→I/O_0…I/O_7 , Generic code: 62C128 alternative: **W24129A**

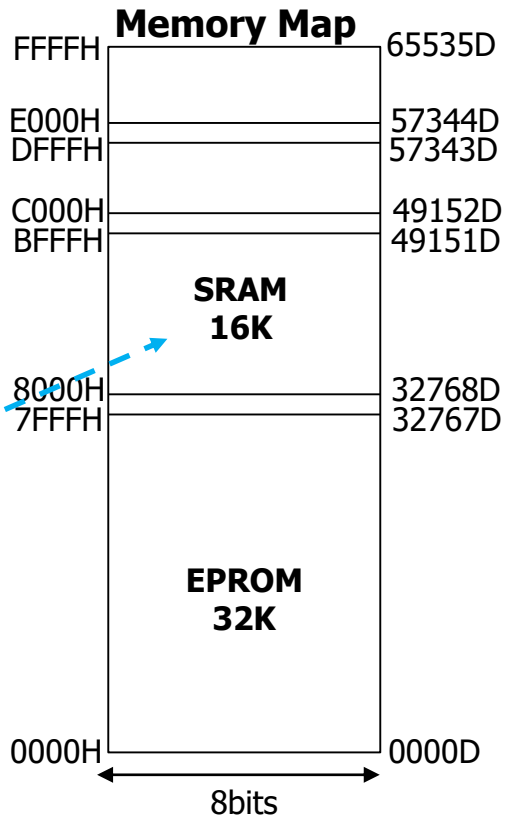
3- x128→ M=128kbit=128x1024 bit

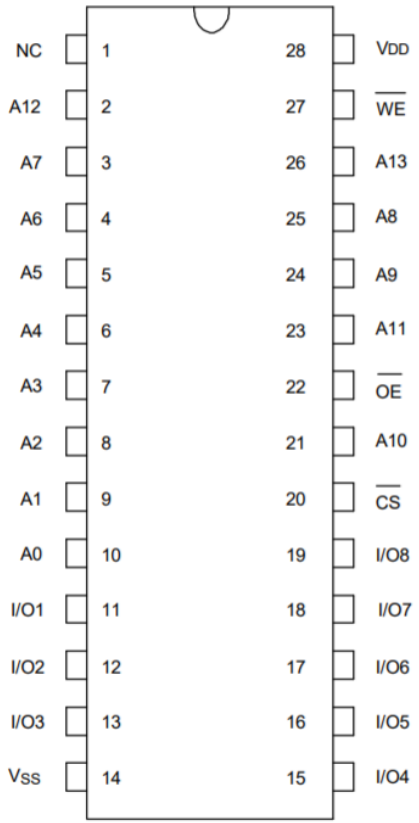
Since 62C/M48 refers 8 bits I/O,

Address bus size= $\log_2$ (128x1024/8)=7+10-3=14

Address lines→ A0..A13







Memory Map

CPU: 64K Addressing Capability, 8Bits, Reset Vector (POR): 0000H, 32K EPROM, 16K SRAM, 8K EEPROM, 8 bit Input, 8bit Output

1- 8K EEPROM : 8x8kbit → 28C64: $\overline{WE}$, $\overline{OE}$, $\overline{CE}$

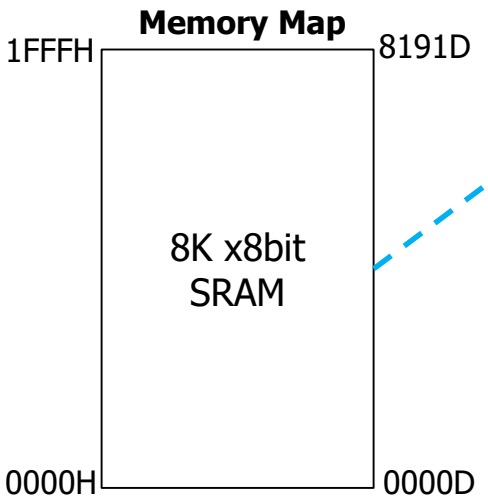
2- 28C→I/O_0...I/O_7 , Generic code: 28C64

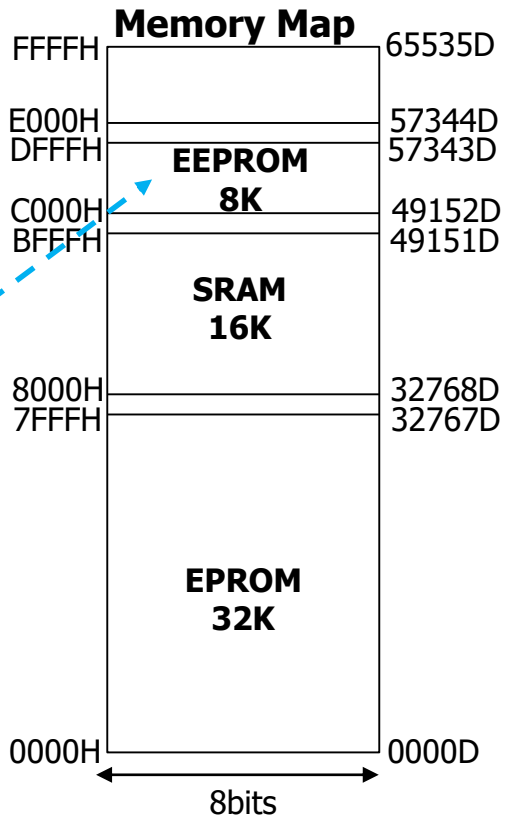
3- x64→ M=64kbit=64x1024 bit

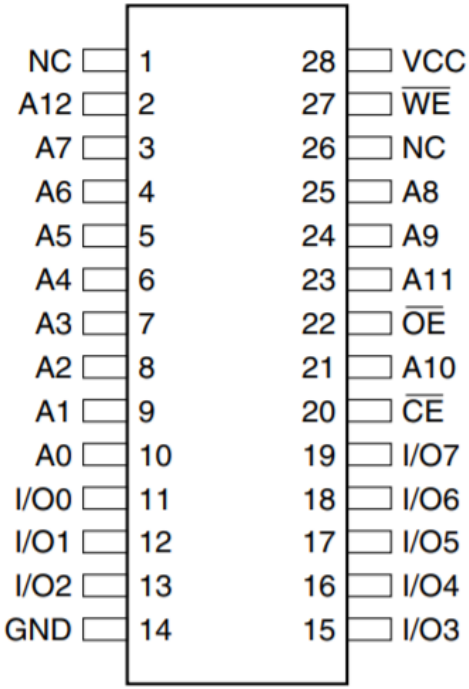
Since 28C refers to 8 bits I/O,

Address bus size= $\log_2$ (64x1024/8)=6+10-3=13

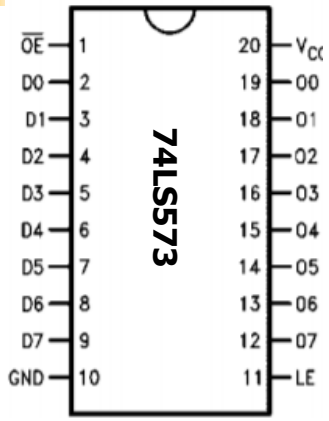
Address lines→ A0..A12







74LS573 TRISTATE LATCH



Pin Names	Description
D0–D7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	3-STATE Output Enable Input (Active LOW)
O0–O7	3-STATE Latch Outputs

$\overline{\text{Output}}$ Enable	Latch Enable	D	Output O
L	H	H	H
L	H	L	L
L	L	X	Q_O
H	X	X	Z

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Input Current			−2.6	mA
I_{OL}	LOW Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

$I_{sink} > I_{source}$

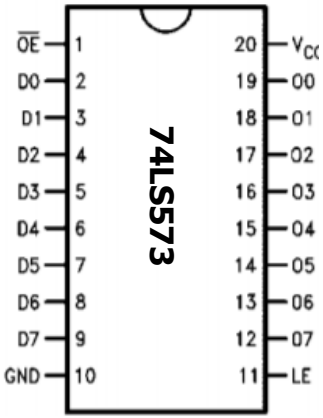
Memory Map

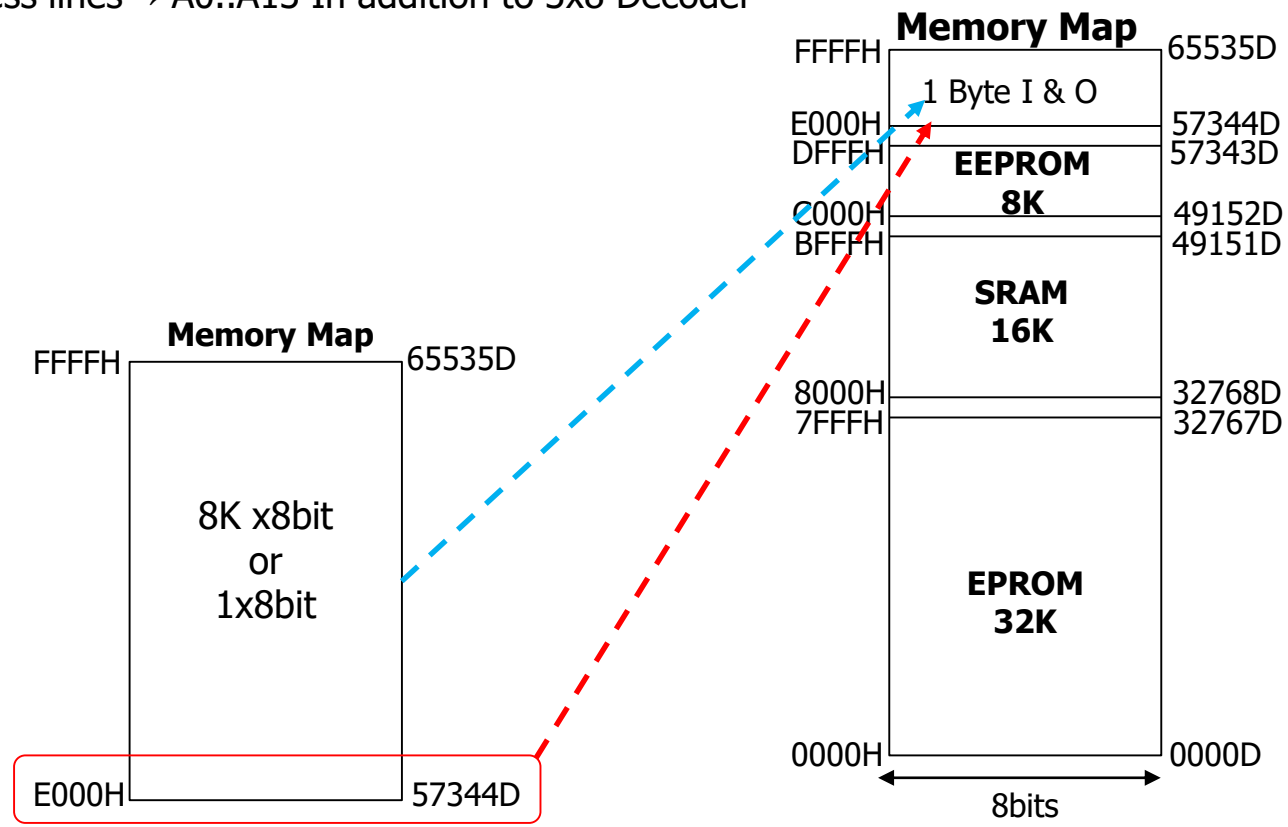
CPU: 64K Addressing Capability, 8Bits, Reset Vector (POR): 0000H, 32K EPROM, 16K SRAM, 8K EEPROM, 8 bit Input, 8bit Output

One 74LS573 for Input and another 74LS573 for Output

Address bus size= 0

Address lines→ A0..A13 In addition to 3x8 Decoder





74LS573 (or 74LS373) Control Bus Connection

$\overline{\text{Output}}$ Enable	Latch Enable	D	Output O
L	H	H	H
L	H	L	L
L	L	X	Q_O
H	X	X	Z

For the 8-bit input:

$\overline{CS}$	$\overline{RD}$	$\overline{OE}$
0	0	0
0	1	1
1	0	1
1	1	1

$\overline{OE}=\overline{RD}+\overline{CS}$

For the 8-bit output:

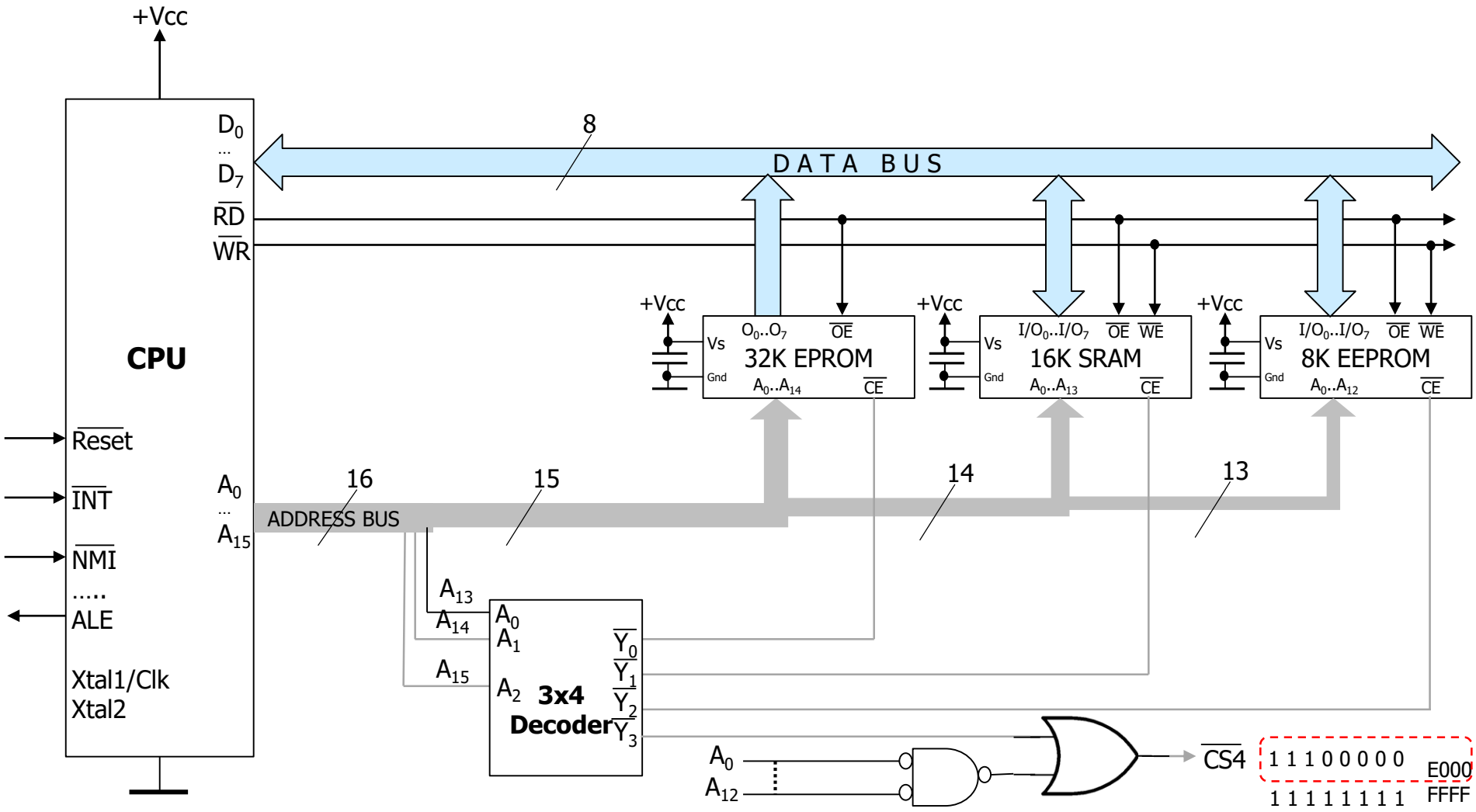
$\overline{CS}$	$\overline{WR}$	LE
0	0	1
0	1	0
1	0	0
1	1	0

$LE=\overline{(\overline{WR}+\overline{CS})}$

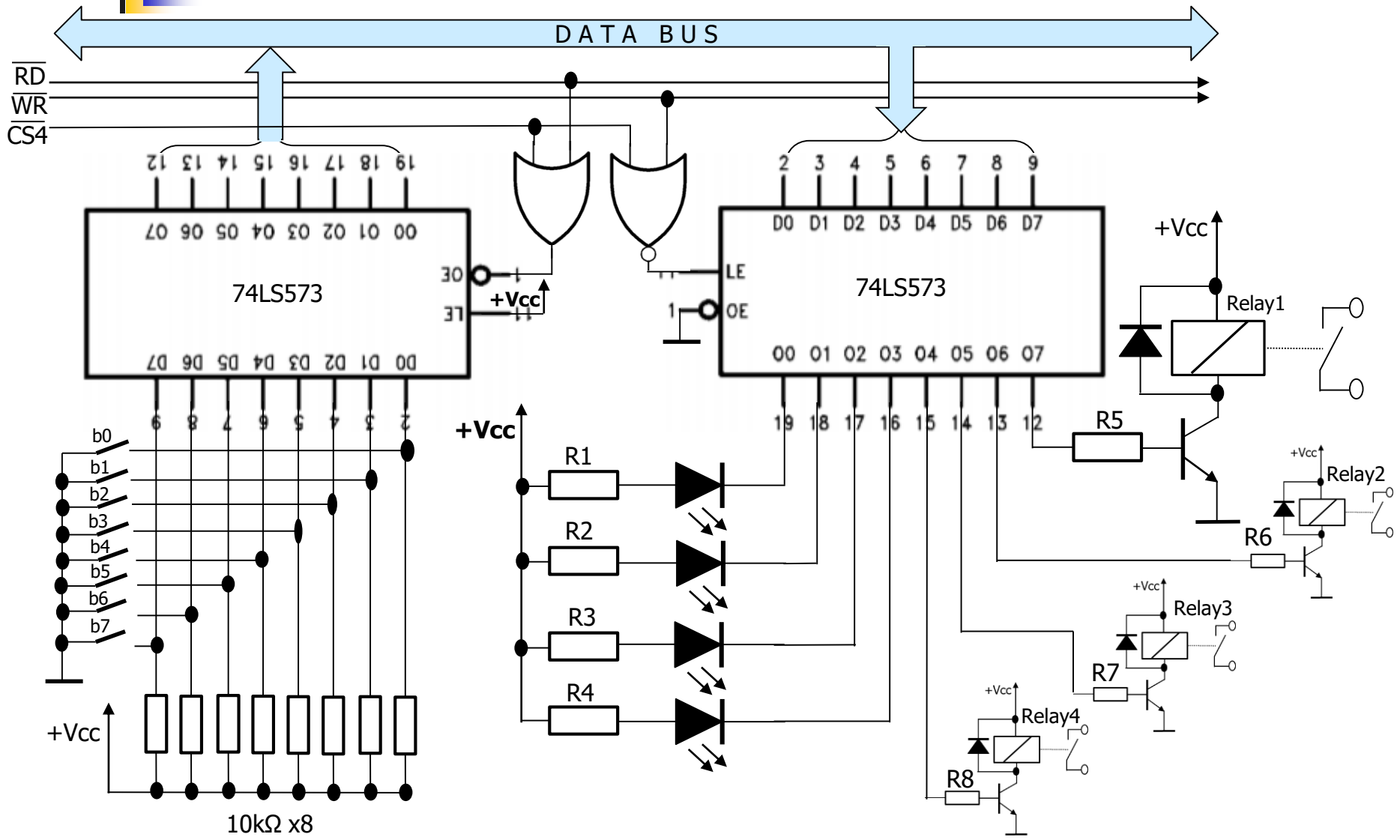
http://www.ninova.itu.edu.tr/EgitimDetay.aspx?eId=30

Address Decoding

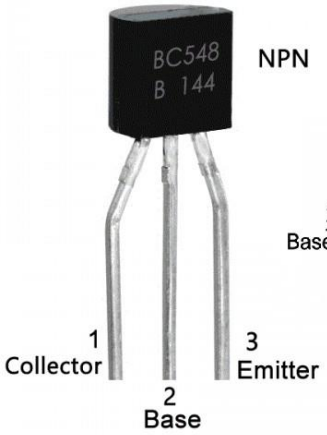
CPU: 64K Addressing Capability, 8Bits, Reset Vector (POR): 0000H, 32K EPROM, 16K SRAM, 8K EEPROM

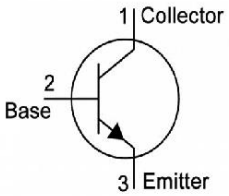


74LS573 Tristate Latch as logical I/O

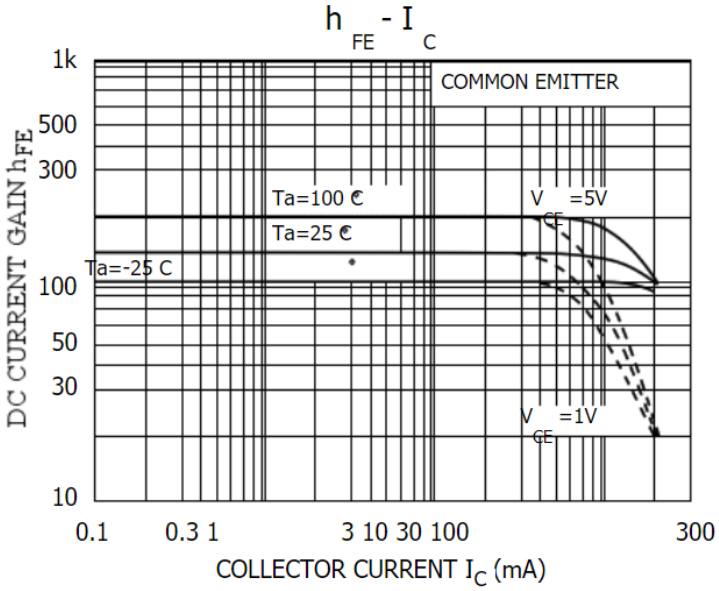


BC548





Ic=100mA
VCEO=30V



ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current		I_{CBO}	V_{CB}=30V, I_E=0	-	-	15	nA
DC Current Gain (Note)	BC546	h_{FE}	V_{CE}=5V, I_C=2mA	110	-	450	
	BC547			110	-	800	
	BC548			110	-	800	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	I_C=100mA, I_B=5mA	-	-	0.6	V
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	I_C=100mA, I_B=5mA	-	0.9	1.1	V
Base-Emitter Voltage		$V_{BE(ON)}1$	V_{CE}=5V, I_C=2mA	0.58	-	0.7	V
		$V_{BE(ON)}2$	V_{CE}=5V, I_C=10mA	-	-	0.75	V
Transition Frequency		f_T	V_{CE}=5V, I_C=10mA, f=100MHz	-	150	-	MHz
Collector Output Capacitance		C_{ob}	V_{CB}=10V, f=1MHz, I_E=0	-	-	4.5	pF
Noise Figure		NF	V_{CE}=6V, I_C=0.1mA R_g=10kΩ, f=1kHz	-	1.0	10 dB	

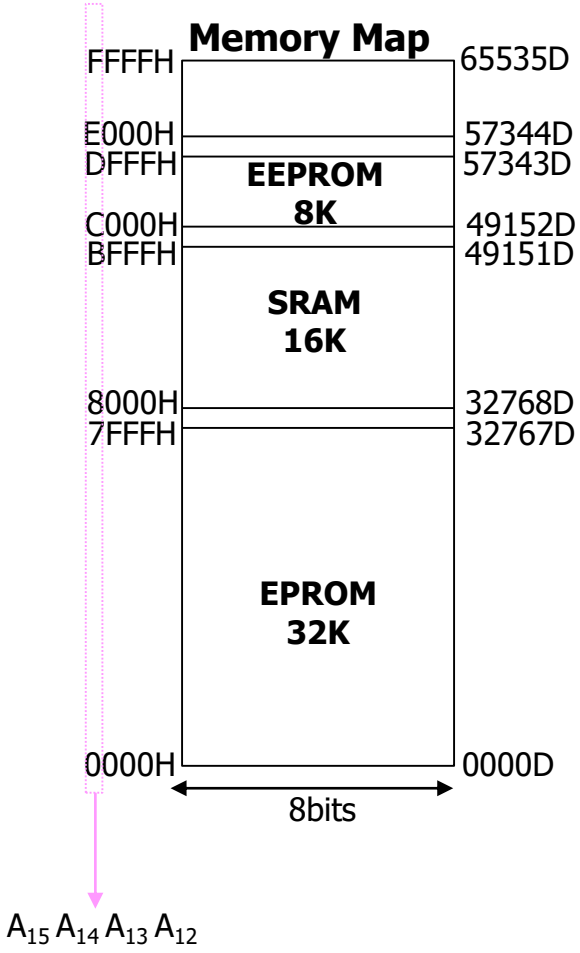
Address Decoder Design

If last segment will not be used:

Segment Size:	CPU:	A15	A14	Output:			
	Decoder:	A1	A0	Y0'	Y1'	Y2'	
16K		0	0	0	1	1	EPROM
16K		0	1	0	1	1	EPROM
16K		1	0	1	0	1	SRAM
16K		1	1	1	1	0	EEPROM

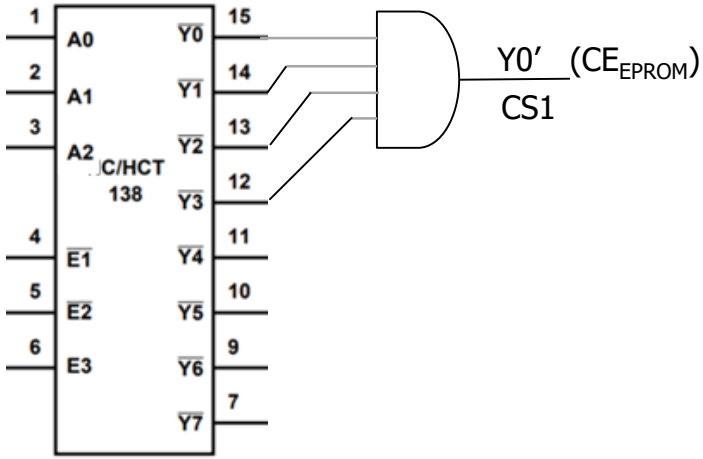
If last segment will be reserved for future:

	CPU:	A15	A14	A13	Output:			FU	
Segment Size:	Decoder:	A2	A1	A0	Y0'	Y1'	Y2'	Y3'	
8K		0	0	0	0	1	1	1	EPROM
8K		0	0	1	0	1	1	1	EPROM
8K		0	1	0	0	1	1	1	EPROM
8K		0	1	1	0	1	1	1	EPROM
8K		1	0	0	1	0	1	1	SRAM
8K		1	0	1	1	0	1	1	SRAM
8K		1	1	0	1	1	0	1	EEPROM
8K		1	1	1	1	1	1	0	I/O Port



If last segment will be reserved for future:

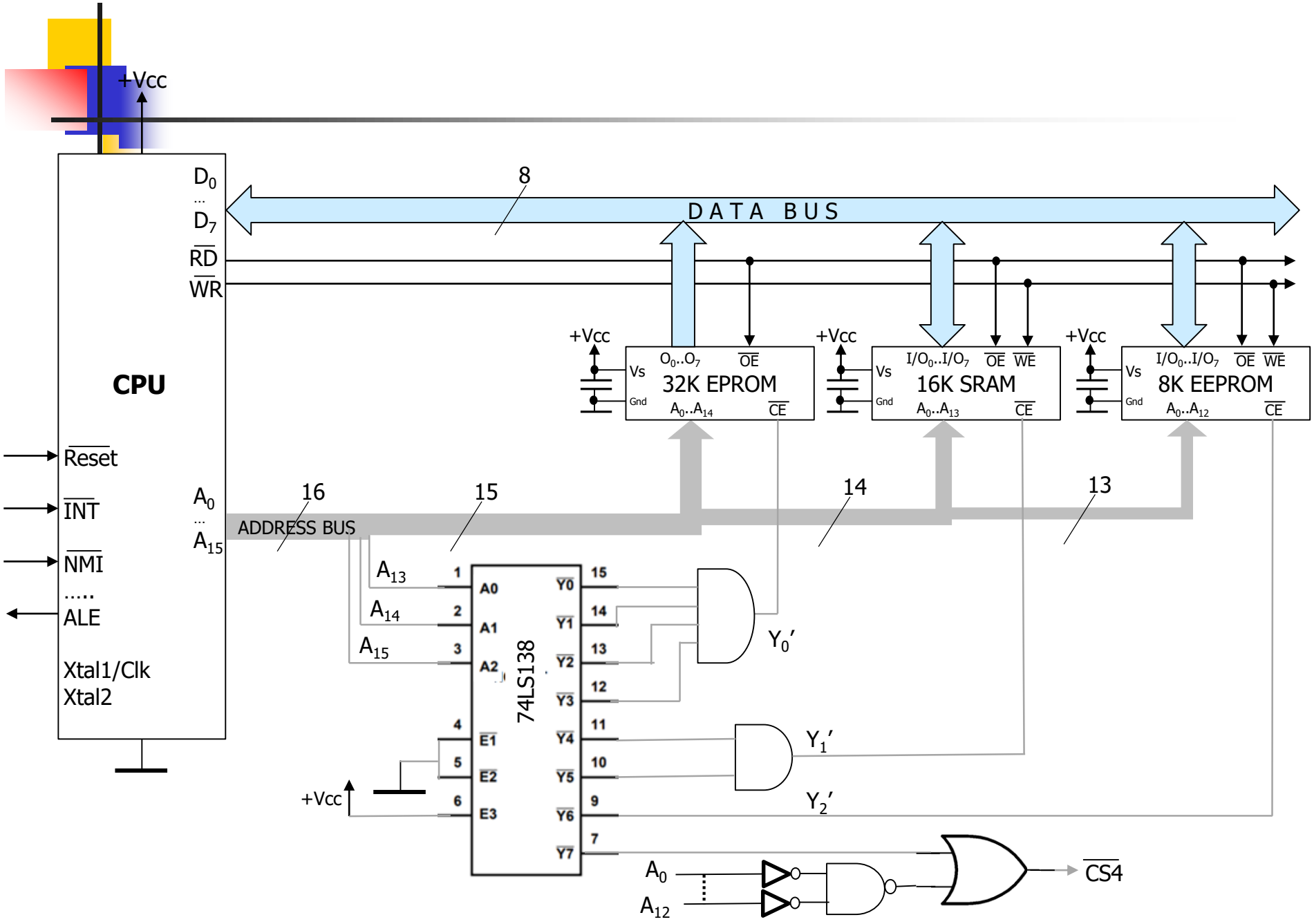
	CPU:	A15	A14	A13	Output:			FU	
Segment Size:	Decoder:	A2	A1	A0	Y0'	Y1'	Y2'	Y3'	
8K		0	0	0	0	1	1	1	EPROM
8K		0	0	1	0	1	1	1	EPROM
8K		0	1	0	0	1	1	1	EPROM
8K		0	1	1	0	1	1	1	EPROM
8K		1	0	0	1	0	1	1	SRAM
8K		1	0	1	1	0	1	1	SRAM
8K		1	1	0	1	1	0	1	EEPROM
8K		1	1	1	1	1	1	0	I/O Port



TRUTH TABLE 'HC138, 'HCT138

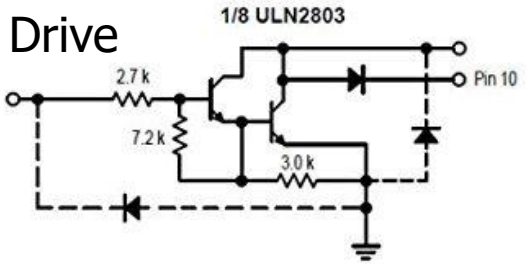
INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

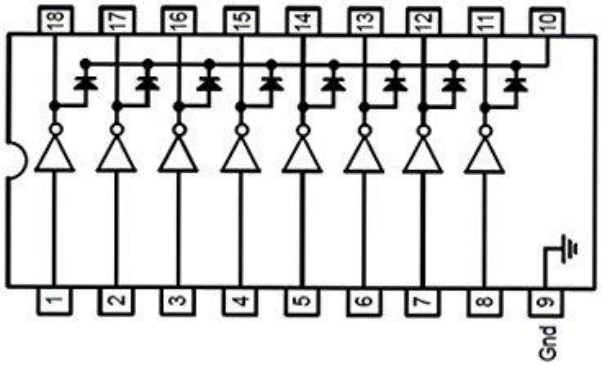
H = High Voltage Level, L = Low Voltage Level, X = Don't Care


+Vcc
CPU
D0
...
D7
RD
WR
8
DATA BUS
Reset
INT
NMI
.....
ALE
Xtal1/Clk
Xtal2
A0
...
A15
16
15
14
13
ADDRESS BUS
+Vcc
O0..O7
OE
Vs
Gnd
32K EPROM
A0..A14
CE
+Vcc
I/O0..I/O7
OE
WE
Vs
Gnd
16K SRAM
A0..A13
CE
+Vcc
I/O0..I/O7
OE
WE
Vs
Gnd
8K EEPROM
A0..A12
CE
A13
A14
A15
74LS138
A0
A1
A2
E1
E2
E3
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y0'
Y1'
Y2'
+Vcc
A0
A12
CS4

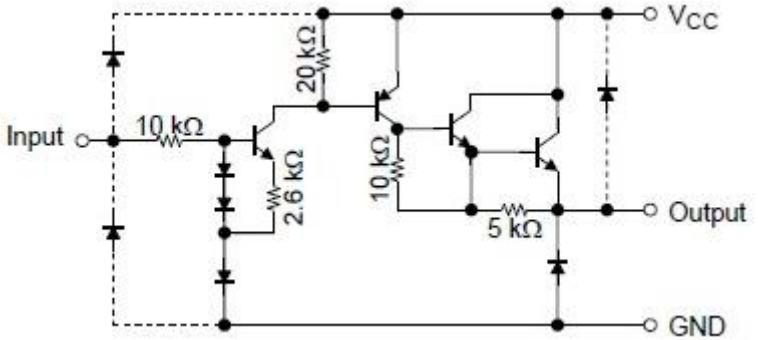
Array drivers and the logical ground isolation

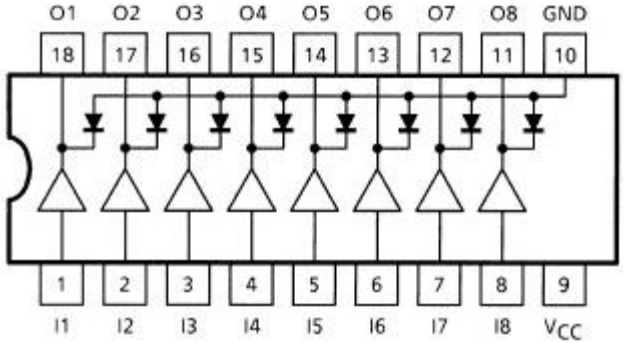
ULN2803
Sink Drive





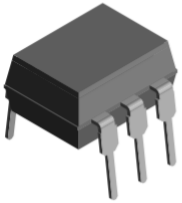
UDN2981
Source Drive

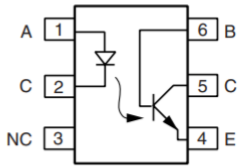




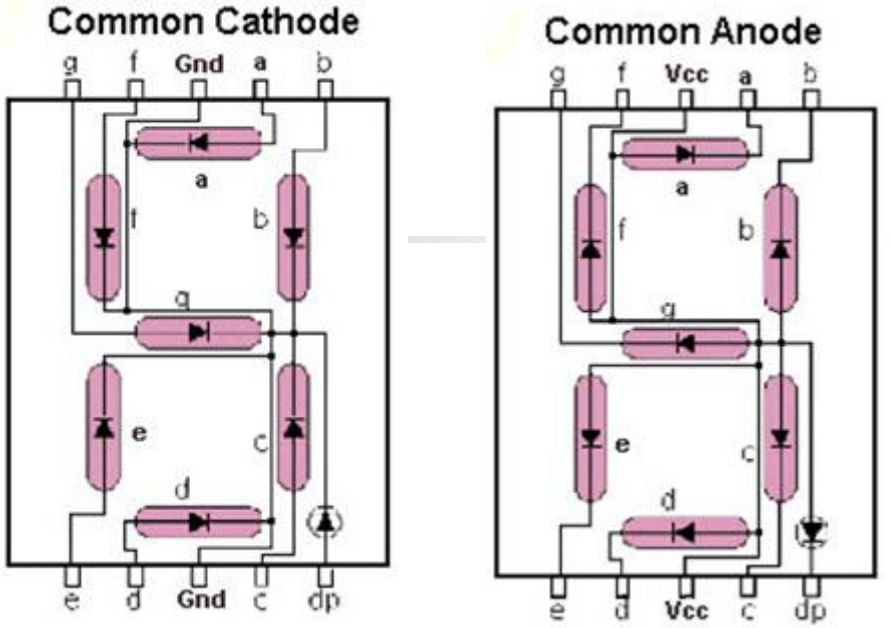
Optocoupler

4N25

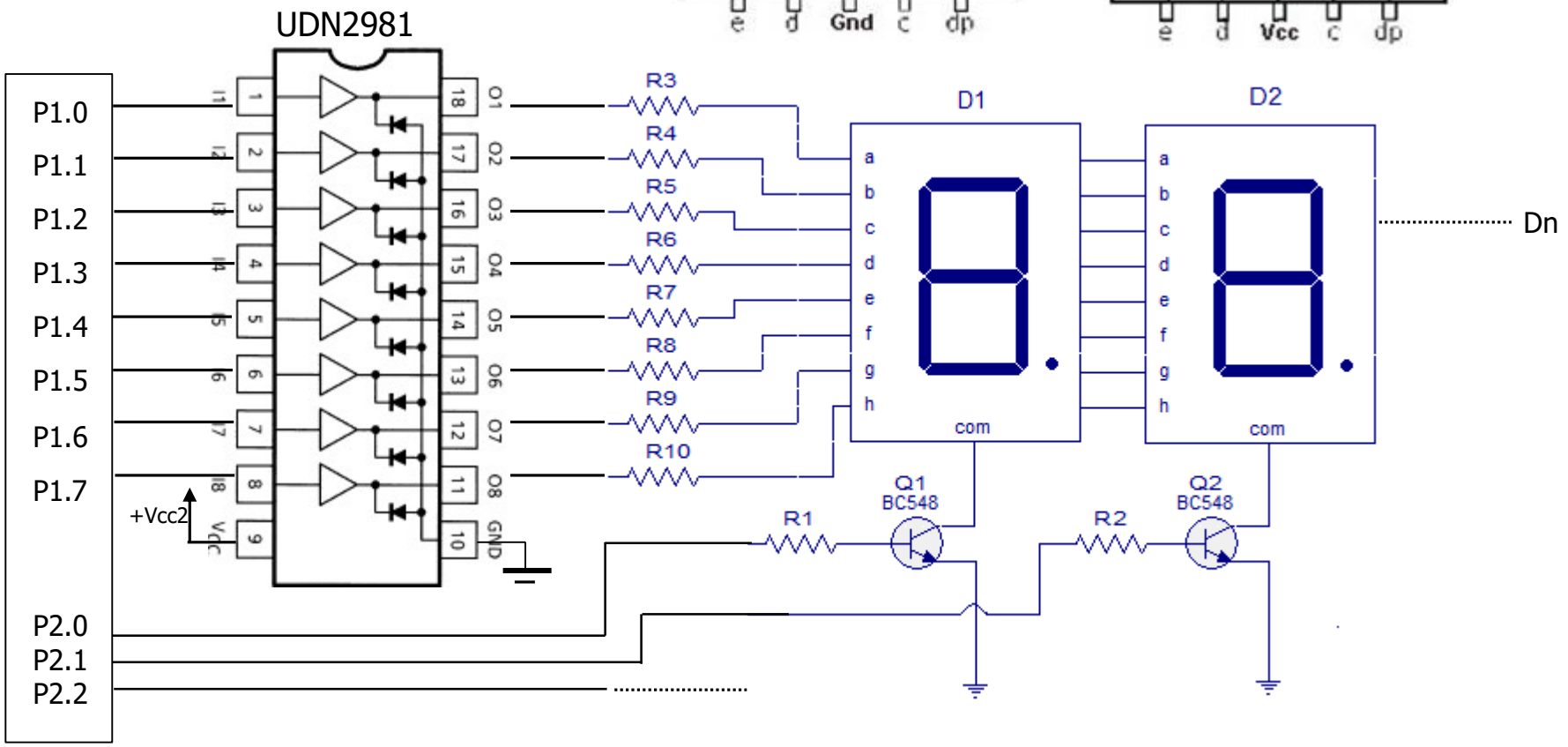




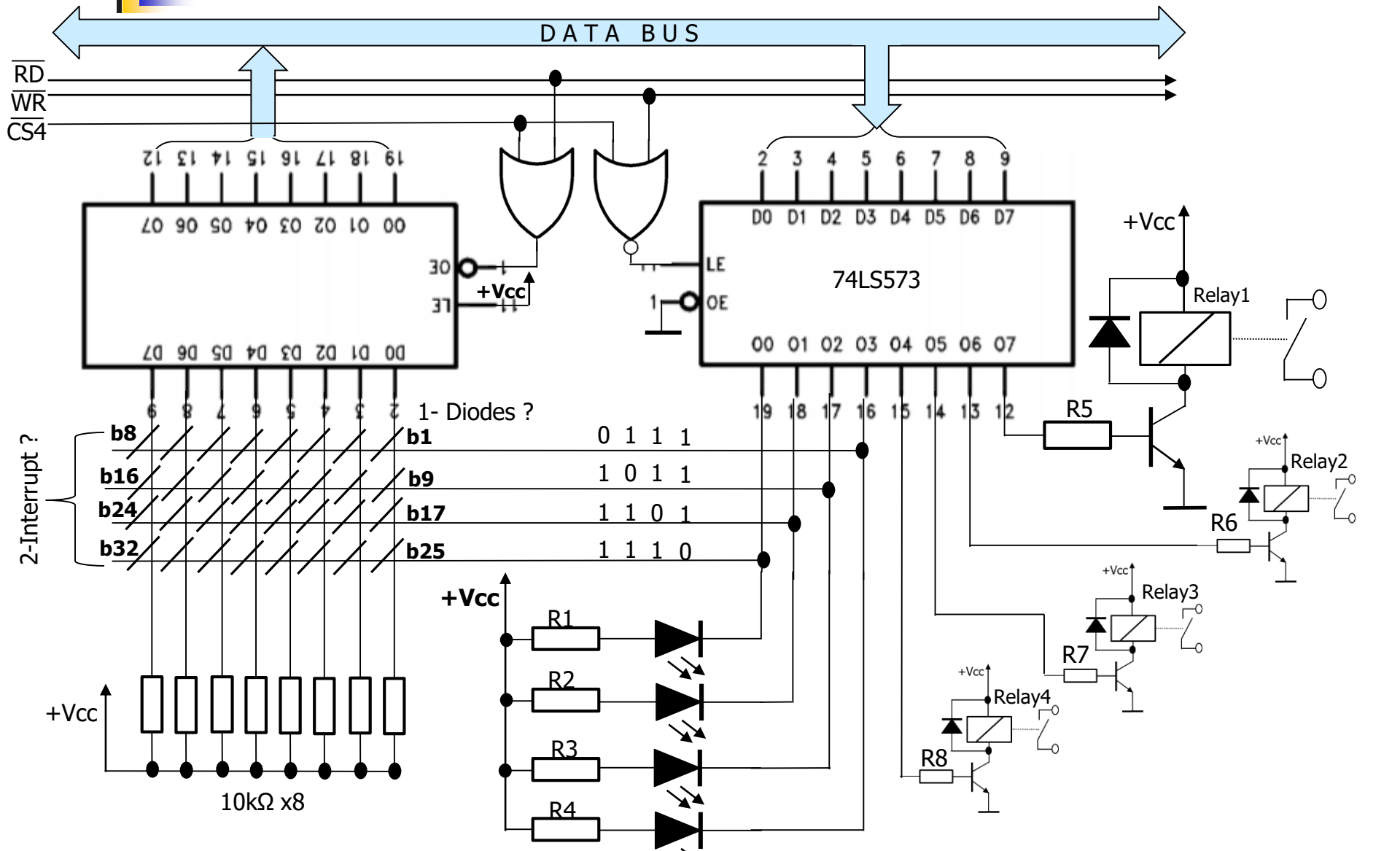
Multiplexed Mode Driver

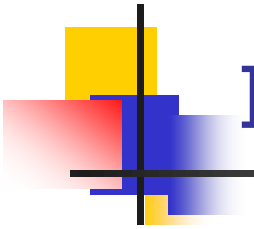


100Hz→Interrupt: Display count x 100Hz
Interrupt period: 1/(800)=1.25ms=1250microsec



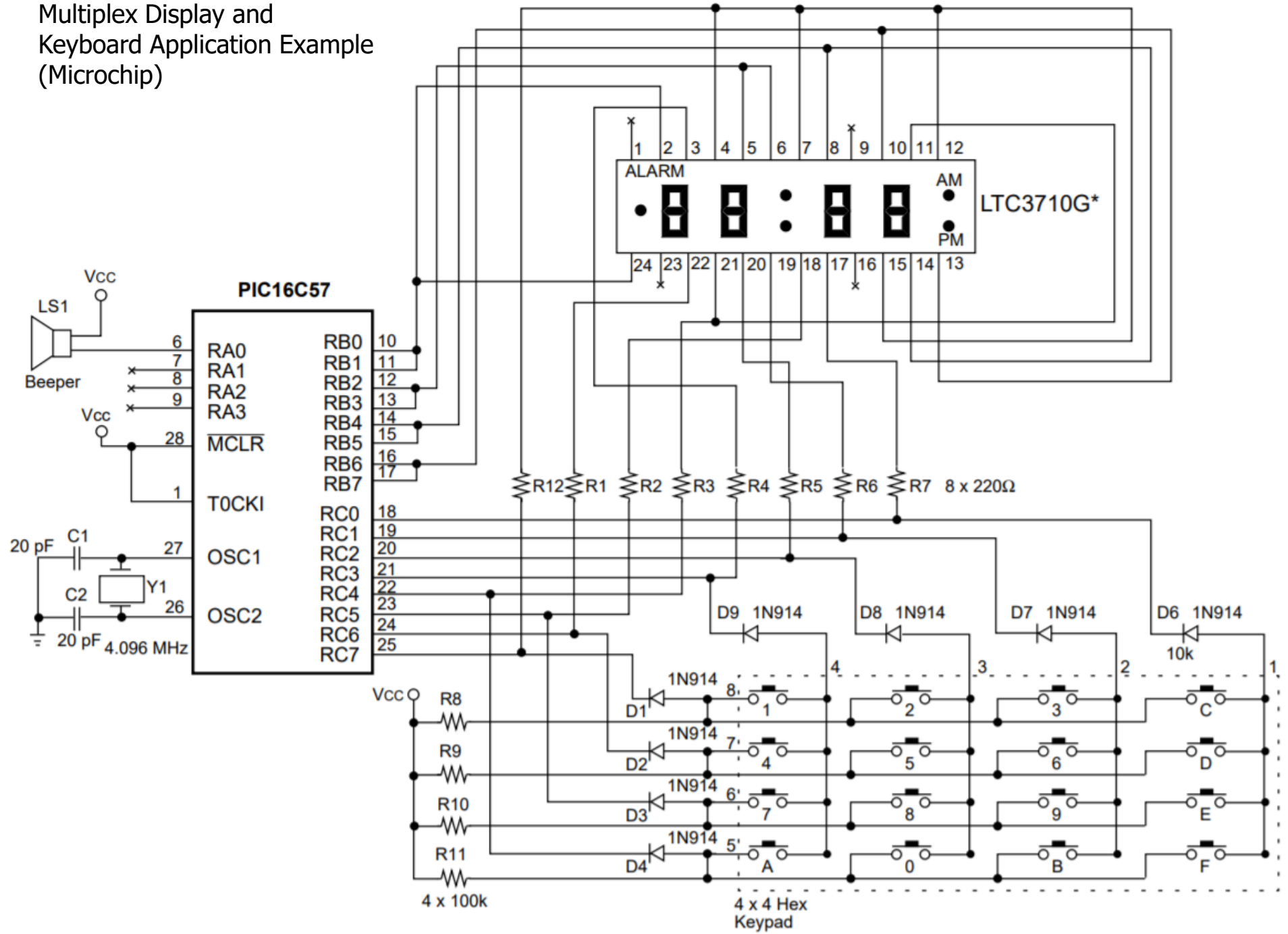
Multiplexed Key Scan with 74LS573

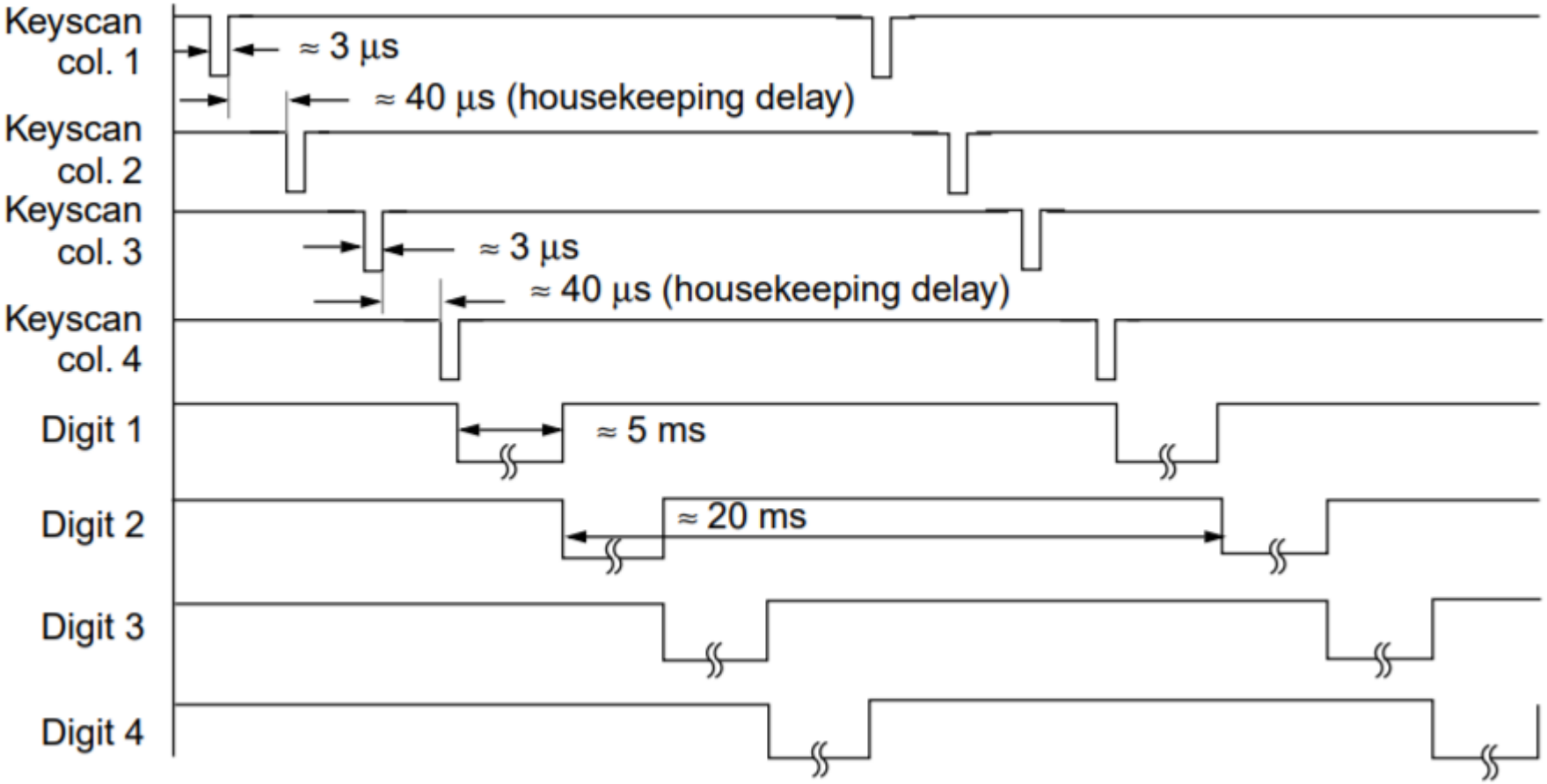




Interrupt and scan if any key is pressed ?

Multiplex Display and
Keyboard Application Example
(Microchip)




Keyscan col. 1
≈ 3 µs
≈ 40 µs (housekeeping delay)
Keyscan col. 2
Keyscan col. 3
≈ 3 µs
≈ 40 µs (housekeeping delay)
Keyscan col. 4
Digit 1
≈ 5 ms
Digit 2
≈ 20 ms
Digit 3
Digit 4

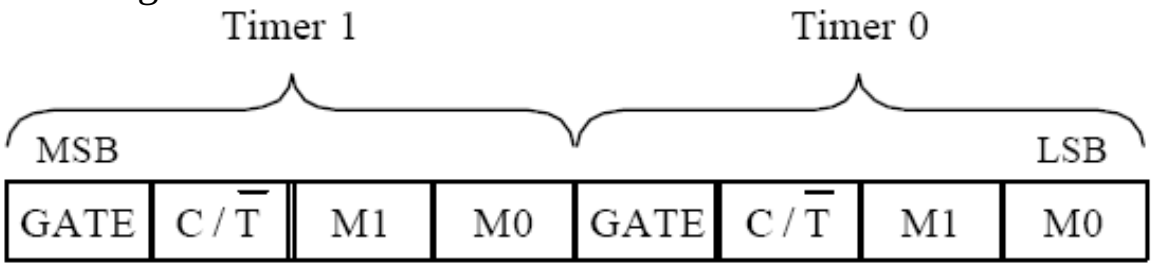
Interrupt Vector Table

Interrupts	ROM Location (Hex)	Pin
Interrupts	ROM Location (HEX)	
Serial COM (RI and TI)	0023	
Timer 1 interrupts(TF1)	001B	
External HW interrupt 1 (INT1)	0013	P3.3 (13)
External HW interrupt 0 (INT0)	0003	P3.2 (12)
Timer 0 (TF0)	000B	
Reset	0000	9

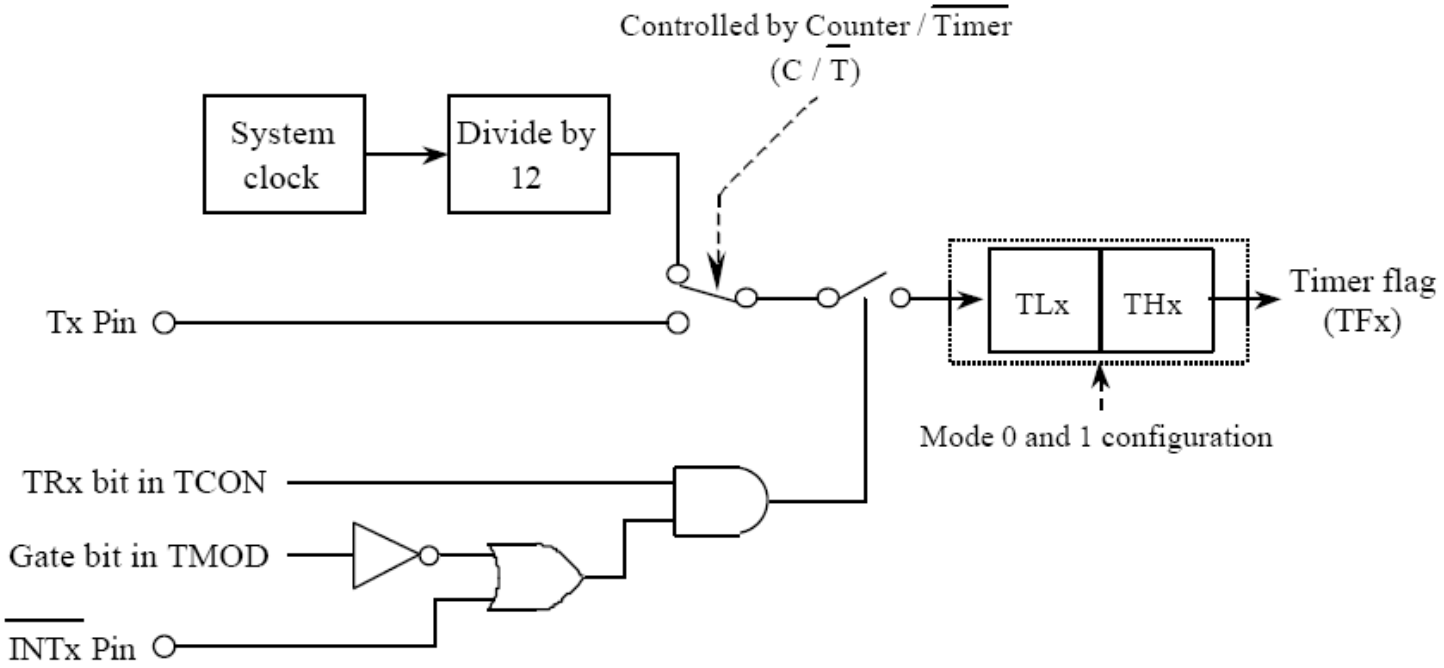
There are six interrupts including RESET in 8051.
•When the reset pin is activated, the 8051 jumps to the address location 0000. This is power-up reset.
•Two interrupts are set aside for the timers: one for timer 0 and one for timer 1. Memory locations are 000BH and 001BH respectively in the interrupt vector table.
•Two interrupts are set aside for hardware external interrupts. Pin no. 12 and Pin no. 13 in Port 3 are for the external hardware interrupts INT0 and INT1, respectively. Memory locations are 0003H and 0013H respectively in the interrupt vector table.
•Serial communication has a single interrupt that belongs to both receive and transmit. Memory location 0023H belongs to this interrupt.

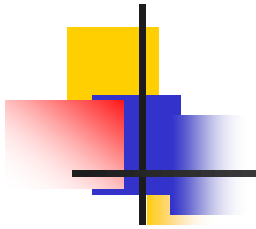
Timer & Counter Interrupts in 8x51 Microcontrollers

TMOD register for 8x51 microcontrollers:



The diagram below shows the timer/counter configurations.





Timer Modes

M1	M2	Mode
0	0	13-bit timer mode.
0	1	16-bit timer mode.
1	0	8-bit auto reload mode.
1	1	Spilt mode.

Mode 0 (13-Bit Timer Mode)

Both Timer 1 and Timer 0 in Mode 0 operate as 8-bit counters (with a divide-by-32 prescaler). Timer register is configured as a 13-bit register consisting of all the 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the register. The timer interrupt flag TF1 is set when the count rolls over from all 1s to all 0s. Mode 0 operation is the same for Timer 0 as it is for Timer 1.

Mode 1 (16-Bit Timer Mode)

Timer mode "1" is a 16-bit timer and is a commonly used mode. It functions in the same way as 13-bit mode except that all 16 bits are used. TLx is incremented starting from 0 to a maximum 255. Once the value 255 is reached, TLx resets to 0 and then THx is incremented by 1. As being a full 16-bit timer, the timer may contain up to 65536 distinct values and it will overflow back to 0 after 65,536 machine cycles.

Mode 2 (8 Bit Auto Reload)

Both the timer registers are configured as 8-bit counters (TL1 and TL0) with automatic reload. Overflow from TL1 (TL0) sets TF1 (TF0) and also reloads TL1 (TL0) with the contents of Th1 (TH0), which is preset by software. The reload leaves TH1 (TH0) unchanged.

Mode 3 (Split Timer Mode)

Timer mode "3" is known as **split-timer mode**. When Timer 0 is placed in mode 3, it becomes two separate 8-bit timers. Timer 0 is TL0 and Timer 1 is TH0. Both the timers count from 0 to 255 and in case of overflow, reset back to 0. All the bits that are of Timer 1 will now be tied to TH0.

Interrupt Enable Register

EA	-	ET2	ES	ET1	EX1	ET0	EX0

- **EA** − Global enable/disable.
- **-** − Undefined.
- **ET2** − Enable Timer 2 interrupt.
- **ES** − Enable Serial port interrupt.
- **ET1** − Enable Timer 1 interrupt.
- **EX1** − Enable External 1 interrupt.
- **ET0** − Enable Timer 0 interrupt.
- **EX0** − Enable External 0 interrupt.

Interrupt Priority in 8051

Interrupt priority can be altered by assigning the higher priority to any one of the interrupts. This is accomplished by programming a register called **IP** (interrupt priority).
IP register contains all 0's after reset.

-	-	-	-	PT1	PX1	PT0	PX0

Example:

A button (b1) and an LED, is connected to a microcontroller from 8x51 family as shown in the figure below. Ports have internal pull up resistors. Write a program that flashes the LED at f=10kHz frequency with 40% duty cycle (40% on, 60%off) as long as **b1** is pressed.