



BLG 231E - Digital Circuits

Assignment 4

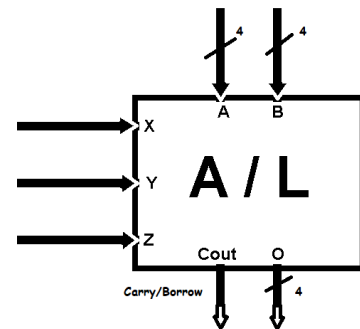
Due Date: Thursday, December 10, 2020, 23:59.

- Please **write and draw neatly**.
- Please prepare your homework using a computer. Points will be taken off for handwritten submissions.
- **Consequences of plagiarism:** Any cheating will be subject to disciplinary action.
- **No late submissions** will be accepted.
- **Submissions:** Submit your solution PDFs to Ninova. Please **write your full name** (first name and last name) **and Student ID** into your solution PDFs.

If you have any questions, please e-mail **Kıymet Kaya (kayak16@itu.edu.tr)**.

1. The combinational circuit ARITHMETIC/LOGIC (A/L) performs the following operations depending on the value of the control inputs X, Y, and Z.

| X | Y | Z | Result (O) | Cout |
|---|---|---|--------------|--------|
| 0 | 0 | 0 | $B - A$ | Borrow |
| 0 | 0 | 1 | $A + B$ | Carry |
| 0 | 1 | 0 | $A - 5$ | Borrow |
| 0 | 1 | 1 | Φ | Φ |
| 1 | 0 | 0 | $A \cdot B$ | Φ |
| 1 | 0 | 1 | Φ | Φ |
| 1 | 1 | 0 | $A \oplus B$ | Φ |
| 1 | 1 | 1 | Φ | Φ |



The meanings of symbols are given below:

| Symbol | Meaning |
|----------|--|
| + | Arithmetic addition |
| - | Arithmetic subtraction |
| \cdot | 4-bit logic AND between corresponding bits of A and B: $A_3 \cdot B_3, \dots, A_0 \cdot B_0$. |
| \oplus | 4-bit logic XOR between corresponding bits of A and B: $A_3 \oplus B_3, \dots, A_0 \oplus B_0$. |
| Φ | Don't care |

Design and draw this circuit using **only** the standard components and logic gates given below, paying attention to the maximum number allowed for the first three:

| Type | Maximum number allowed |
|-----------------------|------------------------|
| 4-bit parallel adders | 2 |
| 8:1 multiplexer | 1 |
| 2:4 decoder | 1 |
| XOR gates | No restriction |
| NOT gates | No restriction |
| OR gates | No restriction |
| AND gates | No restriction |

Note: Even though we have not specified a maximum number allowed on the last four, you should try to use as few as possible (also, you do not need to use all of the gates listed above). Your design should be as simple as possible, containing the fewest number of standard components and logic gates.