BLG351E Experiment 4 "Playing With Time" REPORT	CRN	11477
	Group	G17
	Name #1	Elif ARIKAN
	Name #2	Ömer Malik KALEMBAŞI

Q1) (25 pts.) Explain the TA0CTL register. How the bits of the register were set?

TA0CTL is the control register used to configure the timer.

Q2) (25 pts.) Explain the TA0CCR0 register. How the bits of the register were set?

Register that keeps the value which stops the timer. When TAR reaches to TA0CCR0, interrupt signal will be send.

Q3) (25 pts.) Explain the TA0CCTL0 register. How the bits of the register were set?

We use TA0CCTL0 for compare mode with set the CAP bit of its to zero.

Q4) (25 pts.) How to stop the timer interrupts?

TACCR0 = 0 to stop the Timer.

BLG351E Experiment 5 "LCD Display" REPORT	CRN	11477
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	Name #2	Ömer Malik KALEMBAŞI

Q1) (30 pts.) What is a nibble? How it is used for the LCD display?

A nibble is four bits and is also called a "half byte". The LCD display works by receiving 8-bit instructions. Since, the only upper nibble (D4-D7) of data bus are wired to micro- controller, we should use 4-bit working mode to utilize the LCD. We need 2 nibbles to process a command on the LCD display. While it creates the most significant part of the first nibble command, it creates the least significant half of the second nibble command that we send afterwards.

Q2) (40 pts.) Explain the purposes of input pins of the LCD display which are used in the experiment.

Rs pin which used for register select.
RS=0 :Instruction register, RS=1 : Data Register
R/w pin which is read or write pin which is used to select a read or write mode.
R/W = 0 : write, R/W = 1 : read.
EN pin which is enable pin and it is used to enable or display.
Data lines from 7 to 14 d0 d1 d2 d3 d4 d5 d6 d7, d0-d3 is connected to ground, d4-d5 is used to send from microcontroller to liquid crystal display.

Q3) (30 pts) Why the DDRAM address is changed for the next line of the LCD display?

Subsequent read or writes refer to the DDRAM. Sets the specified value into the address counter. Subsequent read or write operations transfer data from, or to, the display RAM. Adjacent display RAM locations do not necessarily refer to adjacent display positions.