DENEY RAPORU

Deney Adı	Transistor Amplifier Circuits
Deneyi Yaptıran Ar. Gör.	Melih Bilmez
Raporu Hazırlayan **(İsim / Numara / Bölüm)**	Ömer Malik Kalembaşı / 150180112 / Computer Engineering
Grup Numarası ve **Deney Tarihi**	C3/ March 24, 2021

Rapor Notu	Teslim Edildiği Tarih	Teslim Alındığı Tarih
	March 24, 2021	

Experiment 3.1.

Simulate the circuit shown in Fig.1. **BC847A should be used for BJT.**

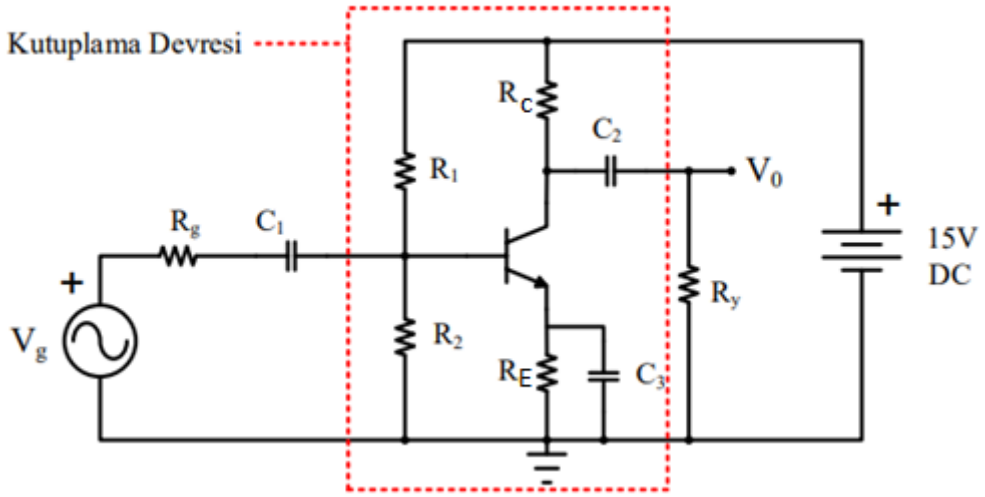


Figure 1. BJT Amplifier

Table 1. Values of components in circuit.

R_1	220 kΩ	**R_g**	10 kΩ
R_2	33 kΩ	**R_Y**	12 kΩ
R_C	8.2 kΩ	**$C_{1,2}$**	4.7 µF
R_E	1.2 kΩ	**C_3**	220 µF

Table 2. Input Signal Parameter (Vg) for experiment 3.1.

Exp: 3.1 – V_g	
Type	Sine
Frequency	5 kHz
DC Offset	0V

Outputs:

1. Note the DC operating points.

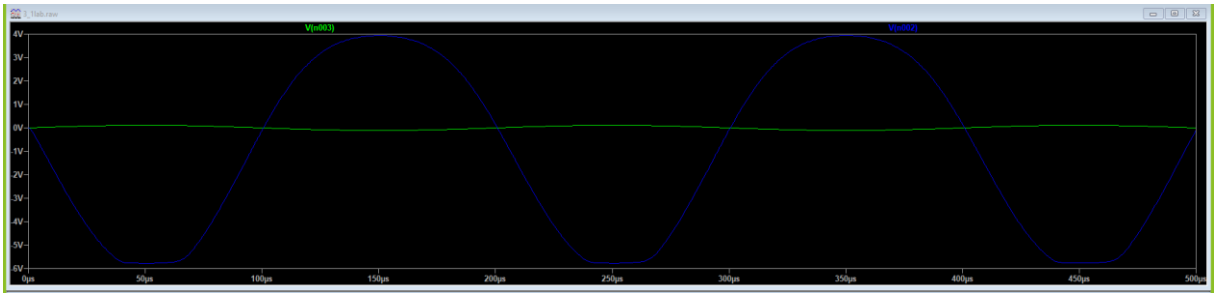
* D:\itu cmpe\spring 20-21\ehb311\deney3\3_1lab.asc

```
        --- Operating Point ---

V(c):           7.13985         voltage
V(b):           1.80684         voltage
V(e):           1.15653         voltage
V(n001):        15              voltage
V(n004):        8.49214e-014    voltage
V(n003):        0               voltage
V(n002):        4.02688e-013    voltage
Ic(Q1):         0.000958555     device_current
Ib(Q1):         5.21625e-006    device_current
Ie(Q1):         -0.000963771    device_current
I(C1):          8.49214e-018    device_current
I(C2):          -3.35573e-017   device_current
I(C3):          2.54436e-016    device_current
I(Ry):          3.35573e-017    device_current
I(Rg):          8.49214e-018    device_current
I(Re):          0.000963771     device_current
I(R2):          5.47527e-005    device_current
I(Rc):          0.000958555     device_current
I(R1):          5.99689e-005    device_current
I(V2):          8.49214e-018    device_current
I(V1):          -0.00101852     device_current
```

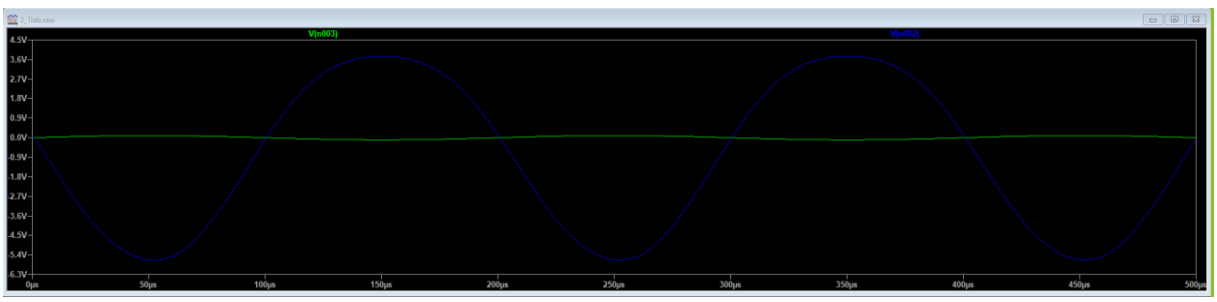
2. What is the Vg value at which clipping starts? Also, is there symmetrical clipping?

There is clipping, starts at Vg=110mV.



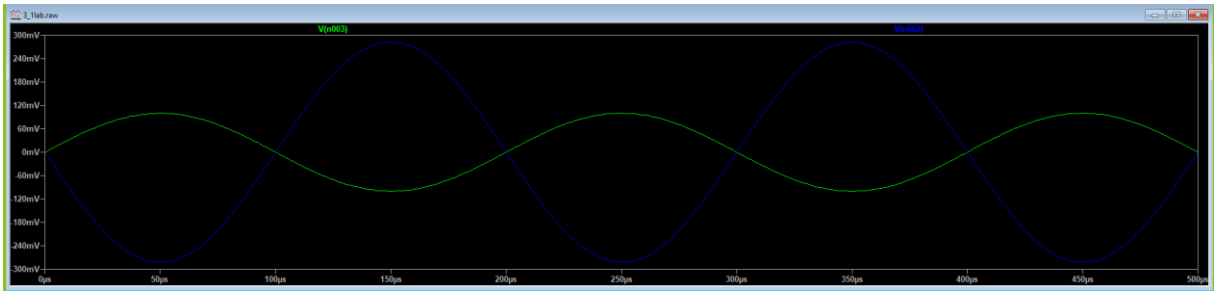
3. Plot the output voltage **(V_O-t)**, input voltage **(V_g -t)** and **(V_e-t)**. What is the voltage gain **(V_O/V_g)**?

3.7V/0.1V = 3



4. Remove the C_3 capacitor from circuit and repeat simulation. Plot the output voltage **(V_O-t)**, input voltage **(V_g -t)** and **(V_e-t)**. What is the voltage gain **(V_O/V_g)**?

282mV/100mV = 2.82



5. Explain the circuit and simulation results.

In AC operation, C3 capacitor will be bypass; in DC biasing resister Re will works. When C3 connected, performance gained.

Experiment 3.2.

Simulate the circuit shown in Fig.2. **BSP89 should be used for MOSFET.**

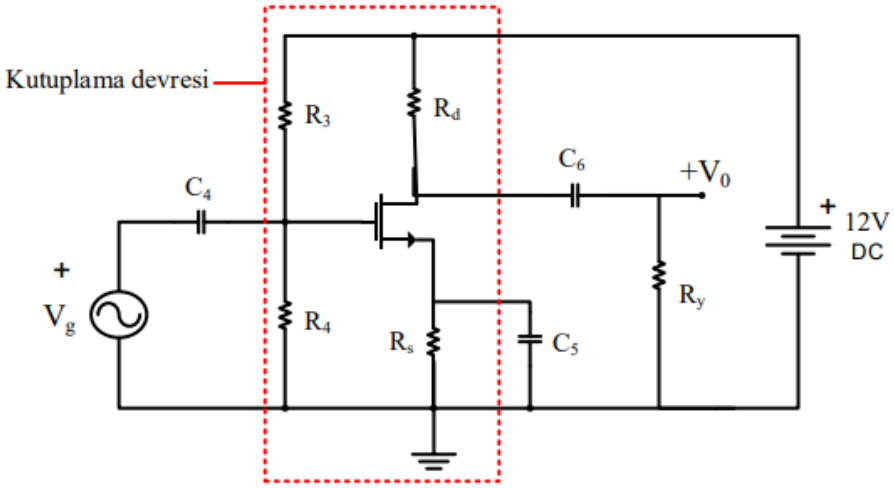


Figure 2. MOSFET Amplifier.

Table 4. Values of components in circuit.

R_3	820 kΩ	**R_S**	220 Ω
R_4	330 kΩ	**R_Y**	10 kΩ
R_d	1 kΩ	**$C_{4,5,6}$**	1 µF

Table 5. Input Signal Parameter (Vg) for experiment 3.2.

Exp: 3.2 – V_g	
Type	Sine
Frequency	50 kHz
DC Offset	0V

Outputs:

1. Note the DC operating points.

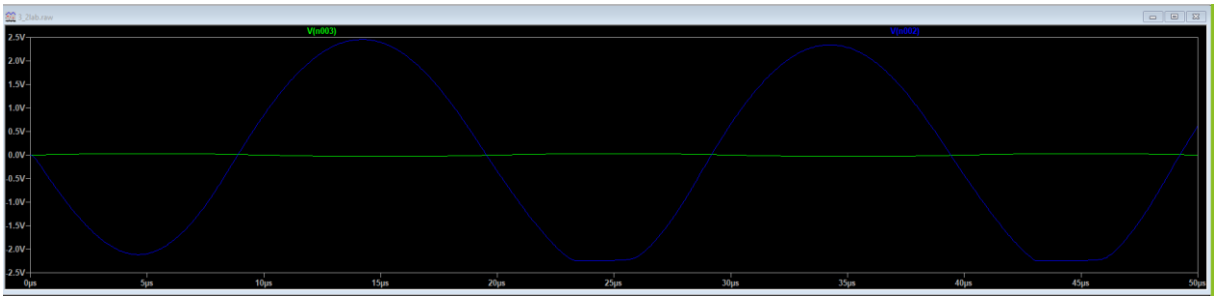
* D:\itu cmpe\spring 20-21\ehb311\deney3\3_2lab.asc

```
      --- Operating Point ---

V(n001):        12              voltage
V(g):           3.44348         voltage
V(d):           4.15258         voltage
V(s):           1.72643         voltage
V(n002):        4.15258e-014    voltage
V(n003):        0               voltage
Id(M1):         0.00784742      device_current
Ig(M1):         -1.14489e-010   device_current
Is(M1):         -0.00784742     device_current
I(C4):          3.44348e-018    device_current
I(C6):          -4.15258e-018   device_current
I(C3):          1.72643e-018    device_current
I(Ry):          4.15258e-018    device_current
I(Rs):          0.00784742      device_current
I(R4):          1.04348e-005    device_current
I(Rd):          0.00784742      device_current
I(R3):          1.04348e-005    device_current
I(Vg):          3.44348e-018    device_current
I(V1):          -0.00785785     device_current
```

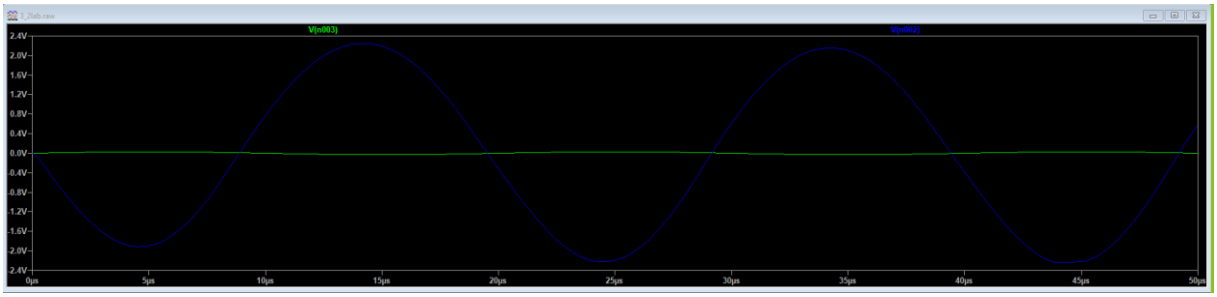
2. What is the Vg value at which clipping starts? Also, is there symmetrical clipping?

There is clipping, starts at Vg=33mV



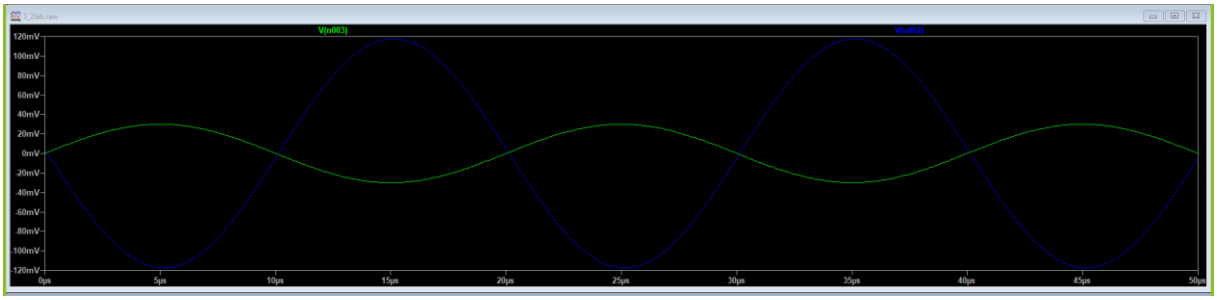
3. Plot the output voltage **(V_O-t)** and input voltage **(V_g -t)**. What is the voltage gain **(V_O/V_g)**?

V_O/V_g = 2.25/0.03 = 75



4. Remove the C_5 capacitor from circuit and repeat simulation. Plot the output voltage **(V_O-t)** and input voltage **(V_g –t).** What is the voltage gain **(V_O/V_g)**?

117mV/30mV = 3.9



5. Explain the circuit and simulation results.

In AC operation, C3 capacitor will be bypass; in DC biasing resister Rs will works. When c5 connected, performance gained.

Last Update: 30.10.2020