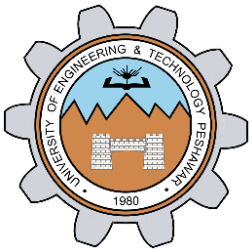
DSD LAB REPORT

LAB # 04



Spring 2021

CSE-308L Digital System Design Lab

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Class Section: **B**

"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Student Signature: _____

Submitted to:

Engr. Madiha Sher

May 06, 2021

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

OBJECTIVES:

This lab will enable students to:

- Code using Behavioral level modeling
- Implement an 8 Bit Ring Counter

TASK:

Implementation of an 8-bit Ring Counter

CODE:

```
ln #
 1 module Ring_8bit (clock, reset, Output);
 2         input clock, reset;
 3         output [7:0] Output;
 4         reg[7:0] A;
 5
 6         always @(posedge clock)
 7                 if (!reset)
 8                         A = 8'b00000001;
 9                 else
10                 begin
11                         A <=  A << 1;
12                         A[0] <= A[7];
13                 end
14                 assign Output = A;
15
16 endmodule
```

TestBench:

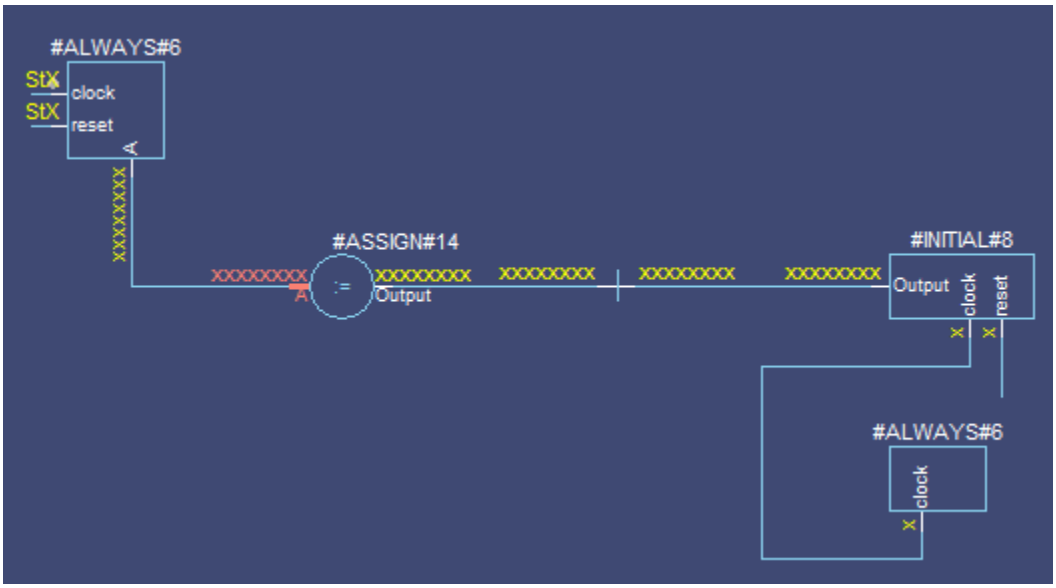
```
ln #
 1 module test_Ring;
 2         reg clock, reset;
 3         wire[7:0] Output;
 4
 5         Ring_8bit counter(clock, reset, Output);
 6         always
 7                 #1 clock = ~clock;
 8         initial
 9         begin
10                 $display("Clock|Reset| Output");
11                 clock = 0;
12                 reset = 1;
13                 $monitor("   %b    |    %b    |   %b",clock,reset,Output);
14
15                 #1 reset = 0;
16                 #1 reset = 1;
17                 #500 $finish;
18         end
19 endmodule
```

OUTPUTS

Truth Table:

```
run
# Clock|Reset| Output
#   0  |  1  | xxxxxxxx
#   1  |  0  | 00000001
#   0  |  1  | 00000001
#   1  |  1  | 00000010
#   0  |  1  | 00000010
#   1  |  1  | 00000100
#   0  |  1  | 00000100
#   1  |  1  | 00001000
#   0  |  1  | 00001000
#   1  |  1  | 00010000
#   0  |  1  | 00010000
#   1  |  1  | 00100000
#   0  |  1  | 00100000
#   1  |  1  | 01000000
#   0  |  1  | 01000000
#   1  |  1  | 10000000
#   0  |  1  | 10000000
#   1  |  1  | 00000001
#   0  |  1  | 00000001
#   1  |  1  | 00000010
#   0  |  1  | 00000010
```

Data Flow:



Wave Form: