Kalev Alpernas

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Research Interests

The intersection of Programming Languages and Serverless Computing:
Serverless, cloud, distributed systems, networks, SDNs, NFVs; Verification, abstract interpretation, formal methods, runtime verification, model checking, IFC, logic.

Education

2016–2021 (planned) **Ph.D. Candidate in Computer Science, Tel Aviv University, Tel Aviv, Israel.**
Advisor: Prof. Mooly Sagiv
Thesis: Correct and Secure Serverless Computing

2014–2016 **M.Sc. in Computer Science, Tel Aviv University, Tel Aviv, Israel.**
GPA: 94.
Advisors: Prof. Mooly Sagiv and Dr. Sharon Shoham
Thesis: Safety Verification of Stateful Networks

2007–2011 **B.Sc. in Computer Science, Tel Aviv University, Tel Aviv, Israel.**
GPA: 88.

Publications

2021 Cloud-Scale Runtime Verification of Serverless Applications. **Alpernas K.**, Panda A., Ryzhyk L., and Sagiv M. *ACM Symposium on Cloud Computing* (SoCC), November 2021.

2020 The wonderful wizard of LoC: paying attention to the man behind the curtain of lines-of-code metrics. **Alpernas K.**, Feldman Y., and Peleg H. *International Symposium on New Ideas, New Paradigms, and Reflections on Programming and Software* (Onward!), November 2020.

2019 Some Complexity Results for Stateful Network Verification. **Alpernas K.**, Panda A., Rabinovich A., Sagiv M., Shenker S., Shoham S., and Velner Y. *Formal Methods in System Design* (FMSD), Volume 54, November 2019.

2018 Secure Serverless Computing Using Dynamic Information Flow Control. **Alpernas K.**, Flanagan C., Fouladi S., Ryzhyk L., Sagiv M., Schmitz T., Winstein K. *Object-Oriented Programming, Systems, Languages and Applications* (OOPSLA), November 2018.

Abstract Interpretation of Stateful Networks. **Alpernas K.**, Manevich R., Panda A., Sagiv M., Shenker S., Velner Y., and Shoham S. *Static Analysis Symposium* (SAS), August 2018.

2016 | Some Complexity Results for Stateful Network Verification. Velner Y., **Alpernas K.**, Panda A., Rabinovich A., Sagiv M., Shenker S., and Shoham S. *Tools and Algorithms for the Construction and Analysis of Systems* (TACAS), April 2016.

Invited Talks

2020 | Correct and Secure Serverless Computing. *Presented at the Languages, Systems, and Data Seminar, UCSC*.

2017 | Modular Safety Verification for Stateful Networks. *Presented at the Israeli Networking Day*.
Modular Safety Verification for Stateful Networks. *Presented at the Communications Systems Engineering seminar, BGU*.

2016 | Some Complexity Results for Stateful Network Verification. *Presented at the Verification Day, TAU*.

Teaching

Tel Aviv University, Teaching Assistant

Fall 2019 | Techniques for Improving Software Productivity.

Fall 2016 | Techniques for Improving Software Productivity.

Fall 2016 | Computer Science Learning in the Community.

Professional Experience

VMware Research

2018 | **Research Intern**
Researched distributed run-time monitoring of cloud-native and serverless applications. Developed the Watchtower runtime monitoring project.

2017 | **Research Intern**
Researched applications of information flow control to serverless platforms. Developed the Trapeze IFC project.

Cadence Design Systems Inc.

2014-2016 | **Lead Software Engineer**
Perspec GUI Team
Sole developer on the team, in charge of all GUI aspects of an SoC and Firmware verification platform.

2012-2014 | **Lead Software Engineer**
Incisive Debug Analyzer Debugger GUI Team
Worked on the development of a post-process HVL and HDL debugger. In charge of developing the debugger GUI, particularly aspects of multi-language and multi-domain integration.

2010-2012 | **Software Engineer**
IntlliGen Constraint Solver Team

Worked on the development of a constrained pseudo-random generator and constraint solver. In charge of developing a constraint-solver and generation debugger, and developing the compiler subsystem.

2009-2010 **Product Validation Engineer**
IntlliGen Constraint Solver Team
Developed automated testing systems for validating the correctness of a constrained pseudo-random generator and constraint solver.

Service

External Reviewer: FMCAD'16, POPL'17, CAV'18, VMCAI'19, POPL'20.

Patents

2017 US 9,792,402 Method and system for debugging a system on chip under test.

2016 US 9,244,814 Enriched Log Viewer.

2015 US 9,189,743 System, Method, and Computer Program Product for Constraint Solving.