# Verilog Interview Questions Answers

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# **Verilog Interview Questions Answers**

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In Verilog certain type of assignments or expression are scheduled for execution at the same time and order of their execution is not guaranteed. This means they could be executed in any order and the order could be change from time to time. This non-determinism is called the race condition in Verilog.

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A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and Cin; A and B are the operands, and Cin is a bit carried in from the next less significant stage.

#### Verilog HDL Program for FULL ADDER | electrofriends.com

This is the one stop educational site for all Electronic and Computer students. If you want to learn something new then we are here to help. We work on Microcontroller projects, Basic Electronics, Digital electronics, Computer projects and also in basic c/c++ programs.

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State whether True or False a) Electro migration depends on current. b) In LOCOS selective oxide growth is achieved using Silicon dioxide. c) CVD process does not consume underlying silicon 2. To remove antenna effect which method is used (i) Metal Splitting (ii) Putting Antenna diode (iii) Metal Slotting (iv) Metal Over Etching

#### Learn Analog - Interview Questions : Analog Circuit Designing

23) Hold violations are prefered to fix \_\_\_\_. a. Befor placement b. After placement c. Before CTS d. AfterCTS ANS given : b (i think its wrong) According to me ...before CTS there is ideal clock and no real clock is present. if real clock is not present we dont know the skew and hence cannot fix hold accurately...

## Physical Design Objective Type of Questions and Answers

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