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23) Hold violations are preferred to fix _____. a. Before placement b. After placement c. Before CTS d. After CTS
ANS given : b (i think its wrong) According to me ...before CTS there is ideal clock and no real clock is present. if real clock is not present we don't know the skew and hence cannot fix hold accurately...

Physical Design Objective Type of Questions and Answers

In Verilog certain type of assignments or expression are scheduled for execution at the same time and order of their execution is not guaranteed. This means they could be executed in any order and the order could change from time to time. This non-determinism is called the race condition in Verilog.

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6) Explain what is a sub-report? Sub-report are inserted into the main part, just like a main report, you also pass queries and parameters to it.

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Why is the capacity of cache memory so limited?

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Case Study, Data Collection methods and Research Design ...

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Simulation - Wikipedia

As it is indicated in the title, this chapter includes the research methodology of the dissertation. In more details, in this part the author outlines the research strategy, the research method ...

CHAPTER 3 - RESEARCH METHODOLOGY: Data collection method ...

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