

Alexandria University
Faculty of Engineering
Electrical Engineering Department

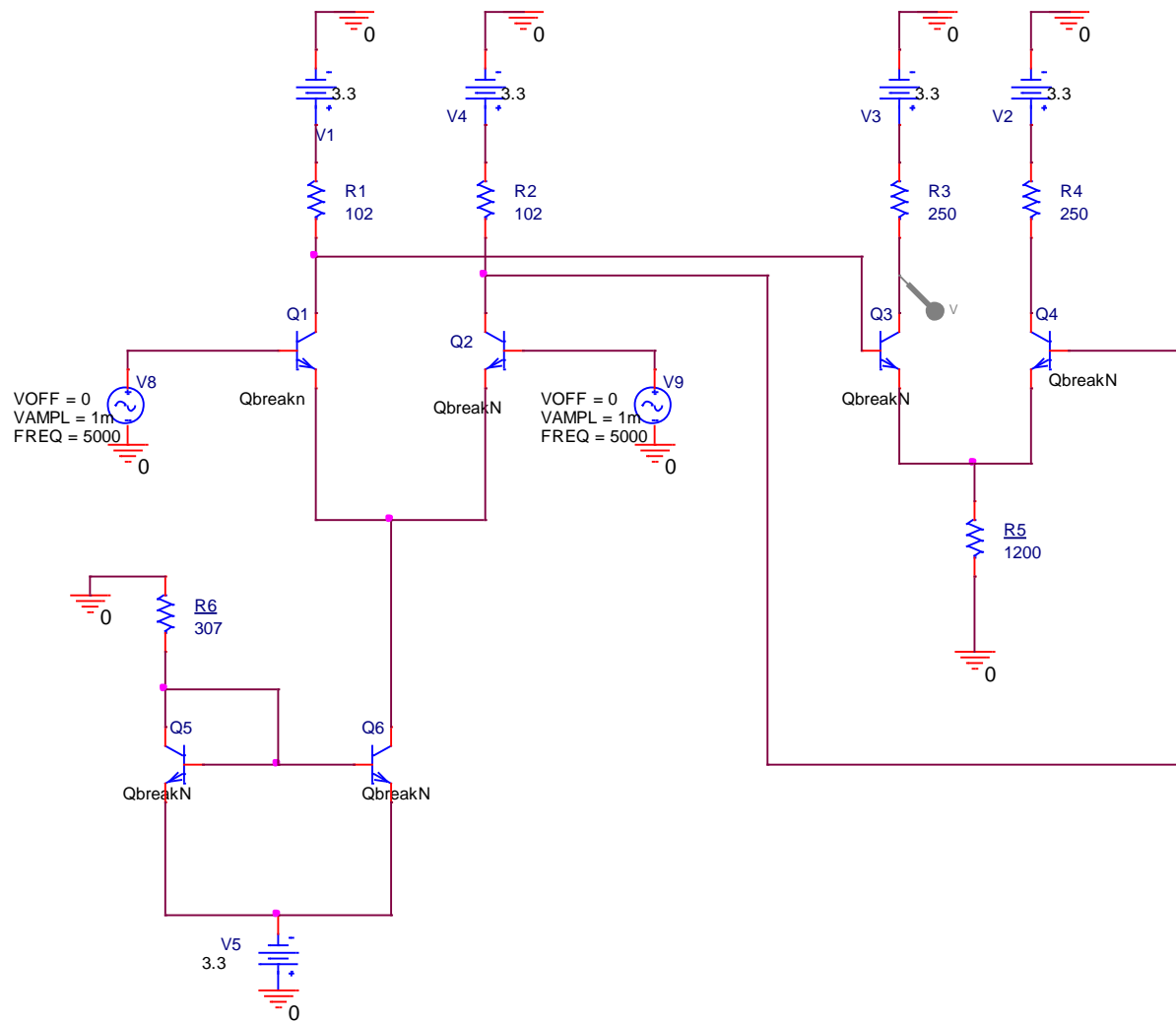


Electronics II: Project **Op-Amp Design**

By: Mostafa Mahmoud Khalil Hassan

Submitted to: Eng. Nour

Circuit Schematic



The unknowns are:

$$R1 = R2, R3 = R4, R5, R6$$

All DC Voltage sources are 3.3 V.

All transistors are NPN BJT transistors.

Hand Analysis

$$\beta = 120, C_{jc} = 1pF, C_{je} = 10pF$$

$$I_{EE1} = \frac{3.3 - 0.7}{R_6} = \frac{2.6}{R_6}$$

$$I_{c1} = I_{c2} \cong I_{E1} = I_{E1} = \frac{I_{EE1}}{2} = \frac{1.3}{R_6}$$

$$r_{\pi1} = \beta \frac{25mV}{I_{E1}} = 2.308R_6$$

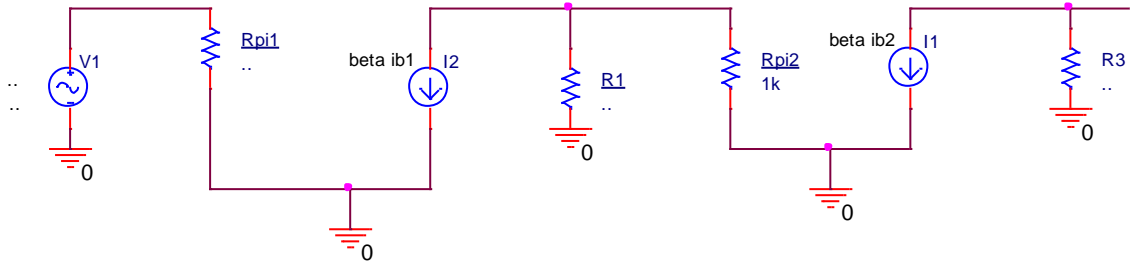
$$V_{c1} = V_{cc} - I_{c1}R_1$$

$$I_{EE2} = \frac{V_{c1} - 0.7}{R_5}$$

$$I_{c3} = I_{c4} \cong I_{E3} = I_{E4} = \frac{I_{EE2}}{2}$$

$$r_{\pi2} = \beta \frac{25mV}{I_{E3}} = \dots$$

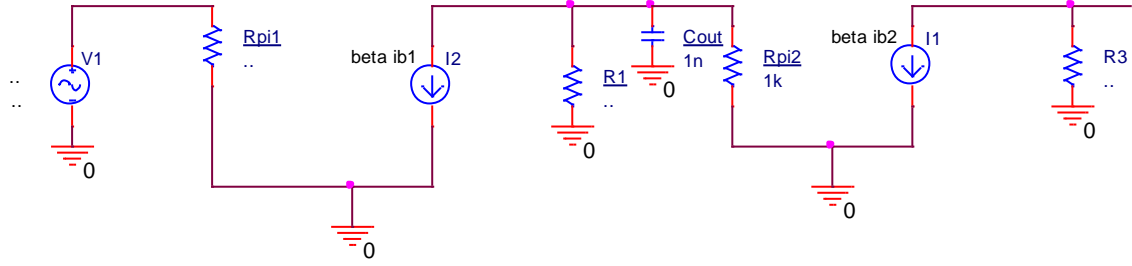
Solving half circuit:



$$A_2 = -\frac{\beta ib_3 R_3}{r_{\pi2} ib_3} = -\frac{\beta R_3}{r_{\pi2}}$$

$$A_1 = -\frac{\beta ib_1 (R_1 // r_{\pi2})}{ib_1 r_{\pi1}} = -\frac{\beta (R_1 // r_{\pi2})}{r_{\pi1}}$$

$$A_d = A_1 A_2 = \frac{\beta^2 R_3 (R_1 // r_{\pi2})}{r_{\pi1} r_{\pi2}}$$



$$C_{out} = 1 + \frac{1}{A_1} = 1.0625pF$$

$$f_{c2} = \frac{1}{2\pi C_{out}(R_1//r_{\pi2})} = \frac{1}{2\pi * 1.0625 * 99} = 1513.059$$

$$f_{c3} = \frac{1}{2\pi C_{in2}(R_1//r_{\pi2})} = 80MHz$$

$$C_{in2} = c_{je} + c_{jc}(1 + |A_2|) = 20pF$$

$$c_{je} = 10 pF \quad , c_{jc} = 1 pF$$

Using the values:

$$R_1 = R_2 = 102\Omega , R_3 = R_4 = 250\Omega , R_5 = 1200\Omega , R_6 = 307\Omega$$

$$\therefore r_{\pi1} = 708.556 \Omega \quad , \quad r_{\pi2} = 3320.91 \Omega$$

Voltage Gain:

$$A_v = \frac{\beta^2 R_3 (R_1//r_{\pi2})}{r_{\pi1} r_{\pi2}} = 151.402$$

Bandwidth:

$$BW = \frac{1}{2\pi * 2 * 10^{-11} * 98.96} = 802786310.82 Hz \cong 80MHz$$

Dissipated Power:

$$P_{diss} = 2(V_{cc}I_{c1} + V_{cc}I_{c3}) = 2 * 3.3 * (4.23456 + 0.90335) = 33.91mW$$

Input resistance:

$$R_{in} = 2 * r_{\pi1} = 1416.9\Omega$$

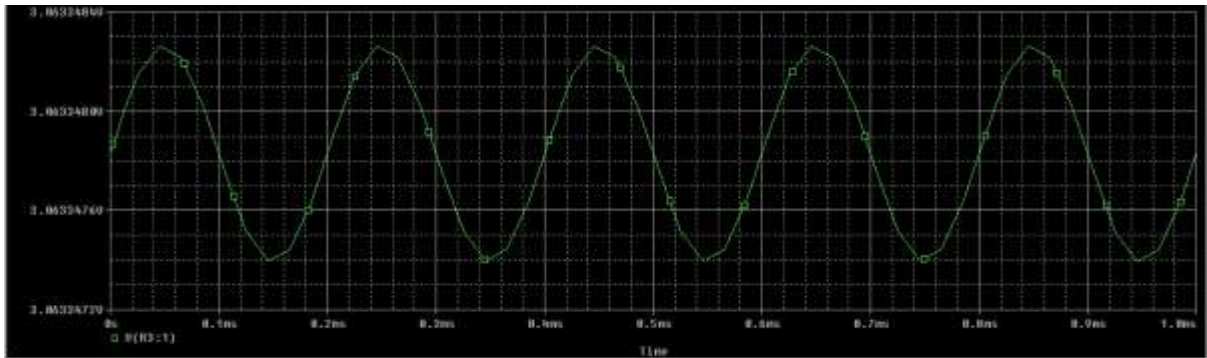
Output resistance:

$$R_{out} = R_3 = 250\Omega$$

When $V_{ce2} > 0.2 \text{ v}$
 So it is from $V_{ce} = 0.2V$ to $V_{cc} = 3.3V$
 $V_{ce2} = V_{cc} - I_c(R_3 + 2R_5) = 3.1 \text{ v}$

Output swing: 0.2 mV peak to peak

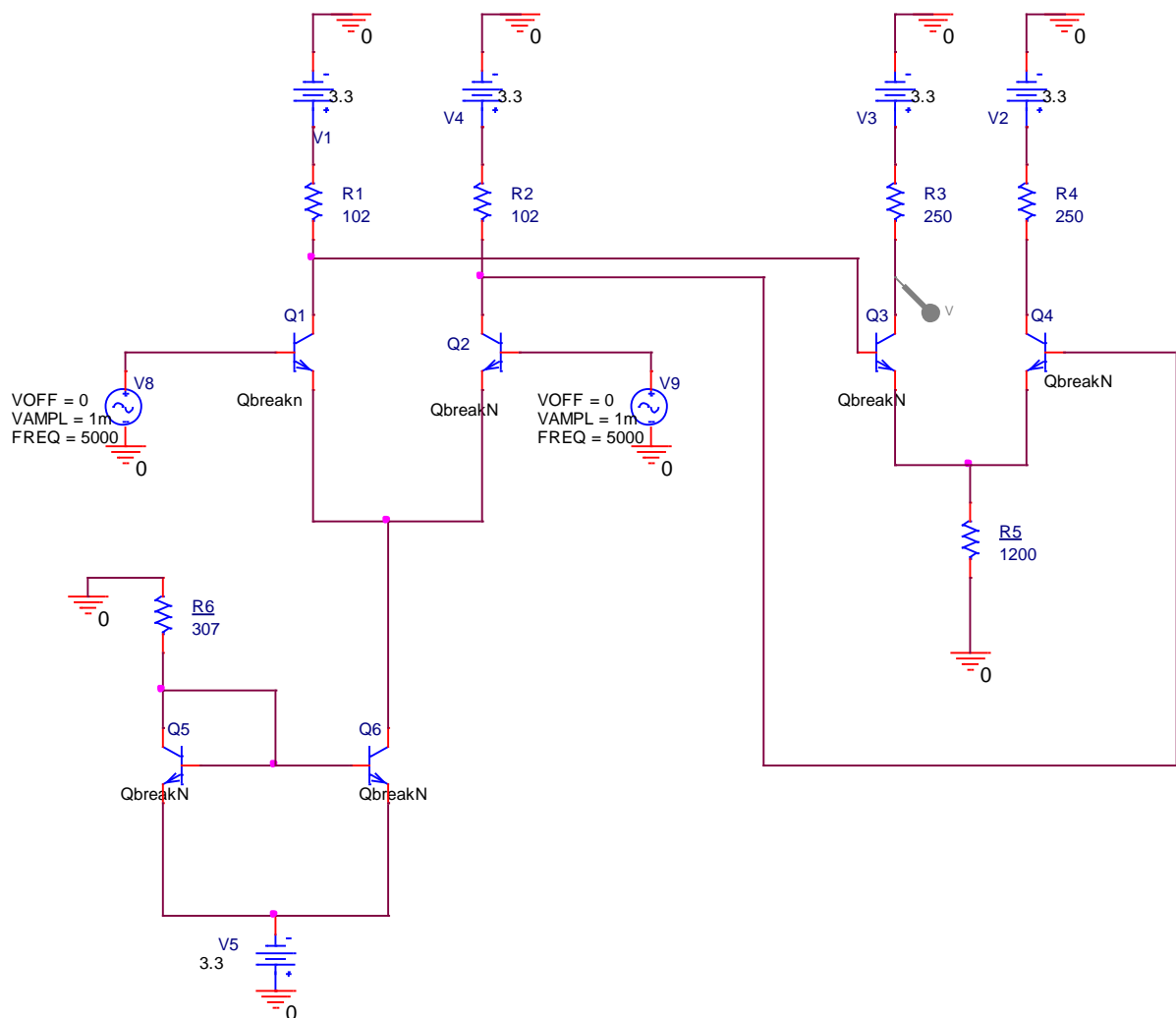
The schematic diagram illustrates a four-stage CMOS differential amplifier. It consists of two main signal paths, each containing two stages. The first stage (left) uses NMOS transistors Q1 and Q2 as input devices, with PMOS load devices Q3 and Q4. The second stage (right) uses PMOS transistors Q5 and Q6 as input devices, with NMOS load devices Q7 and Q8. The circuit includes various biasing components such as current sources (I1, I2), resistors (R1, R2, R3, R4, R5, R6), and capacitors (C1, C2). The output nodes are labeled Vout1 and Vout2. The simulation results show a differential-mode voltage gain of approximately 100 dB and a common-mode rejection ratio (CMRR) of about 60 dB.

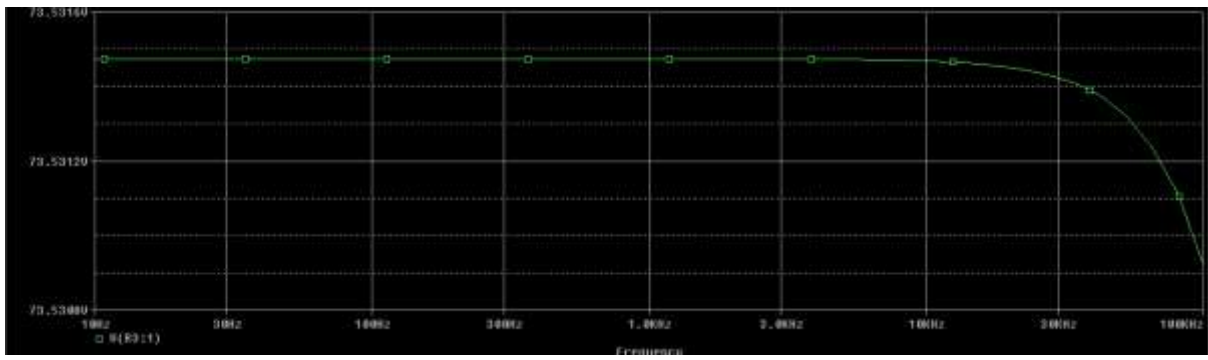
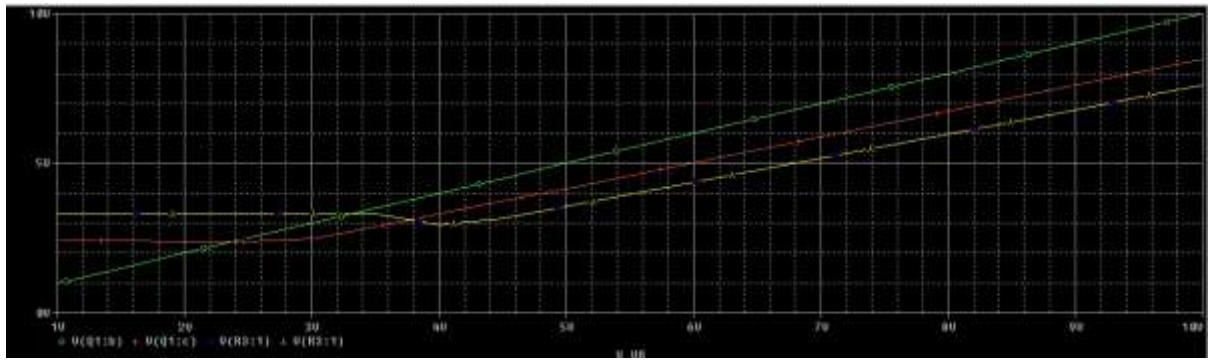


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Fe ba2y el rsomat hena el mafrod b3d el sin de ...

DC Sweep





Fe bardu ba2y rsomat hena .. el simulation el gamel msh 3arf azabato :D