

# Using ADC on Firebird-V Robot

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# Agenda for Discussion

## 1 Analog to Digital Conversion

- Need for ADC
- ADC of LPC2148
- ADC Channels

## 2 Coding ADC

- ADC Initialization
- ADxCR
- ADxGDR
- Program



# Need for ADC



# Need for ADC

✓ IR Proximity sensors



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- ✓ IR Proximity sensors
- ✓ Sharp IR Range sensors



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- ✓ IR Proximity sensors
- ✓ Sharp IR Range sensors
- ✓ white line sensors



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# In-Built ADC of LPC2148



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✓ 10-bit Resolution



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- ✓  $>2.44 \mu\text{s}$  Conversion Time



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- ✓ Input multiplexing among 8 pins in ADC1.
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- ✓ Burst conversion mode for single or multiple inputs.
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- ✓ Global Start command for both converters.
- ✓ Free Running or Single Conversion Mode
- ✓ Interrupt on ADC Conversion complete



# ADC Channels

- Table for ADC Channels

Pin No.	Pin Name	Description
P0.13	AD1.4	ADC input for Battery Voltage Monitoring
P0.29	AD0.2	ADC input for White Line Sensor 3(Right)
P0.28	AD0.1	ADC input for White Line Sensor 2(Center)
P0.12	AD1.3	ADC input for White Line Sensor 1(Left)
P0.4	AD0.6	ADC input for Sharp IR range sensor 2
P0.6	AD1.0	ADC input for Sharp IR range sensor 3
P0.5	AD0.7	ADC input for Sharp IR range sensor 4



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P0.4	AD0.6	ADC input for Sharp IR range sensor 2
P0.6	AD1.0	ADC input for Sharp IR range sensor 3
P0.5	AD0.7	ADC input for Sharp IR range sensor 4



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- 2 **AD1CR** for **ADC1** - ADC1 Control Register



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- ✓ Both the Registers are of 32 Bits.



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- ➋ **AD1CR** for **ADC1** - ADC1 Control Register

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16	BURST	To disable Repeated conversions	



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16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	



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7-0	SEL	Selects pins to be sampled and converted	00000000
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16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	000
20	-	Reserved	0
21	PDN	operational or power-down mode	



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19-17	CLKS	Selects the number of clocks	000
20	-	Reserved	0
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16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	000
20	-	Reserved	0
21	PDN	operational or power-down mode	1
23-22	-	Reserved	



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7-0	SEL	Selects pins to be sampled and converted	00000000
15-8	CLKDIV	To produce the clock	0000 <b>1110</b>
16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	000
20	-	Reserved	0
21	PDN	operational or power-down mode	<b>1</b>
23-22	-	Reserved	0



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7-0	SEL	Selects pins to be sampled and converted	00000000
15-8	CLKDIV	To produce the clock	0000 <b>1110</b>
16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	000
20	-	Reserved	0
21	PDN	operational or power-down mode	<b>1</b>
23-22	-	Reserved	0
26-24	START	Control start of ADC conversion	



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7-0	SEL	Selects pins to be sampled and converted	00000000
15-8	CLKDIV	To produce the clock	00001110
16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	000
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21	PDN	operational or power-down mode	1
23-22	-	Reserved	0
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This register is Used to control ADC operation

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7-0	SEL	Selects pins to be sampled and converted	00000000
15-8	CLKDIV	To produce the clock	0000 <b>1110</b>
16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	000
20	-	Reserved	0
21	PDN	operational or power-down mode	<b>1</b>
23-22	-	Reserved	0
26-24	START	Control start of ADC conversion	000
27	EDGE	Rising or falling edge	



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This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7-0	SEL	Selects pins to be sampled and converted	00000000
15-8	CLKDIV	To produce the clock	0000 <b>1110</b>
16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	000
20	-	Reserved	0
21	PDN	operational or power-down mode	<b>1</b>
23-22	-	Reserved	0
26-24	START	Control start of ADC conversion	000
27	EDGE	Rising or falling edge	0



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7-0	SEL	Selects pins to be sampled and converted	00000000
15-8	CLKDIV	To produce the clock	00001110
16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	000
20	-	Reserved	0
21	PDN	operational or power-down mode	1
23-22	-	Reserved	0
26-24	START	Control start of ADC conversion	000
27	EDGE	Rising or falling edge	0
31-28	-	Reserved	



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This register is Used to control ADC operation

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7-0	SEL	Selects pins to be sampled and converted	00000000
15-8	CLKDIV	To produce the clock	00001110
16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	000
20	-	Reserved	0
21	PDN	operational or power-down mode	1
23-22	-	Reserved	0
26-24	START	Control start of ADC conversion	000
27	EDGE	Rising or falling edge	0
31-28	-	Reserved	0000





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7-0	SEL	Selects pins to be sampled and converted	00000000
15-8	CLKDIV	To produce the clock	00001110
16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	000
20	-	Reserved	0
21	PDN	operational or power-down mode	1
23-22	-	Reserved	0
26-24	START	Control start of ADC conversion	000
27	EDGE	Rising or falling edge	0
31-28	-	Reserved	0000



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This register is Used to control ADC operation

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7-0	SEL	Selects pins to be sampled and converted	00000000
15-8	CLKDIV	To produce the clock	0000 <b>1110</b>
16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	000
20	-	Reserved	0
21	PDN	operational or power-down mode	<b>1</b>
23-22	-	Reserved	0
26-24	START	Control start of ADC conversion	000
27	EDGE	Rising or falling edge	0
31-28	-	Reserved	0000

ADxCR=0x00200E00;



# ADxCR- ADCx Control Register

This register is Used to control ADC operation

Bit	Symbol	Description	Bit Value
7-0	SEL	Selects pins to be sampled and converted	00000000
15-8	CLKDIV	To produce the clock	00001110
16	BURST	To disable Repeated conversions	0
19-17	CLKS	Selects the number of clocks	000
20	-	Reserved	0
21	PDN	operational or power-down mode	1
23-22	-	Reserved	0
26-24	START	Control start of ADC conversion	000
27	EDGE	Rising or falling edge	0
31-28	-	Reserved	0000

ADxCR=0x00200E00;



# ADxCR

contd...



# ADxCR

contd...



# ADxCR

contd...

- Bits 7-0 in ADxCR(SEL)

SEL	Description
7	1- ADx.7 is sampled and converted 0- ADx.7 is not sampled and converted
6	1- ADx.6 is sampled and converted 0- ADx.6 is not sampled and converted
5	1- ADx.5 is sampled and converted 0- ADx.5 is not sampled and converted
4	1- ADx.4 is sampled and converted 0- ADx.4 is not sampled and converted
3	1- ADx.3 is sampled and converted 0- ADx.3 is not sampled and converted
2	1- ADx.2 is sampled and converted 0- ADx.2 is not sampled and converted
1	1- ADx.1 is sampled and converted 0- ADx.1 is not sampled and converted
0	1- ADx.0 is sampled and converted 0- ADx.0 is not sampled and converted



# ADxCR

contd...



# ADxCR

contd...

- Bits 19-17 in ADxCR (CLKS)

Bit Value	Function
000	11clocks/ 10bits
001	10clocks/ 9bits
010	9clocks/ 8bits
011	8clocks/ 7bits
100	7clocks/ 6bits
101	6clocks/ 5bits
110	5clocks/ 4bits
111	4clocks/ 3bits





# ADxCR

contd...

- Bits 19-17 in ADxCR (CLKS)

Bit Value	Function
000	11clocks/ 10bits
001	10clocks/ 9bits
010	9clocks/ 8bits
011	8clocks/ 7bits
100	7clocks/ 6bits
101	6clocks/ 5bits
110	5clocks/ 4bits
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# ADxCR

contd...



# ADxCR

contd...

- Bits 26-24 in ADxCR(START): When the BURST bit is 0, these bits control whether and when an A/D conversion is started,

Bit Value	Function
000	No start
001	Start Conversion now
010	Start conversion when the edge occurs on P0.16/MAT0.2
011	Start conversion when the edge occurs on P0.22/MAT0.0
100	Start conversion when the edge occurs on MAT0.1
101	Start conversion when the edge occurs on MAT0.3
110	Start conversion when the edge occurs on MAT1.0
111	Start conversion when the edge occurs on MAT1.1



# ADxCR

contd...

- Bits 26-24 in ADxCR(START): When the BURST bit is 0, these bits control whether and when an A/D conversion is started,

Bit Value	Function
000	No start
001	Start Conversion now
010	Start conversion when the edge occurs on P0.16/MAT0.2
011	Start conversion when the edge occurs on P0.22/MAT0.0
100	Start conversion when the edge occurs on MAT0.1
101	Start conversion when the edge occurs on MAT0.3
110	Start conversion when the edge occurs on MAT1.0
111	Start conversion when the edge occurs on MAT1.1



# ADxGDR - A/D Global Data Register

This register contains the ADC's DONE bit and the result of the most recent A/D conversion.

Bit	Symbol	Description
5-0	-	Reserved
15-6	RESULT	When DONE is 1, this field contains ADC converted data
23-16	-	Reserved
26-24	CHN	Channel Number
29-27	-	Reserved
30	OVERUN	1 if the results of one or more conversions were lost before the conversion that produced the result in the RESULT bits.
31	DONE	This bit is set to 1 when an A/D conversion completes.



# Syntax for C-Program

## ADC Initialization



# Syntax for C-Program

## ADC Initialization

Init\_ADC\_Pin



# Syntax for C-Program

## ADC Initialization

### Init\_ADC\_Pin

```
void Init_ADC_Pin (void) //Configure ADC Ports
{

PINSEL0= 0x0F003F00; //Set pins P0.4, P0.5, P0.6, P0.12, P0.13 as ADC pins
PINSEL1= 0x05000000; //Set pins P0.28 and P0.29 as ADC pins

}
```





# Syntax for C-Program

## ADC Initialization

### Init\_ADC\_Pin

```
void Init_ADC_Pin (void) //Configure ADC Ports
{
    PINSEL0= 0x0F003F00; //Set pins P0.4, P0.5, P0.6, P0.12, P0.13 as ADC pins
    PINSEL1= 0x05000000; //Set pins P0.28 and P0.29 as ADC pins
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### ADC Initialization



# Syntax for C-Program

## ADC Initialization

### Init\_ADC\_Pin

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    PINSEL0= 0x0F003F00; //Set pins P0.4, P0.5, P0.6, P0.12, P0.13 as ADC pins
    PINSEL1= 0x05000000; //Set pins P0.28 and P0.29 as ADC pins
}
```

### ADC Initialization

```
void Init_ADC() //Set Register Values for starting ADC
{
    AD0CR =
    AD1CR =
}
```



# Syntax for C-Program

## ADC Initialization

### Init\_ADC\_Pin

```
void Init_ADC_Pin (void) //Configure ADC Ports
{
    PINSEL0= 0x0F003F00; //Set pins P0.4, P0.5, P0.6, P0.12, P0.13 as ADC pins
    PINSEL1= 0x05000000; //Set pins P0.28 and P0.29 as ADC pins
}
```

### ADC Initialization

```
void Init_ADC() //Set Register Values for starting ADC
{
    AD0CR =
    AD1CR =
}
```



# Syntax for C-Program Program



# Syntax for C-Program

## Program

Main Program



# Syntax for C-Program

## Program

### Main Program

```
int main(void)
{
    Init_Peripherals();
    LCD_Init();
    while(1)
    {
        LCD_Print(2,1,AD1_Conversion(3),3); //whiteline Left
        LCD_Print(2,7,ADO_Conversion(1),3); //whiteline Center
        LCD_Print(2,13,ADO_Conversion(2),3); //whiteline Right
    }
}
```



# Syntax for C-Program

## Program

### Main Program

```
int main(void)
{
    Init_Peripherals();
    LCD_Init();
    while(1)
    {
        LCD_Print(2,1,AD1_Conversion(3),3); //whiteline Left
        LCD_Print(2,7,ADO_Conversion(1),3); //whiteline Center
        LCD_Print(2,13,ADO_Conversion(2),3); //whiteline Right
    }
}
```



# Syntax for C-Program

## Program





# Syntax for C-Program Program

## AD0 Conversion Function



# Syntax for C-Program

## Program

### AD0 Conversion Function

```
unsigned char AD0_Conversion(unsigned char Ch)
{
    unsigned int Temp;
    if(channel!=0)
    {
        ADOCR = (ADOCR & 0xFFFFF00) | (1<<channel);
    }
    else
    {
        ADOCR = (ADOCR & 0xFFFFF00) | 0x01;
    }
    ADOCR|=(1 << 24);
    while((ADOGDR & 0x80000000)==0);
    Temp = ADOGDR;
    Temp = (Temp>>8) & 0xFF;
    return Temp;
}
```



# Syntax for C-Program Program



# Syntax for C-Program Program

## AD1 Conversion Function



# Syntax for C-Program

## Program

### AD1 Conversion Function

```
unsigned char AD1_Conversion(unsigned char Ch)
{
    unsigned int Temp;
    if(channel!=0)
    {
        AD1CR = (AD1CR & 0xFFFFFFF0) | (1<<channel);
    }
    else
    {
        AD1CR = (AD1CR & 0xFFFFFFF0) | 0x01;
    }
    AD1CR|=(1 << 24);
    while((AD1GDR & 0x80000000)==0);
    Temp = AD1GDR;
    Temp = (Temp>>8) & 0xFF;
    return Temp;
}
```



# Thank You!

Post your queries on: <http://qa.e-yantra.org/>

