DC Motor Velocity Control Using Pulse Width Modulation (PWM)

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Agenda for Discussion

1. Introduction
   - Pulse Width Modulation
   - Duty Cycle
2. PWM Generation in AVR
   - Timer in AVR
   - Timer for PWM generation in Firebird
3. PWM Generation in Firebird V
   - Registers
   - TCCR5A
   - TCCR5B
   - TCNT5
   - OCR5
   - Block Diagram
   - Program

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Duty Cycle

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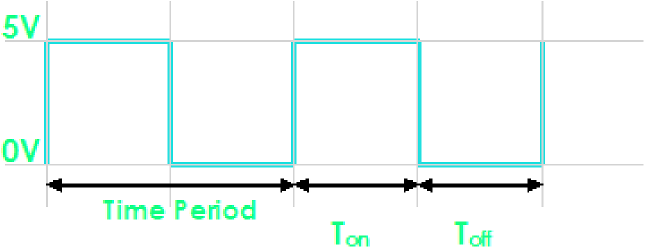
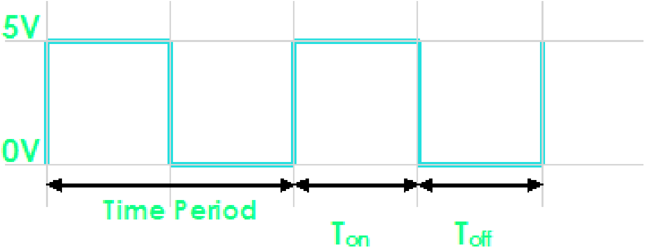


Duty Cycle



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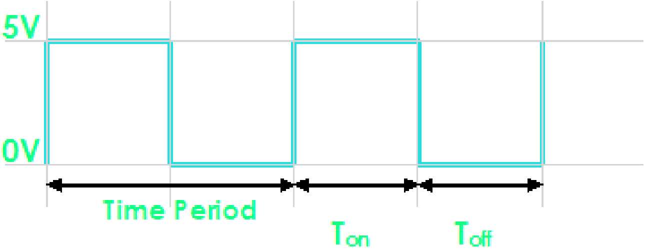

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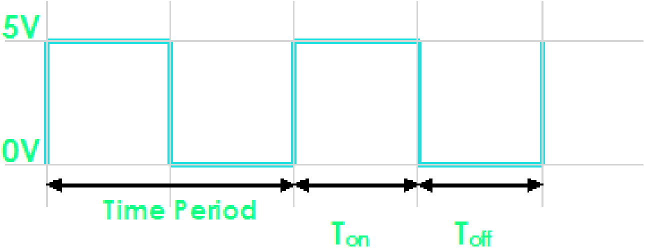

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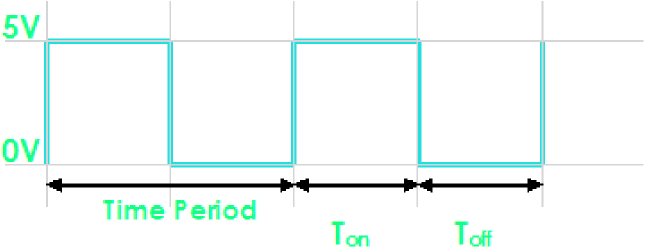

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- ✓ Ton = Time the output remains high.
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- ✓ When output is high the voltage is 5v

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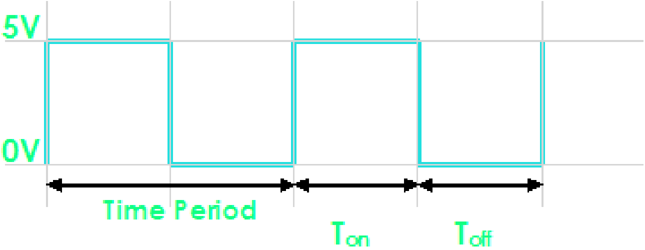

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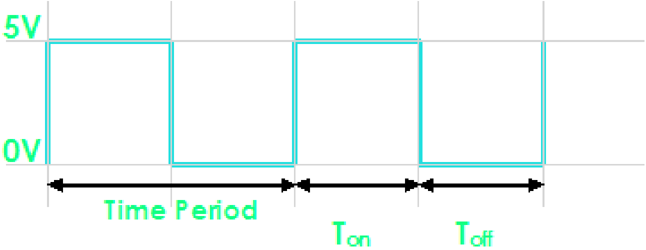

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- ✓ Ton = Time the output remains high.
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- ✓ When output is high the voltage is 5v
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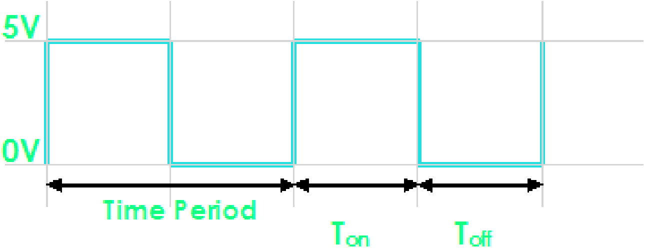
- ✓ Time Period(T) = Ton + Toff

Duty Cycle



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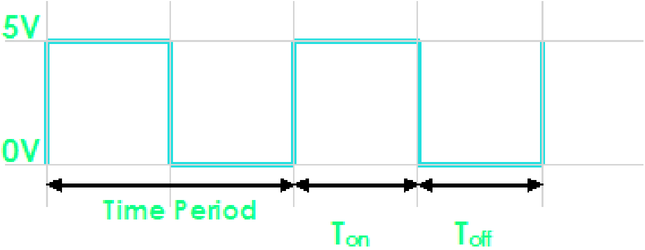
- ✓ Time Period(T) = Ton + Toff
- ✓ Duty Cycle = Ton*100/(Ton + Toff)

Duty Cycle



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- ✓ Ton = Time the output remains high.
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- ✓ When output is high the voltage is 5v
- ✓ When output is low the voltage is 0v
- ✓ Time Period(T) = Ton + Toff
- ✓ Duty Cycle = Ton*100/(Ton + Toff)
- ✓ Duty Cycle = 50%

Duty Cycle (Contd..)

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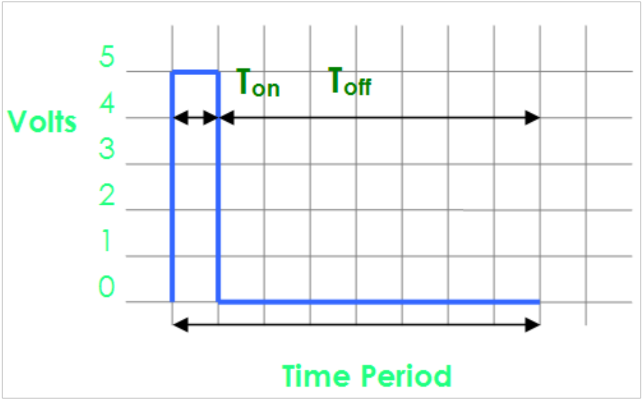
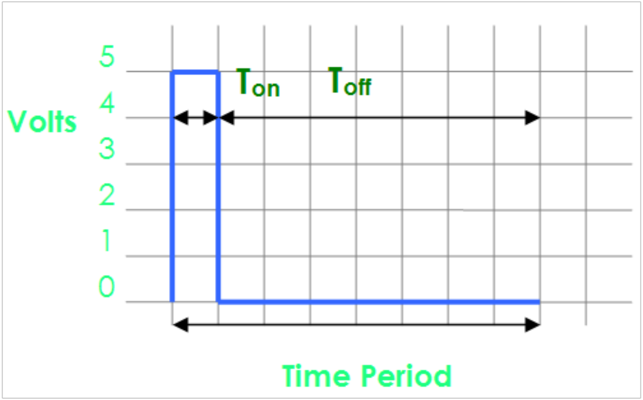
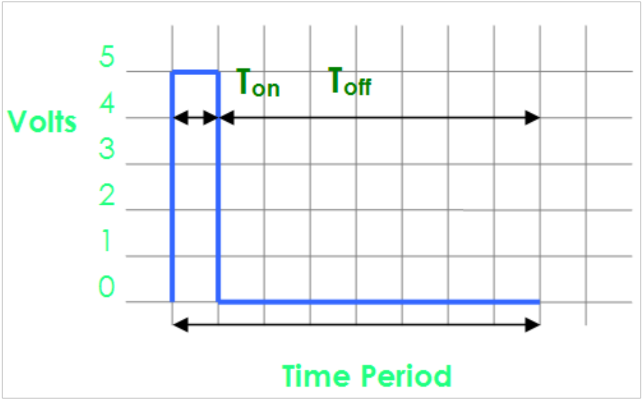


Duty Cycle (Contd..)



✓ Ton = Time the output remains high = 1

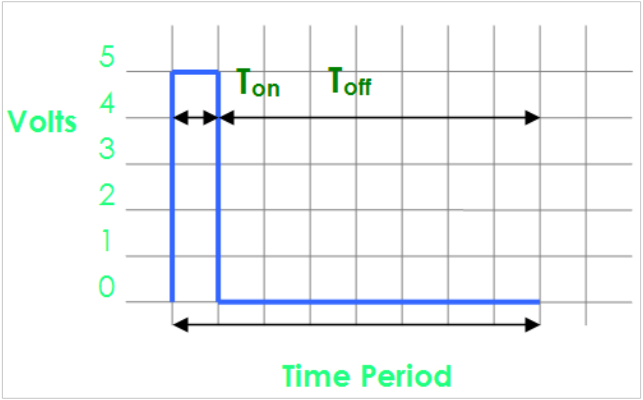
Duty Cycle (Contd..)



✓ Ton = Time the output remains high = 1

✓ Toff = Time the output remains Low = 7

Duty Cycle (Contd..)



- ✓ Ton = Time the output remains high = 1
- ✓ Toff = Time the output remains Low = 7
- ✓ Duty Cycle = 12.5%

Duty Cycle (Contd..)

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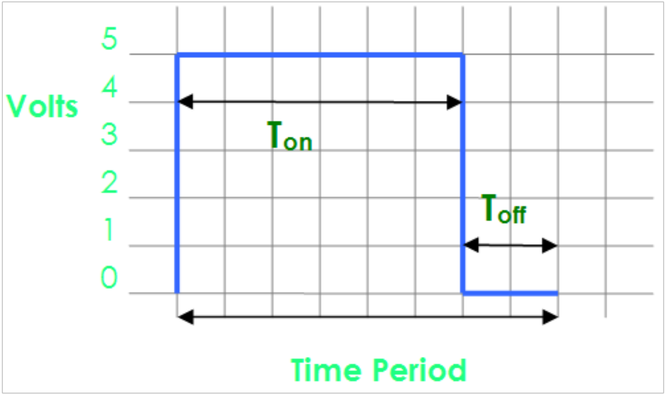
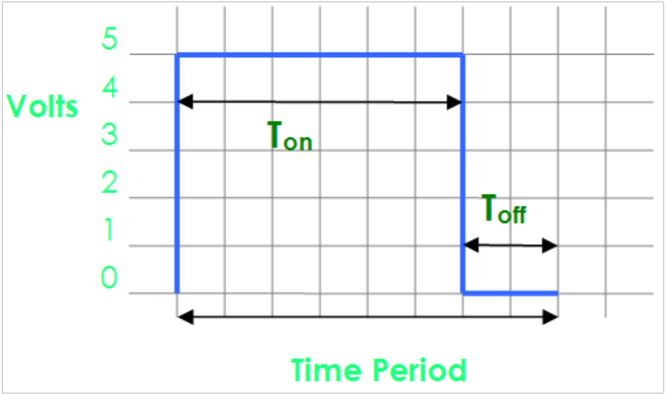
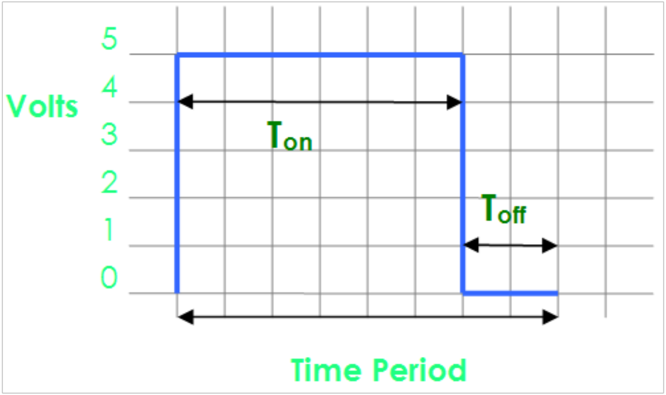


Duty Cycle (Contd..)



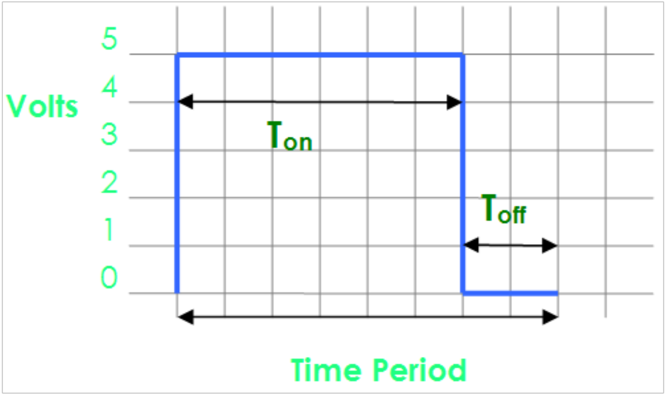
- ✓ Ton = Time the output remains high = 6

Duty Cycle (Contd..)



- ✓ Ton = Time the output remains high = 6
- ✓ Toff = Time the output remains Low = 2

Duty Cycle (Contd..)



- ✓ Ton = Time the output remains high = 6
- ✓ Toff = Time the output remains Low = 2
- ✓ Duty Cycle = 75%

Timer in AVR

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   - For 8-bit counter, roll over occurs at 255 count and
   - For 16-bit counter it occurs at 65535 count

Timer for PWM generation in Firebird

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3. Using FAST PWM mode to vary speed of motors

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    - TCCR5A
    - TCCR5B
    - TCNT5
    - OCR5n

TCCR5A- Timer Counter Control Register A

This register is Used to Configure Timer for PWM generation

TCCR5A- Timer Counter Control Register A

This register is Used to Configure Timer for PWM generation

Bit	Symbol	Description	Bit Value
7	COM5A1	Compare Output Mode for Channel A bit 1	1
6	COM5A0	Compare Output Mode for Channel A bit 0	0
5	COM5B1	Compare Output Mode for Channel B bit 1	1
4	COM5B0	Compare Output Mode for Channel B bit 0	0
3	COM5C1	Compare Output Mode for Channel C bit 1	1
2	COM5C0	Compare Output Mode for Channel C bit 0	0
1	WGM11	Waveform Generation Mode bit 1	0
0	WGM10	Waveform Generation Mode bit 0	1

TCCR5A- Timer Counter Control Register A

This register is Used to Configure Timer for PWM generation

Bit	Symbol	Description	Bit Value
7	COM5A1	Compare Output Mode for Channel A bit 1	1
6	COM5A0	Compare Output Mode for Channel A bit 0	0
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4	COM5B0	Compare Output Mode for Channel B bit 0	0
3	COM5C1	Compare Output Mode for Channel C bit 1	1
2	COM5C0	Compare Output Mode for Channel C bit 0	0
1	WGM11	Waveform Generation Mode bit 1	0
0	WGM10	Waveform Generation Mode bit 0	1

TCCR5A=0xA9

Compare Output Mode Fast PWM

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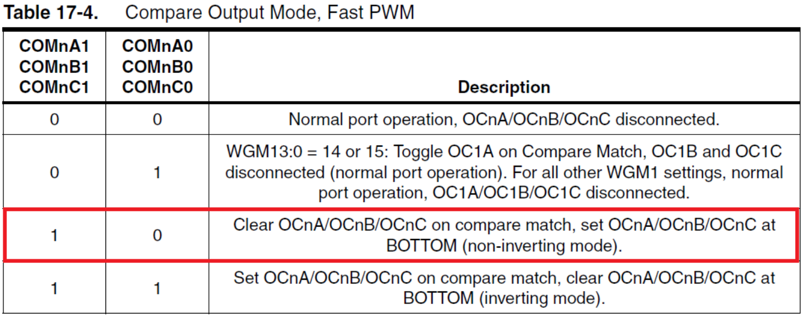


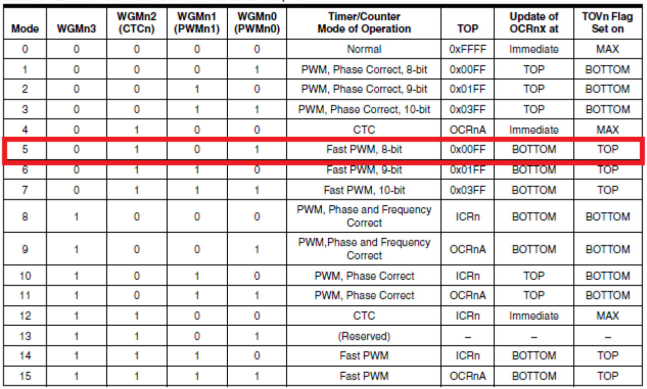
Table 17-4. Compare Output Mode, Fast PWM

COMnA1 COMnB1 COMnC1	COMnA0 COMnB0 COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected.
0	1	WGM13:0 = 14 or 15: Toggle OC1A on Compare Match, OC1B and OC1C disconnected (normal port operation). For all other WGM1 settings, normal port operation, OC1A/OC1B/OC1C disconnected.
1	0	Clear OCnA/OCnB/OCnC on compare match, set OCnA/OCnB/OCnC at BOTTOM (non-inverting mode).
1	1	Set OCnA/OCnB/OCnC on compare match, clear OCnA/OCnB/OCnC at BOTTOM (inverting mode).

Waveform Generation Bit

Waveform Generation Bit

Table 17-2. Waveform Generation Mode Bit Description[1]



Mode	WGMn3	WGMn2 (CTCn)	WGMn1 (PWMn1)	WGMn0 (PWMn0)	Timer/Counter Mode of Operation	TOP	Update of OCRnX at	TOVn Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCRnA	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICRn	BOTTOM	BOTTOM
9	1	0	0	1	PWM,Phase and Frequency Correct	OCRnA	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICRn	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCRnA	TOP	BOTTOM
12	1	1	0	0	CTC	ICRn	Immediate	MAX
13	1	1	0	1	(Reserved)	–	–	–
14	1	1	1	0	Fast PWM	ICRn	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCRnA	BOTTOM	TOP

TCCR5B- Timer Counter Control Register B

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Bit	Symbol	Description	Bit Value
7	ICNC5	Input Capture Noise Canceller	0
6	ICES5	Input Capture Edge Select	0
5	–	Reserved Bit	0
4	WGM53	Waveform Generation Mode bit 3	0
3	WGM52	Waveform Generation Mode bit 2	**1**
2	CS52	Clock Select	0
1	CS51	Clock Select	**1**
0	CS50	Clock Select	**1**

TCCR5B- Timer Counter Control Register B

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6	ICES5	Input Capture Edge Select	0
5	–	Reserved Bit	0
4	WGM53	Waveform Generation Mode bit 3	0
3	WGM52	Waveform Generation Mode bit 2	1
2	CS52	Clock Select	0
1	CS51	Clock Select	1
0	CS50	Clock Select	1

TCCR5B = 0x0B

Clock Select Bit

Clock Select Bit

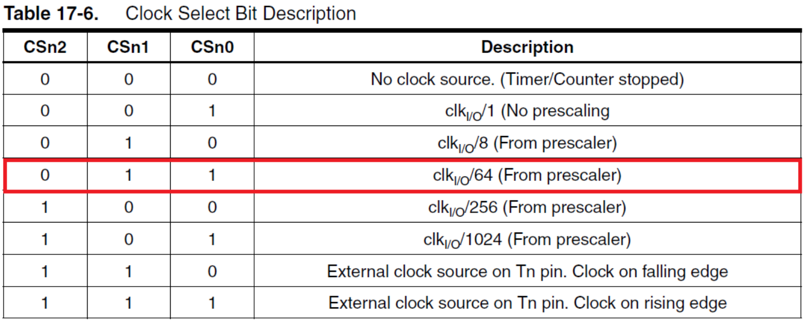

Table 17-6. Clock Select Bit Description

CSn2	CSn1	CSn0	Description
0	0	0	No clock source. (Timer/Counter stopped)
0	0	1	$clk_{I/O}$/1 (No prescaling
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on Tn pin. Clock on falling edge
1	1	1	External clock source on Tn pin. Clock on rising edge

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- Counts from 0 to 65535 if used in 16-Bit Mode

Output Compare Register 5

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- OCR5n is represented as two 8-bit register as OCR5nL and OCR5nH
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- OCR5AL (PortL3) is connected to Left Motor
- OCR5BL (PortL4) is connected to Right Motor

Output Compare Register 5 (Contd..)

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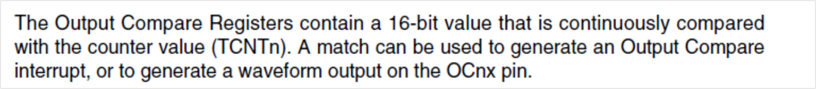
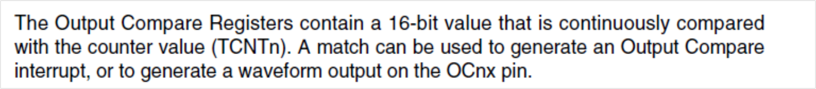


The Output Compare Registers contain a 16-bit value that is continuously compared with the counter value (TCNTn). A match can be used to generate an Output Compare interrupt, or to generate a waveform output on the OCnx pin.

Output Compare Register 5 (Contd..)



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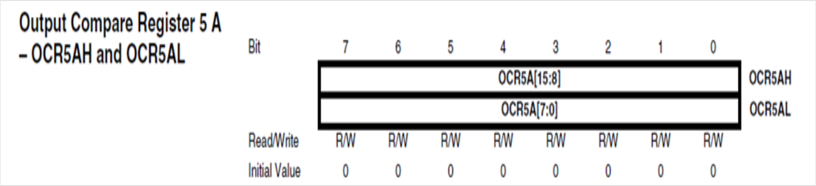

Output Compare Register 5 A – OCR5AH and OCR5AL

Bit	7	6	5	4	3	2	1	0	
	OCR5A[15:8]								OCR5AH
	OCR5A[7:0]								OCR5AL
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Block Diagram - Output Compare Unit

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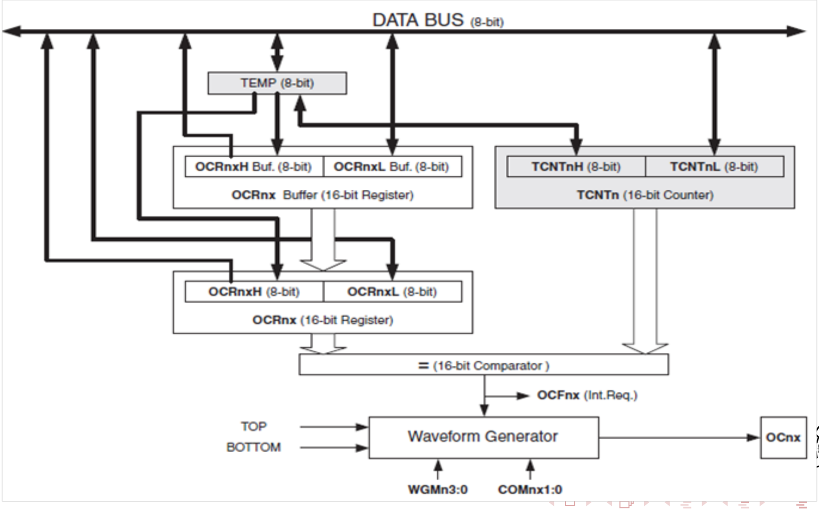

Timing Diagram Fast PWM

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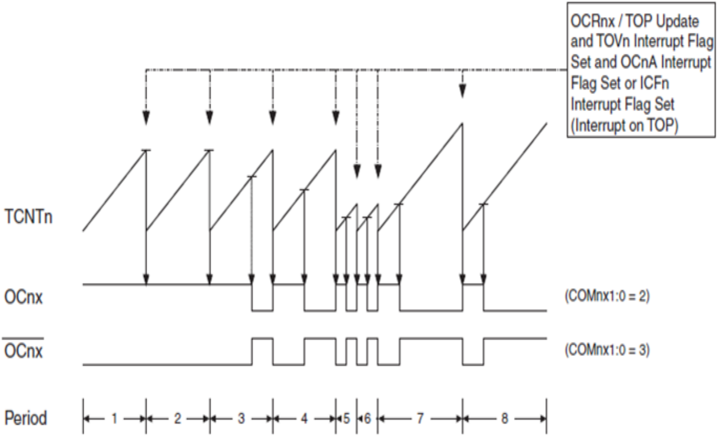
Figure 55. Fast PWM Mode, Timing Diagram


OCRnx / TOP Update and TOVn Interrupt Flag Set and OCnA Interrupt Flag Set or ICFn Interrupt Flag Set (Interrupt on TOP)
TCNTn
OCnx
(COMnx1:0 = 2)
$\overline{\text{OCnx}}$
(COMnx1:0 = 3)
Period
1
2
3
4
5
6
7
8

Syntax for C-Program

PWM Initialization

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Port Pin Config

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void motion_pin_config (void)  //Configure Pins as Output
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 Port A for motion control and Port L for Velocity Control must be defined Output

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PWM Initialization

```
void timer5_init()  //Set Register Values for starting Fast 8-bit PWM
{

   TCCR5A =
   TCCR5B =
   TCNT5H = 0xFF;
   TCNT5L = 0x00;
   OCR5AH = 0x00;
   OCR5AL = 0xFF;
   OCR5BH = 0x00;
   OCR5BL = 0xFF;
}
```

Syntax for C-Program

Program

Syntax for C-Program

Program

Main Program

Syntax for C-Program

Program

Main Program

```
int main(void)
{
  init_devices();
  forward();
  while(1)
  {
    velocity(100,100);
    _delay_ms(500);
    velocity(0,255);
    _delay_ms(500);
  }
}
```

Syntax for C-Program

Program

Main Program

```
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  init_devices();
  forward();
  while(1)
  {
    velocity(100,100);
    _delay_ms(500);
    velocity(0,255);
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Velocity Function

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```

Velocity Function

```
void velocity (unsigned char left_motor, unsigned char right_motor)
{

   OCR5AL = (unsigned char)left_motor;
   OCR5BL = (unsigned char)right_motor;
}
```

Thank You!

Post your queries on: http://qa.e-yantra.org/