

Quartus II 32-bit - D:/quartus/13.1/quartus/bin/cme1214hw1 - cme1214hw1

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity

Cyclone III: EP3C16F484C5

cme1214hw1

Compilation Report - cme1214hw1

C:/Users/kerem/Desktop/cme1214hw1.bdf

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis 00:00
- Filter (Place & Route) 00:00
- Assembler (Generate programming files) 00:00
- TimeQuest Timing Analysis 00:00
- EDA Netlist Writer 00:00
- Program Device (Open Programmer)

Messages

type ID Message

- 332102 Design is not fully constrained for hold requirements
- Quartus II 32-bit TimeQuest Timing Analyzer was successful. 0 errors, 5 warnings
- Running Quartus II 32-bit EDA Netlist Writer
- Command: quartus_eda --read_settings_files=off --write_settings_files=off cme1214hw1 -c cme1214hw1
- 204019 Generated file cme1214hw1.vo in folder "D:/quartus/13.1/quartus/bin/simulation/qsim/" for EDA simulation tool

System (6) Processing (119)

263,437 100% 00:00:19

ENG 21:10

TRQ 26.03.2023

The screenshot displays the Quartus II 32-bit IDE. The main window shows a logic circuit diagram with three inputs: A, B, and C. Input A is connected to the top input of an OR2 gate (inst2). Input B is connected to the bottom input of the OR2 gate. Input C is connected to the top input of an AND2 gate (ins1). The output of the OR2 gate is connected to the input of a NOT gate (inst3). The output of the NOT gate is connected to the bottom input of the AND2 gate. The output of the AND2 gate is connected to the output pin OUTPUT1, which is labeled 'Fina'. The Project Navigator on the left shows the project 'cme1214hw1' under the entity 'Cyclone III: EP3C16F484C5'. The Messages window at the bottom shows compilation messages, including a warning about hold requirements and successful completion of the EDA Netlist Writer.





