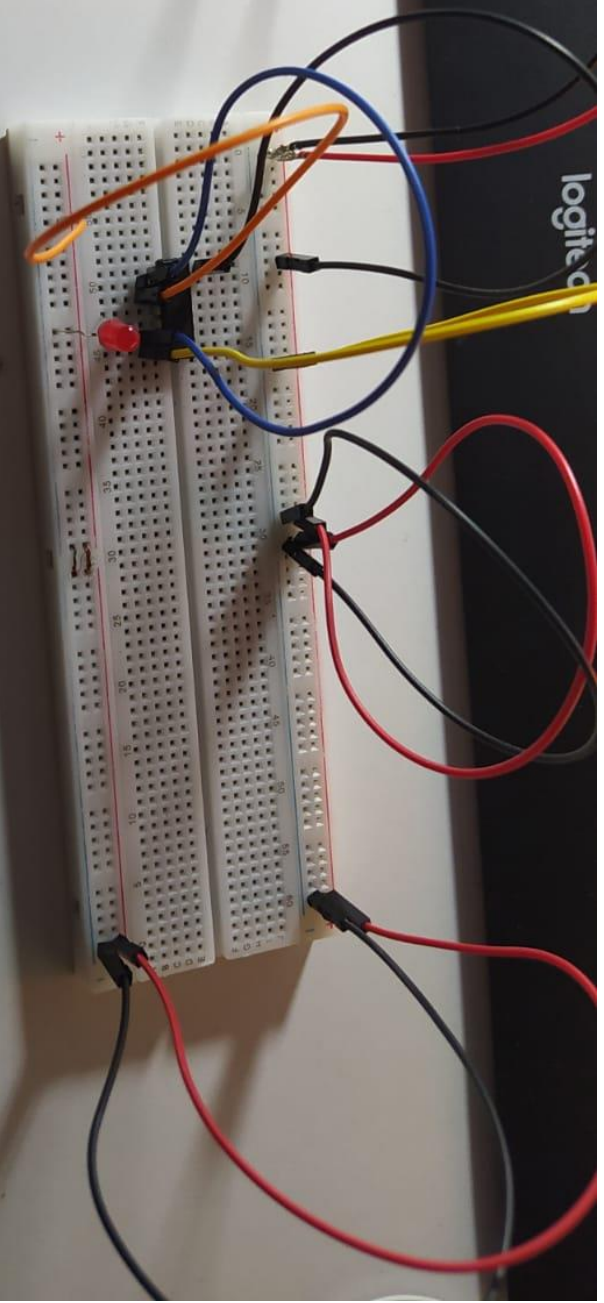


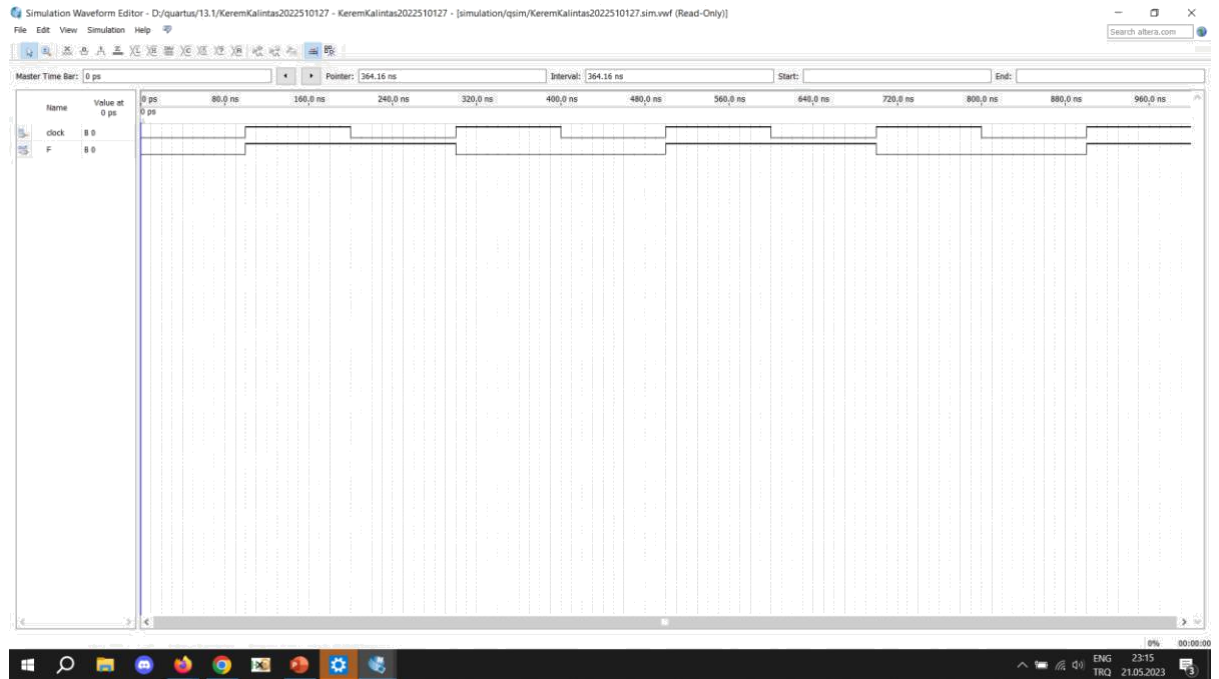
CME1214 Logic Design Homework 4

Divide-by-2 using a D Flip Flop

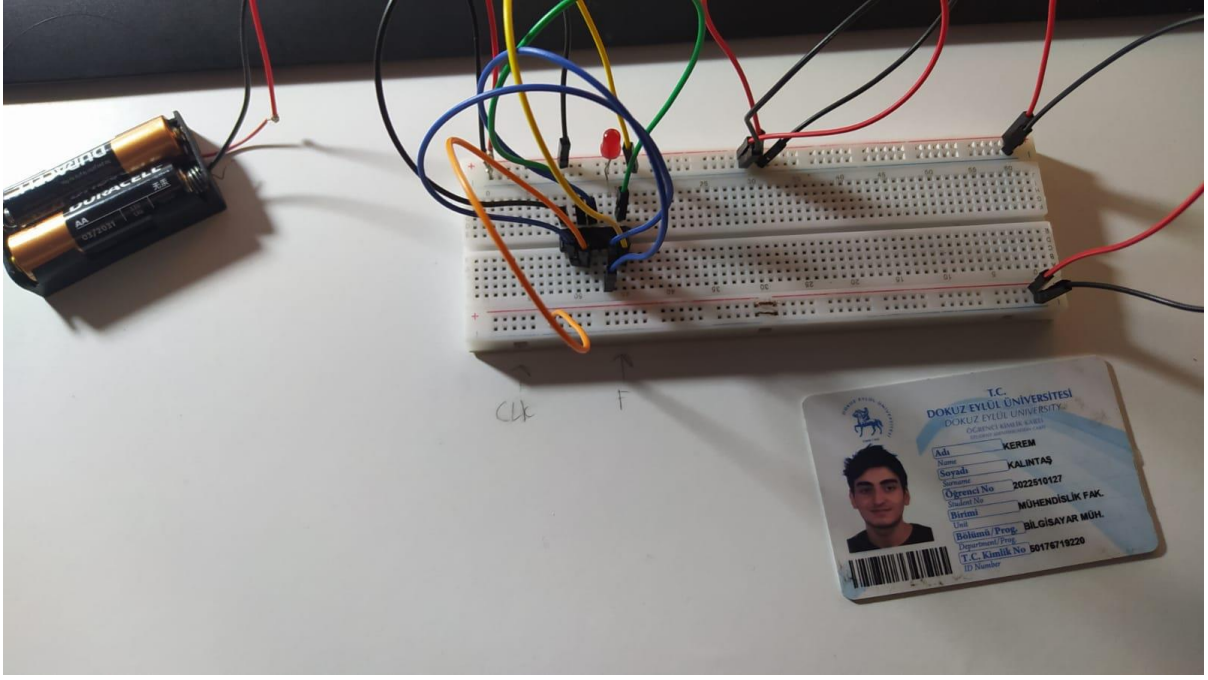


CLK
F





Divide-by-4 using D flip flops





4K

T



Quartus II 64-Bit - D:/quartus/13.1/KeremKalintas2022510127 - KeremKalintas2022510127

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity

Cyclone III: EP3C10K10A066

KeremKalintas2022510127

7474:inst

Tasks

Flow: Compilation

Task

Compile Design 00:00

Analyze & Synthesis 00:00

Fitter (Place & Route) 00:00

Assembler (Generate programming file) 00:00

TimeQuest Timing Analysis 00:00

EDA Netlist Writer 00:00

Program Device (Open Programmer)

Compilation Report - KeremKalintas2022510127

clock INPUT VCC

7474

1PRN 1Q

1D 1Q

1CLK 1Q

2PRN 2Q

2D 2Q

2CLK 2Q

inst D FLIP-FLOP

OUTPUT F

Messages

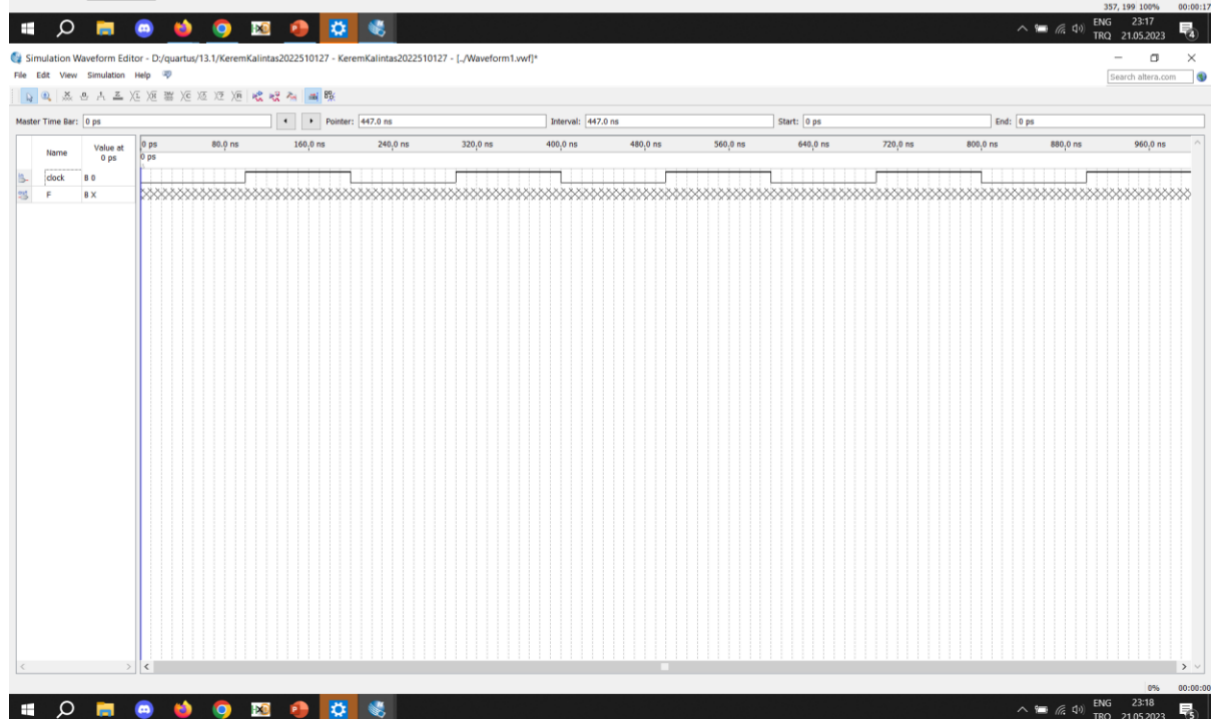
Type ID Message

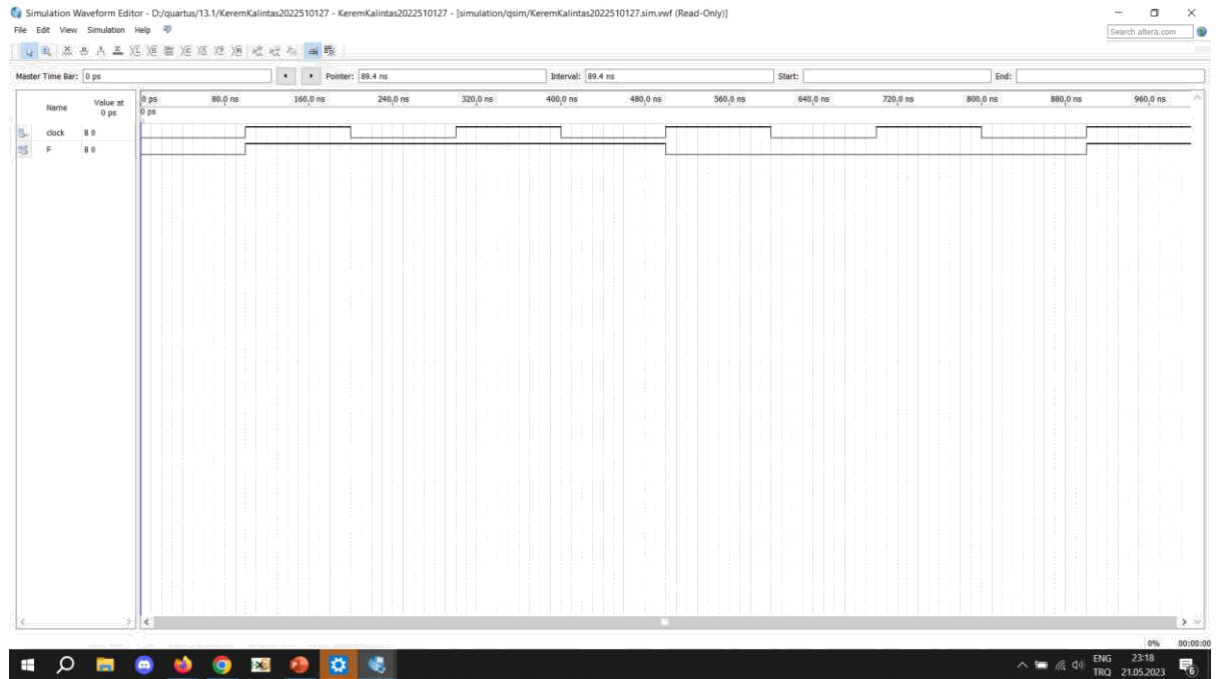
204019 Generated file KeremKalintas2022510127.vo in folder "D:/quartus/13.1/simulation/qsim/" for EDA simulation tool

Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings

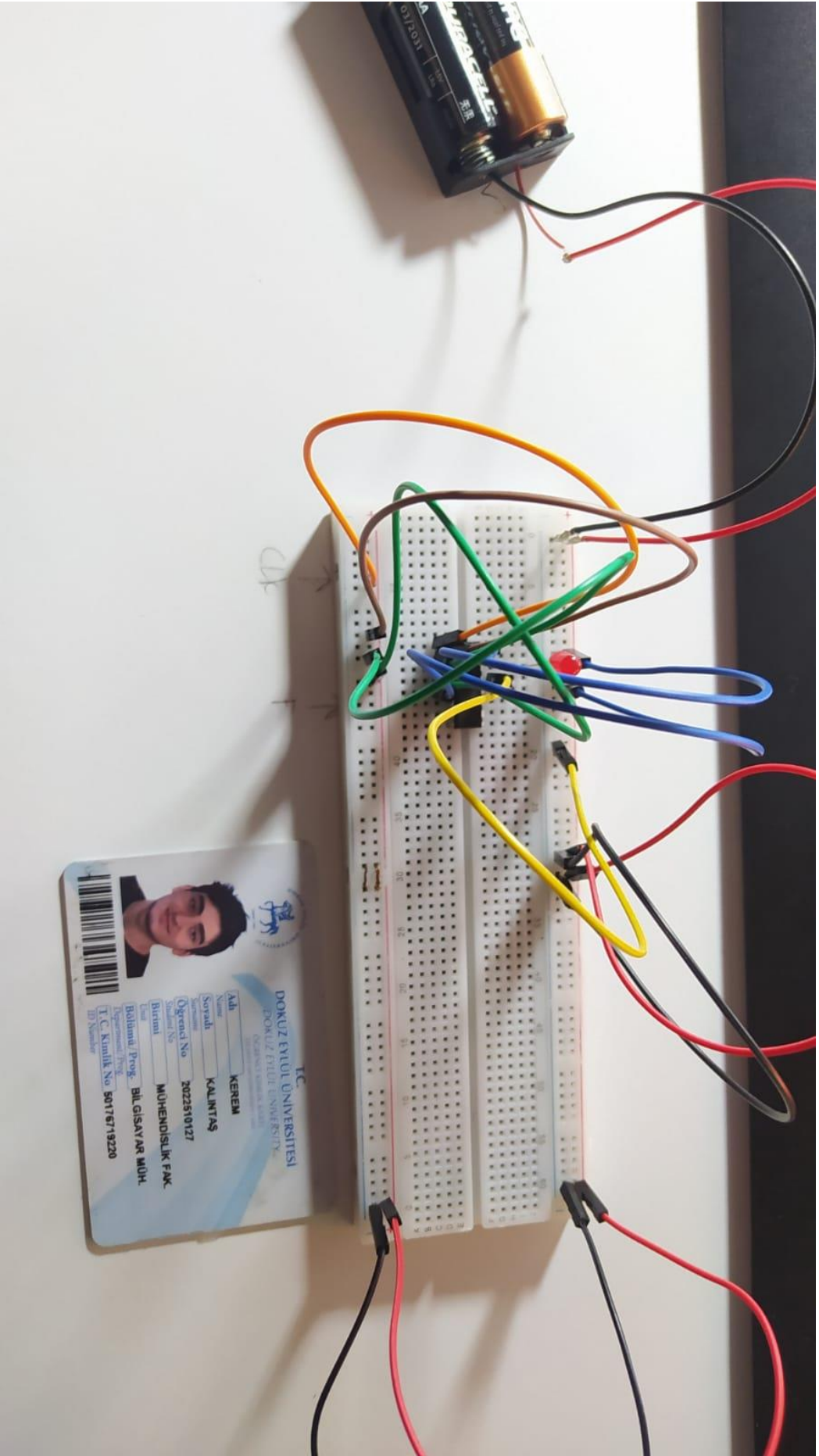
293000 Quartus II Full Compilation was successful. 0 errors, 11 warnings

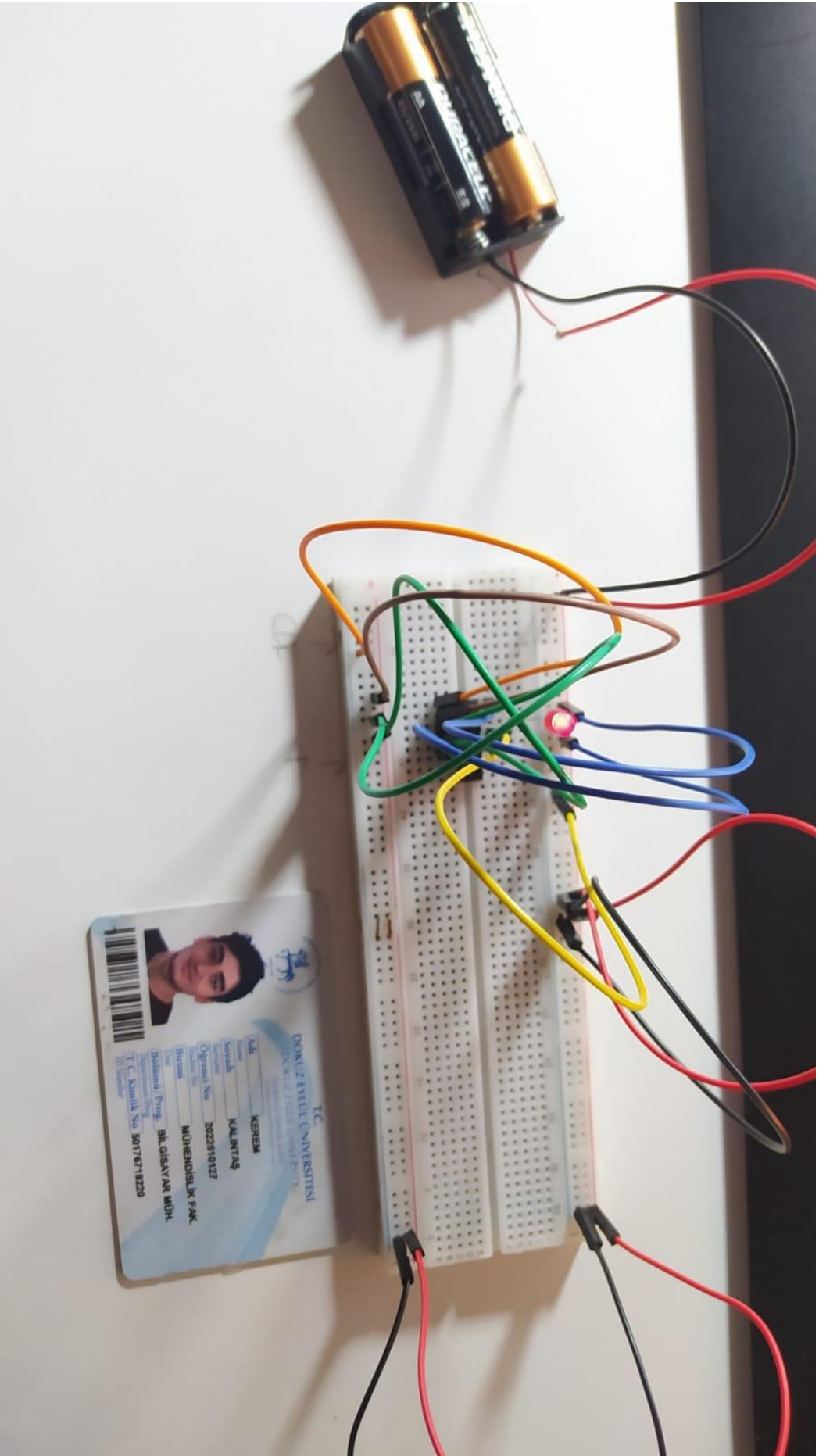
System (2) Processing (111)

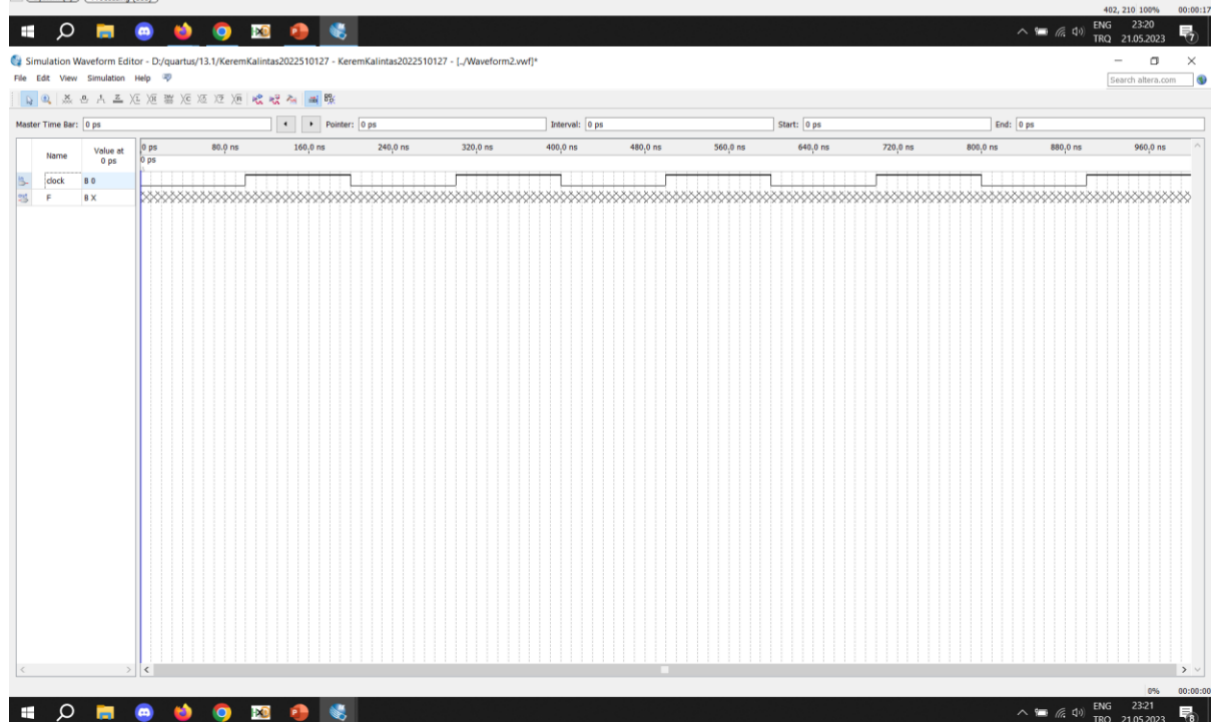
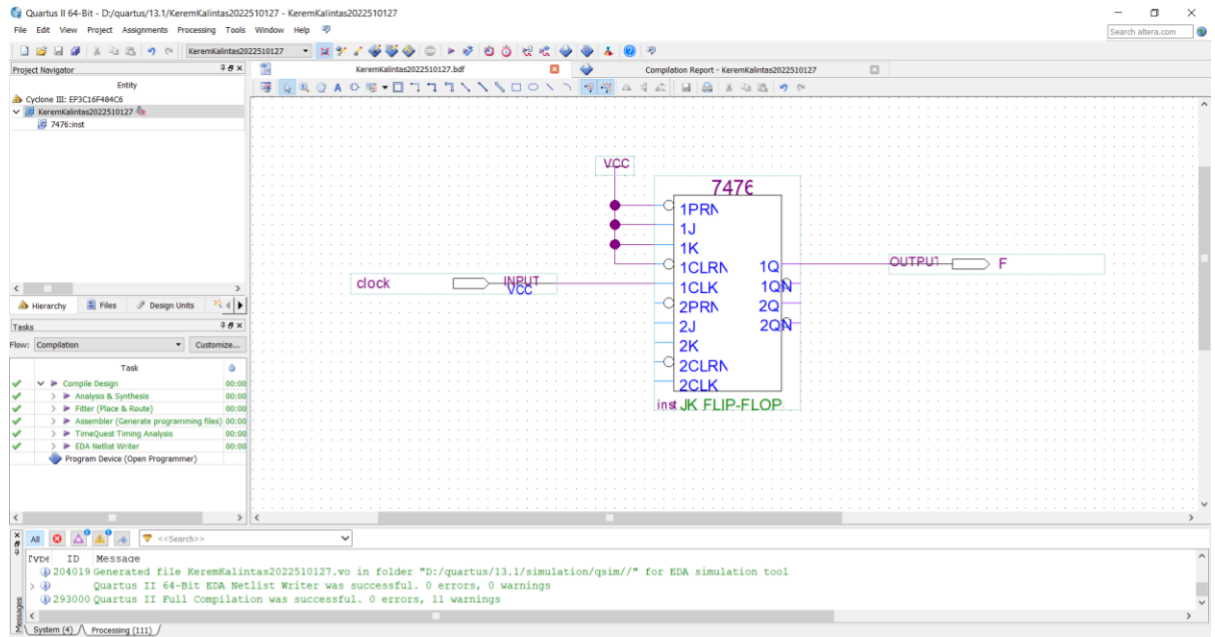


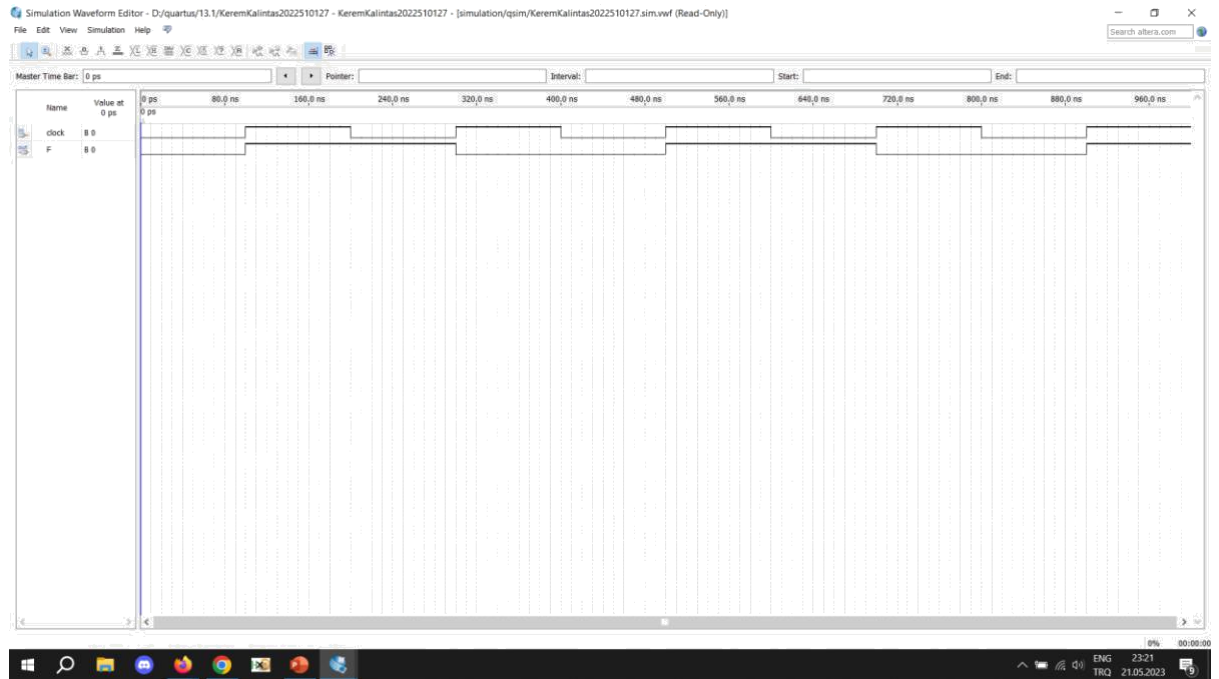


Divide-by-2 using a JK Flip Flop

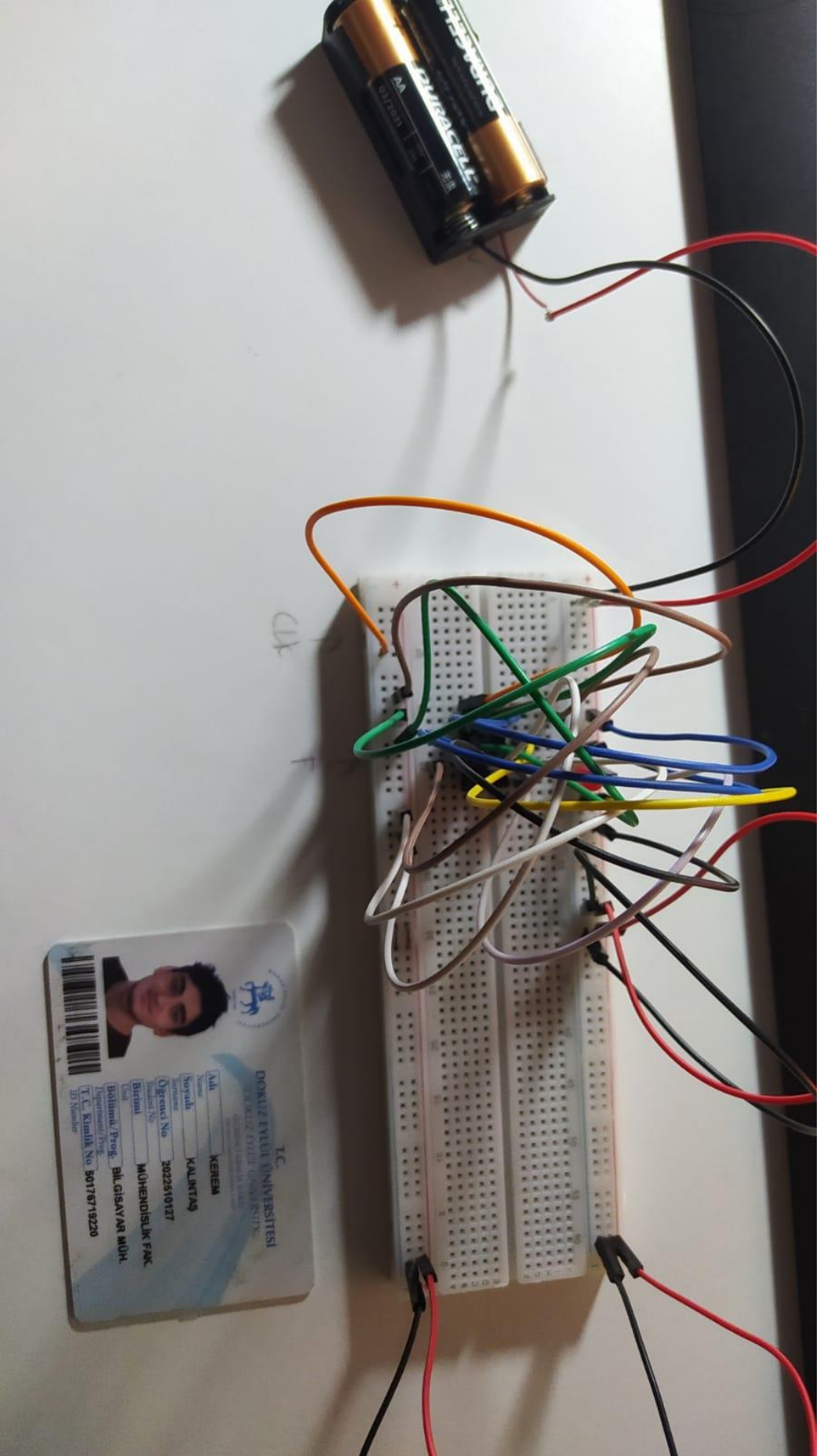








Divide-by-4 using JK Flip Flops





CH

L



