

# CME1214 Logic Design Homework 2

## Experiment 1

$F(w, x, y, z) = \sum (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$

w	x	y	z	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Karnaugh Map

w\y	00	01	11	10
00	1	1	0	1
01	1	1	0	1
11	1	1	0	1
10	1	1	0	0

$$F = \overline{w}x\overline{y} + \overline{w}y\overline{x} + w\overline{x}\overline{y} + w\overline{x}y + \overline{w}\overline{z}y + x\overline{y}z$$

$$= \overline{y}(\overline{w}x + \overline{w}x + wx + wx) + z(\overline{w} + x)$$

$$= \overline{y} + z(\overline{w} + x)$$

NOT OR AND

Quartus II 64-Bit - D:/quartus/2022510127KeremKalintas/hw2/hw2

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity

Cyclone III: EP3C10F484C6

hw2

Tasks

Flow: Compilation

Task

Compile Design 00:00

Analyze & Synthesis 00:00

Fitter (Place & Route) 00:00

Assembler (Generate programming files) 00:00

TimeQuest Timing Analysis 00:00

EDA Netlist Writer 00:00

Program Device (Open Programmer)

Messages

Type ID Message

204019 Generated file hw2\_6\_1200mv\_85c\_vhd\_slow.sdo in folder "D:/quartus/2022510127KeremKalintas/hw2/simulation/modelsim/" for EDA simulation tool

204019 Generated file hw2\_6\_1200mv\_0c\_vhd\_slow.sdo in folder "D:/quartus/2022510127KeremKalintas/hw2/simulation/modelsim/" for EDA simulation tool

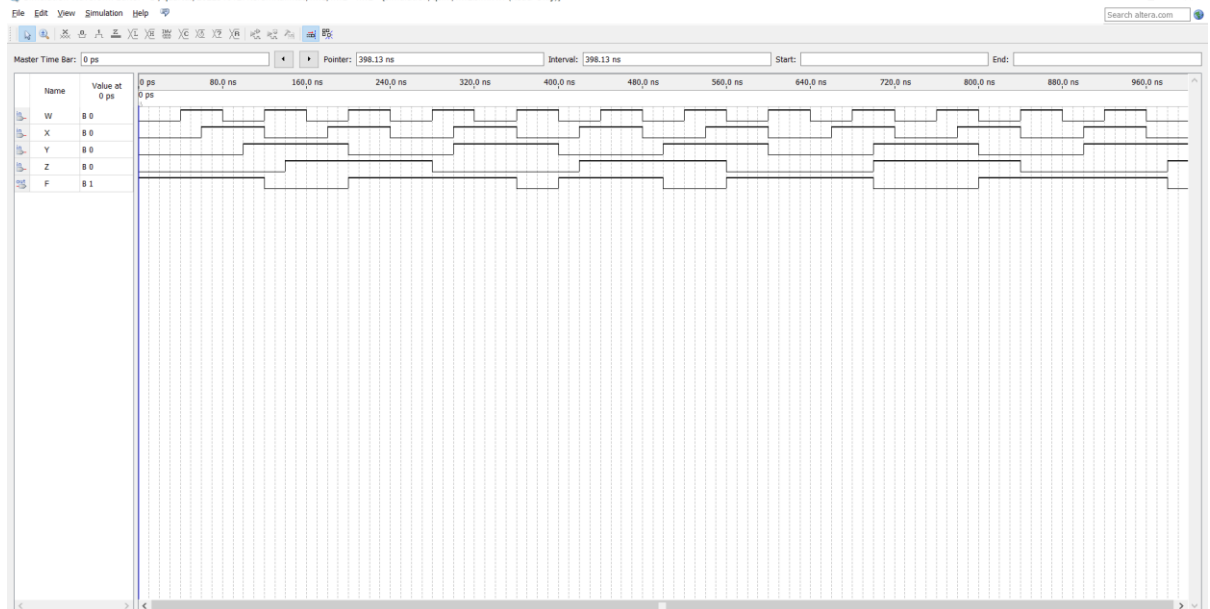
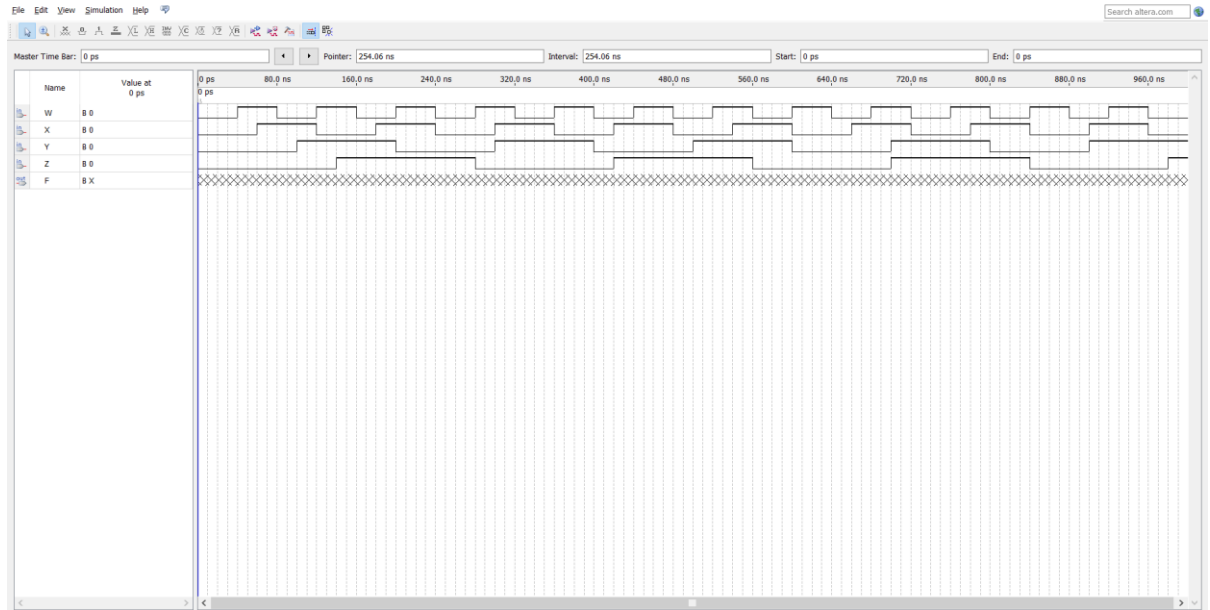
204019 Generated file hw2\_min\_1200mv\_0c\_vhd\_fast.sdo in folder "D:/quartus/2022510127KeremKalintas/hw2/simulation/modelsim/" for EDA simulation tool

204019 Generated file hw2\_vhd.sdo in folder "D:/quartus/2022510127KeremKalintas/hw2/simulation/modelsim/" for EDA simulation tool

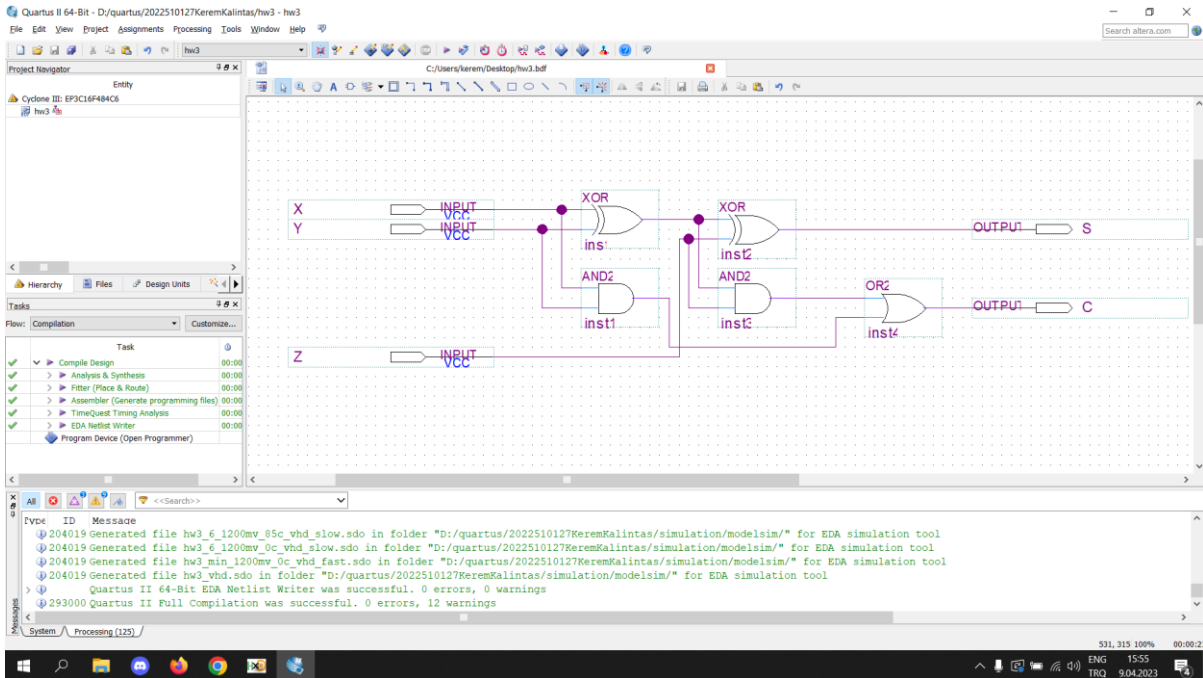
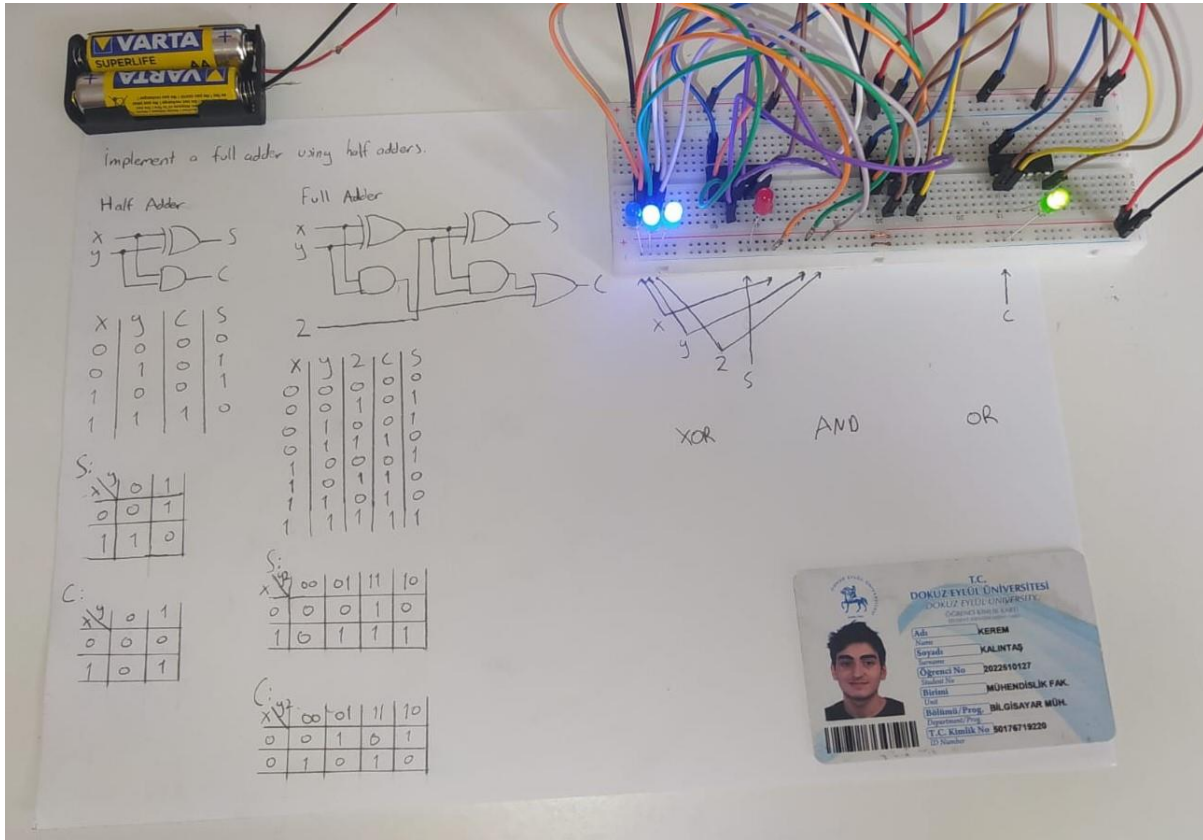
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings

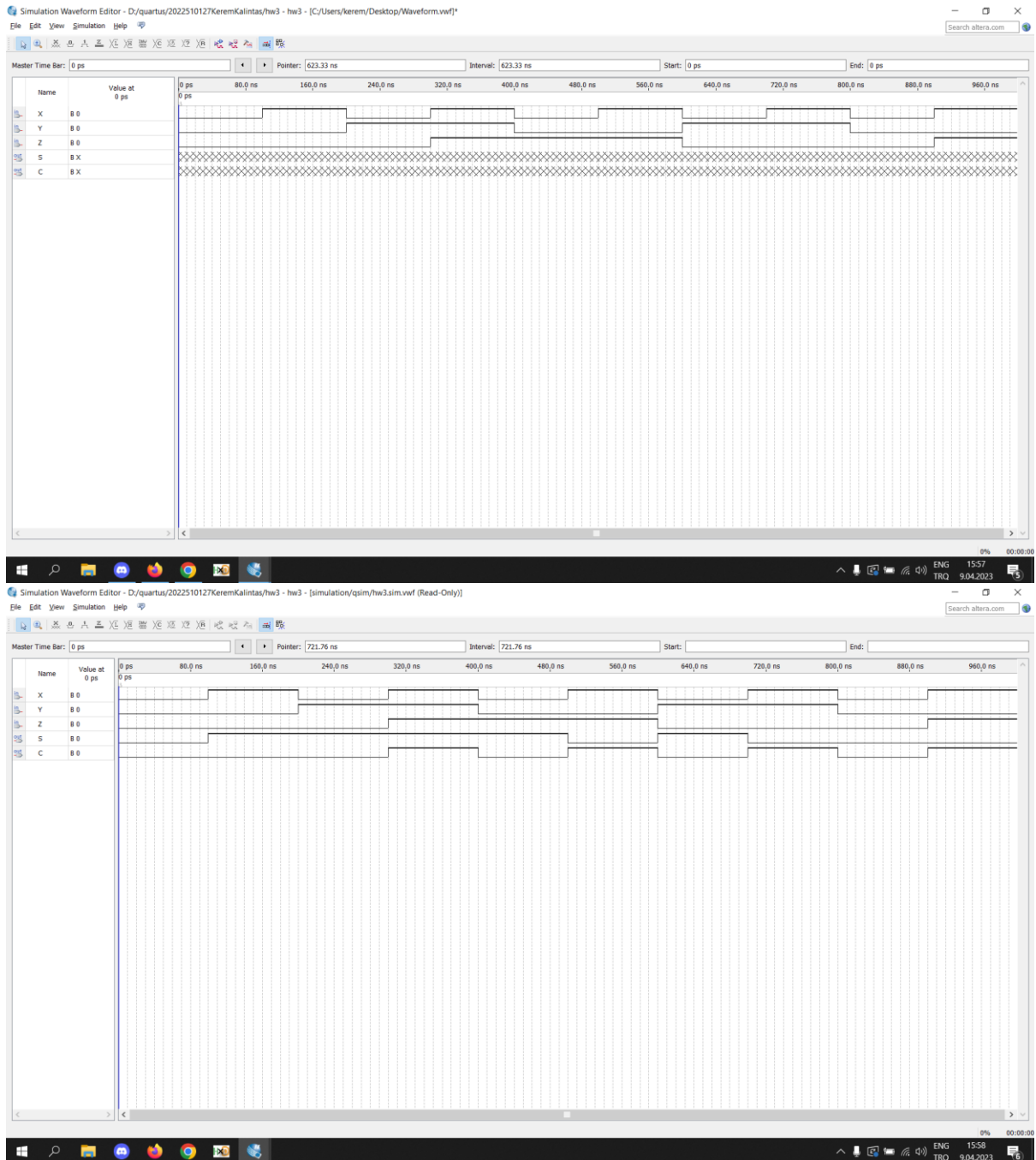
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings

System Processing (125)



## Experiment 2





Kerem Kalintas 2022510127