CME 1214 Logic Design
Experiment 5

3-bit Synchronous Counter

a. Preliminary Work

Draw state diagram, state table, Karnaugh maps and diagrams of the design. Construct and test the designed circuits in MaxPlus II.

b. Equipments

- JK Flip Flops (74LS73 or 74LS76) and other necessary ICs such as Inverter, OR, AND
- Breadboard
- Connection cables

c. Experiment

Design a 3-bit synchronous counter using logic gates and JK flip flops. The circuit should output your number without repetition in MOD 8. For example, for a student number 1900510082 the circuit should output 1,0,5,2 in succession. (MOD 8 produces 1,1,0,0,5,1,0,0,0,2 and without repetition it counts 1,0,5,2)