CME1214 Logic Design
Experiment 2

Preliminary Work

1. Examine function F and
   a. Draw the truth table of F and then simplify F using Karnaugh map.
   b. Use Quartus to implement logic design of F.
   c. Simulate your circuit and verify that it works correctly using the waveform.

$$F(w, x, y, z) = \sum(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$$

2. Design a **half adder** circuit using logic gates and then design **2-bits full adder** using half adder circuit(s).
   - Give the truth tables and Karnaugh maps of the designs.
   - Use Quartus to implement your designs.
   - Simulate your circuits and verify that they work correctly using the waveform.

Equipments

- AND (IC 7408), OR (IC 7432), NOT (IC 7414), XOR (IC 7486)
- Breadboard
- Connection cables
- Any other equipments necessary for the experiments.

Lab Work

1. Simplify the Boolean function F and implement it by using integrated circuits(IC).
2. Implement half adder and 2-bits full adder circuits by using ICs.

The preliminary work and report are expected from each student.
See the Instructions at the end of the document.

Instructions:

- You should only *one* "**pdf**" file that contains both **your prelab screenshots** and **photos of experiments**.
- **The file path of your screenshots** should be **visible**, otherwise your work won't get any point.
- **Your student card** should in **the photos of the experiments**, otherwise your work won't get any point.

Your "pdf" file name should be "studentNo_name_surname.pdf"