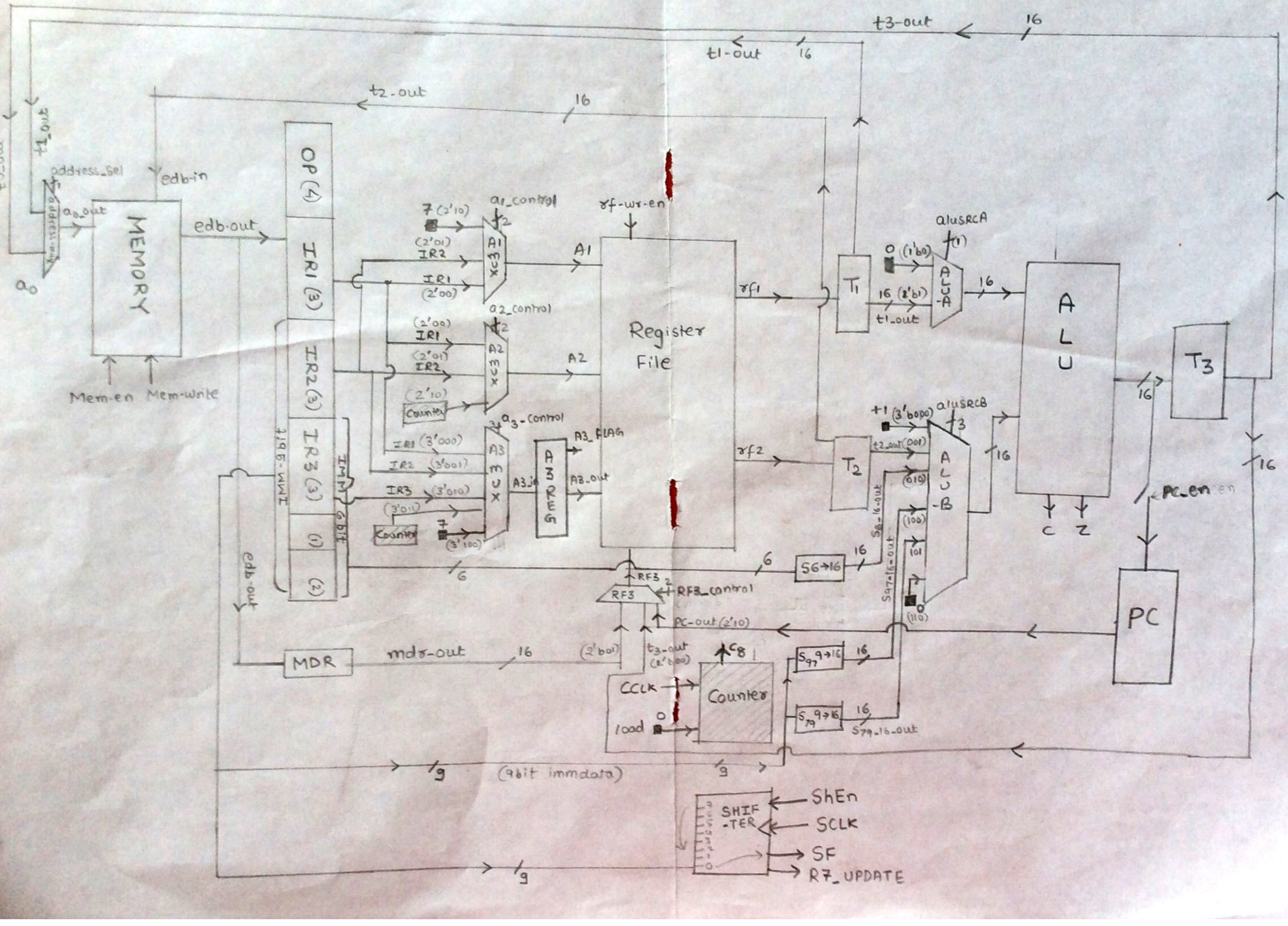

MEMORY
edb-out
edb-in
address_sel
a_0
Mem-en
Mem-write
t2-out
t1-out
t3-out
OP (4)
IR1 (3)
IR2 (3)
IR3 (3)
IMM 6bit
IMM-9bit
MDR
mdr-out
a1_control
a2_control
a3_control
A1
A2
A3
A3_FLAG
A3_out
Counter
Register File
rf-wr-en
rf1
rf2
RF3
RF3_control
PC-out
T1
T2
T3
alusRCA
alusRCB
ALU
C
Z
PC
PC_en
S6→16
Counter
CCLK
load
SHIFTER
ShEn
SCLK
SF
R7_UPDATE
(9bit immdata)

IITB – RISC
EE 309
Datapath Description

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1. **Memory:**
   We have 32 memory locations of 16 bit each, i.e. memory is 64 Bytes. If reset all the memory locations are cleared. Asynchronous read and synchronous write memory is implemented.

2. **ALU:**
   Arithmetic and logical unit which has two inputs as the output of two muxes ALU-A and ALU-B. It performs 3 operations i.e., NAND, AND, Compare. {Compare is used only for Beq instruction.}. ALU Outputs a 16-bit result according to the operation it performs on the two operands, it sets/clears Carry and Zero flag according to the instruction. On reset, all the outputs are cleared. The operation to be performed (add, nand or compare) will be determined by the Op_code of the instruction. Additional signals are provided to control updating of the zero flag and carry flags.

3. **Register File:**
   Register file contains 8 registers (R7-R0) of 16 bits each. It has three Address inputs (A1, A2, A3) out of which A1, A2 correspond to addresses from where we need to read our data, and the corresponding values are read through RF1, Rf2. A3 corresponds to address of the register where we need to write the data given through RF3-mux. We have a Rf-write-En bit which if 1 enables writing to the register and reads from the register when 0. It's synchronous write and asynchronous read.

4. **IR register:**
   16 bit instruction is stored in the Instruction Register. The first bits (MSB) corresponds to Op_code. The next three bits corresponds to IR1. Next three to them corresponds to IR2 and the next bits corresponds to IR3 and last 2 bits shows carry flag and zero flag respectively.

5. **Counter:**
   A 3-bit Upcounter is implemented for the execution of LM and SM instructions. It uses a special signal called cclk (counter clock) which is generated only in the states where counter is to be increased. Load resets the counter to zero.

6. **Shifter:**
   Shifter has two inputs a 9-bit input from instruction register and a Shifter enable flag (which if set allows shifting). The shifter output 1 MSB bit at every positive edge of the sclk (shifter clock) which is generated only on the states where shifting is required (for LM and SM instructions). It aslo generates a flag whether to update R7 or not.

7. **Temporary Registers:**
    1) **T1:** It stores the data that is read through RF1 synchronously.
    2) **T2:** It stores the data that is read through RF2 synchronously.
    3) **T3:** It stores the output of ALU synchronously.
    4) **Mdr :** It stores data coming out of memory synchronously
    5) **A3 register:** It stores the address of destination address of register file and checks whether the address is pointing R7 and generates flag accordingly.

8. **PC (register):**
   It stores updated PC values if PC_en flag is set. it is implemented in coherence with R7 register so as to avoid conflicts causing due to use of R7 as a destination register in some of the cases. It stores value of R7 +1 synchronously when pc_en is high. If R7 is not updated during execution of instruction then pc writes back that R7+1 to R7.

9. **Sign Extender:**
    1) **S6->16:** It takes 6 bits imm. data from IR and pads it with zeroes in MSB to make the output 16 bits.
    2) **S_{97}9->16:** It takes 9 bits imm. data from IR and shifts them to MSB. It then pads it with zeroes in LSB to make the output 16 bits.
    3) **S_{79}9->16:** It takes 7 bits imm. data from IR and shifts them to MSB. It then pads it with zeroes in LSB to make the output 16 bits.

10. **Multiplexers:**
    1) **ALU-A:** It has 2 inputs of 16 bits each (i.e. t1_out and 0) and a 2 bits control signal decides the output.
    2) **ALU-B:** It has 6 inputs of 3 bits each (i.e 1, t2_out, s6_16, s97_16, s79_16) and a 3 bits control signal decides the output.
    3) **RF3-mux:** It has 3 inputs of 16 bits each (i.e. t3_out, pc_out, mdr_out) and a 2 bits control signal decides the output.
    4) **Address-mux:** It has 2 inputs of 16 bits each (i.e. t1_out, t3_out) and a 1 bit control signal decides the a0 out.
    5) **A1-mux:** It has 3 inputs of 3 bits each (i.e., IR1, IR2, 7) and 2-bit control signal decides the output.
    6) **A2-mux:** It has 3 inputs of 3 bits each (i.e. IR1, IR2, Counter_Out) and 2-bit control signal decides the output.
    7) **A3-mux:** It has 5 inputs of 3 bits each (i.e. IR1, IR2, IR3, Counter_Out, 7) and a 3-bit control signal decides the output.