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1  -----
2  -- Entity:          hextosevenseg
3  -- Written By:      Kevin Brenneman Richard Lucas
4  -- Date Created:    8/27/15
5  -- Description:     converts hexadecimal to seven segment display
6  --
7  -- Revision History (date, initials, description): 9/3/15, KB RL, Initial Build
8  --
9  -- Dependencies:
10 --     none
11 -----
12 library IEEE;
13 use IEEE.STD_LOGIC_1164.ALL;
14
15 -- Uncomment the following library declaration if using
16 -- arithmetic functions with Signed or Unsigned values
17 --use IEEE.NUMERIC_STD.ALL;
18
19 -- Uncomment the following library declaration if instantiating
20 -- any Xilinx primitives in this code.
21 --library UNISIM;
22 --use UNISIM.VComponents.all;
23
24 entity hextosevenseg is
25     Port ( Hex          : in  STD_LOGIC_VECTOR(3 downto 0);
26           Segment      : out STD_LOGIC_VECTOR(0 to 6));
27
28 end hextosevenseg;
29
30 architecture Behavioral of hextosevenseg is
31
32 begin
33
34     Segment <= "0000001" when (Hex = "0000") else -- 0
35               "1001111" when (Hex = "0001") else -- 1
36               "0010010" when (Hex = "0010") else -- 2
37               "0000110" when (Hex = "0011") else -- 3
38               "1001100" when (Hex = "0100") else -- 4
39               "0100100" when (Hex = "0101") else -- 5
40               "0100000" when (Hex = "0110") else -- 6
41               "0001111" when (Hex = "0111") else -- 7
42               "0000000" when (Hex = "1000") else -- 8
43               "0000100" when (Hex = "1001") else -- 9
44               "0001000" when (Hex = "1010") else -- A
45               "1100000" when (Hex = "1011") else -- B
46               "0110001" when (Hex = "1100") else -- C
47               "1000010" when (Hex = "1101") else -- D
48               "0110000" when (Hex = "1110") else -- E
49               "0111000" when (Hex = "1111") else -- F
50               "0000001";
51
52 end Behavioral;
53
54
```