```
1   ----------------------------------------------------------------------------
2   -- Entity:        4 to 1 mux
3   -- Written By:    Kevin Brenneman Richard Lucas
4   -- Date Created:  8/27/15
5   -- Description:   4 to 1 mux with 4 bits out
6   --
7   -- Revision History (date, initials, description): 9/2/15, KB RL, Initial Build
8   --
9   -- Dependencies:
10  --    none
11  ----------------------------------------------------------------------------
12  library IEEE;
13  use IEEE.STD_LOGIC_1164.ALL;
14
15  -- Uncomment the following library declaration if using
16  -- arithmetic functions with Signed or Unsigned values
17  --use IEEE.NUMERIC_STD.ALL;
18
19  -- Uncomment the following library declaration if instantiating
20  -- any Xilinx primitives in this code.
21  --library UNISIM;
22  --use UNISIM.VComponents.all;
23
24  entity mux4to1 is
25     Port ( x0      : in  STD_LOGIC_VECTOR(3 downto 0);
26            x1      : in  STD_LOGIC_VECTOR(3 downto 0);
27            x2      : in  STD_LOGIC_VECTOR(3 downto 0);
28            x3      : in  STD_LOGIC_VECTOR(3 downto 0);
29            sel     : in  STD_LOGIC_VECTOR(1 downto 0);
30            y : out STD_LOGIC_VECTOR(3 downto 0));
31  end mux4to1;
32
33  architecture Structural of mux4to1 is
34
35  begin
36
37  with sel select
38     y   <= x0 when "00",
39            x1 when "01",
40            x2 when "10",
41            x3 when "11",
42            x0 when others;
43
44
45  end Structural;
46
47
```