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1   ----------------------------------------------------------------------------
2   -- Entity:        lab02 top level
3   -- Written By:    Kevin Brenneman Richard Lucas
4   -- Date Created:  8/27/15
5   -- Description:   top level to combine lab 1 with a 7 segment display
6   --
7   -- Revision History (date, initials, description): 9/2/15, KB RL, Initial Build
8   --
9   -- Dependencies:
10  --    mux.vhd
11  --    FullAdder.vhd
12  --    rippe_carry_adder.vhd
13  --    adderSubtractor_4bit.vhd
14  --    hextosevseg.vhd
15  ----------------------------------------------------------------------------
16  library IEEE;
17  use IEEE.STD_LOGIC_1164.ALL;
18
19  entity lab02_kjb5568_rjl5336 is
20      Port ( BTNU      : in  STD_LOGIC;
21             BTNC      : in  STD_LOGIC;
22             BTND      : in  STD_LOGIC;
23             SWITCH    : in  STD_LOGIC_VECTOR(7 downto 0);
24             ANODE     : out STD_LOGIC_VECTOR(7 downto 0);
25             SEGMENT   : out STD_LOGIC_VECTOR(0   to   6);
26             LED       : out STD_LOGIC_VECTOR(4 downto 0));
27  end lab02_kjb5568_rjl5336;
28
29  architecture Behavioral of lab02_kjb5568_rjl5336 is
30
31  component mux4to1 is
32      Port( x0       : in  STD_LOGIC_VECTOR(3 downto 0);
33            x1       : in  STD_LOGIC_VECTOR(3 downto 0);
34            x2       : in  STD_LOGIC_VECTOR(3 downto 0);
35            x3       : in  STD_LOGIC_VECTOR(3 downto 0);
36            sel      : in  STD_LOGIC_VECTOR(1 downto 0);
37            y        : out STD_LOGIC_VECTOR(3 downto 0));
38  end component;
39
40  component hextosevenseg is
41      Port( Hex      : in  STD_LOGIC_VECTOR(3 downto 0);
42            Segment  : out STD_LOGIC_VECTOR(0   to   6));
43  end component;
44
45  Component addersubtractor_4bit is
46     Port(   A        : in  STD_LOGIC_VECTOR (3 downto 0);
47             B        : in  STD_LOGIC_VECTOR (3 downto 0);
48             SUBTRACT : in  STD_LOGIC;
49             OVERFLOW : out STD_LOGIC;
50             SUM      : out STD_LOGIC_VECTOR (3 downto 0));
51  end component;
52
53  --internal signals
54  signal SEL         : STD_LOGIC_VECTOR (1 downto 0);
55  signal mux_out     : STD_LOGIC_VECTOR (3 downto 0);
56  signal sum_int       : STD_LOGIC_VECTOR (3 downto 0);
57  signal overflow    : STD_LOGIC;
```

```
58  begin
59
60
61  --implementation of lab 1 (4bit adder/subtractor)
62  addersubtractor: addersubtractor_4bit port map (
63        A => switch ( 7 downto 4),
64        B => switch ( 3 downto 0),
65        Subtract => BTND,
66        Overflow => overflow,
67        sum => sum_int);
68
69
70  --implementation of hex to seven seg
71  hexto7: hextosevenseg port map (
72        hex => mux_out,
73        segment => segment);
74
75  --implementation of the 4:1 mux
76  MUX:    mux4to1 port map (
77        x0 => sum_int,
78        x1 => sum_int,
79        x2 => switch(7 downto 4),
80        x3 => switch(3 downto 0),
81        sel => sel,
82        y => mux_out);
83
84  --logic for sel signal (2 bits)
85  sel <= "10" when (BTNC = '1') else
86         "11" when (BTNU = '1') else
87         "00";
88
89  Anode <="11111110";
90  LED (3 downto 0) <= sum_int;
91  LED(4) <= overflow;
92  end Behavioral;
93
94
```