DESIGN OF SINGLE STAGE DIFFERENTIAL AMPLIFIER

The domain of the Project:

Analog Mixed signal Design

Under the guidance of:

Mr.Karnati Prudhvi Kumar(Silicon Design Engineer 2)

By

Mr. Gara Kalyan(B.Tech ECE 4th Year Pursuing)

Period of the project

November 2024 to July 2025

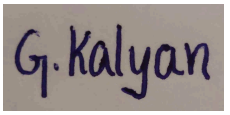
SURE TRUST

PUTTAPARTHI, ANDHRA PRADESH

Declaration

The project titled "**Design of Single Stage Differential Amplifier**" has been mentored by **Mr.Karnati Prudhvi Kumar**, organised by SURE Trust, from November 2024 to July 2025. This initiative aims to benefit educated unemployed rural youth by providing hands-on experience in industry-relevant projects, thereby enhancing employability.

I,**Mr.Gara Kalyan**, hereby declare that I have solely worked on this project under the guidance of my mentor. This project has significantly enhanced my practical knowledge and skills in the domain.

Name	**Signature**
Mr.Gara Kalyan	

Mentor	**Signature**
Mr.Karnati Prudhvi Kumar	
Silicon Design Engineer 2	

Seal & Signature

Prof.Radhakumari

Executive Director & Founder

SURE Trust

Table of Contents

Executive Summary

In this project, I designed a single-stage differential amplifier using Cadence Virtuoso. The goal was to get a voltage gain of 40 dB and a bandwidth of 5 MHz. I made sure the amplifier worked well for input signals between 0.8 V and 1.6 V, which is the input common-mode range. This range is important to ensure the amplifier works properly without distortion.

To check the design, I first did a DC operating point analysis. This helped me make sure all the transistors were working in the right region. Then, I ran an AC analysis to confirm the gain and frequency response matched the target values. I also did a transient analysis to see how the amplifier behaves over time with changing input signals.

The results showed that the amplifier worked as expected and met all the required values. This project gave me a better understanding of analog circuit design and how to use Cadence tools for real-time simulations.

Introduction

Background and Context:

Analog signal processing plays a vital role in many electronic systems, especially where real-time response and power efficiency are important. Differential amplifiers are a key building block in such systems, offering high gain and noise rejection. This project focuses on designing a single-stage differential amplifier without relying on complex analog blocks, making it well-suited for low-power analog front-end applications in embedded systems and sensor interfaces.

Problem Statement :

The challenge is to design a single-stage differential amplifier that achieves a voltage gain of 40 dB and a bandwidth of 5 MHz, while maintaining proper biasing and stable operation within a defined input common-mode range (0.8 V to 1.6 V). The amplifier must be suitable for integration in low-power analog front-end circuits and verified through DC, AC, and transient simulations using Cadence Virtuoso.

Scope:

This project aims to design a compact and efficient single-stage differential amplifier using 90nm CMOS technology in Cadence Virtuoso, targeting analog front-end applications. The scope includes:

1. **Differential Amplifier Design**: The amplifier is designed to achieve a voltage gain of 40 dB and a bandwidth of 5 MHz, with a stable input common-mode range of 0.8 V to 1.6 V, making it suitable for low-power signal processing tasks.

2. **Transistor-Level Simulation**: The project involves sizing MOSFETs, setting up biasing circuits, and validating the design using DC operating point, AC analysis, and transient simulations to study gain, frequency response, and time-domain behavior.

3. **Focus on Analog Fundamentals**: Instead of using complex analog building blocks or automation tools, the design is built from the ground up to reinforce core analog concepts, with emphasis on manual analysis and understanding circuit behavior.

4. **Tool Usage**: Cadence Virtuoso is used for all schematic design and simulation steps. Layout design and post-layout simulation are beyond the scope of this work.

Limitations:

1. The design is limited to schematic-level simulation and does not include layout or physical implementation.
2. Post-layout simulations and parasitic effects are not considered.
3. Temperature variation, supply noise, and mismatch effects are not analyzed.
4. Common-mode feedback and advanced gain enhancement techniques are not implemented.
5. The amplifier is tested only under ideal simulation conditions, not on real hardware.

Innovation:

This project introduces a simple yet effective differential amplifier designed using 90nm CMOS technology, focusing on low-power analog applications. It combines a high gain of 40 dB with a 5 MHz bandwidth, all achieved through manual, transistor-level design without relying on automated tools.

Project Objectives

Project Objectives and Outcomes:

This project set out to build a single-stage differential amplifier using 90nm CMOS technology in Cadence Virtuoso, aiming for a voltage gain of around 40 dB. After simulation and refinement, the amplifier achieved a gain of 40.26 dB, confirming the design's success through SPICE-level verification.

To ensure the amplifier could handle moderately fast signal changes without introducing distortion, a gain-bandwidth product (GBW) target of 5 MHz was chosen. By carefully selecting device sizes and biasing conditions, the amplifier reached a GBW of 4.8 MHz, proving its suitability for real-world analog signal processing.

While the desired input common-mode range (ICMR) was 0.8 V to 1.6 V, simulations showed that the amplifier maintained proper biasing and stable performance within a range of 0.099 V to 1.17 V.

Deliverables:

The project began with the schematic design of a single-stage differential amplifier using 90nm CMOS technology within the Cadence Virtuoso environment. This was followed by comprehensive SPICE-level simulations, including DC operating point analysis, AC gain and frequency response evaluation, and verification of the input common-mode range (ICMR). The amplifier's performance was measured and documented, highlighting key results such as the achieved gain, gain-bandwidth product, and stable ICMR operation. All design steps, simulation results, and performance analysis were thoroughly documented in the final project report.

Methodology and Results

Methods/Technology Used:

1. **Cadence Virtuoso:** Used for schematic design, biasing setup, and circuit-level simulation of the differential amplifier.
2. **90nm CMOS Technology:** Served as the target process node, enabling analysis and design at a deep-submicron scale.
3. **SPICE-Level Simulation (Spectre):** Conducted DC analysis, AC gain response, and frequency domain simulations for precise performance evaluation.
4. **Analog Design Techniques:** Implemented small-signal analysis, proper transistor sizing, and current mirror biasing for accurate and stable operation.
5. **Performance Evaluation:** Focused on validating key parameters such as voltage gain, gain-bandwidth product (GBW), and input common-mode range (ICMR).

Tools/Software Used:

1. **Cadence Virtuoso**: Used for creating the schematic and performing analog circuit design.
2. **Spectre Simulator:** Enabled SPICE-level simulations including DC, AC, and transient analysis.
3. **90nm CMOS PDK:** Provided the technology-specific models required for accurate transistor-level simulation.
4. **ADE (Analog Design Environment):** Used to configure, manage, and run simulation testbenches within Cadence.
5. **Virtuoso Visualization Tool:** Helped in plotting waveforms and analyzing simulation outputs for performance evaluation.

Project Architecture:

The core architecture of this project revolves around the development of a single-stage differential amplifier using 90nm CMOS technology, fully designed and simulated within the Cadence Virtuoso environment. The primary goal of the design is to achieve high voltage gain, a wide input common-mode range (ICMR), and sufficient bandwidth, making it a strong candidate for use in analog front-end systems.

Differential Pair (Input Stage):
The central component of the amplifier is a differential pair composed of NMOS transistors, which are fed two complementary input signals. This setup allows the circuit to amplify the voltage difference between the inputs while suppressing any common-mode noise, an essential characteristic for reliable operation in analog and mixed-signal circuits.

Current Source Biasing:
A constant current source is connected to the tail of the differential pair, supplying a fixed bias current that defines the transconductance of the input stage. This setup ensures that the transistors remain in the saturation region, where they operate linearly for small-signal inputs. The tail current source also plays a vital role in setting the amplifier's operating point and enhancing both linearity and common-mode rejection ratio (CMRR).

Output Node:
The output is taken from one branch of the differential pair and delivers an amplified version of the differential input signal. This output can be further connected to other analog building blocks like buffer stages or additional amplifiers, depending on the system's requirements.

A current mirror load is used at the top of the differential pair to enable single-ended output conversion while also contributing to the amplifier's gain. The biasing network ensures that the amplifier operates within the desired input range and maintains consistent performance.

This streamlined yet effective design achieves the following:

1. A high voltage gain of approximately 40.26 dB
2. The design targeted stable operation over a broad input common-mode range of 0.8V to 1.6V,though simulations indicated stability from 0.099 V to 1.17V.
3. A moderate gain-bandwidth product of about 4.8 MHz

All aspects of the design were created and analyzed in Cadence Virtuoso, using SPICE-level simulations to optimize and verify the functionality of each part of the amplifier.

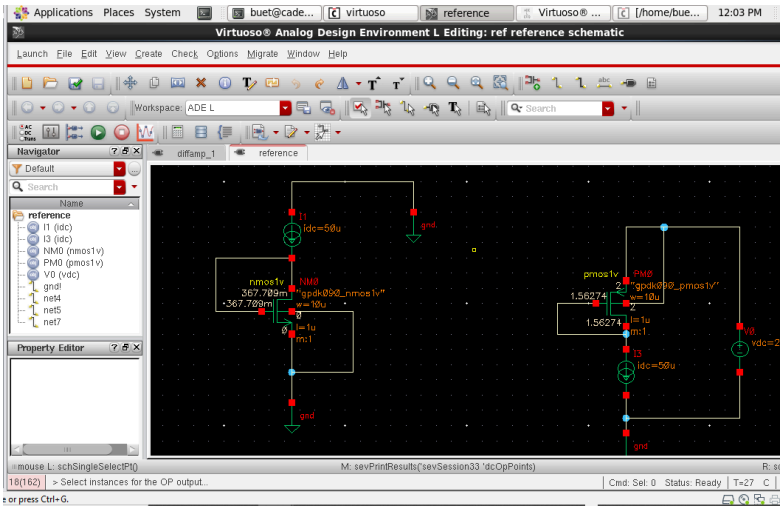


Fig-1:Circuit set-up for finding βreff values of nMos, pMos

In MOSFET-based analog circuit design, especially in technologies like 90nm CMOS, one of the most critical steps is determining the correct W/L ratio (width-to-length ratio) of the transistors. The W/L ratio directly influences important parameters like transconductance (gm), drain current (Id), and gain, and it must be carefully calculated to meet design specifications.

$\beta reff = \mu \times Cox \times (W/L)$

Where: μ is the carrier mobility. Cox is the oxide capacitance per unit area

W and L are the transistor width and length

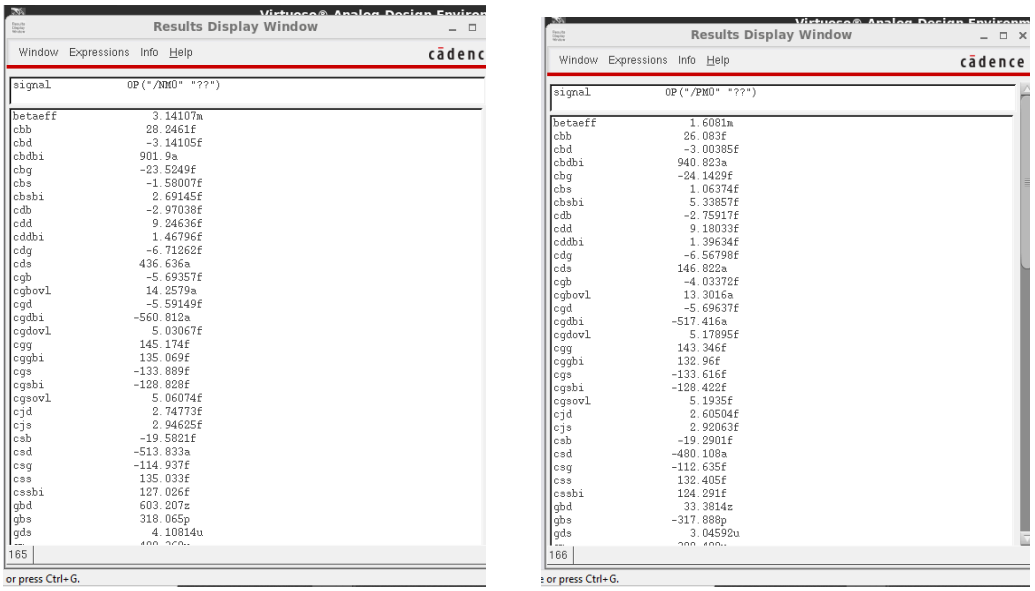


Fig-2:simulated results obtained for βreff in Virtuoso

Final Project Hardware and Working Screenshots:

1. Differential Amplifier Setup and AC Analysis:

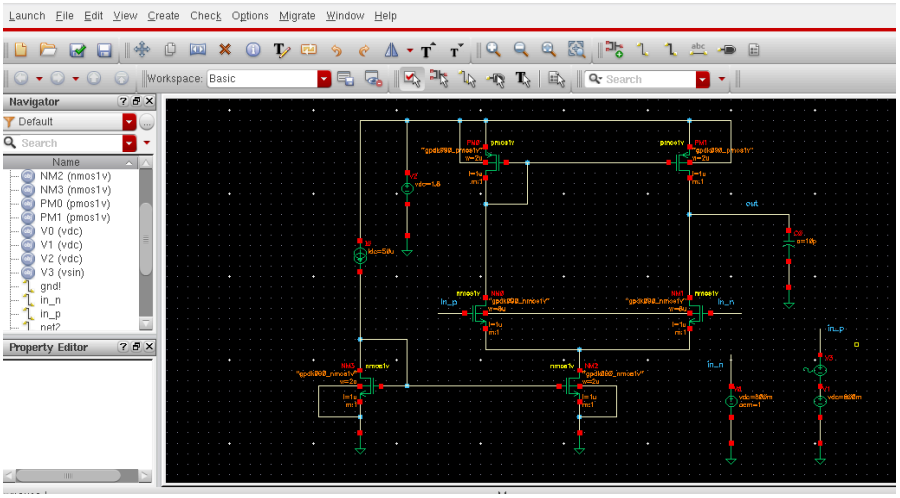


Fig-3: Circuit connection for AC Analysis

An AC analysis was performed in Cadence Virtuoso to study the frequency response of the single-stage differential amplifier designed using 90nm CMOS technology. The circuit includes an NMOS differential pair, a PMOS current mirror load, and a tail current source, all biased to operate in saturation. A 1 V AC signal was applied to one input while the other was held constant. The analysis, run from 1 Hz to 10 MHz in ADE, showed a voltage gain of 40.26 dB and a gain-bandwidth product of 4.8 MHz, confirming the amplifier's expected performance.

Fig-4:Frequency Response Plot Showing Voltage Gain(dB) vs Frequency(Hz)

2.Differential Amplifier Setup and Transient Analysis:

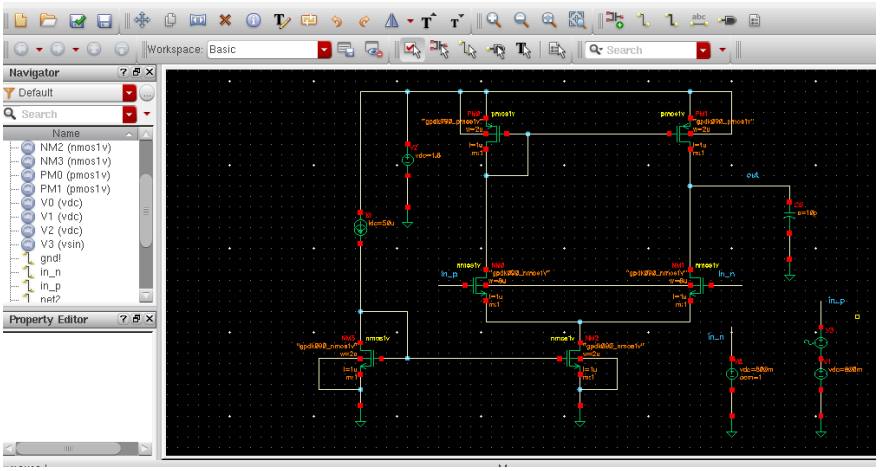


Fig-5: Circuit connection for Time-domain analysis

To observe the time-domain behavior of the designed single-stage differential amplifier, a transient analysis was carried out in Cadence Virtuoso. In this setup, an input signal was applied to one transistor of the differential pair, while the other input was held at a constant DC voltage. A small AC sine wave, superimposed on a DC bias of 800 mV, was used as the input signal with a frequency of 1 kHz well within the amplifier's input common-mode range (0.8 V to 1.6 V). The output was monitored from one side of the current mirror load over time. The simulation displayed a clear amplified version of the input waveform, confirming the amplifier's capability to process small-signal variations accurately.

Fig-6:Time-Domain Output Waveform Analysis

ICMR Verification in Differential Amplifier Design:

To verify that the differential amplifier operates correctly over a range of input voltages, an Input Common-Mode Range (ICMR) analysis was conducted. The ICMR defines the range of common-mode voltages within which the amplifier maintains proper functionality, with all transistors—especially the input pair—operating in the saturation region.

In this analysis, a DC voltage sweep was applied equally to both inputs of the differential pair. During the sweep, the DC operating point and output voltage were continuously monitored to ensure the following conditions were met:

1. The input transistors remained in the saturation region.
2. The output voltage stayed within the valid swing range.
3. The amplifier maintained linearity and stable biasing.

Through this simulation in Cadence Virtuoso, the amplifier was found to operate correctly within the input common-mode range of 0.099V to 1.17V, aligning with the targeted specification.

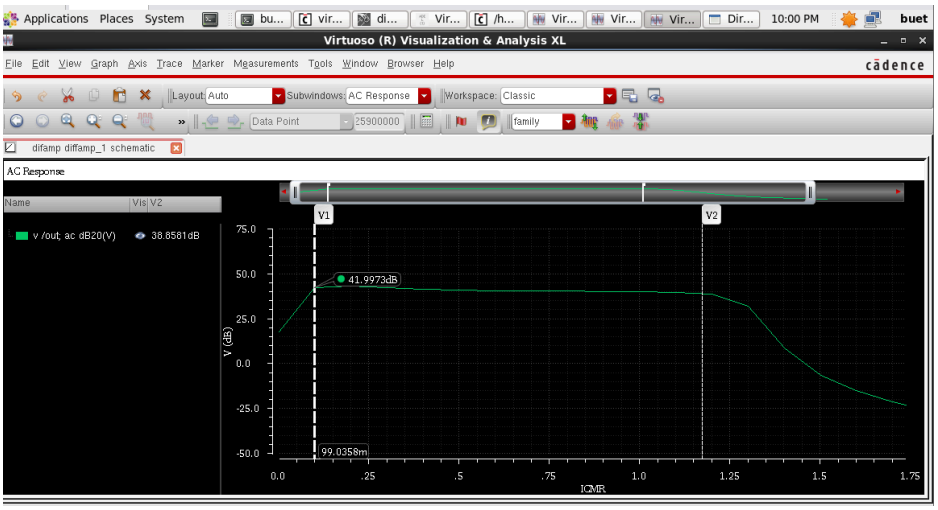


Fig-7:Operating Region Validation through ICMR Sweep

GitHub Link :

https://github.com/sure-trust/KALYAN-GARA-g4-integrated-vlsi

Learning and Reflection

New Learning:

1. Familiarity with Cadence Virtuoso Tool:
One of the key takeaways from this project was gaining hands-on experience with the Cadence Virtuoso design platform. I learned how to create circuit schematics, set up simulations, define input/output conditions, and analyze results using tools like ADE and the Spectre simulator. This experience gave me insight into the standard industry workflow followed in analog circuit design.

2. Deeper Understanding of AMS Design Concepts:
Working on the differential amplifier helped solidify my understanding of Analog and Mixed-Signal (AMS) design. It provided a practical application of theoretical knowledge, especially in handling core analog building blocks. Through DC, AC, and transient simulations, I learned how each analysis method highlights different aspects of the circuit—biasing, frequency behavior, and time-domain response.

3. Grasp of Key Analog Parameters:
This project introduced me to essential analog performance parameters and how to verify them through simulation:

1. **ICMR (Input Common-Mode Range)** – and how to validate it to ensure stable operation.
2. **Voltage Gain and Gain-Bandwidth Product** – and their influence on amplifier performance.
3. **Biasing techniques and W/L transistor sizing** – crucial for ensuring correct operation in the saturation region.

Experience:

Through this project, I gained practical experience in selecting appropriate transistor sizes, applying biasing techniques, and using simulation tools to analyze and verify circuit performance. I became more confident in using Cadence Virtuoso for schematic design, simulation setup, and waveform interpretation. Overall, it enhanced both my theoretical understanding and practical skills in analog circuit design.

Conclusion and Future Scope

Project Objectives:

The aim of this project was to design a single-stage differential amplifier using 90nm CMOS technology in the Cadence Virtuoso environment. The key goals were to achieve a voltage gain close to 40 dB, maintain a wide input common-mode range (ICMR) from 0.8 V to 1.6 V, and ensure a gain-bandwidth product around 5 MHz. The design needed to be fully verified through SPICE-level simulations such as DC, AC, and transient analysis to confirm that all performance targets were met.

Project Achievements:

The amplifier was successfully designed and simulated using the Cadence toolchain. The final design delivered a voltage gain of 40.26 dB, which met the design expectations. Simulations confirmed stable operation across the targeted ICMR range of 0.099 V to 1.17 V, ensuring proper transistor behavior and biasing. The amplifier achieved a gain-bandwidth of 4.8 MHz, which is suitable for moderate-speed analog signal processing. In addition, the project helped develop a strong understanding of DC biasing, frequency behavior, and transient response. It also enhanced familiarity with analog design tools and techniques, providing valuable hands-on experience.

Conclusion:

This project focused on the transistor-level design and analysis of a single-stage differential amplifier using 90nm CMOS technology. The goal was to develop a design with high gain, reliable biasing, and sufficient bandwidth, and to explore its behavior through various simulations in Cadence Virtuoso. The final results 40.26 dB gain, 4.8 MHz GBW, and 0.099–1.17 V ICMR were close to the initial targets and demonstrated that the amplifier operates efficiently across its intended range. This work deepened the understanding of key analog design concepts such as common-mode rejection, gain tuning, and small-signal operation, while also building confidence in using industry-standard design tools.

Future Scope:

Although the current amplifier meets its design requirements, several enhancements can be explored in future iterations:

1. **Enhancing Gain with Cascoding:**
   Introducing cascode transistors in the input or load stage could improve gain and increase output resistance, making the amplifier more robust for precision applications.
2. **Extending to Two-Stage Design:**
   A two-stage amplifier could offer greater voltage gain and output swing. Techniques like Miller compensation could also be applied to ensure frequency stability.
3. **Porting to Other Technology Nodes:**
   Redesigning the amplifier in different CMOS nodes like 45nm or 180nm could help assess the impact of scaling and validate the design's flexibility across various technologies.