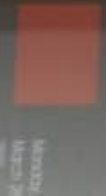
Taxonomy Memory: Based on Read/Write or Volatility

- Read/Write Memories (RWM or RAM)
- Read only Memories (ROM)
- Volatile
- Non-volatile

Of *RAM/ROMs*: The *muddle* within

- Both could be RAMs
- Huh, how is that?

Read Only Memory (ROM)



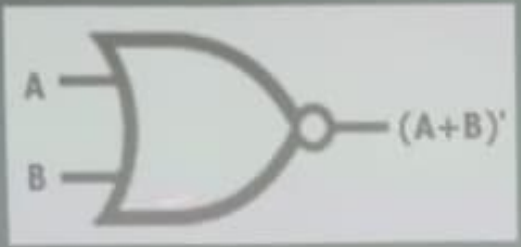
- A PC uses it to hold BIOS both for system and I/O adapters
- Various forms:
  - Mask ROM
  - PROM
  - EPROM
  - EEPROM
- Non volatile

RAM (RWM)

- Flip-flop:

  A circuit made out of logic gates that stores one-bit of information forms the basic building block of the RAM

NOR Gate: A Quick look



NOR GATE		
A	B	(A+B)'
0	0	1
0	1	0
1	0	0
1	1	0

SR – Flip-Flop
(Cross-coupled NOR Gates)

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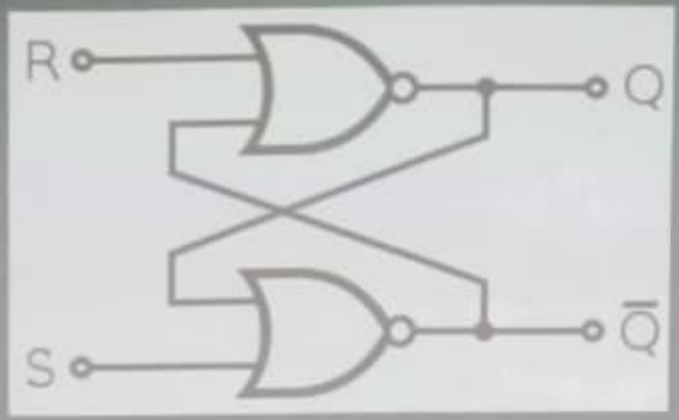

R	S	Q	Q'
1	0	0 (Reset)	1
0	0	0 (Older value)	1
0	1	1 (Set)	0
0	0	1	0
1	1	0/1 Confusing results for confusing inputs!	

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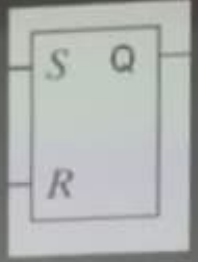

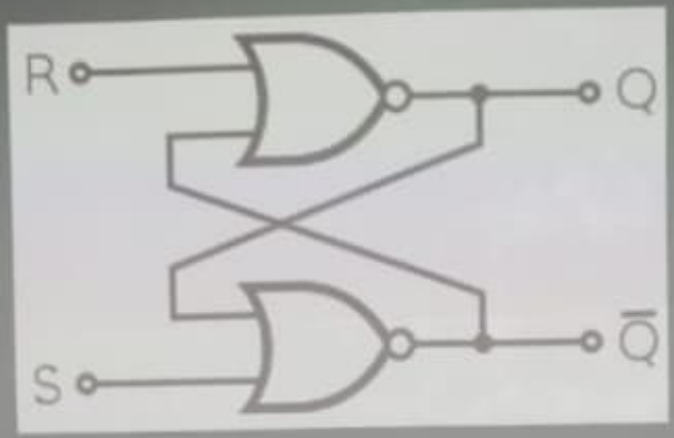

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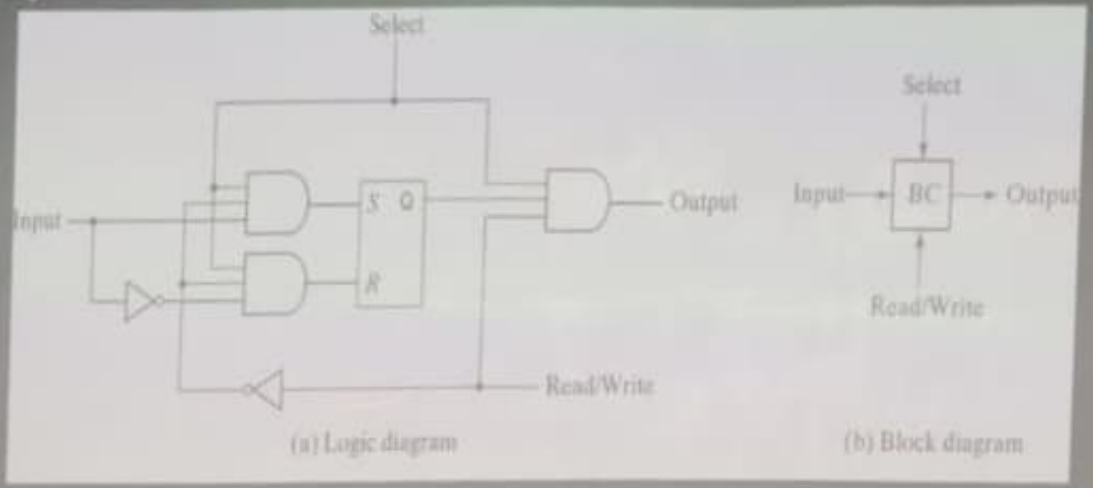
RAM: One bit Storage

- Basis of each SRAM cell is an S-R latch
- Note that data goes to both S and R
- Select enables operation
- Read/write enables read write, but not both



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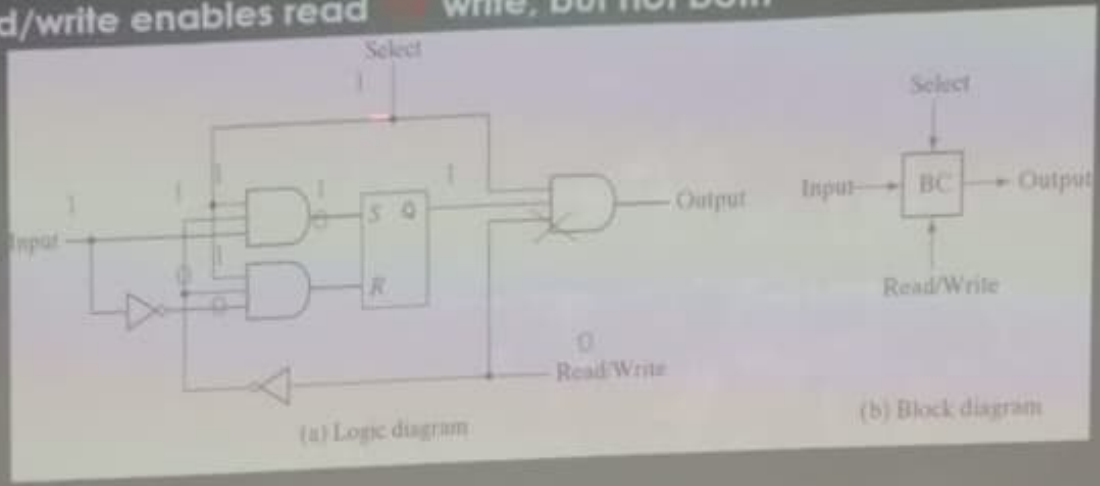

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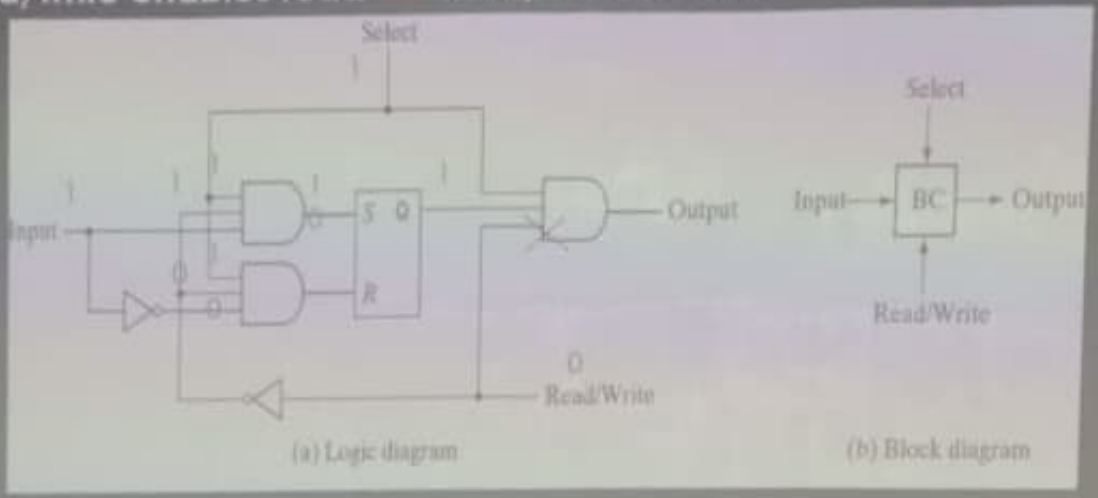
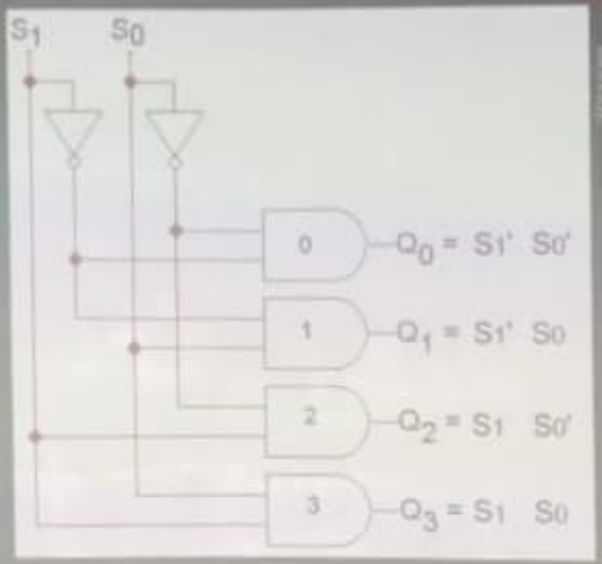


2-to-4 decoder RECAP

2 inputs and 2^2 *outputs*

S1	S0	Q 3	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0



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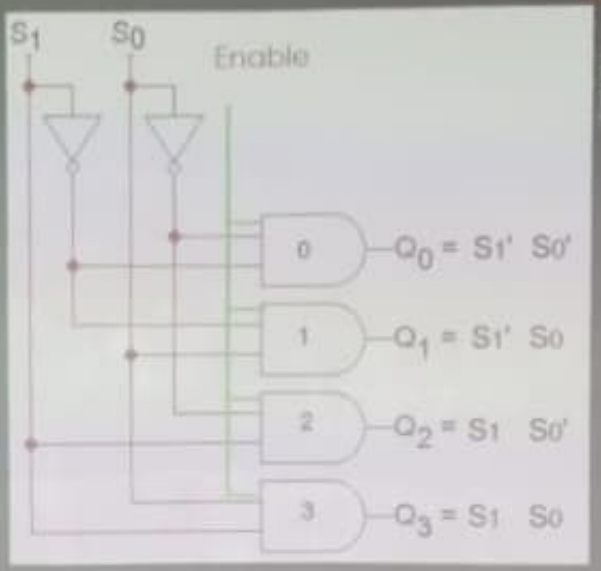
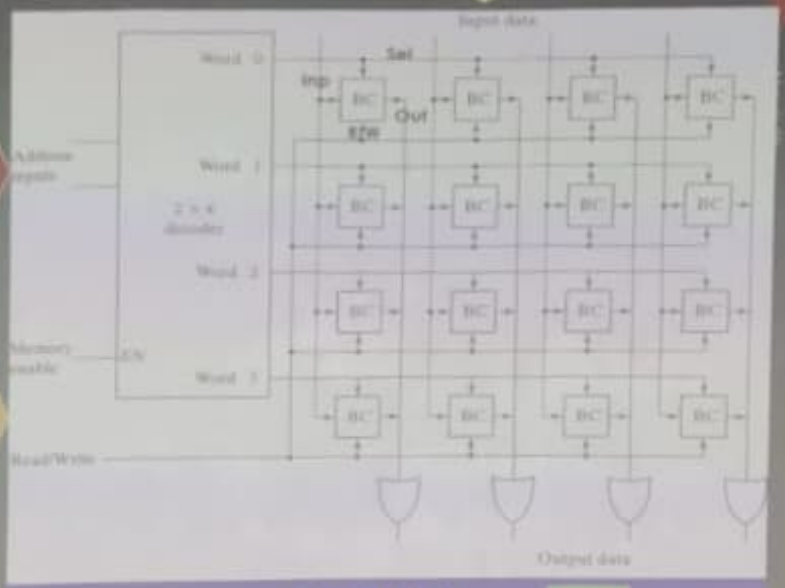


RAM (R/W Memory)

Data input



Address Bus

Control Bus

4x4 RAM

Data output

- How many address bits would I need for 16 words?

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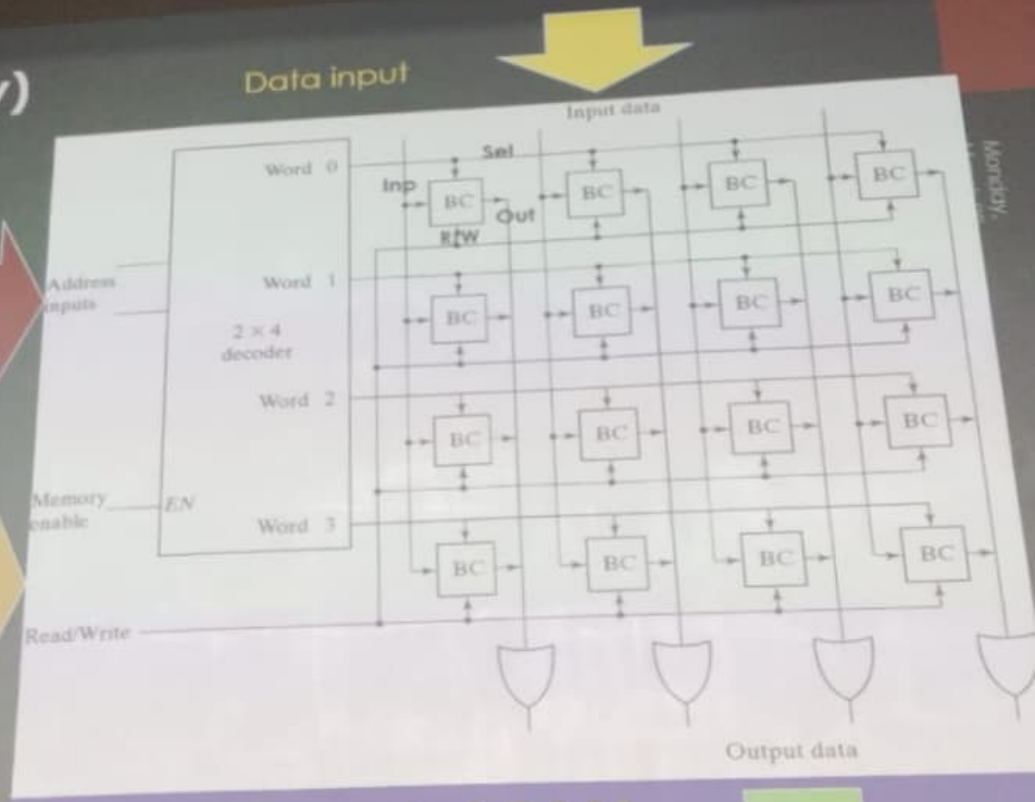
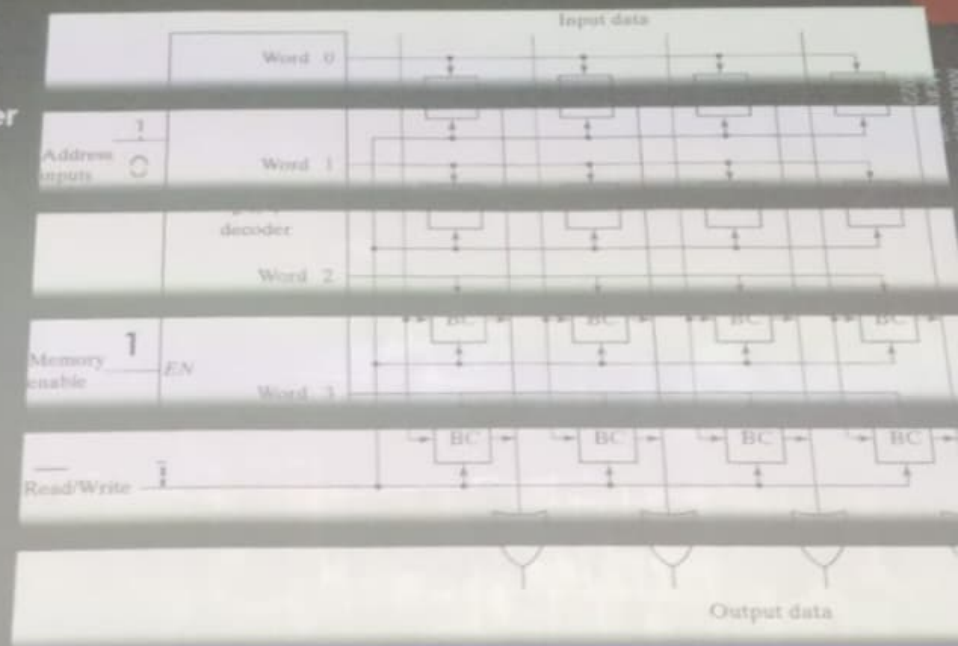


4x4 RAM

RAM

- Address inputs go into decoder
  - Only one output active
- Word line selects a row of bits (word)
- Data passes through OR gate
- Each binary cell (BC) stores one bit
- Input data stored if Read/Write is 0
- Output data driven if Read/Write is 1



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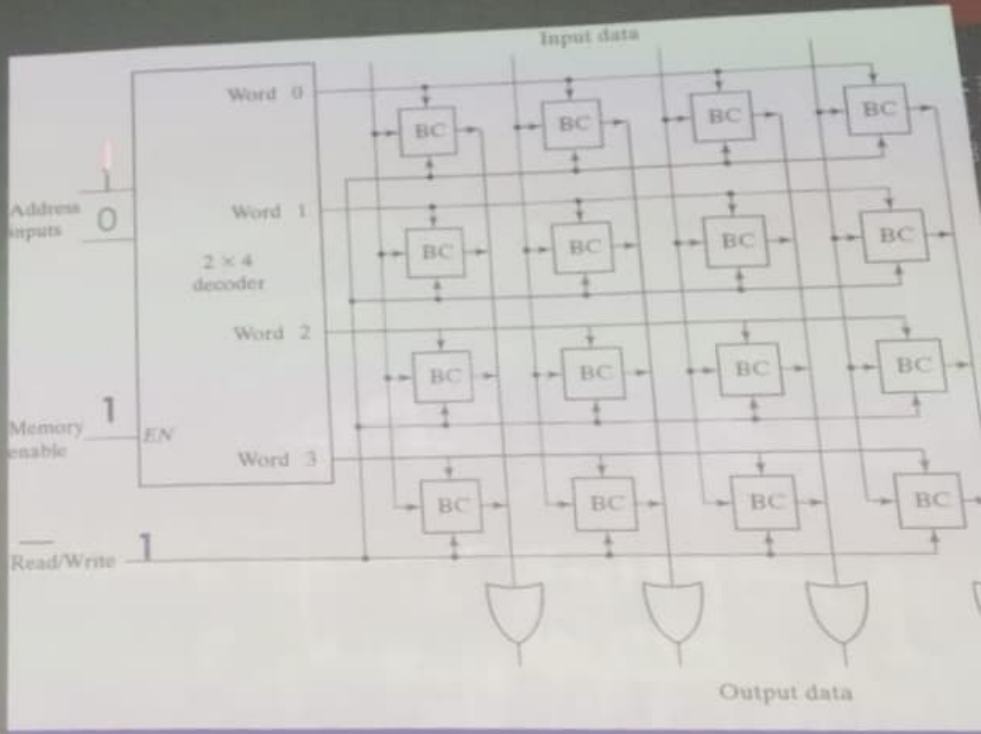

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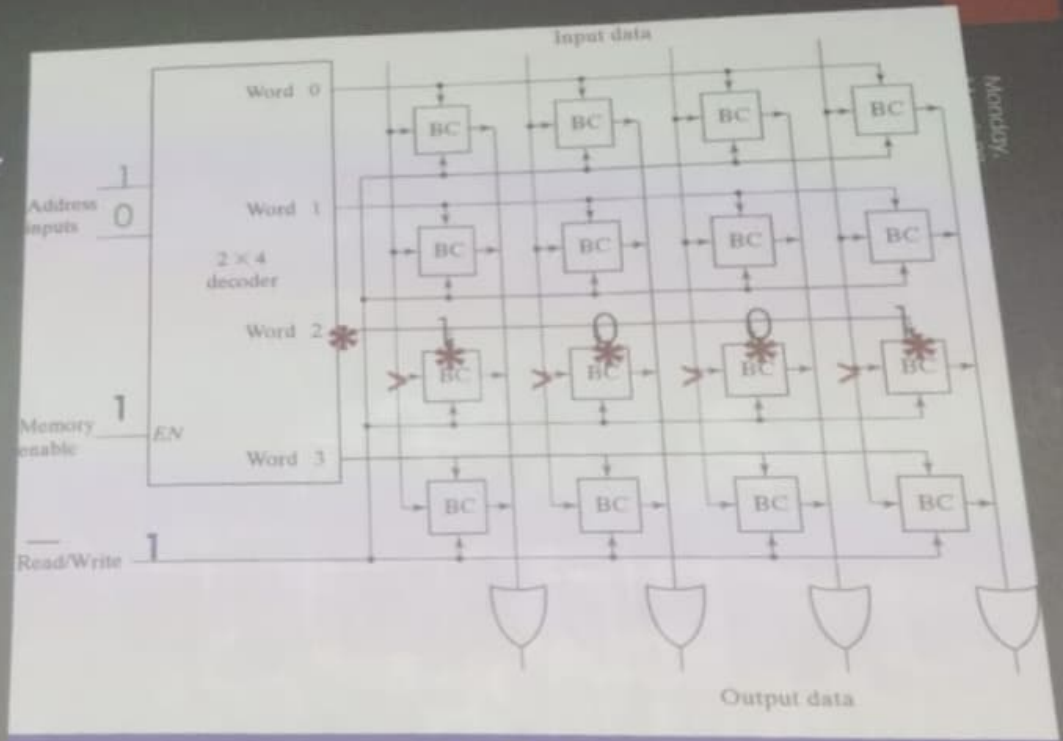
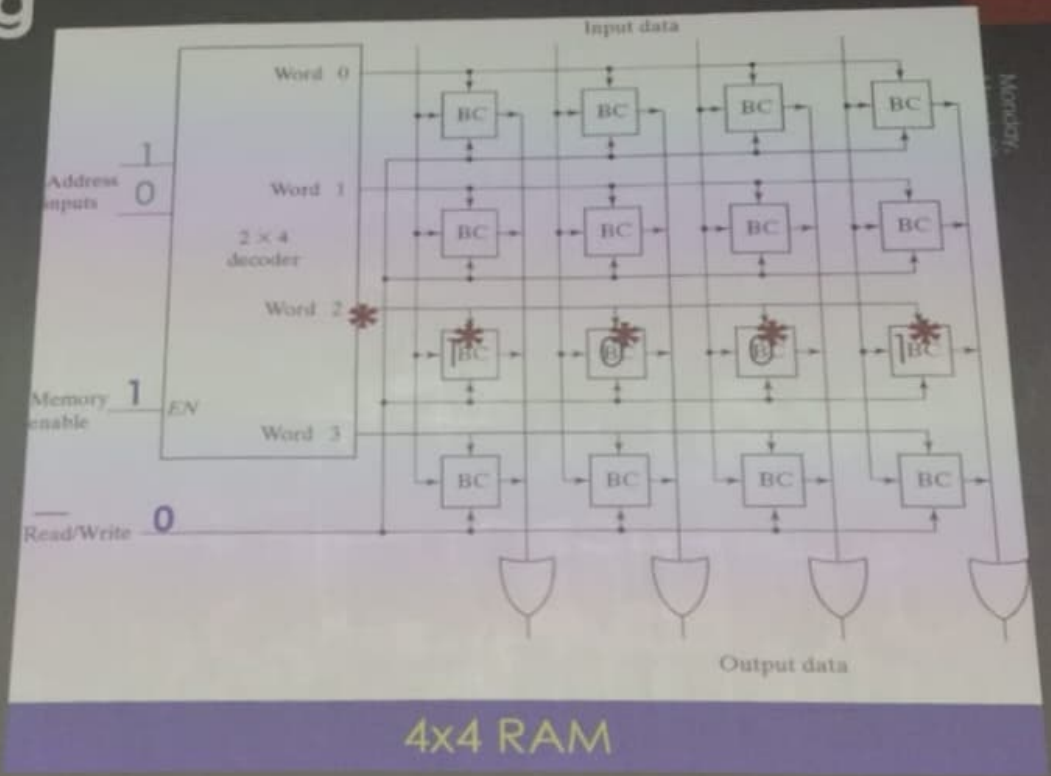


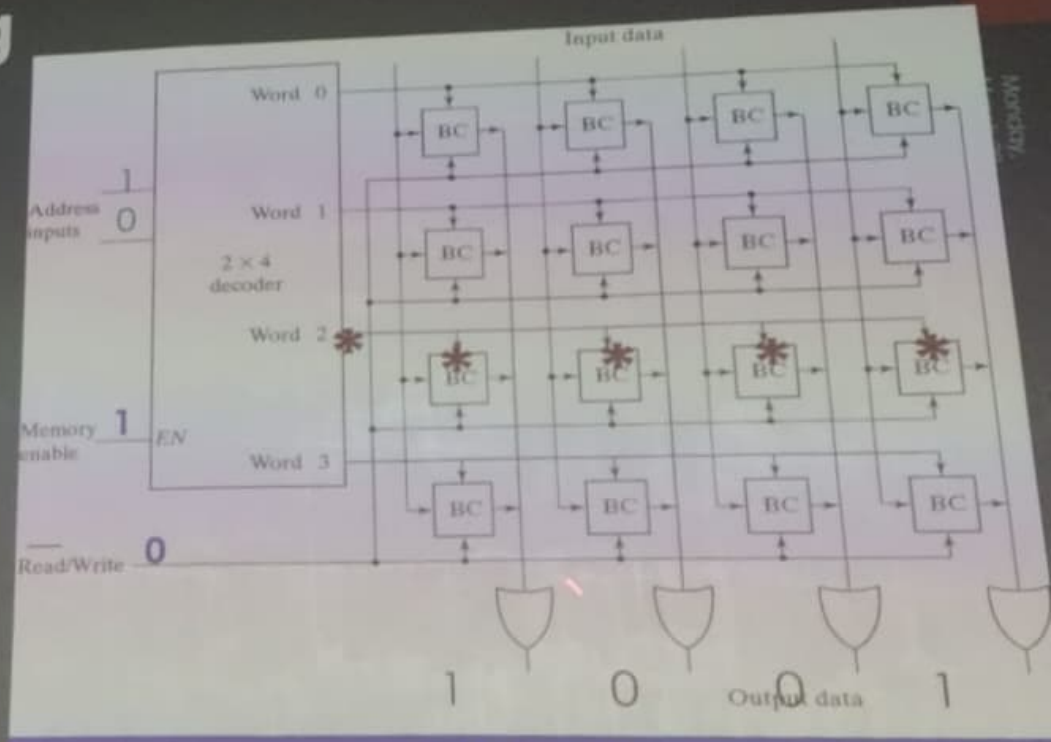
4x4 RAM

RAM Reading



4x4 RAM

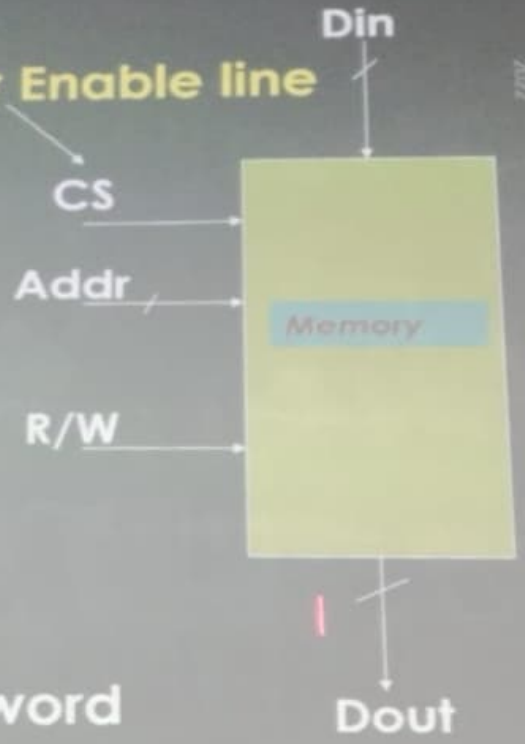
RAM Reading



4x4 RAM

Memory

- Typical →
  - Data input bus
  - Data output bus
  - Address
  - Read/Write control
  - Chip Select



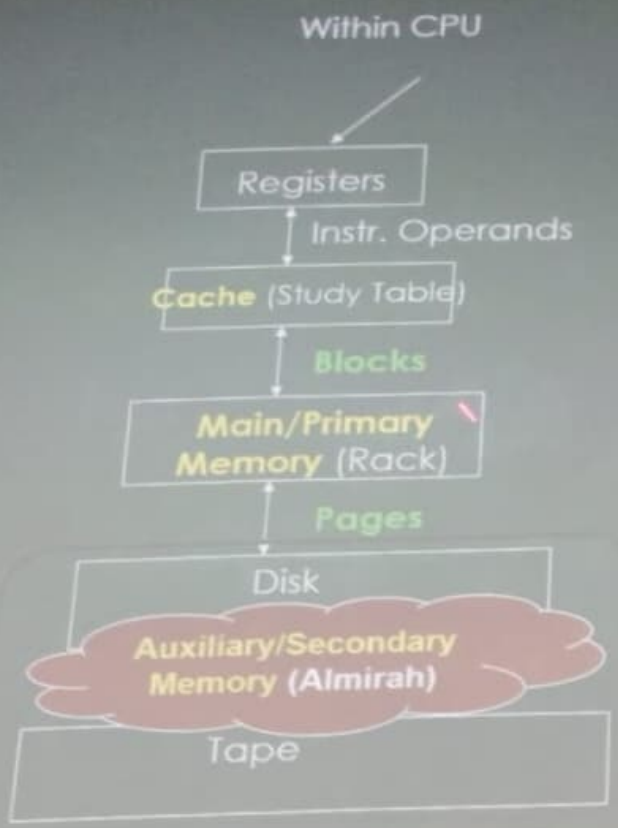
Size: m x n

where m = no. of words & n = bits/word

Organizing Levels of Memory (STORAGE)

Storage	Almirah	Rack	Study Table
Capacity (books stored)	High	Medium	Small
Speed of Access	Slow	Medium	Fast
Transfers done in one stroke	Several Books	One book	Page

Levels of the Memory Hierarchy

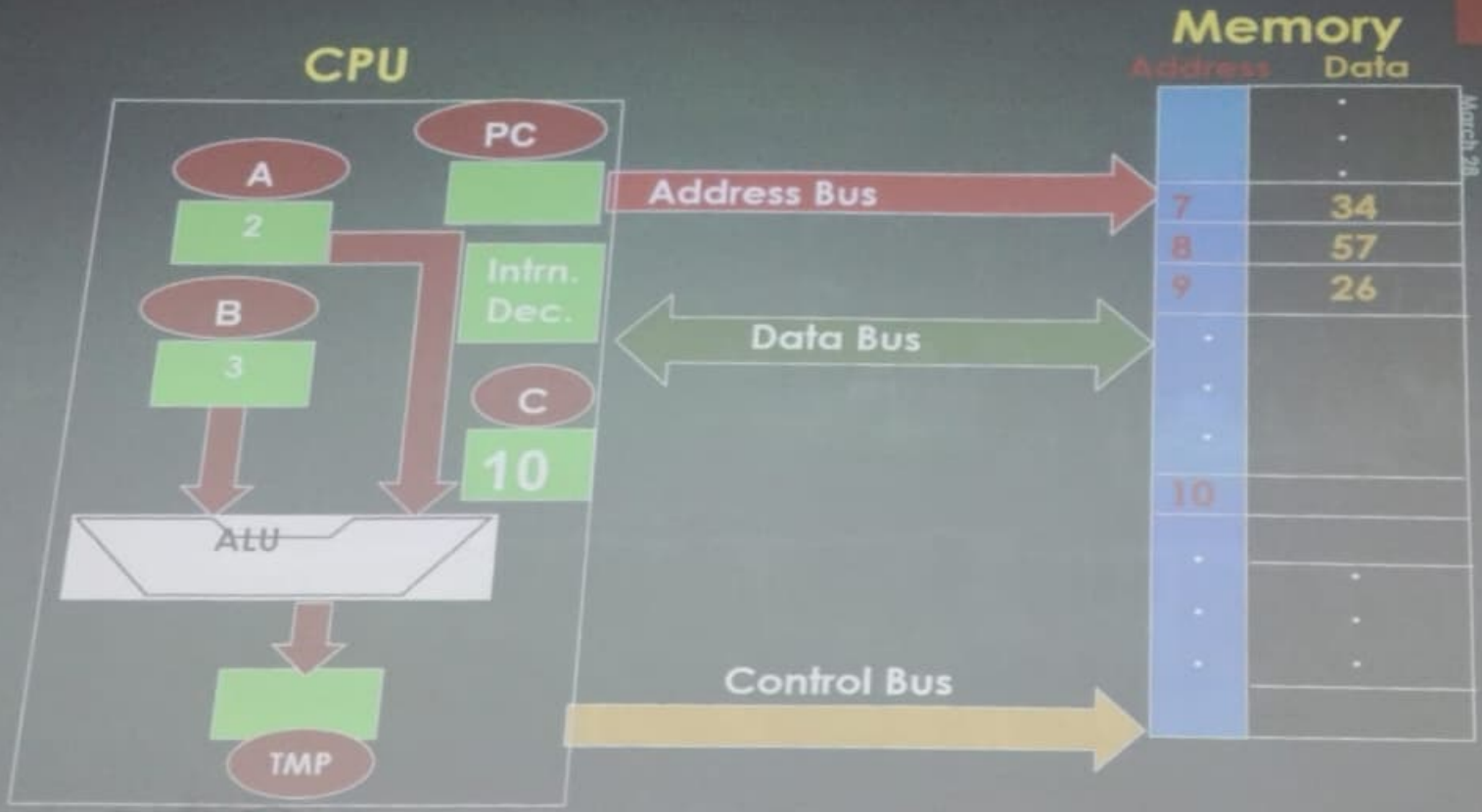


Execution of some hypothetical Instructions

Address	Assembly Instructions	Comments
7H	ADD A, B	;Add content of register A with that of B and store it in A i.e. [A] ← [A] + [B]
8H	STA [C]	; Store contents of register A to the memory location whose address is contained in register C.

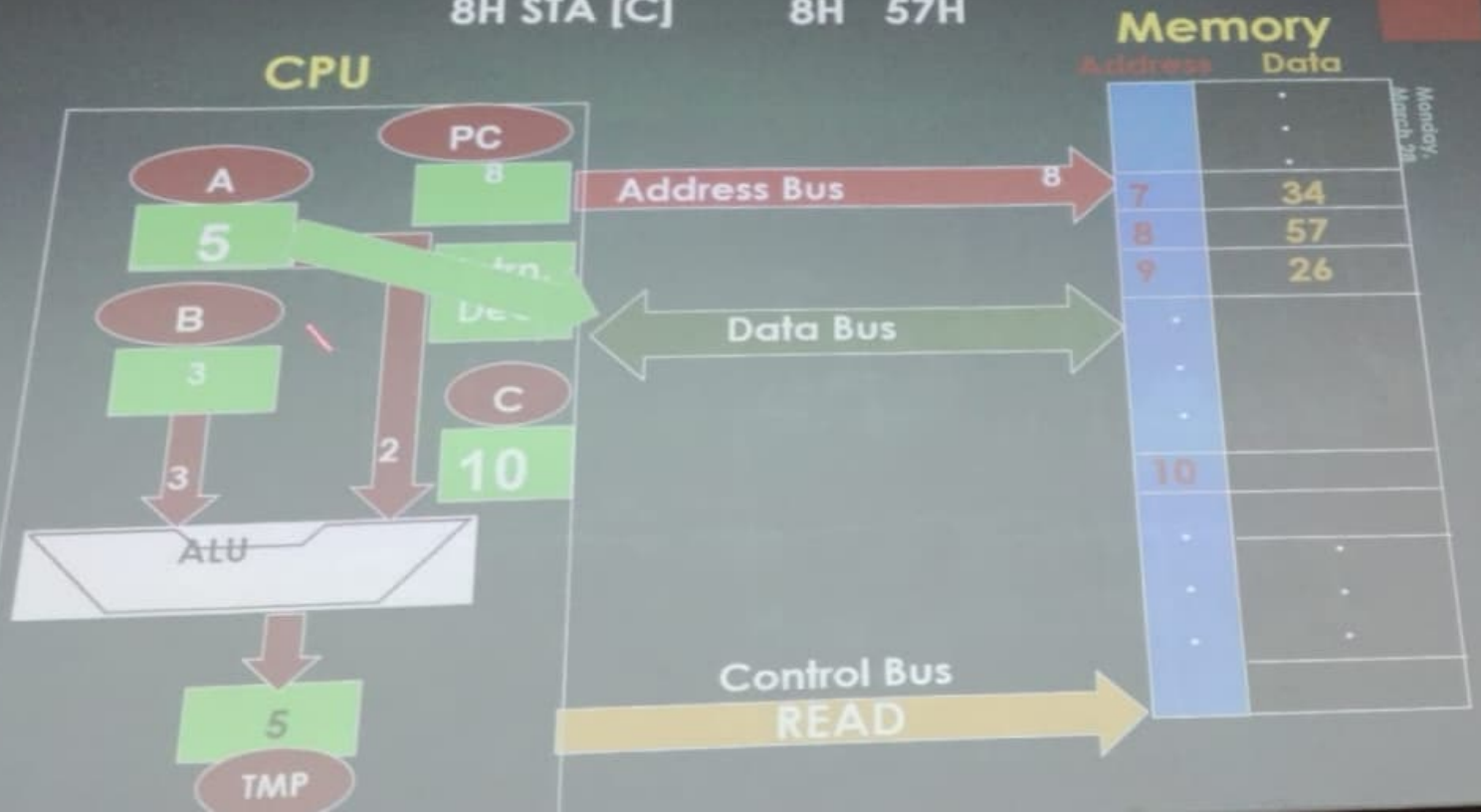
Address	Machine Language	Assembly Instructions
7H	34	ADD A, B
8H	57	STA [C]

Execution


CPU
PC
A
2
B
3
Intrn.
Dec.
C
10
ALU
TMP
Address Bus
Data Bus
Control Bus
Memory
Address
Data
7
34
8
57
9
26
10
Monday,
March 28

Execution

7H ADD A, B 7H 34H
8H STA [C] 8H 57H



Take a deep breath and exhale.
Sit calmly and
DO NOT TALK OR DISTURB ANYONE

Bidding Farewell to Hardware for now!
Coming next at a Lecture Hall near you.

Sailing The Sea of Cs

Nota Bene:

Boarding will be allowed only from the Starboard side.

Port side access is prohibited

Naturally, no one will be allowed after the ship sets sail!
So be on time & board the ship well in advance!