EE 101-18/19-MS-SD	EE 101 (Mid Semester)	Max. Marks: 30

Give answers in the response sheet and include SI units, where necessary.
Power factor should include lead/lag and phasors use peak values of the magnitude.
All answers for electrical networks should be rounded off to 2 decimal places.

Name:	Roll No:
Tutorial Group:	Invigilator's Signature:

Q1. In a certain network, the source voltage and the current delivered by the source are given by:

$$v = 80\sin(200t + 45°)\text{V}\ ,\ i = 20\sin(200t - 15°)\text{A}$$

Determine:

a. the impedance Z in polar form
b. complex power in Cartesian form
c. the magnitude of complex power
d. the magnitude of active power
e. the magnitude of reactive power
f. the power factor

Marks: ½ + ½ + ½ + ½ + ½ + ½ = 3

Q2. A digital circuit has two control inputs (S_1 and S_2), two data inputs (X_1 and X_2) and one output (Z). As shown in **Tab.Q2**, the circuit performs logic operations on the data inputs as determined by the control inputs. Find:

a. the minimal SOP form of Z
b. the minimal POS form of Z

S_1	S_2	Z
0	0	$X_1 + \bar{X}_2$
0	1	$\bar{X}_1 + \bar{X}_2$
1	0	$X_1 + X_2$
1	1	$\bar{X}_1 + X_2$

Tab.Q2

Marks: 1½+1½ = 3

Q3. The parameters of the network shown in **Fig.Q3**, are:

$$V_1 = 20\angle 0°\text{V},\ V_2 = 20\angle -30°\text{V}$$
$$R_1 = 3\Omega\ ,\ R_2 = 3\Omega\ ,\ R_3 = 10\Omega$$
$$X_L = 4\Omega\ ,\ X_C = 4\Omega$$

Determine in phasor form (polar):

a. the current I_A
b. the current I_B
c. the voltage drop V_{AB}

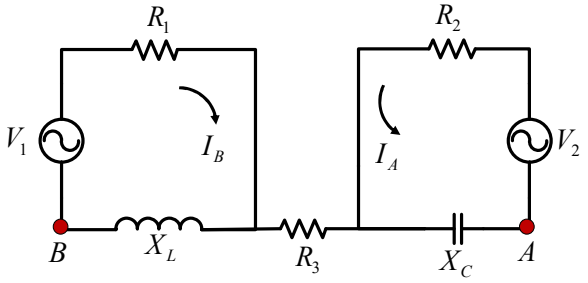

Fig.Q3

Marks: 1½+1½+1½ = 4½

Q4. Consider the logic circuit shown in **Fig.Q4,** consisting of two 4-to-1 multiplexers.

a. Draw the Karnaugh Map for the function $F(W, X, Y, Z)$
b. Find the minimum SOP form of F.
c. Find the minimum POS form of F.

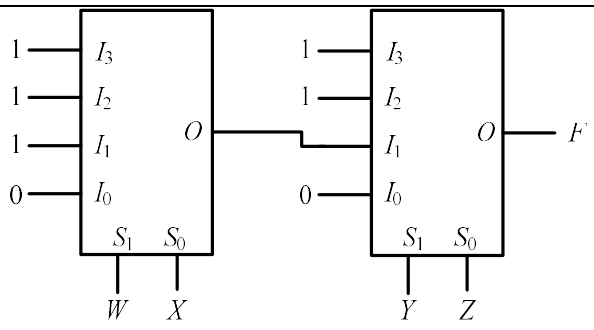

Fig.Q4

Marks: 1+1+1 = 3

Q5. The parameters of the network shown in **Fig.Q5** are: $R_1 = 5\Omega$, $R_2 = 3\Omega$, $R_3 = 5\Omega$, $R_4 = 2\Omega$, $V = 10\angle -30°\text{V}$, $X_{C1} = 2\Omega$, $X_{C2} = 2\Omega$ and $X_L = 5\Omega$. Consider the Thevenin equivalent of the circuit to the left of terminals A and B. Determine in phasor form:

a. Thevenin equivalent voltage
b. Thevenin equivalent impedance
c. the current I_{AB}

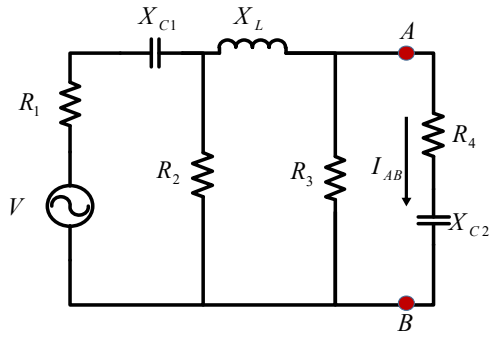

Fig.Q5

Marks: 1½+1½+1½ = 4½

Q6. The parameters of the network shown in **Fig.Q6** are $R_1 = 4\Omega$, $R_2 = 1\Omega$, $L = 0.25\text{H}$, $C = 0.1\text{F}$ and $V_s = 12\text{V}$. The switch S has been closed for a long time. It is open at $t = 0$. Find:

a. $i(0^+)$ b. $v(0^+)$
c. $\frac{d}{dt}i(0^+)$ d. $\frac{d}{dt}v(0^+)$
e. $i(\infty)$ f. $v(\infty)$

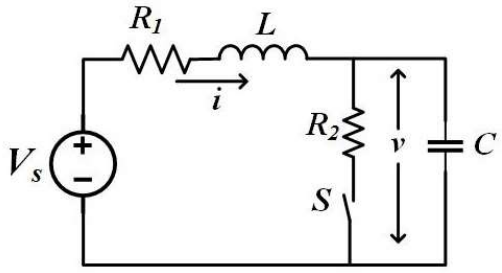

Fig.Q6

Marks: ½ + ½ + ½ + ½ + ½ + ½ = 3

Q7. Find the minimal SOP for J_1, K_1, J_2 and K_2 such that the circuit shown in **Fig.Q7a** has its outputs Q_1 and Q_2 in response to inputs I_1 and I_2, as shown in **Fig.Q7b.**

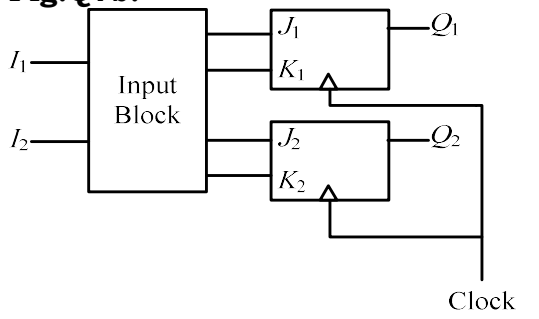

Fig.Q7a

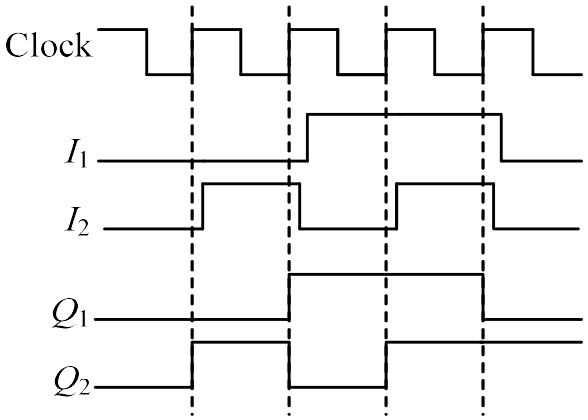

Fig.Q7b

Marks: 1+1+1+1 = 4

Q8. Consider the state diagram in **Fig.Q8** corresponding to a sequential circuit having 2 JK flip-flops. The state of the flip-flops are denoted by variables A (inputs J_A and K_A) and B (inputs J_B and K_B). Let the state of the circuit be denoted by AB and the input by W.

a. Write the state table.
b. Write the state equations in the minimal SOP form.
c. Express J_A , K_A , J_B , K_B in the minimal SOP form.

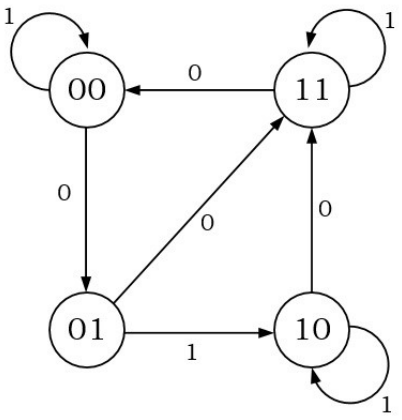

Fig.Q8

Marks: 2+1+2 = 5