Indian Institute of Technology Guwahati, Deptt. of Comp. Sc. & Engg.

CS221 (Digital Design) Quiz B1, Time: 50 minutes, Marks: 20 Date: 16th Oct 2019

Name: Model Solution	Roll No: Maybe diffent Solution exist

Write answer in the space provided. Draw diagram for FSM if asked. But **no need to draw diagram of circuit** instead write the "**FINAL Boolean Functions**" for the implementation.

Q1: [1+1+2+2 Marks] A *BC* flip-flop has four operations, no change, clear to 0, set to 1 and complement, when inputs *B* and *C* are 00, 01, 10 and 11 respectively. (a) Derive the characteristics equation for this *BC* Flip flop (b) Show how this *BC* flip-flop can be converted to a D-flip flop, (c) Draw FSM diagram for this flip flop, (d) How can you design this *BC* flip-flop given a D flip flop.

B	C	Q^+
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

$$Q^+ = \bar{B}\bar{C}Q + B\bar{C} + BC\bar{Q}$$
$$= \bar{B}\bar{C}Q + (B\bar{C}Q + B\bar{C}\bar{Q}) + BC\bar{Q}$$
$$= \bar{B}\bar{C}Q + B\bar{C}Q + B\bar{C}\bar{Q} + BC\bar{Q}$$
$$= (\bar{B}+B)\bar{C}Q + B\bar{Q}(\bar{C}+C)$$
$$= \bar{C}Q + B\bar{Q} = \boxed{B\bar{Q} + C'Q}$$

Same as JK FF

set $B=D$, $C=D'$

$D = B = C'$

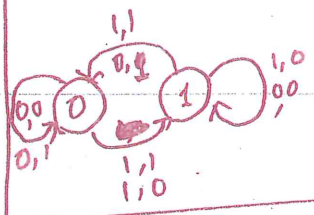
Will reset

$Q^+ = B\bar{Q} + \bar{C}Q$

$= DQ + DQ$

$= D(\bar{Q}+Q)$

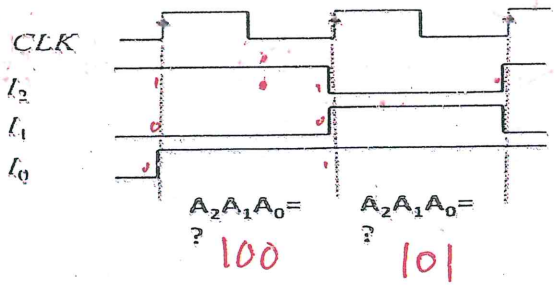
$Q^+ = D$

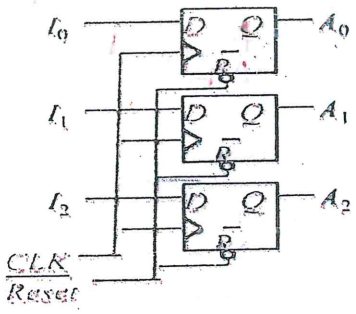


$Q^+ = B\bar{Q} + C'Q$

Diagram also fine

Q2: [2 Marks] Given the input wave form to a 3 bit PIPO register, write output (in binary) for both clock cycles. No partial marks will be awarded.





Q3: [4 marks] Design and implement a 3 bit grey code synchronous counter using D-FFs. The gray code sequence for 3 bit counter is as follows: 000, 001, 011, 010, 110, 111, 101 and 100.

PS	NS		
	F_1	F_2	F_3
000	0	0	1
001	0	1	1
010	1	1	0
011	0	1	0
100	0	0	0
101	1	0	0
110	1	1	1
111	1	0	1

A BC

$F_1 = \Sigma m(2,5,6,7) = B\bar{C} + AC$

$F_2 = \Sigma m(1,2,3,6) = B\bar{C} + A\bar{C}$

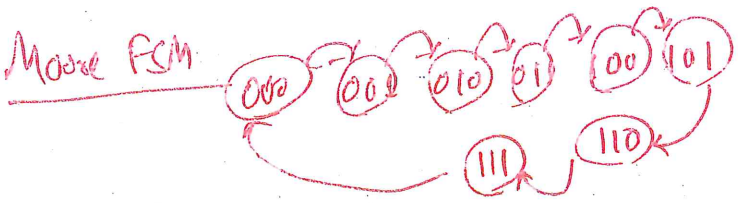
$F_3 = \Sigma m(0,1,6,7) = \bar{A}\bar{B} + AB$

Model Solution

Base on Gompy

Q4: [2+2+2 Marks] Design a FSM (preferably Moore FSM) to generate the following 3 wave pulse trains given a simple alternating clock C as input. Implement that FSM controller using D-FFs. Write (a) the output functions in-terms of input and current states and also (b) write next state functions in-terms of input and current state.

Z1: 00101000 00101000 00101000....
Z2: 11011011 11011011 11011011....
Z3: 00110111 00110111 00110111....



F_1 F_2 F_3	
000	001
001	010
010	011
011	100
100	101
101	110
110	111
111	000

ABC

NS Logic

$NF_1 = \sum m(3,4,5,6) = \bar{A}BC + A\bar{B} + AC$

$NF_2 = \sum m(1,2,5,6) = \bar{B}C + B\bar{C}$

$NF_3 = \sum m(0,2,4,6) = \bar{B}\bar{C} + B\bar{C}$

Output logic

	Z_1	Z_2	Z_3
000	0	1	1
001	0	0	0
010	1	1	1
011	0	0	0
100	1	1	1
101	0	0	0
110	0	1	1
111	0	0	0

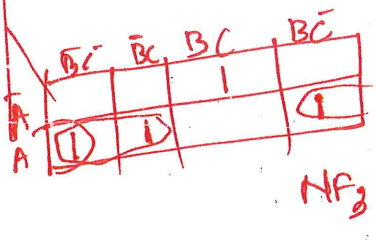
OR $Z_1 = \sum m(2,4) = \bar{A}BC + A\bar{B}\bar{C}$

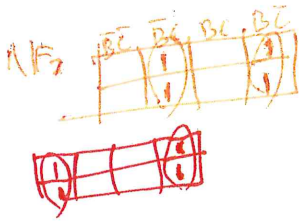
$Z_2 = \sum m(0,1,3,4,6,7) = \bar{B}\bar{C} + \bar{A}C + BA$

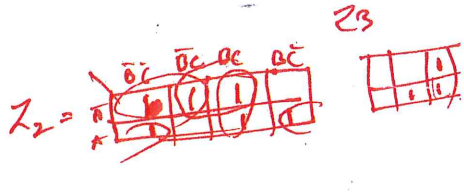
$Z_3 = \sum m(2,3,5,6,7) = B + AC$

OFs

$Z_2 = \bar{B}\bar{C} + \bar{A}C + AB$







Q5: [2 Marks] Re-implement FSM of Question 4 design using concepts from Question 3 (Gray code). And write the observations between previous implementation and current implementation.

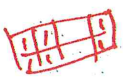
Associate output $Z_1Z_2Z_3$ to sequence of State

000, 001, 0

remap to Binary Sequence

Gray Sequence	OFs = Z_1 Z_2 Z_3	Binary Sequence	Z_1 Z_2 Z_3
000	0 1 0	000	0 1 0
001	0 1 0	001	0 1 0
011	1 0 1	010	0 1 1
010	0 1 1	011	1 0 1
110	1 1 0	100	0 1 1
111	0 0 1	101	0 1 1
101	0 1 1	110	1 1 0
100	0 1 1	111	0 0 1

$Z_1 = \sum m(3,6) = \bar{A}BC + AB\bar{C}$



$Z_2 = \sum m(0,1,2,4,5,6) = \bar{B} + \bar{C} = \bar{B}\bar{C}$

$Z_3 = \sum m(2,3,4,5,7) = BC + A\bar{B} + \bar{A}B$

Input logic for Z_2 is Simpler