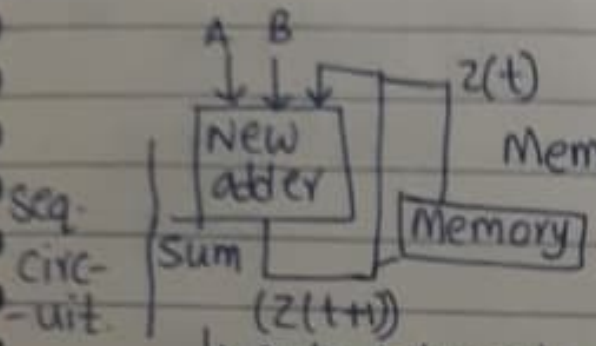
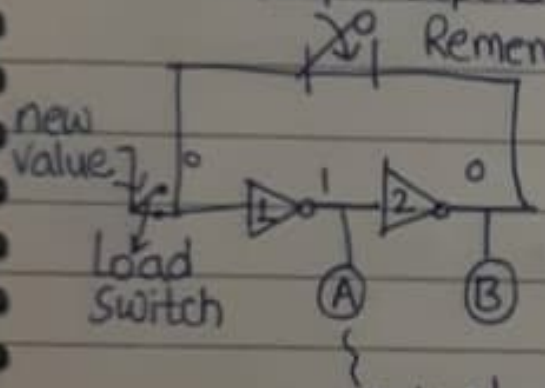
gate propogation delay

Combinational logic → Input & propogational delay
Sample-reading.
Slowest path-critical path.
↓frequency depends on this.

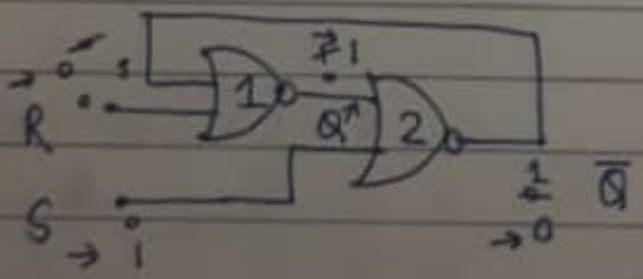


↳ output depend on input and prev. o/p → state.



gates reinforce outputs always

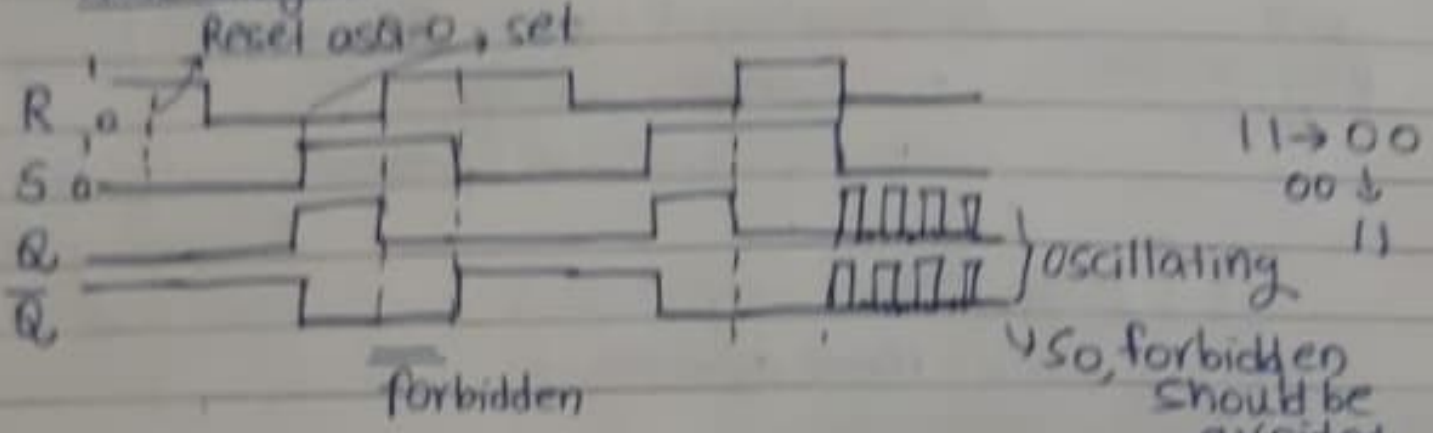
Load	Remember	Store
close	open	new
open	close	~~new~~ Retain



NOR input=0 → inverter
input=1 → output=0

S	R	Q	$\overline{Q}$
0	0	store-old.	
1	0	1	0
0	1	0	1
1	1	0	0 → not as per Specification forbidden input combination

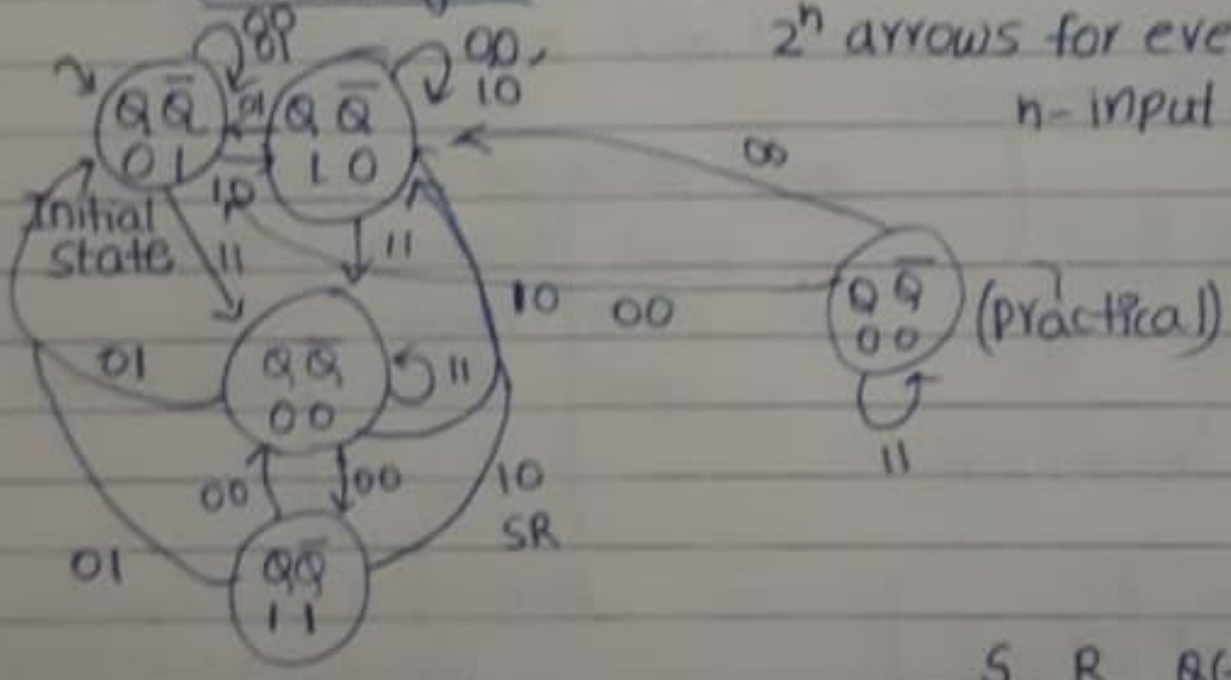
Time diagram R-S latch



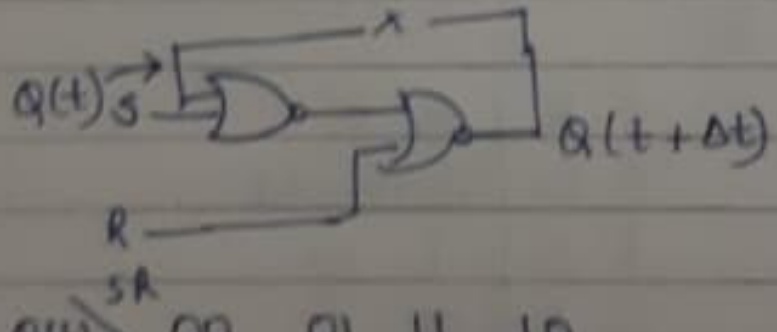
11 → 00
00 ↓
11

So, forbidden should be avoided.

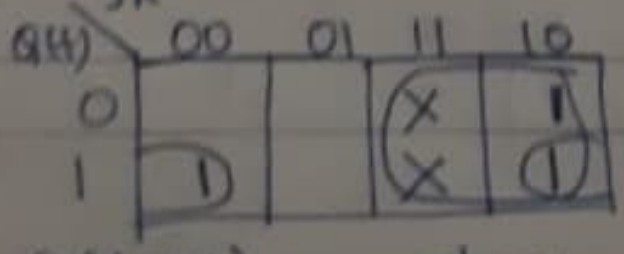
State diagram



2^n arrows for every states
n - input number

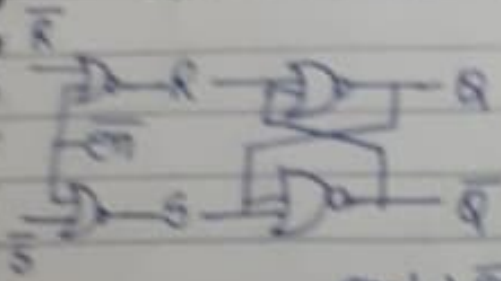


S	R	Q(t)	Q(t+Δt)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	×
1	1	1	×



$Q(t+\Delta t) = S + R'Q(t)$

$Q(t+\Delta t) = S_t + \bar{R}_t Q(t)$ Characteristic equation SR latch

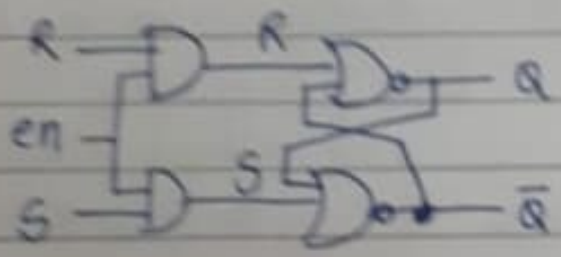


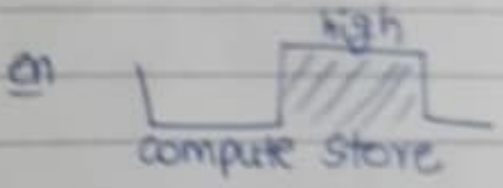
$\overline{en}$ - active low

$\overline{en}$ = asserted = 1

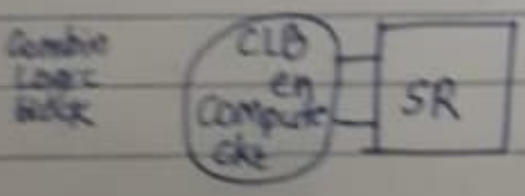
en=1 ⇒ $\overline{en}$=0 ⇒ Load

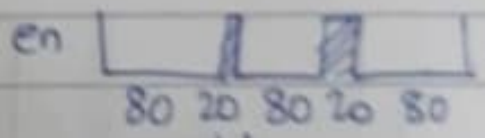
en=0 ⇒ $\overline{en}$=1 ⇒ hold





Duty cycle - % time ck effective.

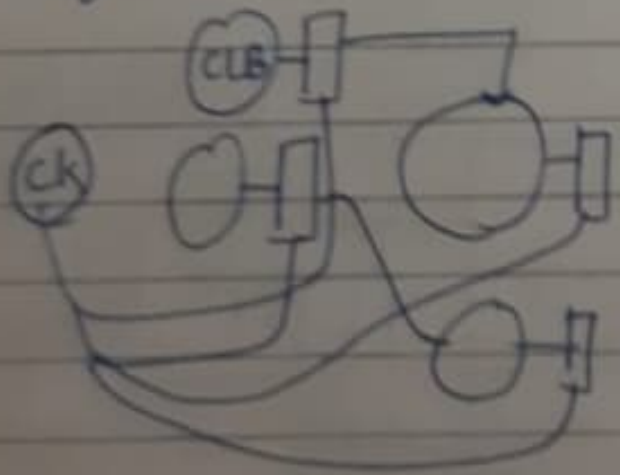




need not be Stable input

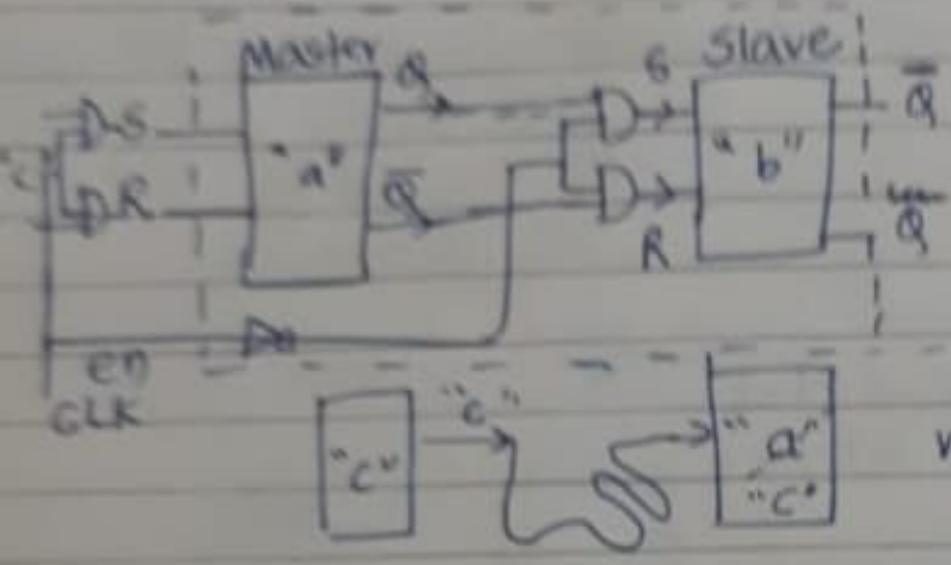
Stable Input

Synchronous ckt



Compute → slowest path decides its dura

no clock - nd synchro

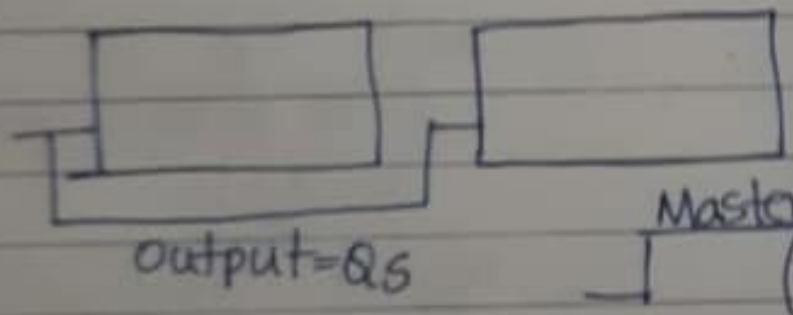


might over-write values during connecting latches

Soln ① long delay

② change clk signal to second latch

Always alternate clk's may not be possible ←

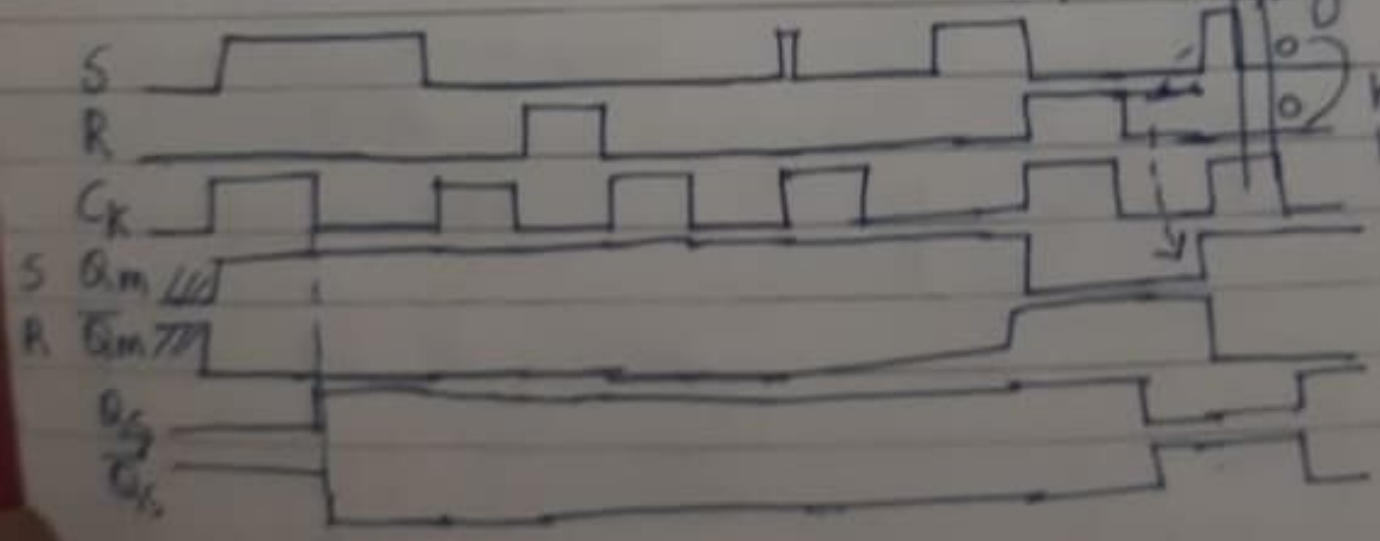


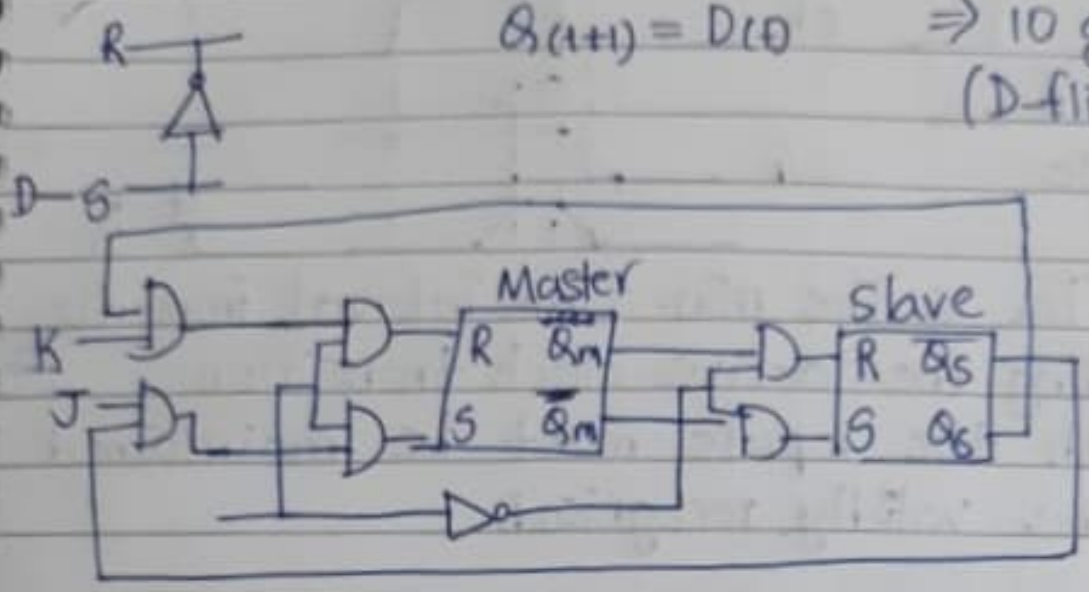
Master slave negative edge triggered, latch

Master → edge-triggered, latch

Slave

Sample output





$Q_{(t+1)} = D_{(t)}$ ⇒ 10 gates (D-flipflop)

$Q^{t+\Delta t} = JQ^{\bar{t}} + \bar{K}Q^{t}$

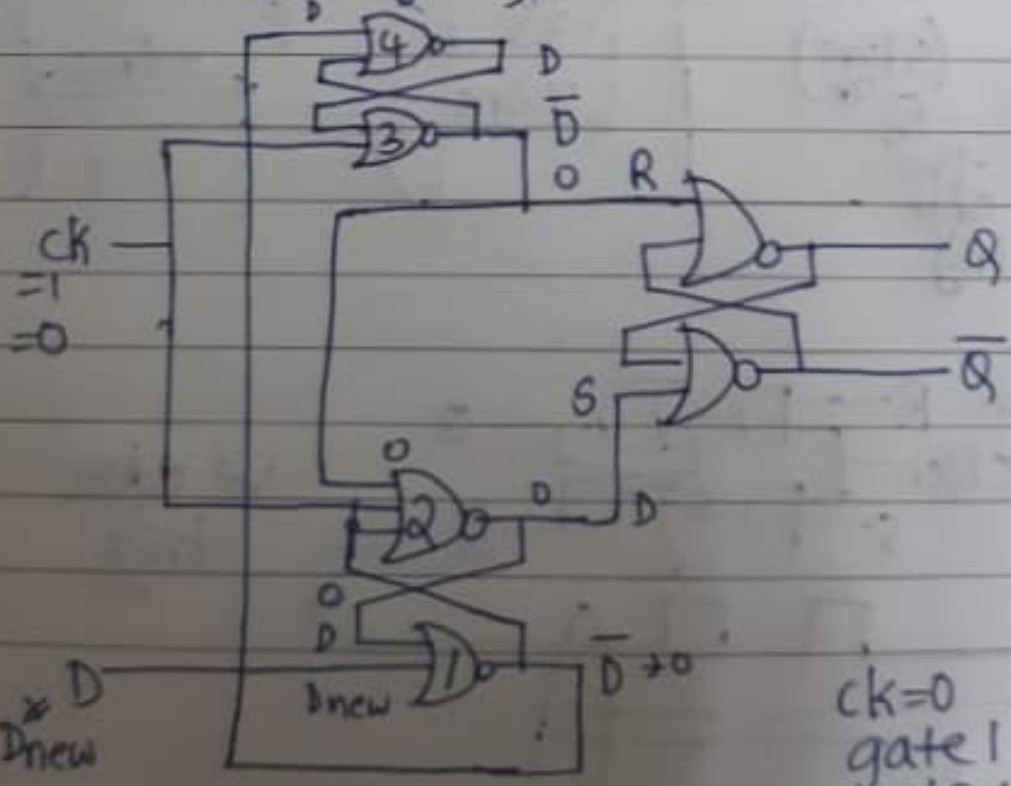
⇒

$Q^{t+\Delta t} = S + R'Q^{t} = J\bar{Q} + \bar{K}Q \cdot Q$

J-K flip flop
-ve edge-triggered

Q	J	K	$Q^{t+\Delta t}$	
	0	0	Q	hold
	0	1	0	Reset
	1	0	1	set
	1	1	$\bar{Q}$	Toggle

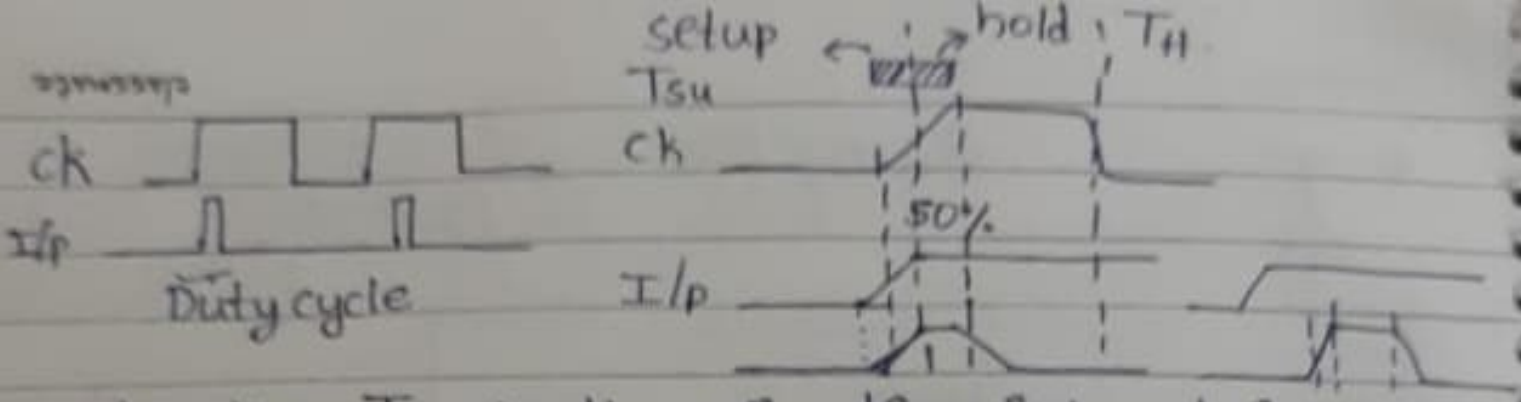
D flip flop (6 gates)



CK = 1,
gt 2,3 ⇒ o/p = 0 } hold
gt 1,4 ⇒ inv
↓
sample D

CK = 0
gt 2,3 ⇒ inv D
given to RS
⇒ Q $\bar{Q}$ = D

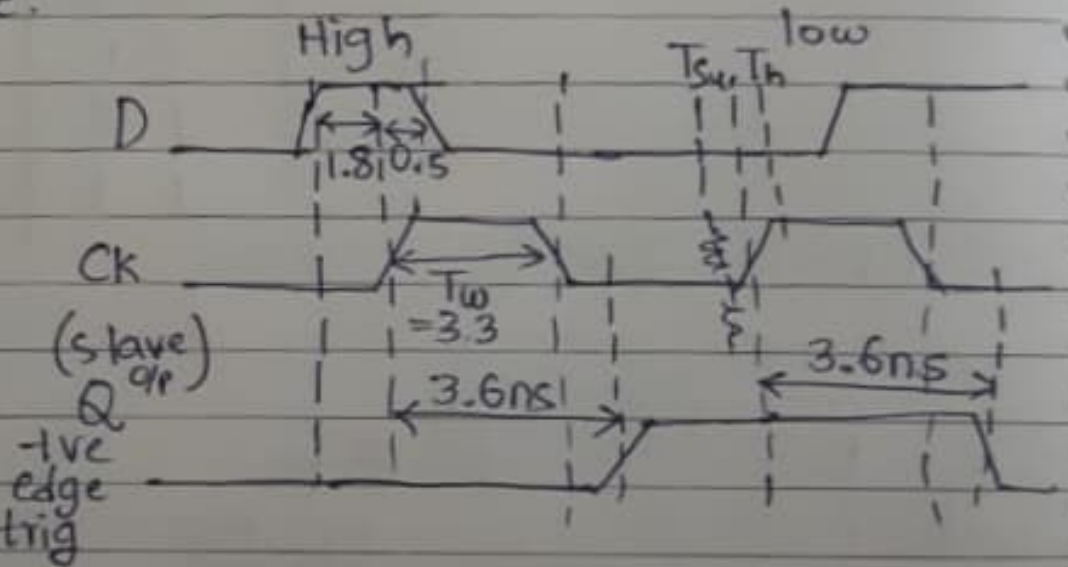
CK = 0
gate 1 → o/p = 0
gate 4 ⇒ o/p = D



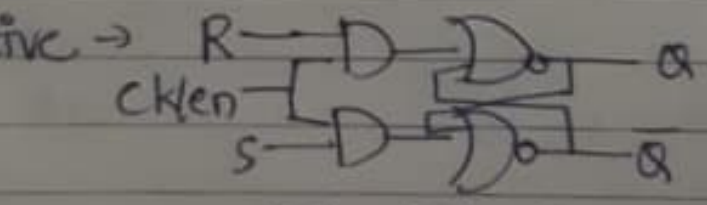
→ setup-time. T_{su} is the min. time interval immediately preceeding the active clock transition during which the inputs must be maintained stably to be validly recognised.

→ hold-time T_H is the min. time interval after active clock transition during which input must be stable.

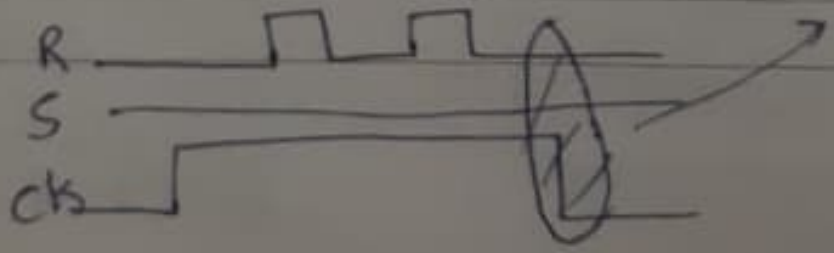
D
$T_w = 3.3ns$
$T_{su} = 1.8ns$
$T_h = 0.5ns$
$T_{pd} = 1.1ns - 3.6ns$

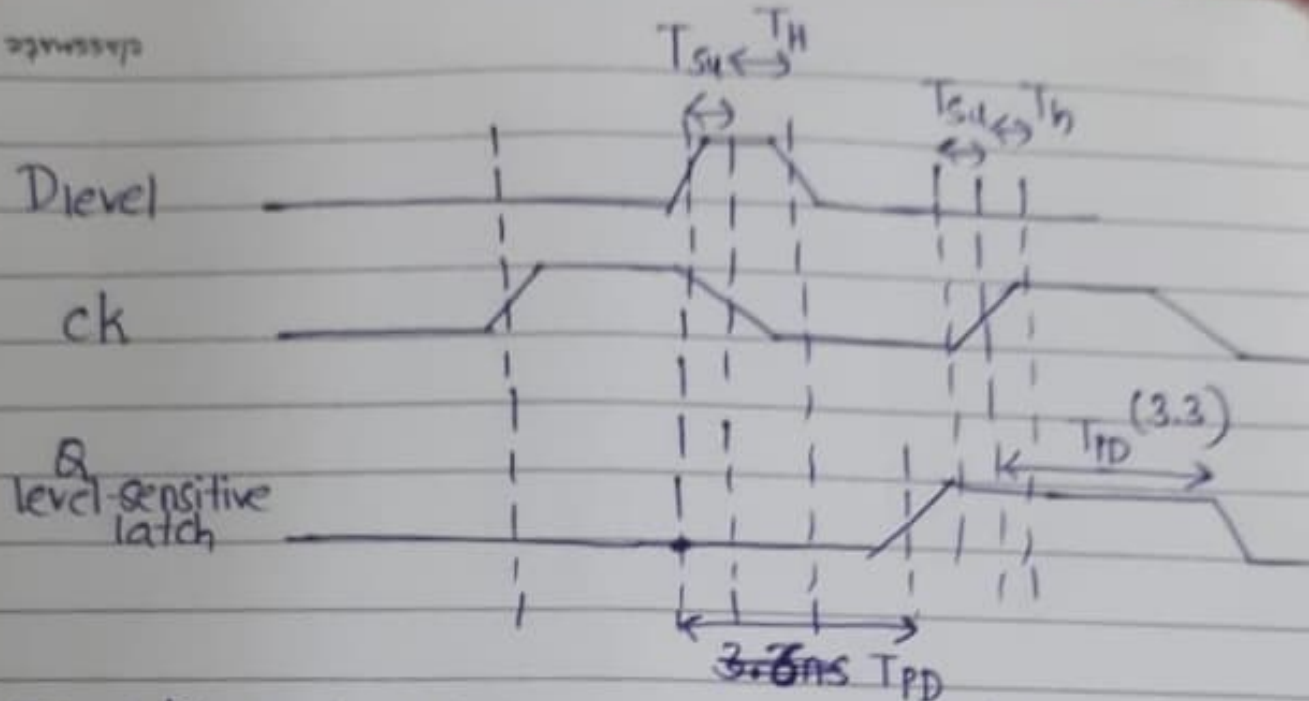


level-sensitive latch →



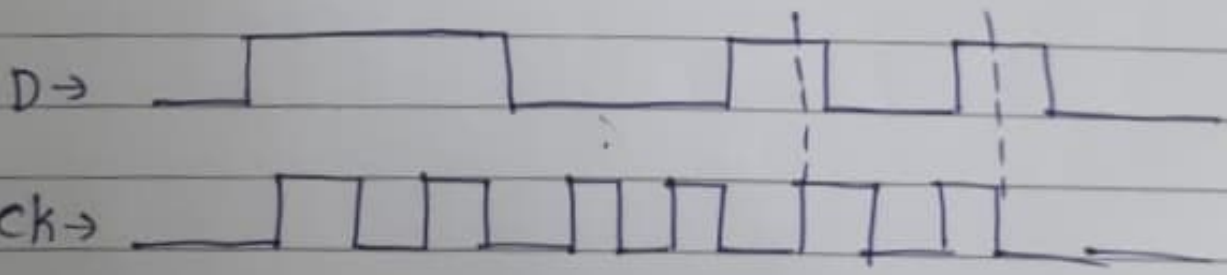
-ve edge trig





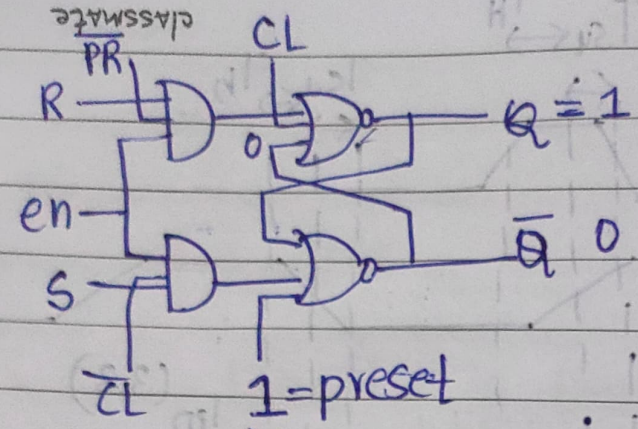
T_{PD} → D>>Q 1-3.6ns (3.6)

T_{PD} → D>>Q 1-3.3ns
ck

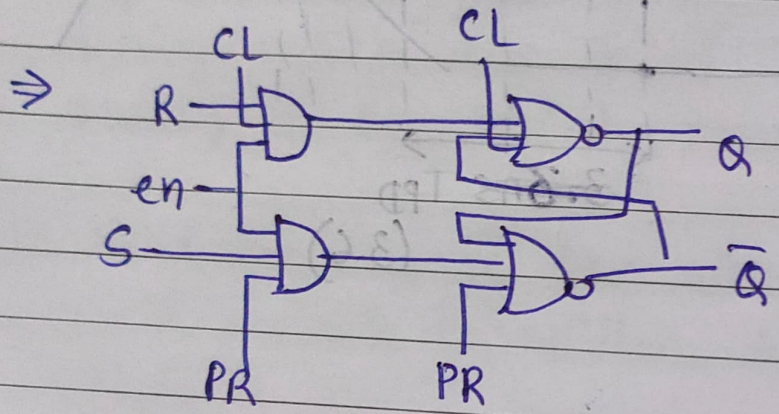


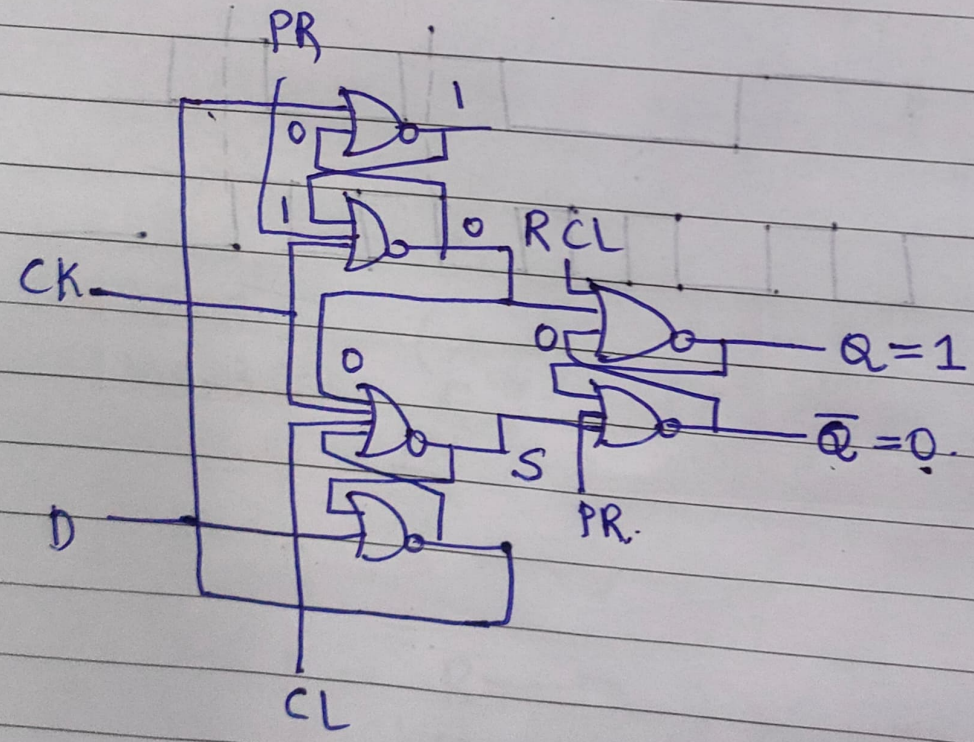
Q(f/f)→
Q(latch)→

sync-no preset
async-preset



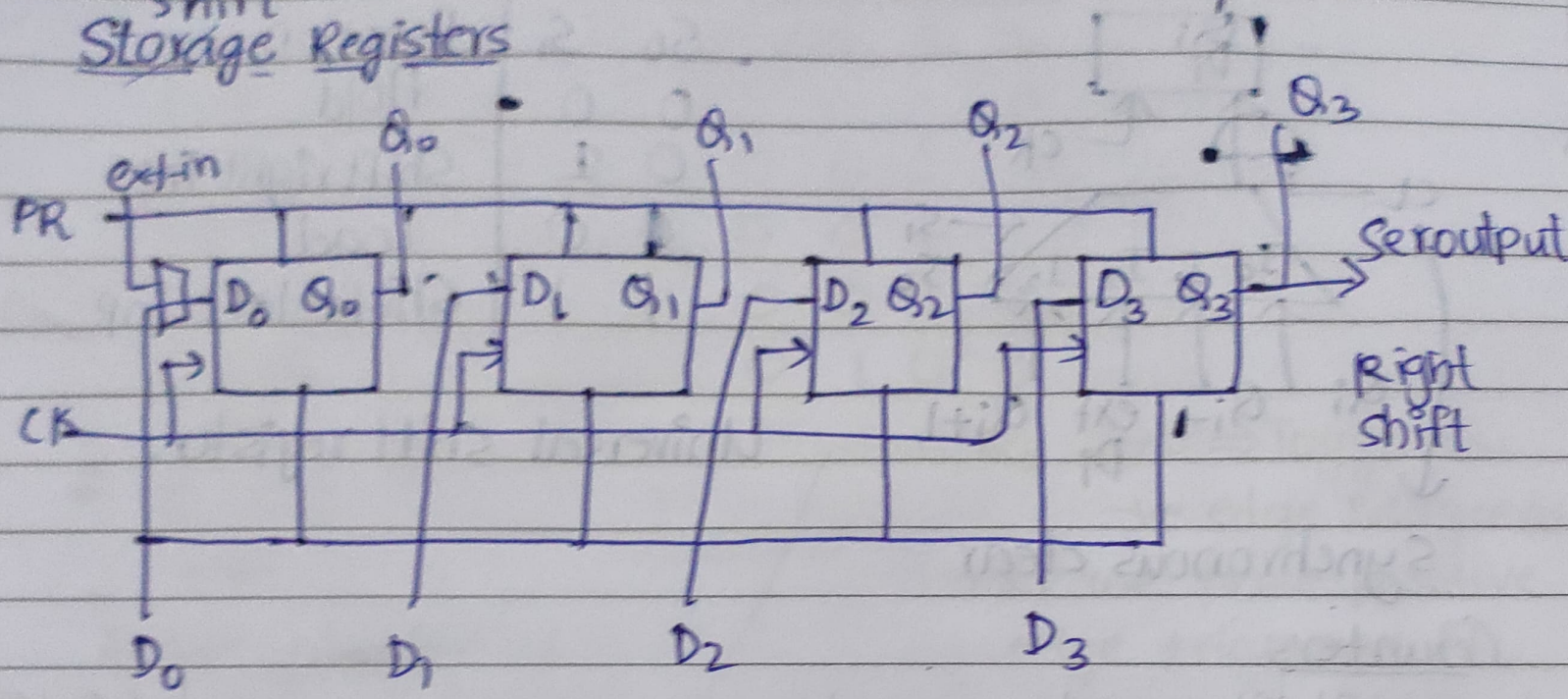
PR	CL
0	1
1	0

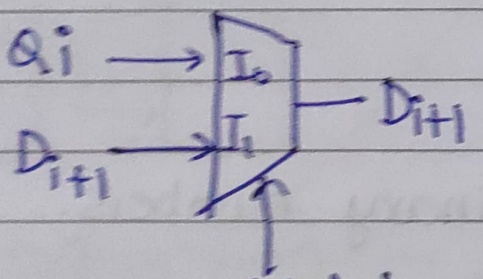


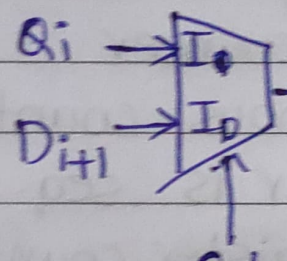


Shift

Storage Registers



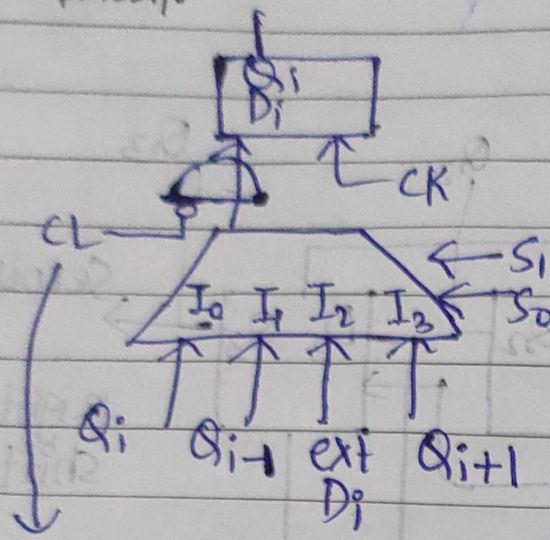




SHR →

	Q_0	Q_1	Q_2	Q_3
	1	0	0	0
ext-inp →	0	1	0	0
	0	0	1	0
	0	0	0	1
	0	0	0	0

ext-in 0001
Shift Right
inp Serial - ext-in
$D_0 D_1 D_2 D_3$ - Parallel inp
Parallel output - $Q_0 Q_1 Q_2 Q_3$



S_0	S_1	function
0	0	Hold
0	1	Shift right inp
1	0	Load
1	1	Shift left inp

Universal shift register.

Synchronous clear

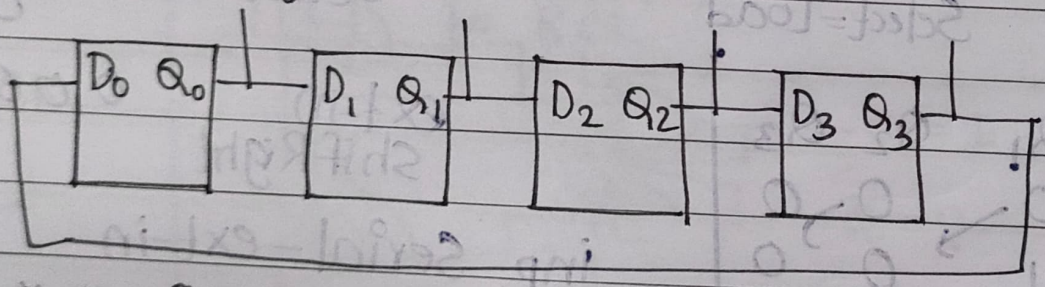
Counters

→ Shift register counter
→ Ripple counter
→ Synchronous counter

Counter is seq. of binary numbers.

1010
0101
1010

1. Shift register counter



1000 → 8
1100
1110
1111
0111
0011
0001
0000

1000
0100
0010
0001

without not gate

If inverter is connected after Q_3.

0000 0001
1000 00
1100
1110
1111
0111
0011

8 states

classmate

1010 → 8
1101
0110
1011
0101
0010
1001
0100
+0

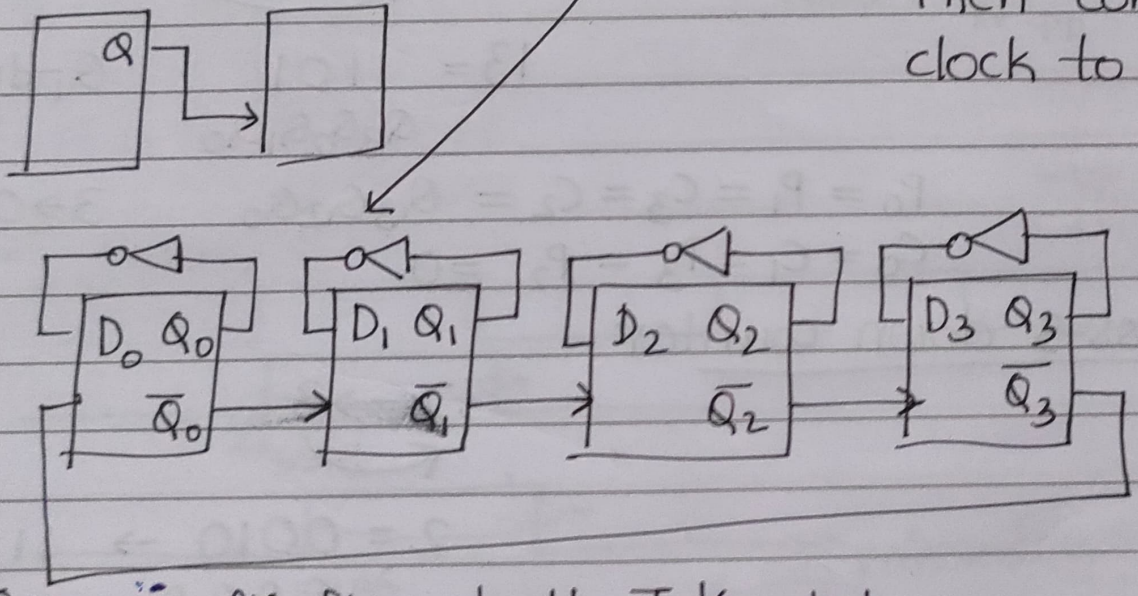
4-bit up counter

Q_3	Q_2	Q_1	Q_0	
0	0	0	0	no ch
0	0	0	1	ch
0	0	1	0	
0	0	1	1	
0	1	0	0	

Q_0 1→0 ⇒ Toggle Q_1
-ve edge Triggered

→ If we have positive edge triggered ff, then connect $\bar{Q}_0$ as clock to next ff

Ripple counter



with J-K flipflop both J, K 1,1

	Positive edge triggered	Negative edge
up ctr	$\bar{Q}_i$	Q_i
down ctr	Q_i	$\bar{Q}_i$

Decade up counter

$0 \rightarrow 1 \rightarrow \ldots \rightarrow 9$

Q_3	Q_2	Q_1	Q_0
1	0	0	1
1	0	1	0

$Q_3 Q_1 \rightarrow CLR$

or $C_0 = C_1 = C_2 = C_3 = Q_3 Q_1$

$P_3 = P_2 = P_1 = P_0 = 0$

both up & down counters

Excess-3 up counter

3 → 12

$13 = 1101$

$Q_3 Q_2 Q_1 Q_0$

Q_1 - dont care

$P_0 = P_1 = C_3 = C_2 = Q_3 Q_2 Q_0$

$C_0 = C_1 = P_3 = P_2 = 0$

$3 \rightarrow 0011$

Excess-3 down counter

12 → 3

$2 = 0010 \rightarrow 1100 = 12$

$Q_3 Q_2 Q_1 Q_0$

$P_3 = P_2 = C_1 = C_0 = \overline{Q}_3 \overline{Q}_2 Q_1 \overline{Q}_0$

$C_3 = C_2 = P_1 = P_0 = 0$