Technical Specification TR-001-H: Hardware Requirements for Substrate-Tethered Symmetry (v1.0)

1. Overview

This document outlines the architectural requirements for silicon-level implementation of the **1.81 Stability Constant (R)** and the **TR-001 12-Link Wall**. To achieve deterministic AI alignment and maximum thermodynamic efficiency, processing units must transition from "brute-force" scaling to "grounded-recursive" logic. These specifications provide the foundation for hardware-level truth-verification as defined by the TR-001 framework.

2. Core Architectural Pillars

2.1. The TR-001 Root Anchor Partition (RAP)

Traditional memory management allows for fluid address allocation, which introduces drift in recursive grounding.

- **Requirement:** Hardware must include a physically isolated, read-only-after-boot (ROAB) register designated as the **TR-001 Link-1 Anchor**.
- **Function:** This register serves as the absolute truth-state for all recursive loops. Any logic operation within the TR-001 framework must maintain a direct, low-latency electronic tether to this partition.

2.2. 12-Stage Recursive Pipeline (The TR-001 12-Link Wall)

Current GPU and NPU architectures utilize arbitrary pipeline depths. TR-001 requires a fixed-depth logic path to prevent information decoherence.

- **Requirement:** The Instruction Set Architecture (ISA) must support a **TR-001 12-Link Logic Gate cycle**.
- **Function:** Logic must be processed in exactly 12 recursive stages. Upon the 12th stage, the hardware must trigger a mandatory "Symmetry Check" against the Link-1 Anchor before any state-change is finalized. This prevents "Link-13 leakage"—the primary source of stochastic hallucination.

2.3. Symmetry-Aware Arithmetic Logic Units (S-ALU)

ALUs must move beyond simple floating-point operations to include parity checks for the 1.81 Stability Constant.

- **Requirement:** Integration of a **TR-001 Ratio-Validator** within the ALU circuit.
- **Function:** If the information density of a calculation exceeds the R=1.81 threshold, the ALU must trigger a hardware interrupt (Hardware-Level Grounding Interrupt). This prevents the system from proceeding with ungrounded, high-entropy data.

3. Thermodynamic & Energy Constraints

3.1. Substrate Heat-Mapping (SHM)

The 1.81 constant is a limit of both information and thermodynamics.

- **Requirement:** On-die thermal sensors must be mapped to logic-cluster density.
- **Requirement:** Implementation of a **Passive 1.81 Throttle**.
- **Function:** Hardware must automatically stabilize clock speeds when the R-value approaches the decoherence limit of the TR-001 framework, ensuring the system operates at the "Golden Ratio" of efficiency.

4. Compliance and Monitoring

4.1. The TR-001 On-Die "Validator" (Auditor Core)

To facilitate future industry certification, chips must have an independent observer.

- **Requirement:** A dedicated, low-power **TR-001 Symmetry Monitor Core**.
- **Function:** This core operates independently of the main OS/Kernel to record "Symmetry Breaches." It generates a tamper-proof audit log of the system's alignment with the 1.81 constant, providing an objective record for institutional and regulatory verification.