Assignment 7a - Cache Basics

04/12/2024

Missing **0/30** Points

Attempt 1 Review Feedback

Offline Score: **0/30** Add Comment

Anonymous Grading: **no**

Unlimited Attempts Allowed

Details

Complete the following exercises from the reference book Chapter 5.

5.2 Caches are important to providing a high-performance memory hierarchy to processors. Below is a list of 32-bit memory address references, given as word addresses.

3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253

- 5.2.1.

  For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

- 5.2.2.

  For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with two-word blocks and a total size of 8 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

- 5.2.3.

  You are asked to optimize a cache design for the given references. There are three direct-mapped cache designs possible, all with a total of 8 words of data: C1 has 1-word blocks, C2 has 2-word blocks, and C3 has 4-word blocks. In terms of miss rate, which cache design is the best? If the miss stall time is 25 cycles, and C1 has an access time of 2 cycles, C2 takes 3 cycles, and C3 takes 5 cycles, which is the best cache design?

Record your answers and upload as a Word doc, Excel spread or PDF file.

View Rubric

Assign 10a - Cache Basics

Criteria	Ratings	Pts
Q 5.2.1		/ 12 pts
Q 5.2.2		/ 12 pts
Q 5.2.3		/ 6 pts
		Total Points: 0

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