EE213 (Fall 2018)

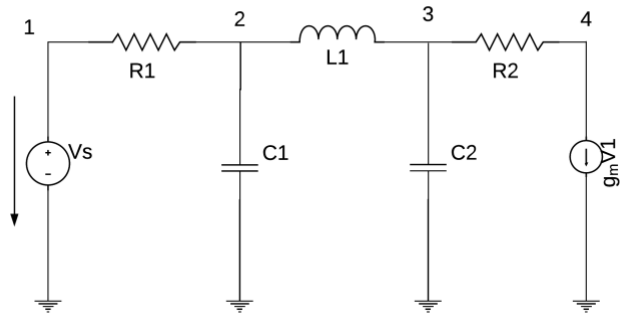
Homework 2

1) For the following circuit, where $g_m V1$ is voltage controlled current source, which is controlled by the voltage at node 1.

   (a) Drive the MNA equation using the element stamp method (or the brutal force method starting with KCL law) in the frequency domain.

   (b) Write the MNA equation in the time domain

   (c) Write the MNA equation in the Gx + Cdx/dt = Bu in the frequency domain, where G and C are conductance and reactive matrices and B is the input matrix, *x* and *u* is state and input source vectors.



2) For the following nonlinear circuit with one NMOS FET and one diode,
   (a) Write the MNA equation in the time domain

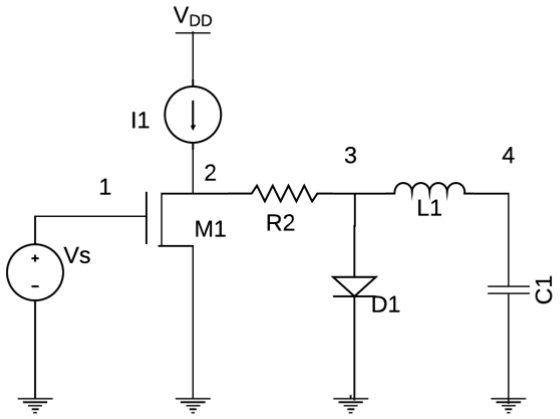
   (b) Assume that R2 = 1, C1 = 1, L1 = 1, Vs = 2, W=L, K = 1, $\alpha = 10$, time step h =1, V_t = 0.5 and I1 = 1A for the NMOS FET, perform the Newton Raphson iteration for the first step (k=1) and compute all the node voltage of the circuit after one-time step. Assume at t =0, the node voltages, V_2 =1V, $V_3 = V_4 = 0$ and V_1 = Vs.

   The equation for the I_{ds} for NMOS FET M1, working in the linear region, is defined as

$$I_{ds} = \frac{W}{L} K[(V_{gs} - V_t)V_{ds} - \frac{1}{2}V_{ds}^2]$$

   The diode equation for D1 is given below

$$I_d = e^{\alpha V} - 1$$



3) Let x’ = -x + t, use the Forward Euler, Back Euler and Trap methods respectively to compute the solution for two steps. The time step h = 0.1, X(t=0) = 1.