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Roll No:

MCA(Integrated) (SEM II) THEORY EXAMINATION 2021-22 COMPUTER ORGANIZATION

·	COMPUTER ORGANIZATION
Time:	3 Hours Total Marks: 70
	Attempt all Sections. If require any missing data; then choose suitably.
١.	Attempt all questions in brief. SECTION A $2x7 = 14$
	a. Explain the difference between clock eyele and clock frequency.
	b. Explain about Arithmetic and Lovic Unit
	C. What is bus arbitration?
	d. Define RISC.
	e. Discuss the principle operation of miero programmed control unit. (i) What is the need for DMA transfer?
	g. Define HIT and MISS ratio in memory with an example?
2.	Attempt any three of the fellow SECTION B
	with a general block diagram eval.
	b. Discuss various techniques used for Modes of Transfer?
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	u. Differentiate synchronous and asynchronous communication?
	e. Explain 2D and 2-1/2 D organizations with their merits and demerits.
3.	Attempt any one part of the following: a. What is bus arbitration problem? Explain the four schemes for bus master and slave. b. Design 4-bit combinational circuit using 4 full adders.
4.	Attempt any one part of the following: 7x1 = 7
	a. Explain Micro instruction Format in detail.
	b. Explain about address sequencing in control memory with neat diagrams?
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5,	Attempt any one part of the following: 7x1 = 7
	a. Sketch the internal organization of CPU out with its functionalities and block diagram •
	b. What do you mean instruction cycle? How is instruction executed? Explain the interrupt cycle with an example.
6.	Attempt any one part of the following: $7x1 = 7$
	a. Describe the Input-output subsystem organization and interfacing
	b. Give the block diagram of DMA controller? Why are the read and write control lines in
	a DMA controller bidirectional? Under what condition and for what purpose they are
	used as inputs? Under what conditions and for what purpose are they used as outputs?
7.	Attempt any one part of the following: 7x1 = 7
	a. What are the different mapping schemes deployed in virtual memory and explain?
	b. A digital computer has a memory unit of 64K*16 and a cache memory of 1K words. the cache memory uses direct mapping with a block size of four words.
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	address format?
	at the stable can accommodate?
	ii. How many blocks eache can accommodate. How many bits are there in each word of the cache? Include a valid
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