

IC Layout using L-EDIT with its simulation using T-Spice

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Why use L-edit?

- ❖ L-Edit is a freeware and is very useful for academic purposes
- ❖ Though industry uses Cadence, L-Edit can illustrate the significant points for laying out CMOS circuits. Cadence is rather complex in comparison.
- ❖ L-Edit can be used to extract parasitic capacitance which enables us to predict the delay in CMOS circuits.



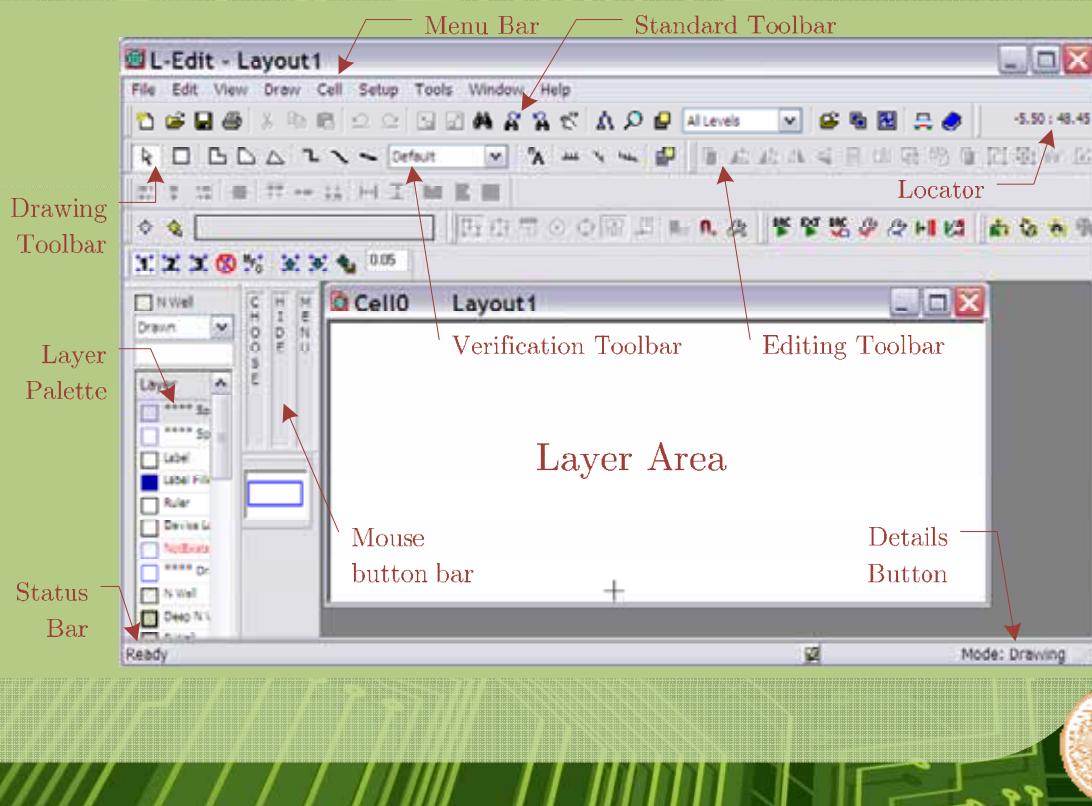
DOWNLOAD INSTRUCTIONS

- The materials about L-Edit (Handout, Spice models , etc.) can be found in Dr Pipat Prommee's website.
<http://www.kmitl.ac.th/~kppipat>
- L-Edit Pro student version. You can also download L-Edit from
<http://www.tannereda.com/long-form>

Setup

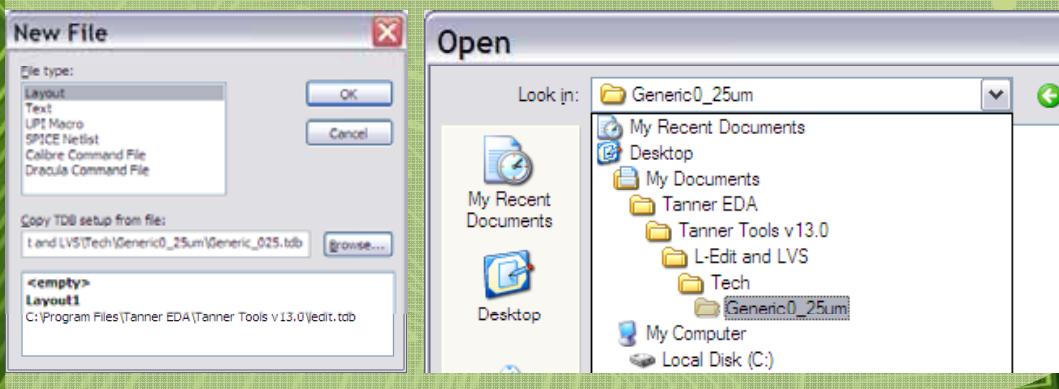
- This version must run in 256 colors.
- For Windows XP users, set the display by right clicking the short cut created for L-edit and choosing properties.
- Then click the compatibility tab. Under display settings click 256 colors.
- Open L-edit

L-EDIT Windows

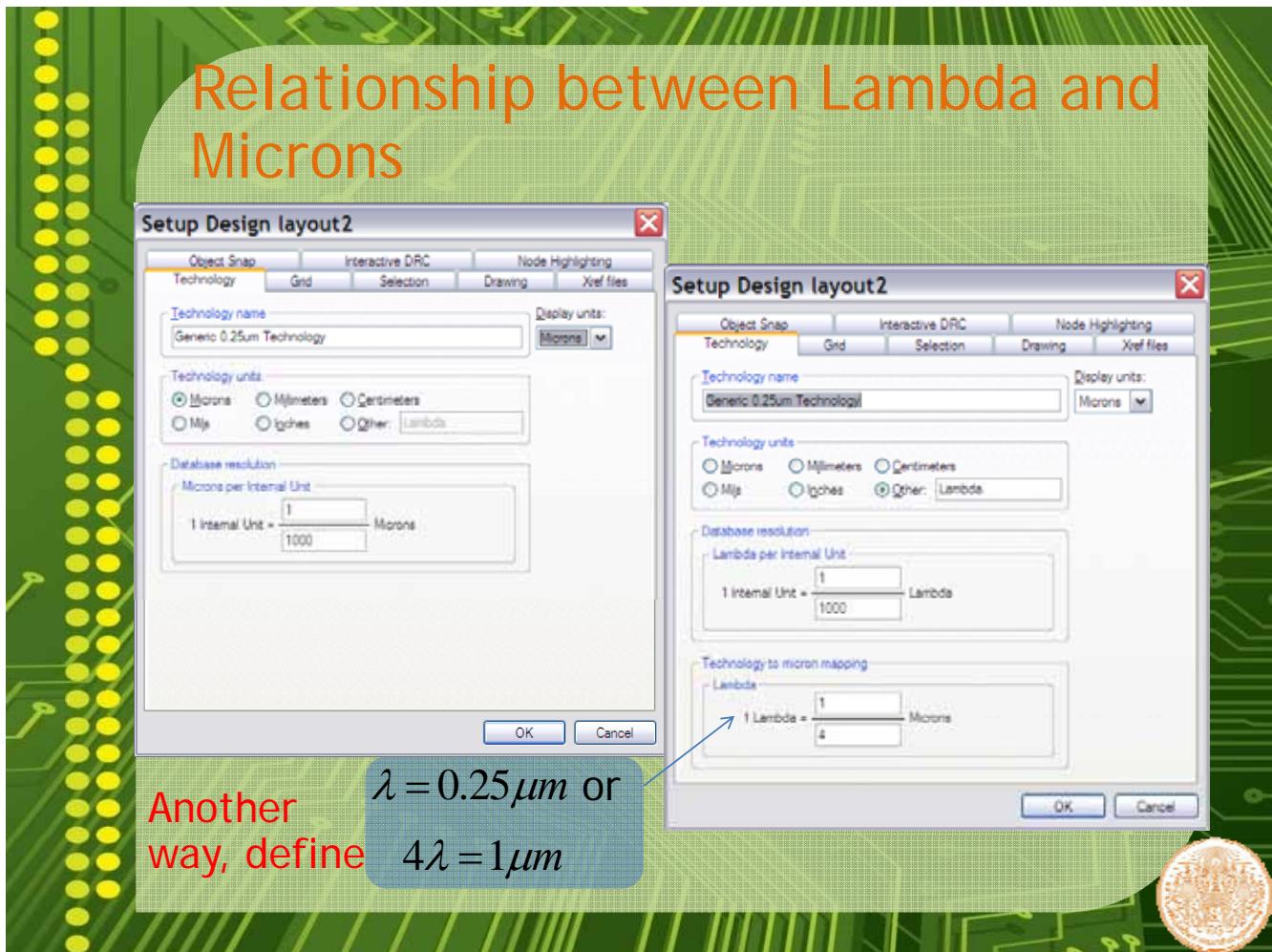


Drawing Layout

- Create new Layout file
 - File > New.
 - In the following open window, Browse and choose ‘Generic_025.tdb’ in ‘Copy TDB setup from file’ area. It usually locates in \My Documents\Tanner EDA\Tanner Tools v13.0\L-Edit and LVS\Tech\Generic0_25um\.



Relationship between Lambda and Microns

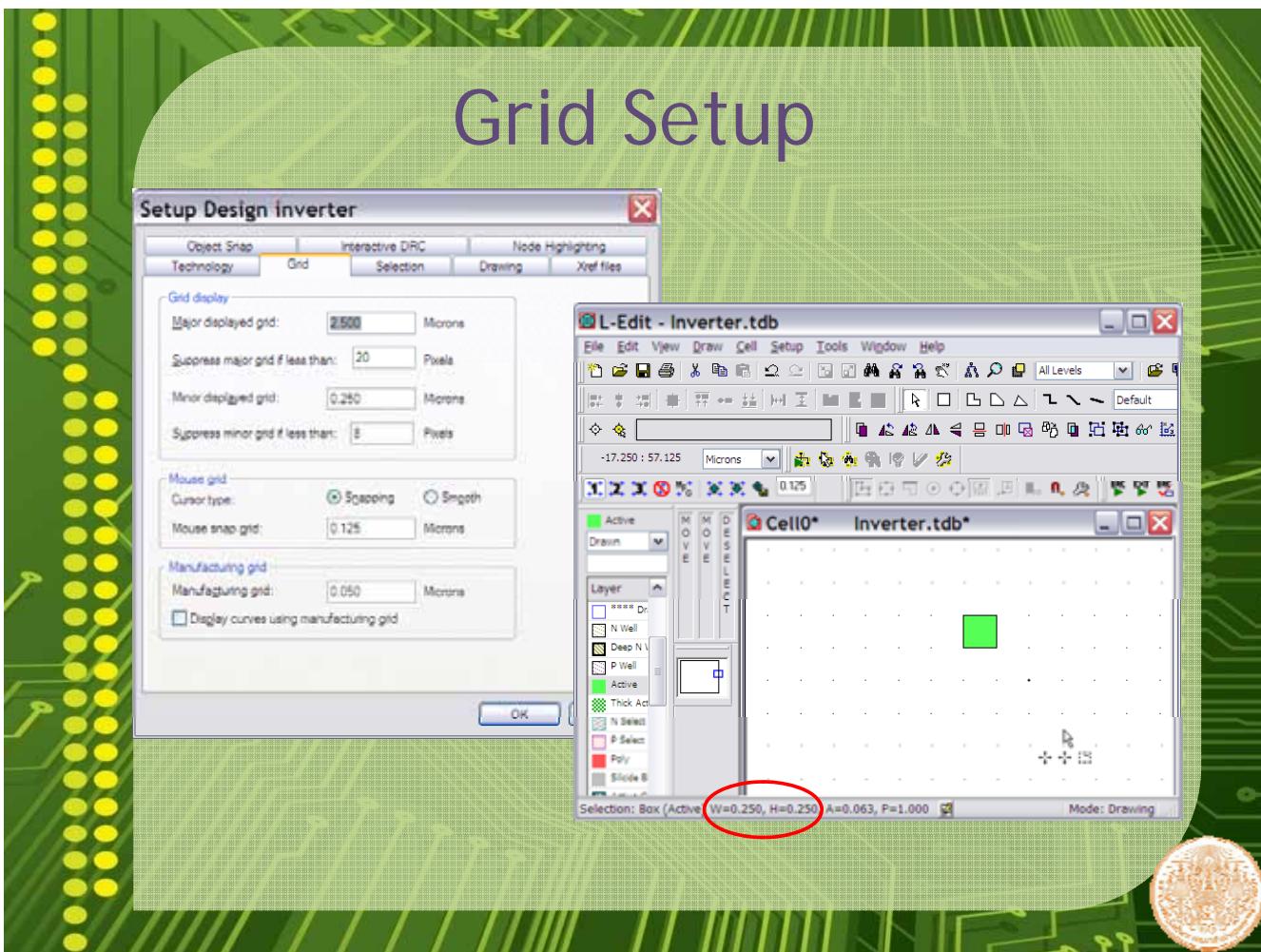


To establish GRID

- Zoom the window to see grid
- Distance between grid points is $1 \mu\text{m}$
- In order to set mouse snap to Grid :
 - Click Setup -> Design
 - Click on the Grid tab
 - Set Mouse snap grid to 1 locator unit

Now the technology is setup!

Grid Setup



Inverter Layout

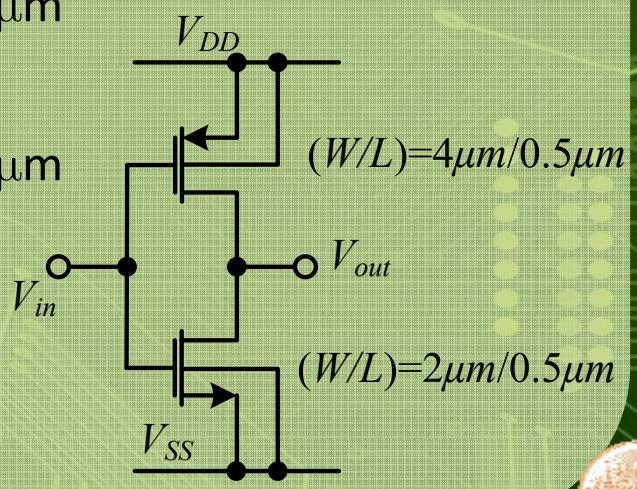
- Layout Specifications:

NMOS:

- $L = 0.5 \mu\text{m}$, $W = 2 \mu\text{m}$

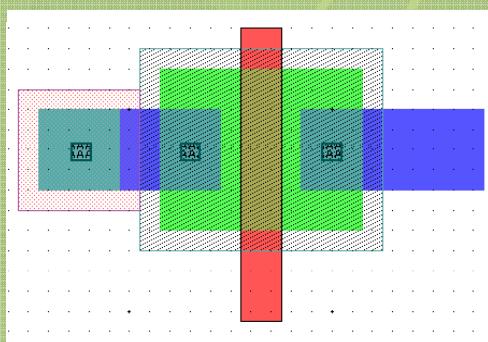
PMOS:

- $L = 0.5 \mu\text{m}$, $W = 4 \mu\text{m}$

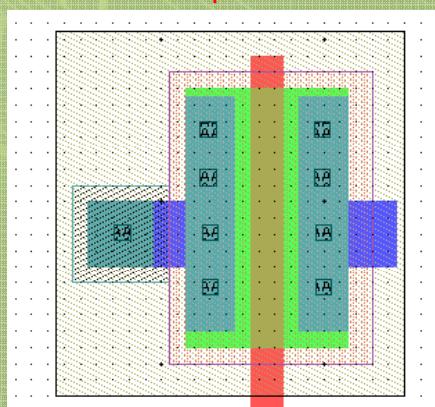


NMOS and PMOS

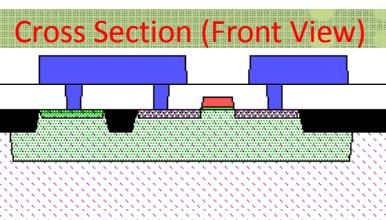
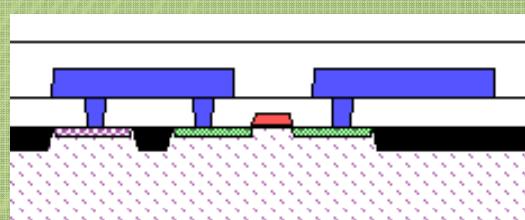
Top view



Top view

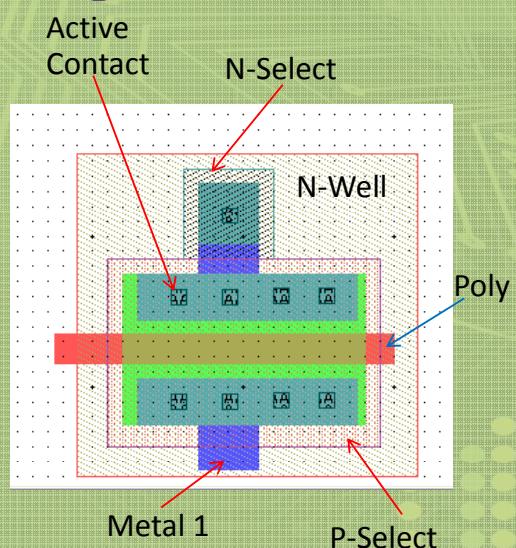


Cross Section (Front View)



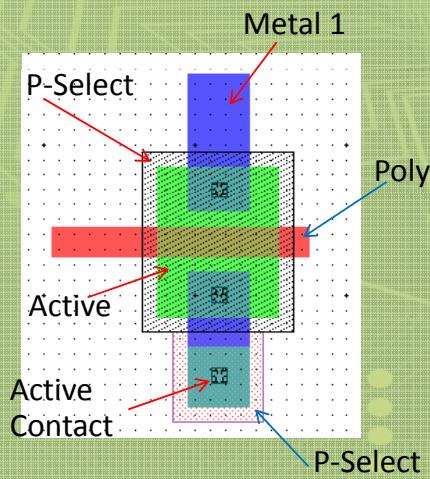
PMOS Design

- Choose N-Well in the left palette and draw a box.
- In the N-Well area, draw P-Select. Notice that the size and position should obey Design Rule, which can be found at http://www.mosis.org/Technical/Layermaps/lm-scmos_scnpc.html.
- With the help of DRC button , the violation of design rule can be shown by right clicking the place which is highlighted. It is a good idea to run DRC at each stage of your design so that you can fix any error along the way
- Draw Active.
- Draw Poly.



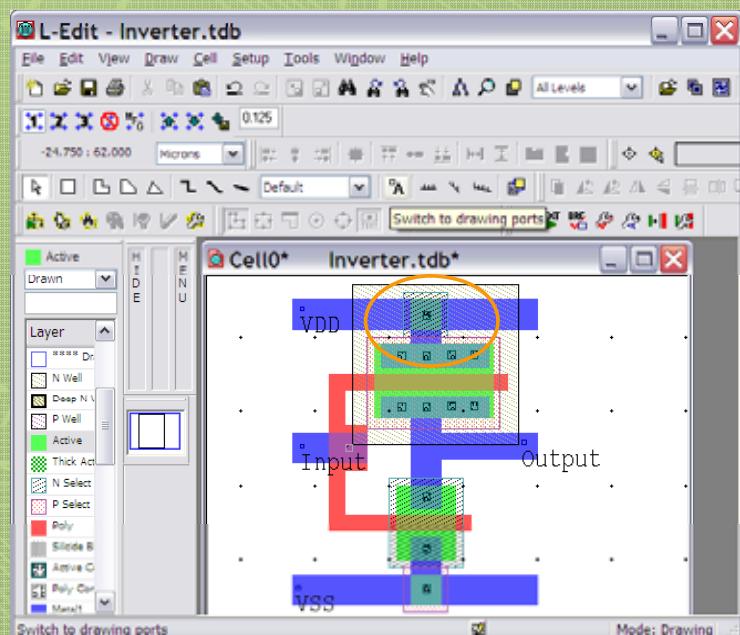
NMOS Design

- Do not need to draw P-Well because the empty grid of L-Edit stands for P-Well.
- Draw N-Select.
- Draw Active.
- Draw Poly.



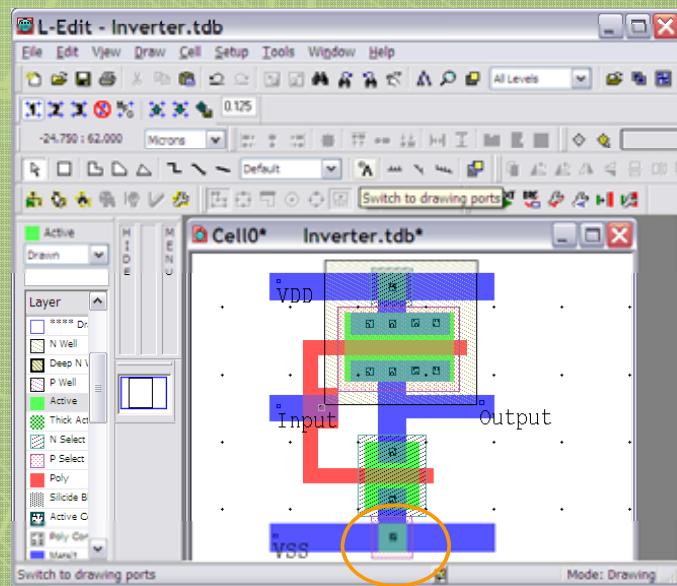
Connects P-Substrate

- For PMOS, place a small N-Select on the N-Well, add a small Active layer. From this active layer put contacts to the Metal1 layer that connects to VDD.



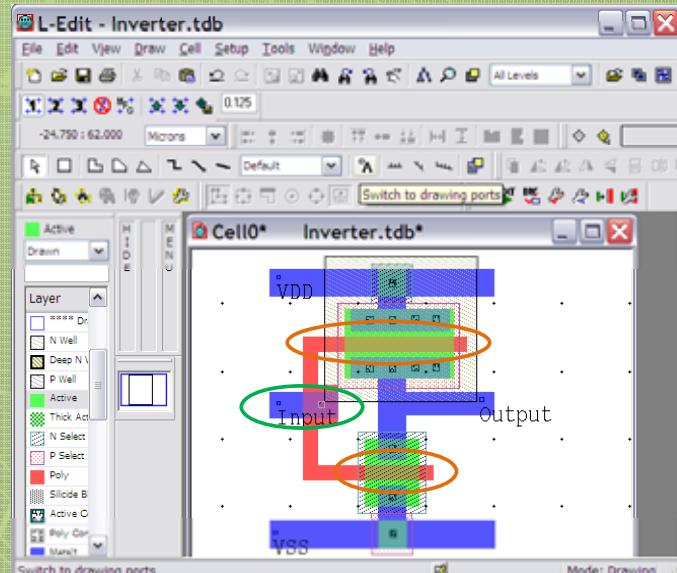
Connects N-Substrate

- For NMOS, on the P-substrate, place a small P-Select and then Active layer. From this active layer put contacts to the Metal1 layer that connects to VSS.



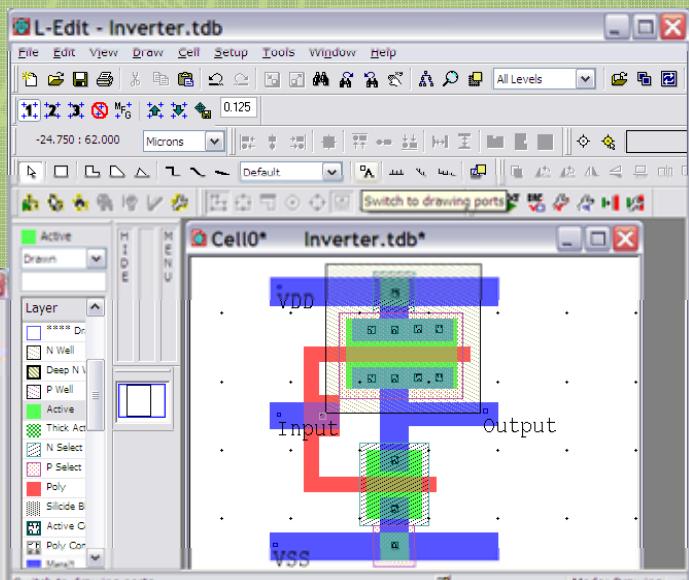
Connect Poly and Metal

- Connect Poly of PMOS and NMOS for input.
- Add an input connect between Metal1 and Poly.
- Connects poly and Metal1 by using 'Poly Contact' at input.
- Connect source of PMOS to VDD by Metal1.
- Connect source of NMOS to VSS by Metal 1.
- Connect Drain of PMOS and NMOS by Metal 1.



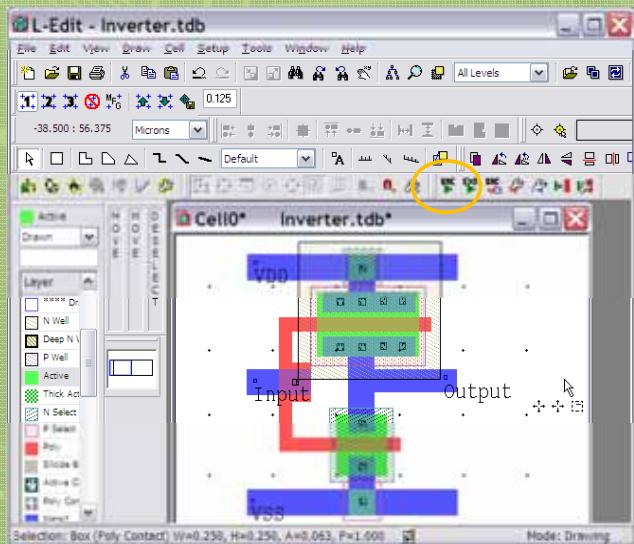
Connects port names

- Using 'Switch to Drawing Port' button
- Assigned port name of different ports, VDD, VSS, Output, Input



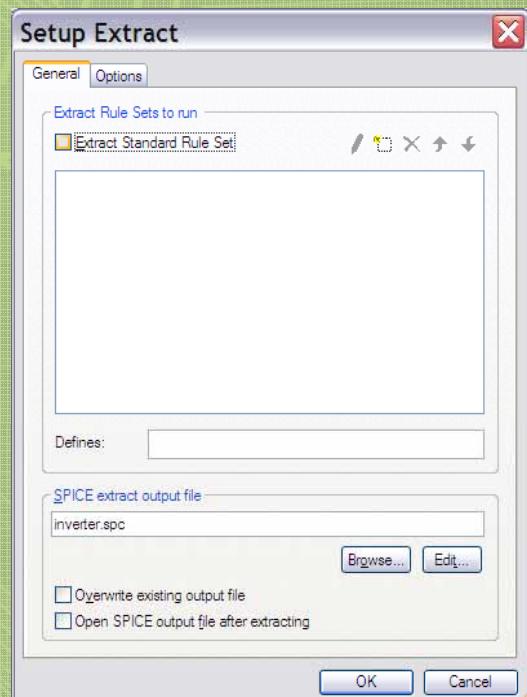
Design Rule Check (DRC)

- Click Tools -> DRC (or the DRC box in the toolbar)
- Run DRC for the total layout.
- Click the Write errors to file box, and give a descriptive filename
- Fix the errors listed.
- Once there is no DRC error shown, the layout is ready to be extracted.



Extract Data for Simulate

- Press Menu Tool>Extract Setup
- Uncheck ‘Extract Standard Rule Set’
- Browse and choose folder for locate the output data.
- Set file name ‘inverter.spc’
- Check ‘Extract Standard Rule Set’ and press ‘OK’



MOSIS TSMC 0.25um Level49 (mosis025.md)

```

* DATE: May 21/01
* LOT: T14Y          WAF: 101
* Temperature_parameters=Default
.MODEL NMOS NMOS (           LEVEL = 49
+VERSION = 3.1      TNOM = 27      TOX = 5.8E-9
+XJ = 1E-7      NCH = 2.3549E17   VTH0 = 0.3877332
+K1 = 0.4503218   K2 = 7.498548E-3   K3 = 1E-3
+K3B = 2.7511903   W0 = 1E-7      NLX = 2.684962E-7
+DVTOW = 0        DVT1W = 0       DVT2W = 0
+DVT0 = 0.4948826   DVT1 = 0.5924031   DVT2 = -0.5
+U0 = 300.237024   UA = -1.207596E-9   UB = 2.358208E-18
+UC = 2.411595E-11   VSAT = 1.423302E5   A0 = 1.4820567
+AGS = 0.2493074   BO = 2.000837E-7   B1 = 3.568634E-6
+KETA = 9.120027E-4   A1 = 3.802033E-5   A2 = 0.4500971
+RDSW = 117.272191   PRWG = 0.5      PRWB = -0.2
+WR = 1        WINT = 0       LINT = 4.377598E-9
+XL = 3E-8      XW = -4E-8     DWG = -2.290208E-8
+DWB = 5.476111E-9   VOFF = -0.0948739   NFACTOR = 1.9975727
+CIT = 0        CDSC = -2.4E-4    CDSCD = 0
+CDSCB = 0       ETA0 = 4.108112E-3   ETAB = 8.333134E-4
+DSUB = 0.0311455   PCLM = 1.8275359   PDIBLC1 = 0.9990847
+PDIBLC2 = 4.688174E-3   PDIBLCB = -0.0999829   DROUT = 0.8506408
+PSCBE1 = 7.991332E10   PSCBE2 = 5.16406E-10   PVAG = 0.0099971
+DELTA = 0.01      RSH = 4.4      MOBMOD = 1
+PRT = 0        UTE = -1.5     KT1 = -0.11
+KT1L = 0        KT2 = -0.022    UA1 = 4.31E-9
+UB1 = -7.61E-18   UC1 = -5.6E-11   AT = 3.3E4
+WLN = 0        WLN = 1       WW = 0
+WVN = 1        WWL = 0       LL = 0
+LLN = 1        LW = 0       LWN = 1
+LWL = 0        CAPMOD = 2     XPART = 0.5
+CGDO = 6.14E-10   CGSO = 6.14E-10   CGBO = 1E-12
+CJ = 1.753617E-3   PB = 0.99      MJ = 0.4591946
+CJSW = 4.328986E-10   PBSW = 0.99      MJSW = 0.3552107
+CISWG = 3.29E-10    PBSWG = 0.99      MJSWG = 0.3552107
+CF = 0        PVTH0 = -0.01     PRDSW = -10
+PK2 = 2.428891E-3   WKETA = 0.0103867   LKETA = -7.732829E-3 )

```

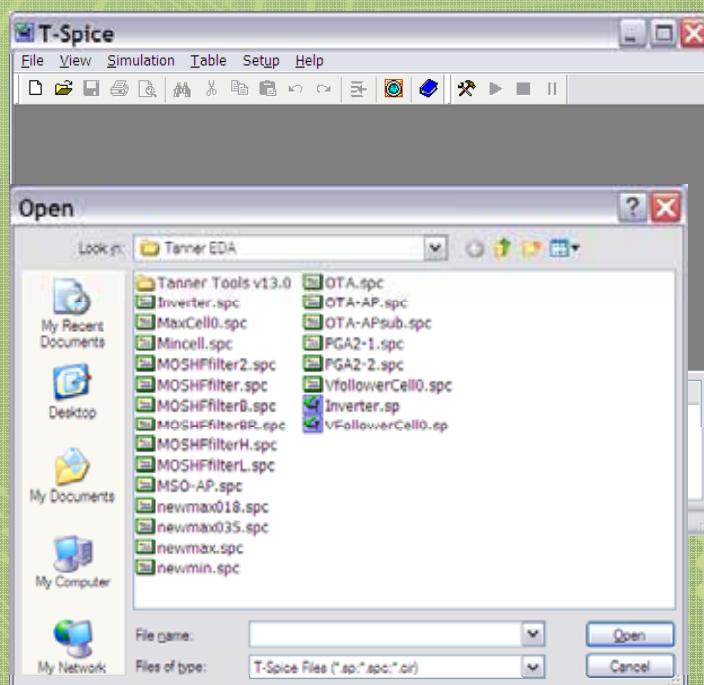
Add Model file

- Click icon ‘pencil’ on Setup Extract Dialog
- Go to Output tab and type used MOSIS model ‘.INCLUDE mosis025.md’ in SPICE include statement then press ‘OK’
- Finally, Press Menu Tool>Extract



T-Spice Simulation

- Open T-spice Program
- Open Menu File> open
- Select file ‘Inverter.spc’ which was previous extracted.



Simulations using T-Spice

- File 'Inverter.spc' is open.
- Transistor M1 and M2 are created with the values, W, L and parasitic elements based on your individual design
- At drain, source of transistor are named as port labels.

The screenshot shows the T-Spice software interface with the file 'Inverter.spc' open. The window title is 'T-Spice - Inverter.spc'. The menu bar includes File, Edit, View, Simulation, Table, Setup, Window, Help. The toolbar has various icons for simulation types like AC, DC, and transient analysis. The main pane displays the SPICE code:

```
* Extract Definition File: Generic_025.ext
* Extract Date and Time: 02/12/2011 - 23:01
.INCLUDE mosis025.md

* NODE NAME ALIASES
*   1 = Output (-23 , 56.375)
*   2 = VDD (-30.5 , 60.875)
*   3 = Input (-30.5 , 56.25)
*   4 = VSS (-30.625 , 51.5)

M1 Output Input VDD VDD NMOS L=500n W=4u AD=4p PD=10u AS=4p PS=
M2 VSS Input Output VSS VSS NMOS L=500n W=2u AD=2p PD=6u AS=2p PS=6

* Total Nodes: 4
* Total Elements: 2
* Total Number of Shorted Elements not written to the SPICE file: 0
* Output Generation Elapsed Time: 0.031 sec
* Total Extract Elapsed Time: 1.625 sec
.END
```

The status bar at the bottom shows 'Ready' and 'Ln 1, Col 1'.

Simulations using T-Spice

- Add following commands for verifying the transient response.

```
VDD VDD 0 dc 1.5
VSS VSS 0 dc 0
Vin Input 0 PULSE(0 1.5 5n .01n .01n 5n 10n)
.TRAN .01n 50n
.print tran V(Input) V(Output)
```

- Press F5 or Run button.

The screenshot shows the T-Spice software interface with the file 'Inverter.spc' open. The window title is 'T-Spice - [Inverter.spc *]'. The menu bar includes File, Edit, View, Simulation, Table, Setup, Window, Help. The toolbar has various icons for simulation types like AC, DC, and transient analysis. The main pane displays the SPICE code with two yellow circles highlighting specific parts:

```
VDD VDD 0 dc 1.5
VSS VSS 0 dc 0
Vin Input 0 PULSE(0 1.5 5n .01n .01n 5n 10n)
.TRAN .01n 50n
.print tran V(Input) V(Output)
```

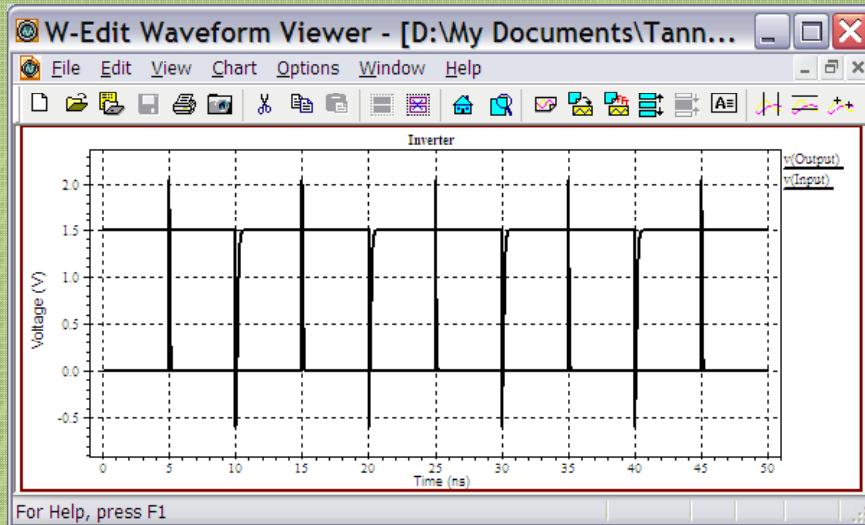
A green circle highlights the command `.TRAN .01n 50n`. A yellow circle highlights the command `.print tran V(Input) V(Output)`.

The status bar at the bottom shows 'Ready' and 'Ln 25, Col 1'.



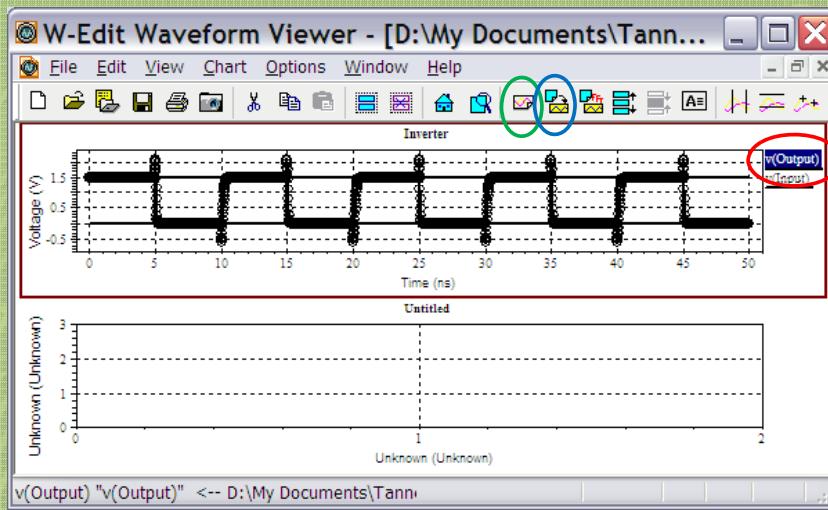
Verify the results

- W-Edit is automatic open.
- The simulation results of Vin and Vout are shown in the same graph



Customize the output results

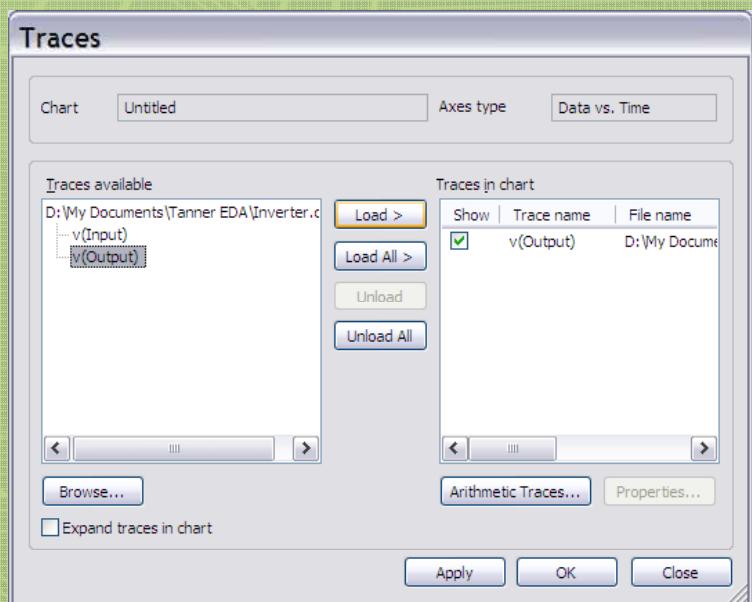
- Customize the waveform by adding more one chart by using new chart button.
- Remove v(Output) from upper chart by press mouse on its and press DEL.
- Press mouse on lower chart and add trace in lower chart



Customize the output results

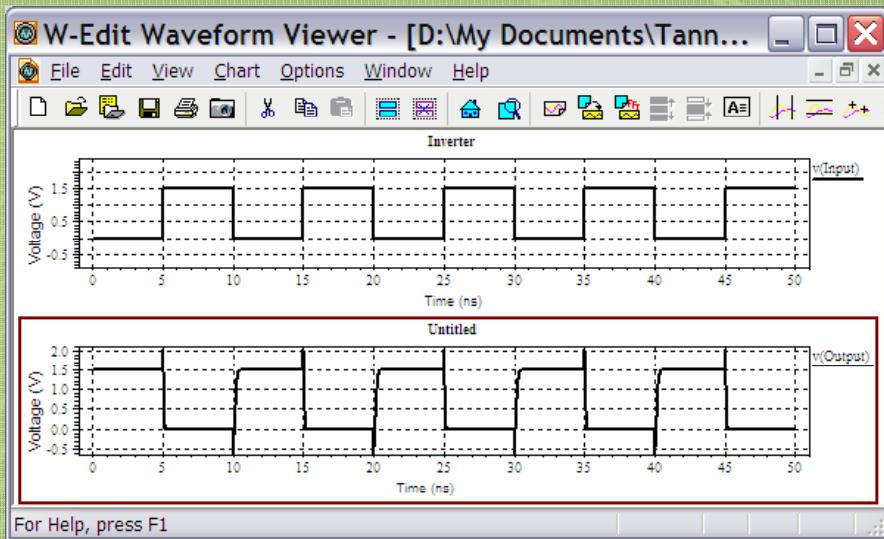
- Load v(Output) data into the chart.

- Press OK



Transient Results

- The results of input and output waveform are shown in upper and lower charts, respectively.

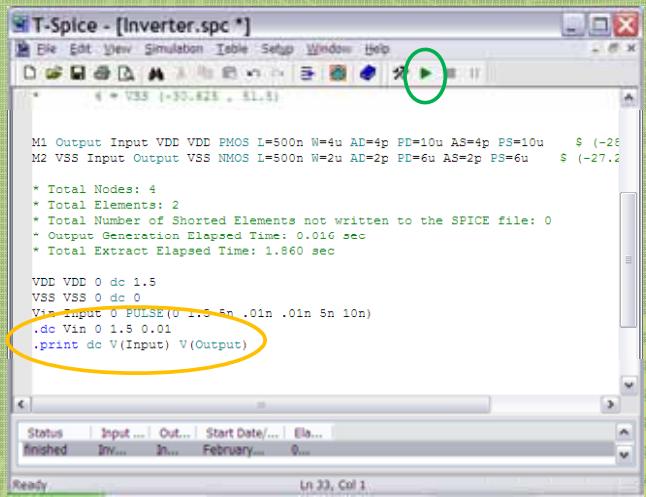


Simulations using T-Spice

- Add following commands for verifying the DC analysis.

```
VDD VDD 0 dc 1.5  
VSS VSS 0 dc 0  
.DC Vin 0 1.5 0.01  
.print DC V(Input) V(Output)
```

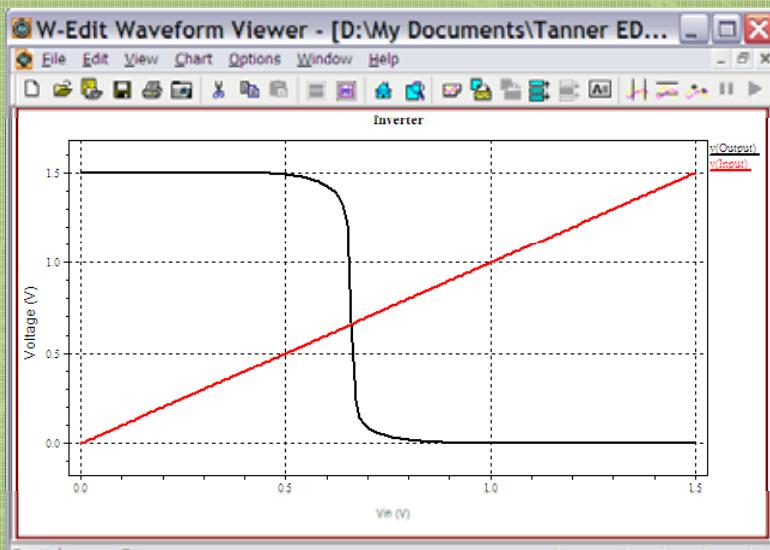
- Press F5 or Run button.



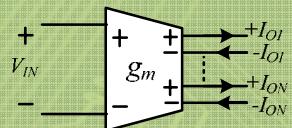
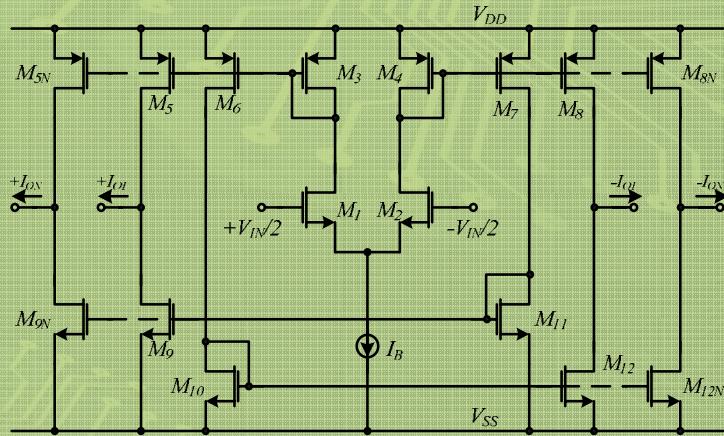
```
T-Spice - [Inverter.spc *]  
File Edit View Simulation Table Setup Window Help  
V3.5 (+30.825, 81.8)  
M1 Output Input VDD VDD PMOS L=500n W=4u AD=4p PD=10u AS=4p PS=10u S (-26  
M2 VSS Input Output VSS NMOS L=500n W=2u AD=2p PD=6u AS=2p PS=6u S (-27.2  
* Total Nodes: 4  
* Total Elements: 2  
* Total Number of Shorted Elements not written to the SPICE file: 0  
* Output Generation Elapsed Time: 0.016 sec  
* Total Extract Elapsed Time: 1.860 sec  
  
VDD VDD 0 dc 1.5  
VSS VSS 0 dc 0  
Vin Input 0 PULSE(0 1.5 5n .01n .01n 5n 10n)  
.dc Vin 0 1.5 0.01  
.print dc V(Input) V(Output)
```

DC Analysis Results

- The results of output while input varied are compared in the same chart.



Assignment (OTA Layout)



Transistor	W (μm)	L (μm)	Transistor	W (μm)	L (μm)
M ₁ , M ₂	5	0.5	All PMOS	5	0.5
All NMOS	3	0.5	NMOS Current mirror	5	0.5

CMOS OTA Schematic

Assignment (OTA Layout)

- Tricks
 - Using Metal1 and Metal2 which are located in different layer.
 - Bias current needs a current mirror.
 - Substrate of M1 and M2 are connected to VSS

