LEDIT Layout Tool

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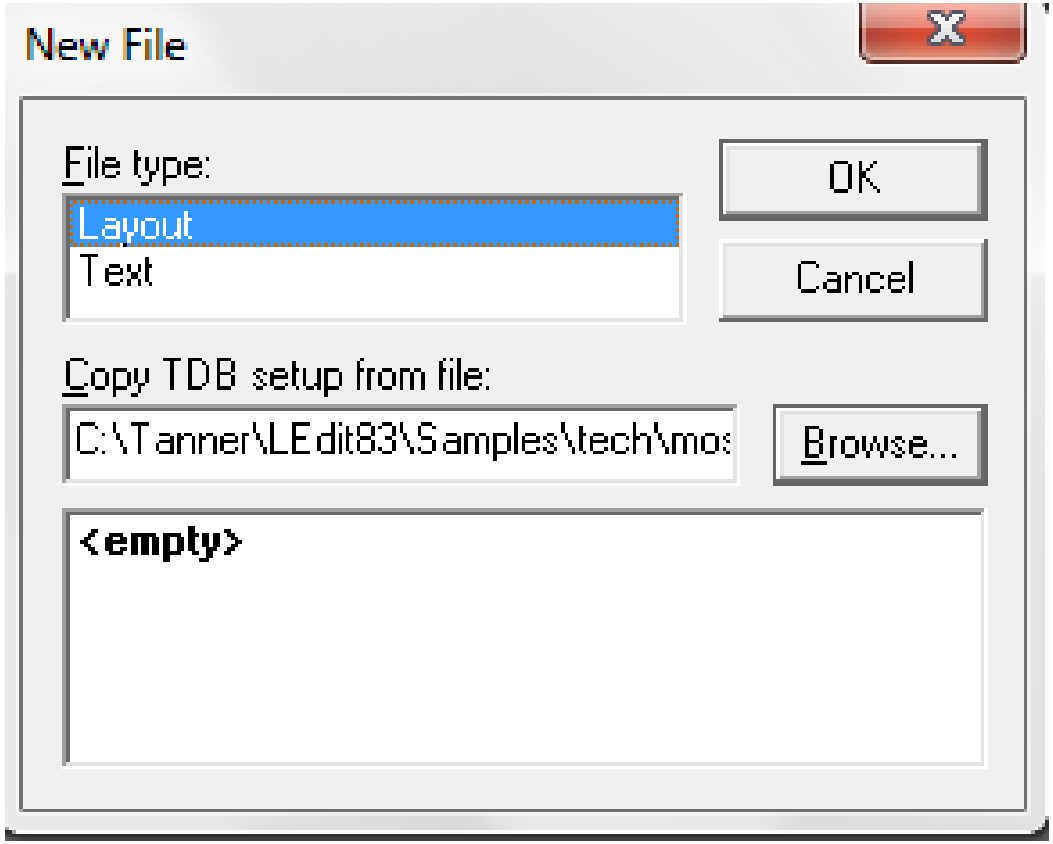
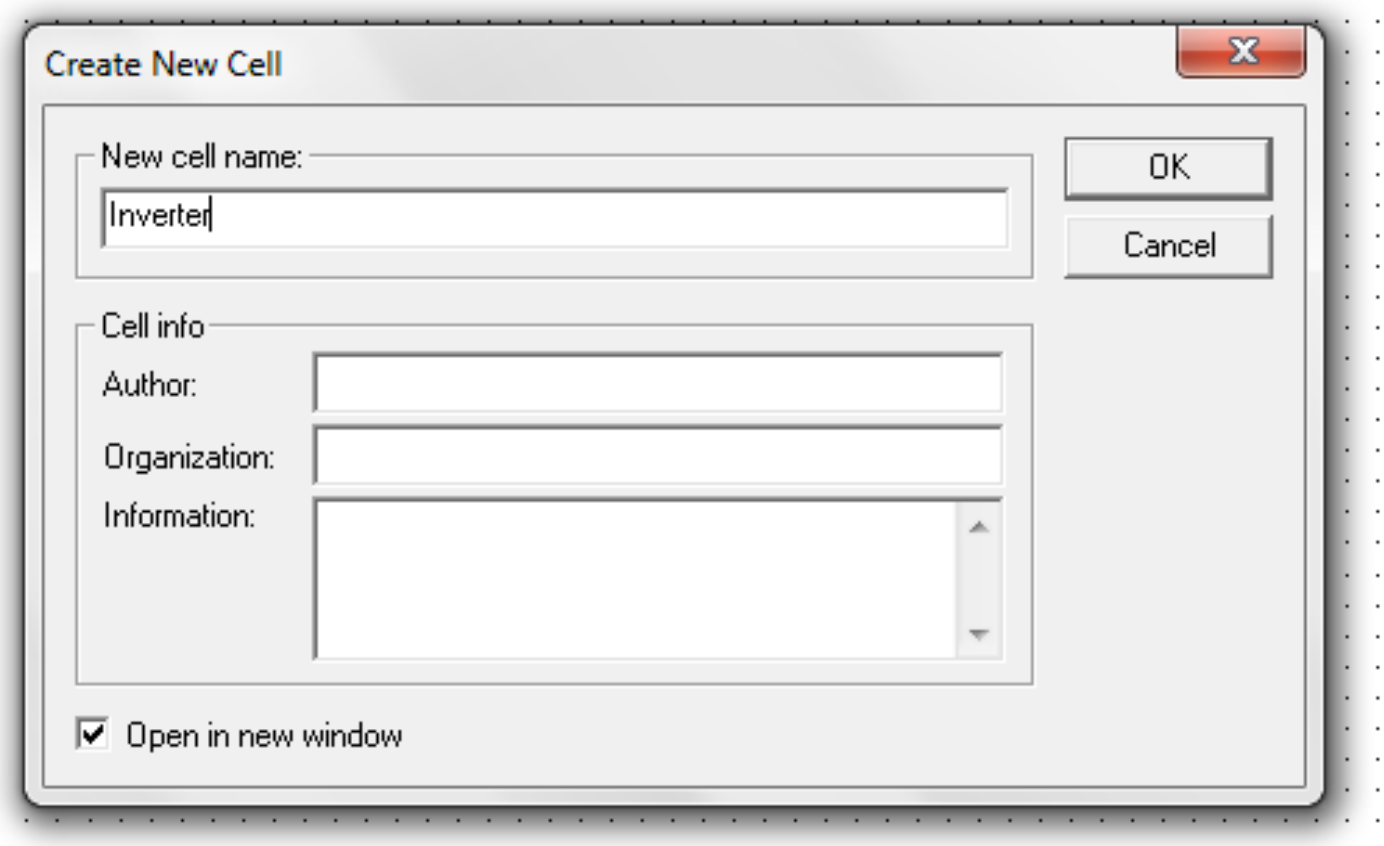
1. Create new Layout

- File → New
- Browse:
  LEDIT83→Samples→Tech→mosis→mhp_ns5.tdb



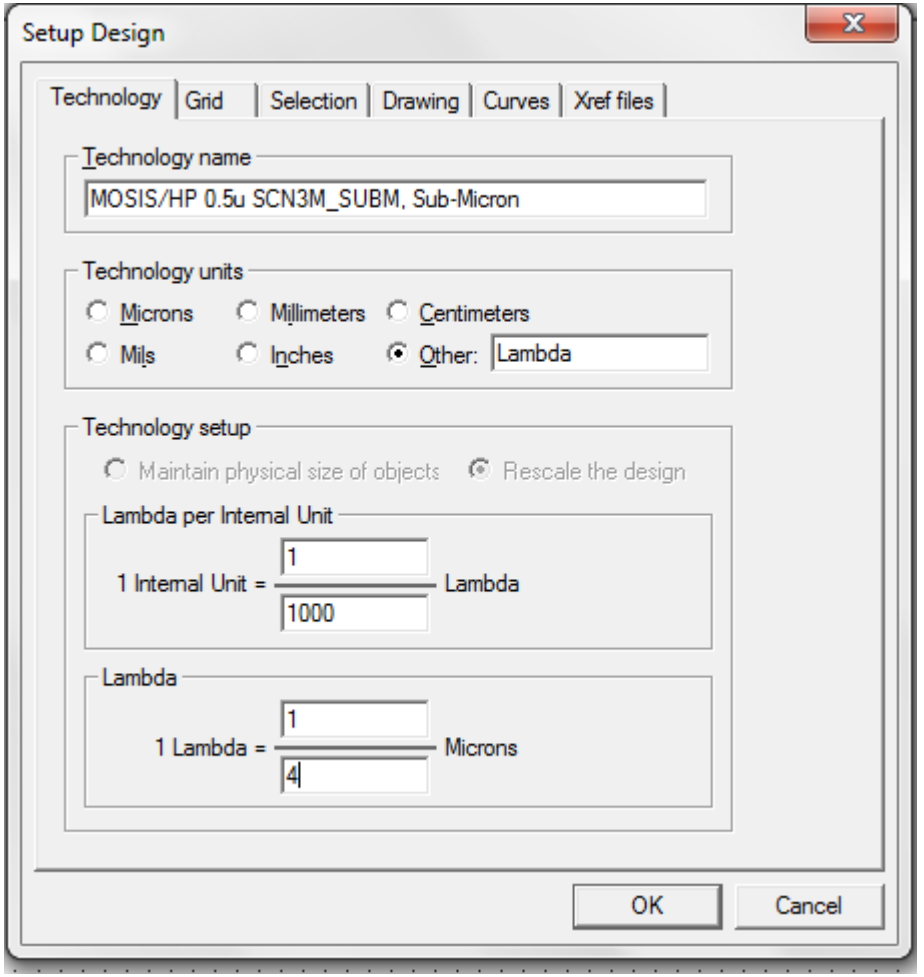
2. Create New Cell

- Menu Bar→ Cell→ New



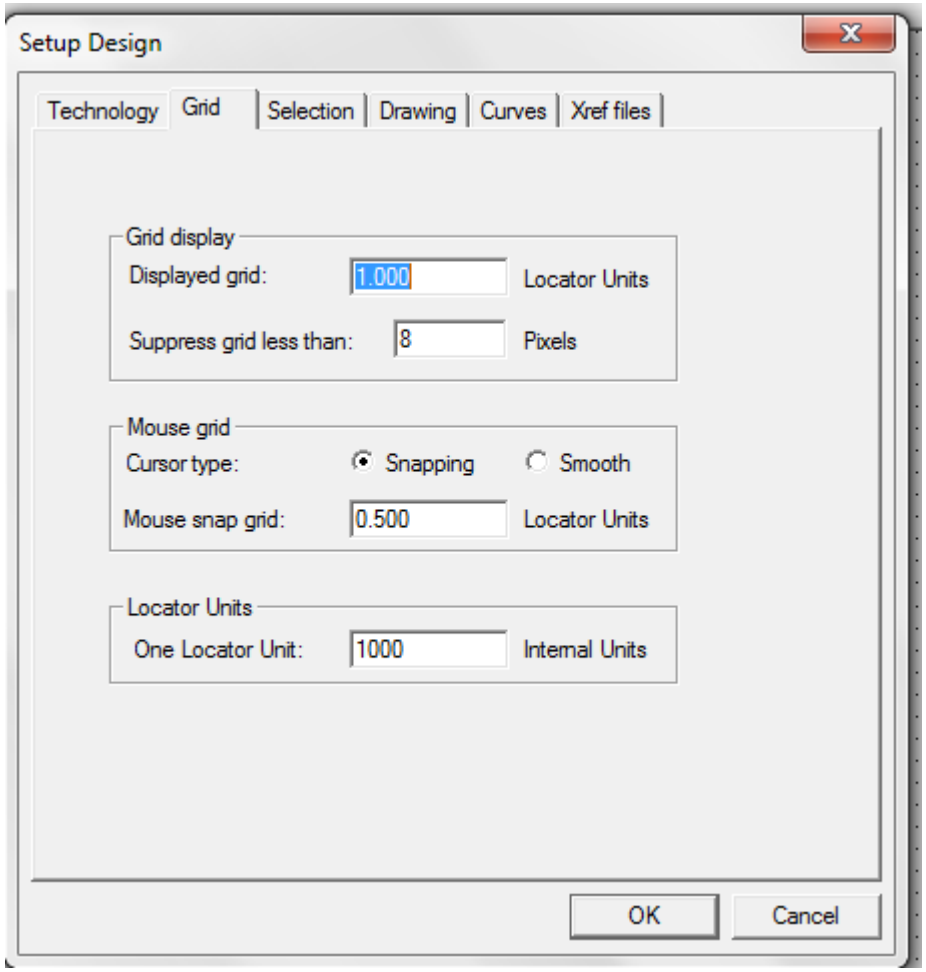
3. Setup Design Technology

- Menu Bar→ Setup→ Design
- Technology Name: SCN3MSUB
- 1 Lambda = 0.25u=1/4

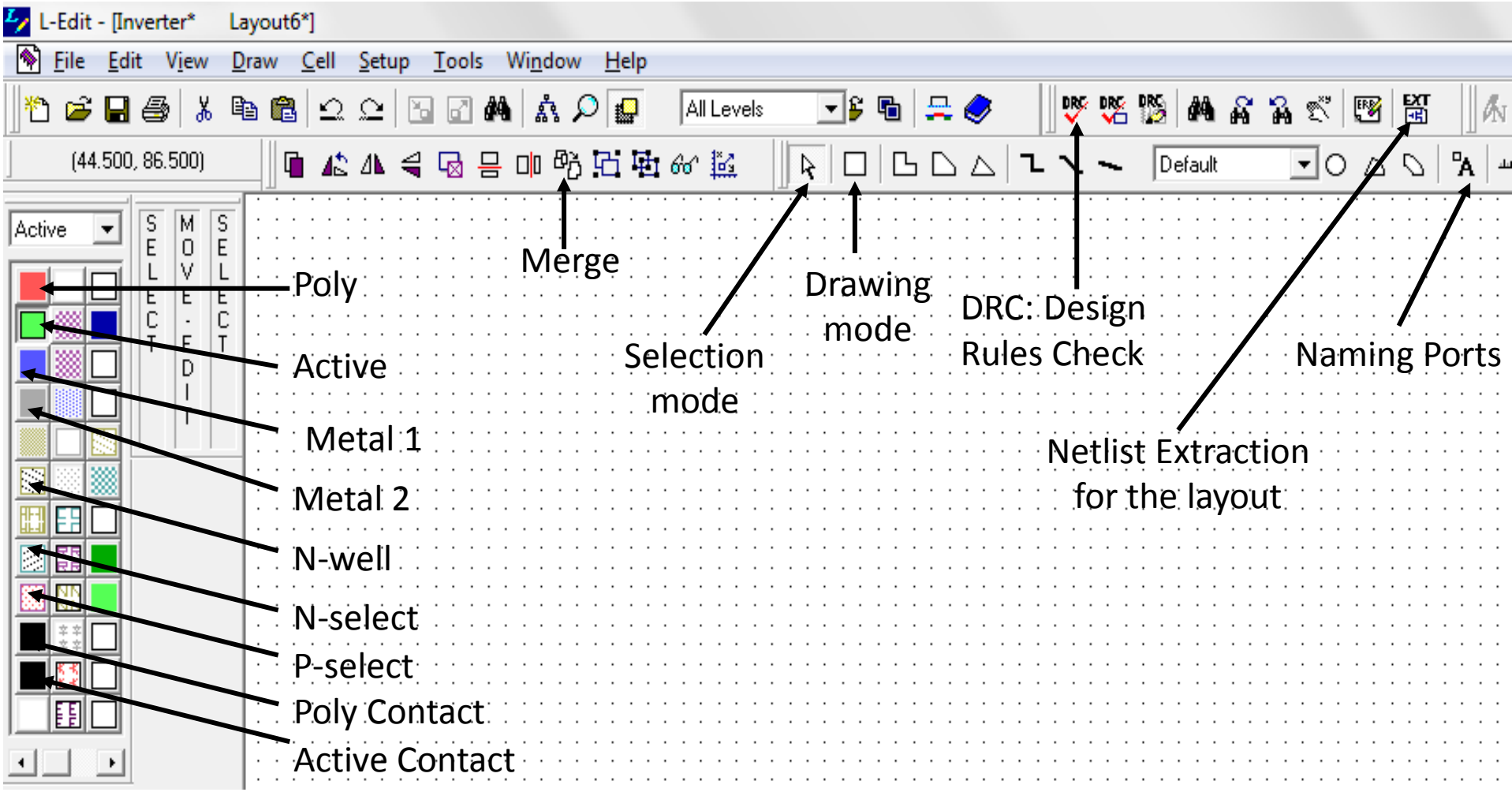


3. Setup Design Technology

- Setup Grid Step = 1 Lambda



4. LEDIT Hints



5. LEDIT Shortcuts

CTRL + C	Copy
CTRL + V	Paste
CTRL + X	Cut
CTRL + (→,←, up, down)	move
CTRL + A	Select all
W	Zoom to selection

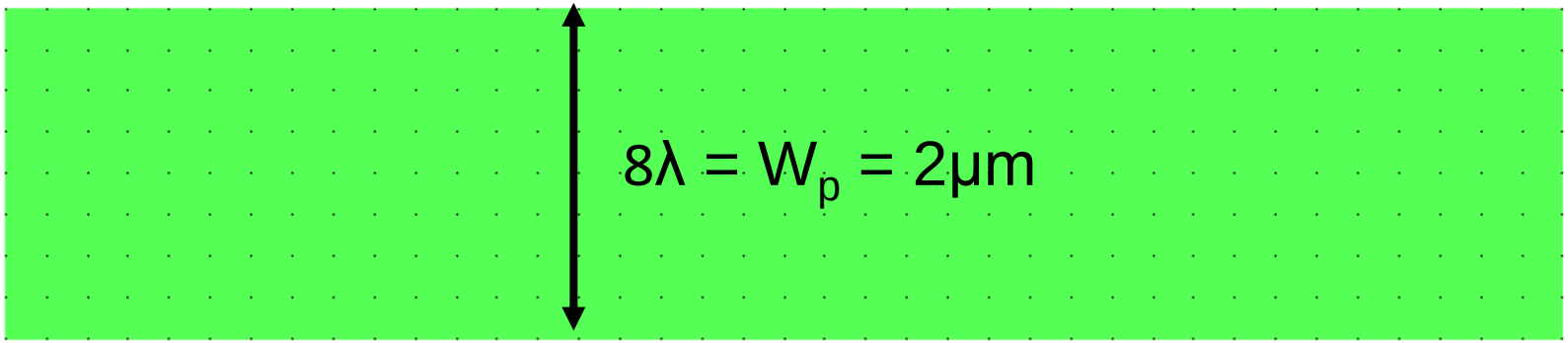
6. CMOS Inverter Layout

- Develop a suitable layout for a CMOS inverter with 0.25um technology using the following aspect ratios:

  (W/L)n=1u/0.5u (W/L)p=2u/0.5u

- For a 0.25um technology
  - 1u = 1/0.25= 4 Lambda
  - 0.5u = 2 Lambda
  - 2u = 8 Lambda

6.1. Active Layer for PMOS



Hints:

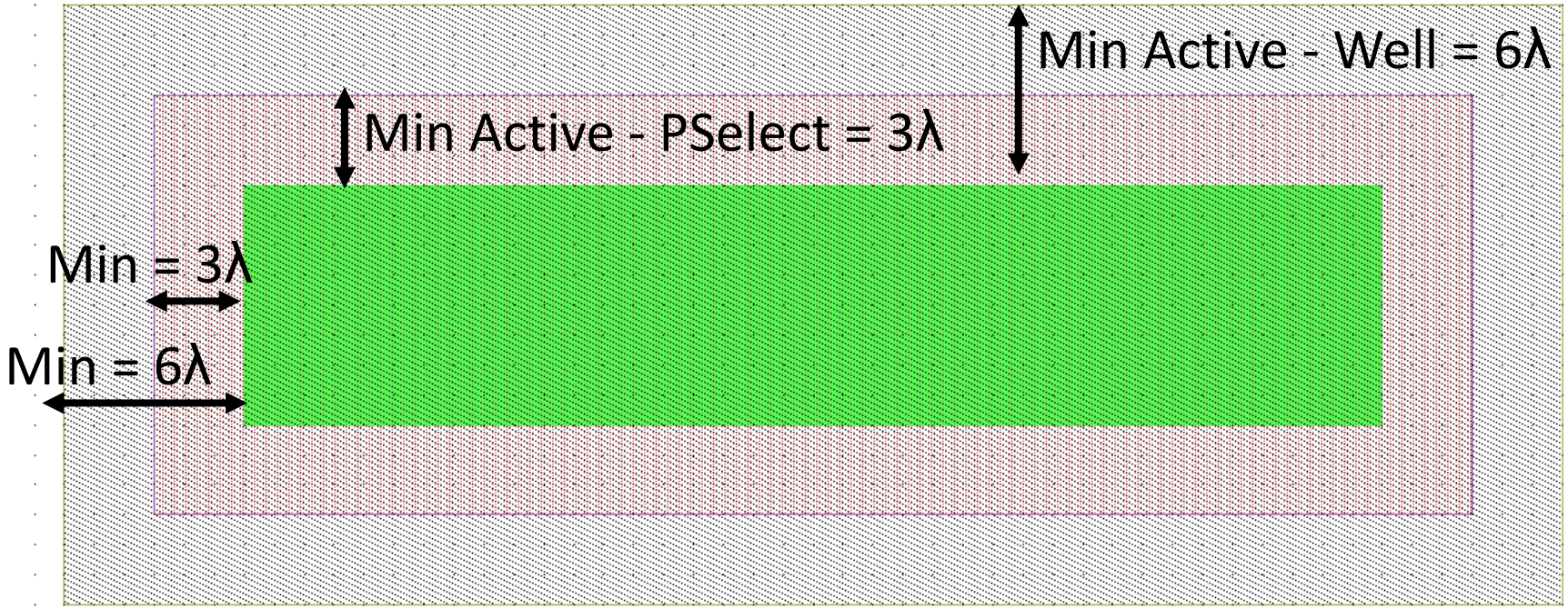
To move any Layer:

1. Select the layer
2. Press ALT + Click in the middle of the layer and move it.

To edit the size of any Layer:

1. Select the layer
2. Press ALT + Click on the layer side required to edit.

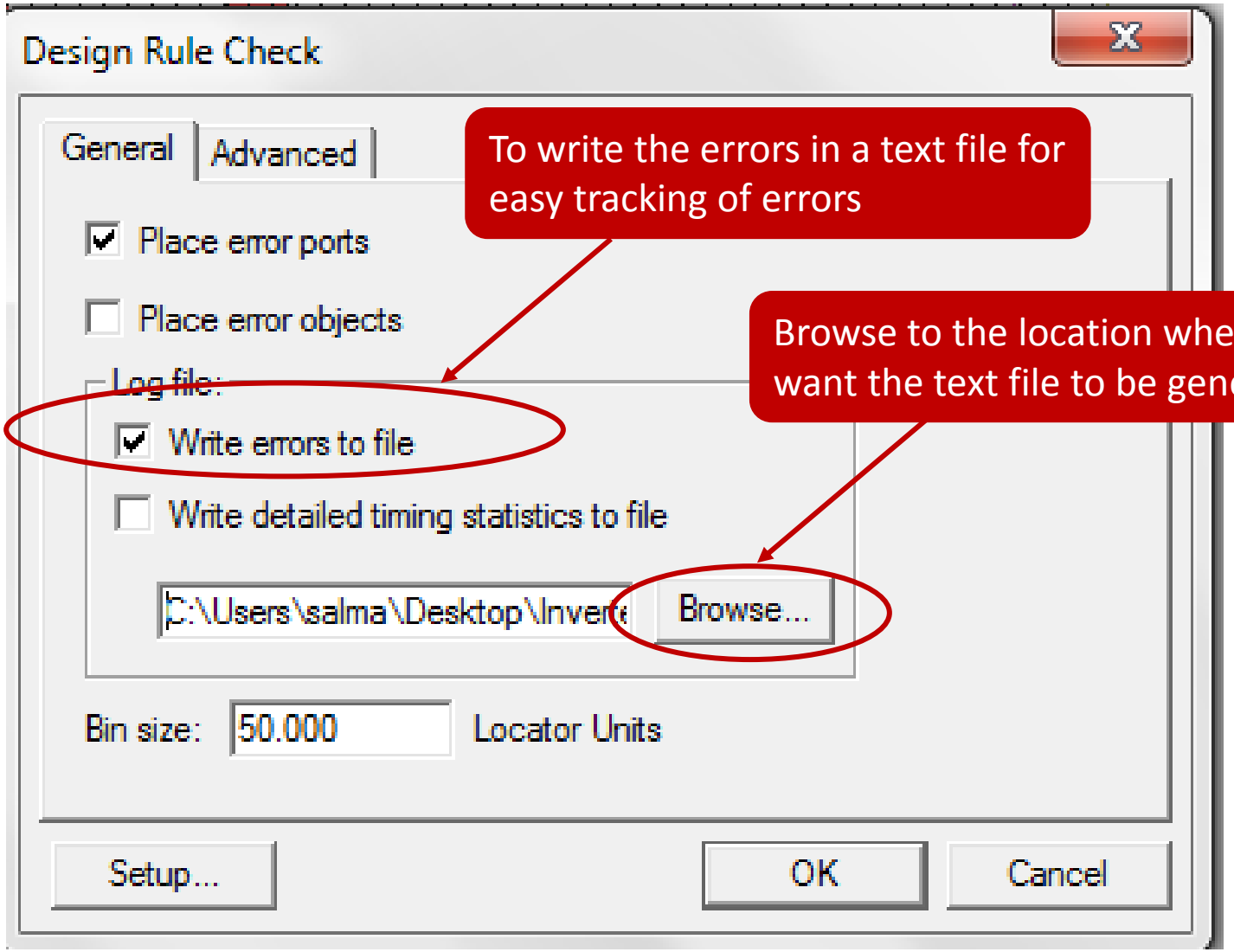
6.2. PSelect and N-Well Layer for PMOS



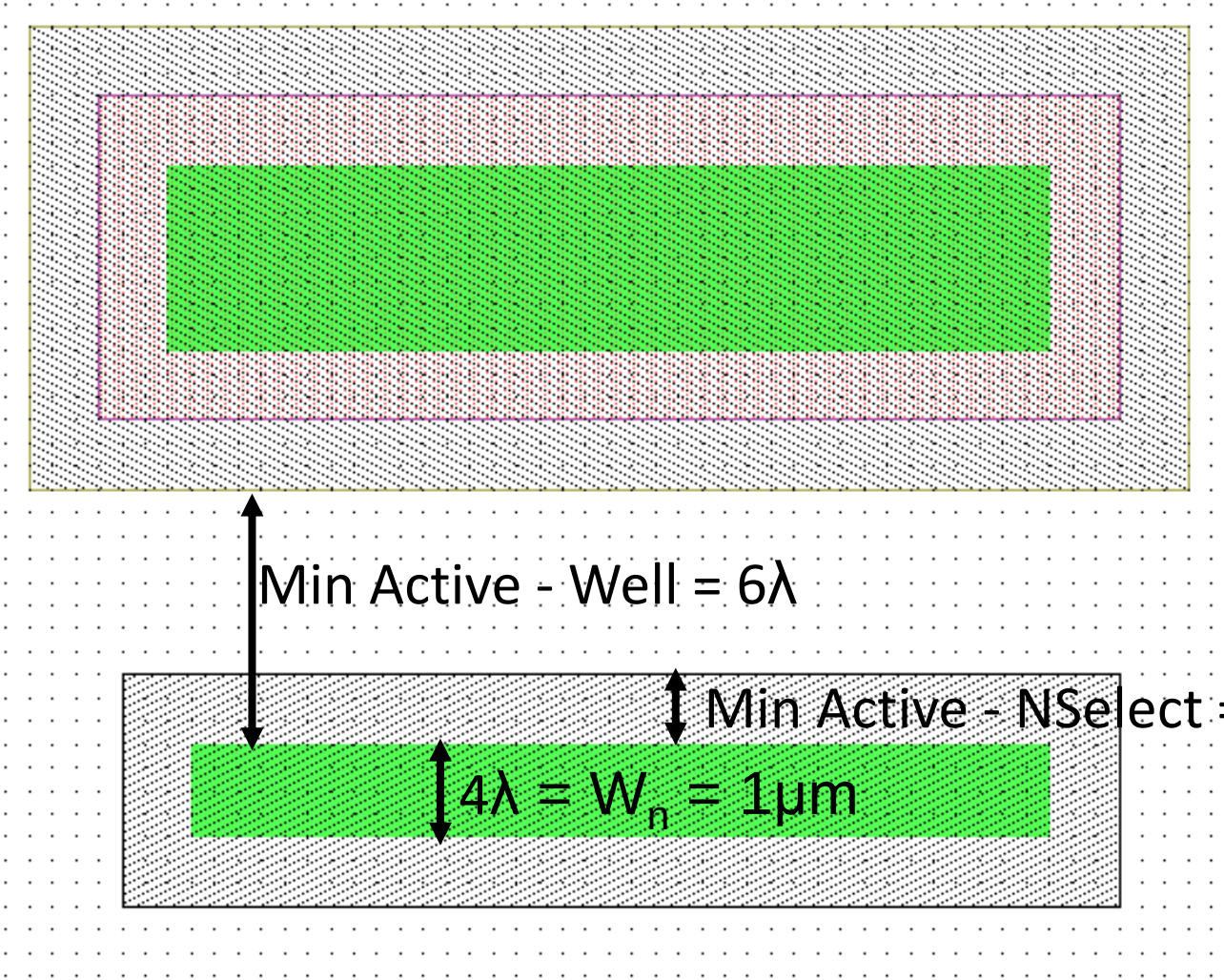
Hint:

Perform a DRC Check after each step

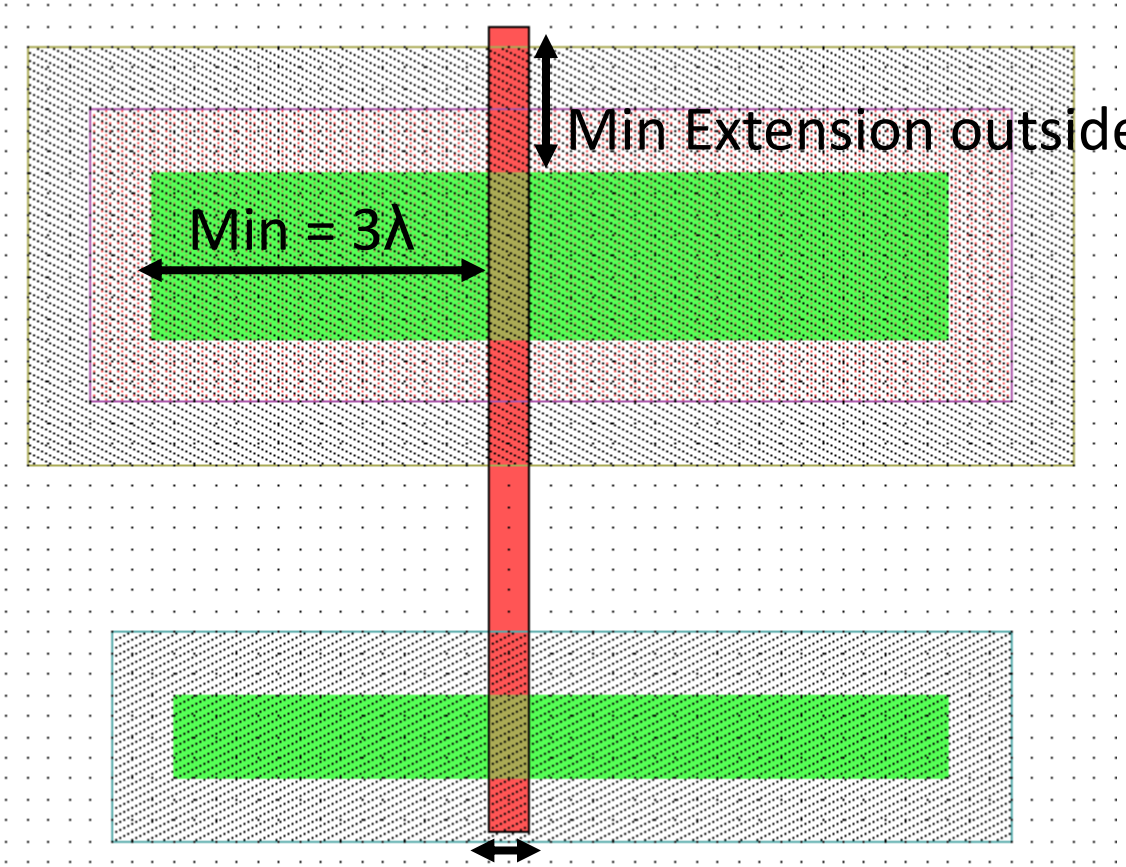
Design Rules Check



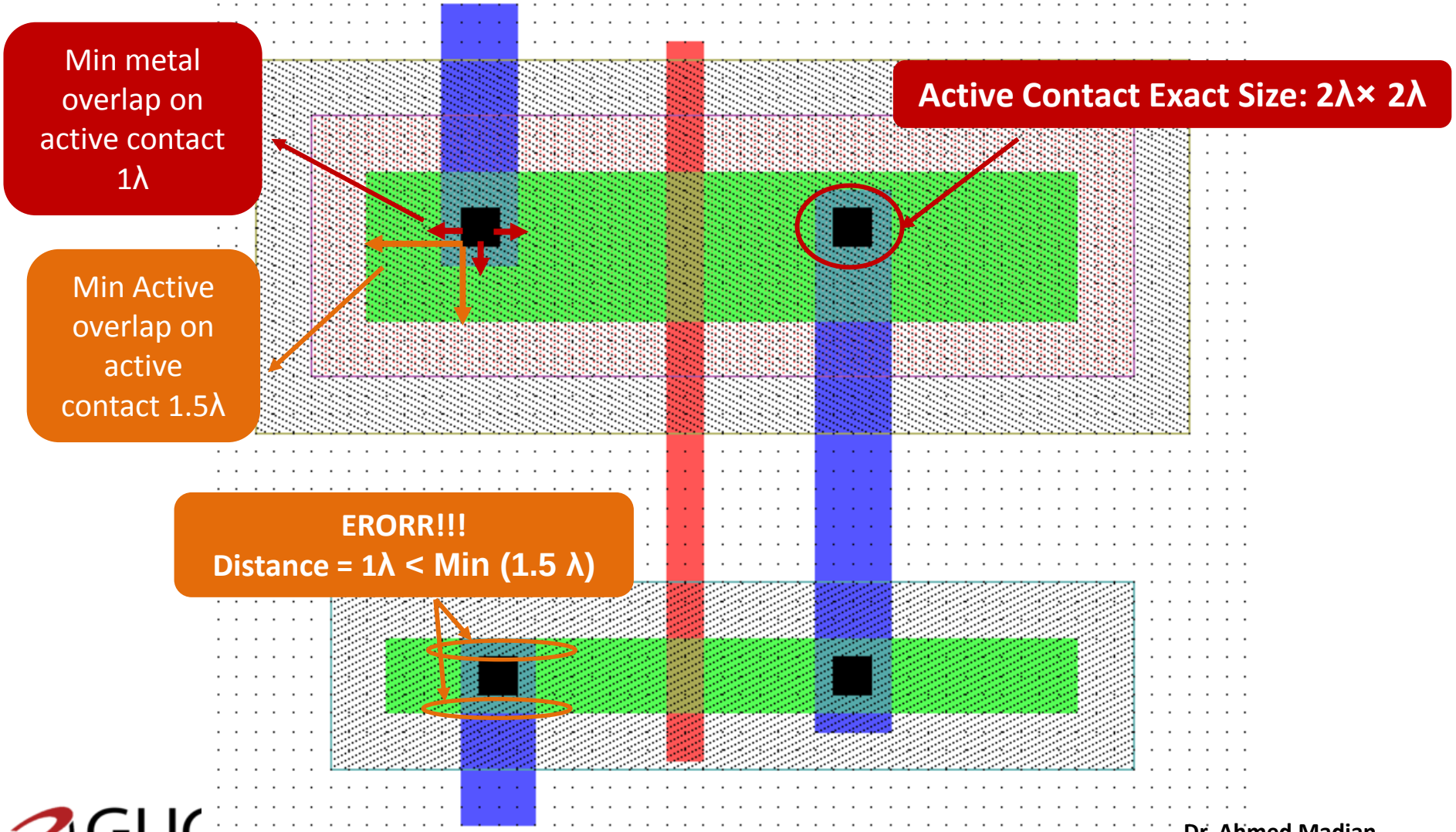
6.3. Active and N-Select Layers for NMOS



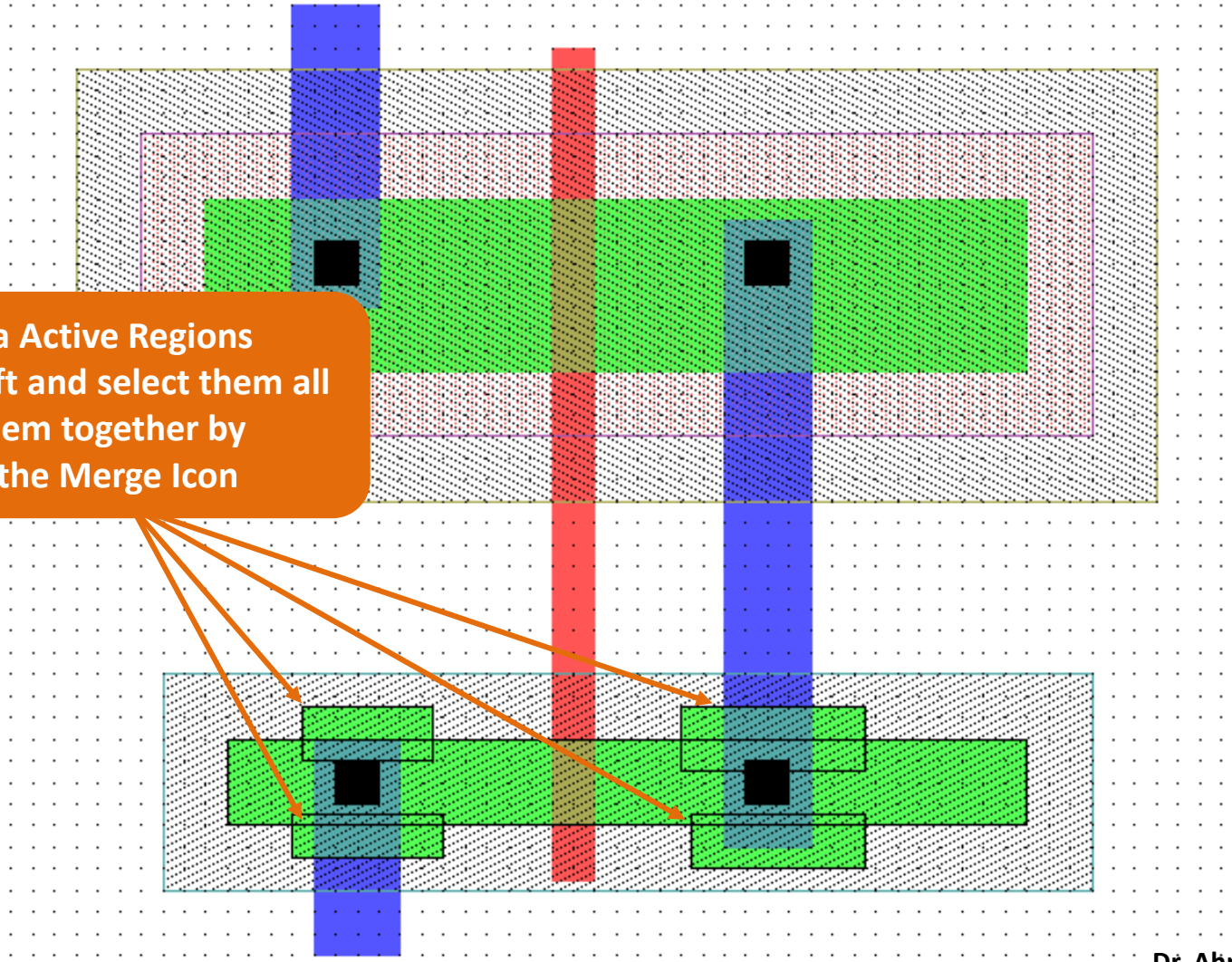
6.4. Poly Layer for NMOS and PMOS Gates



6.5. Active Contact and Metal Layer for Drain/Source Connections

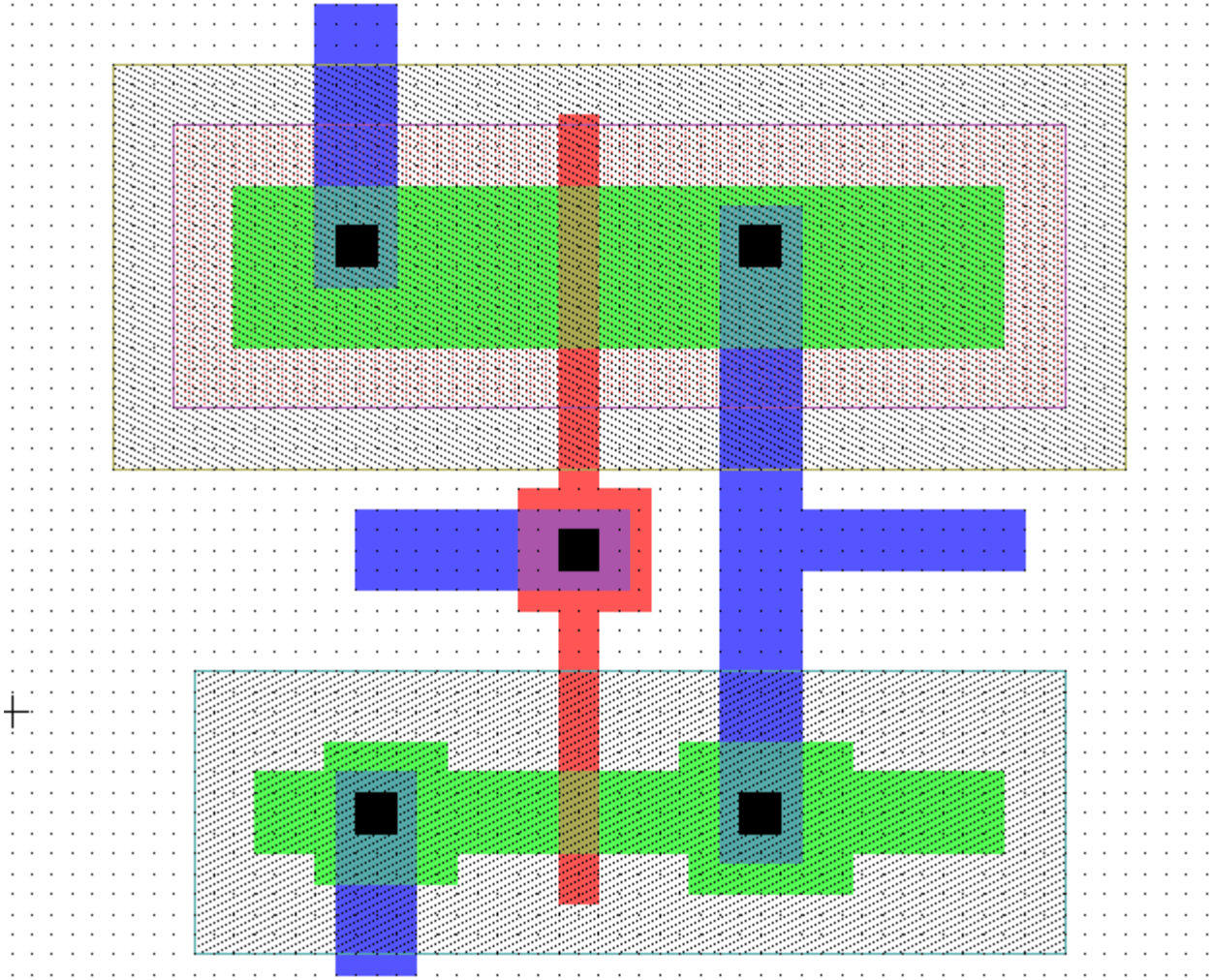


6.5. Active Contact and Metal Layer for Drain/Source Connections

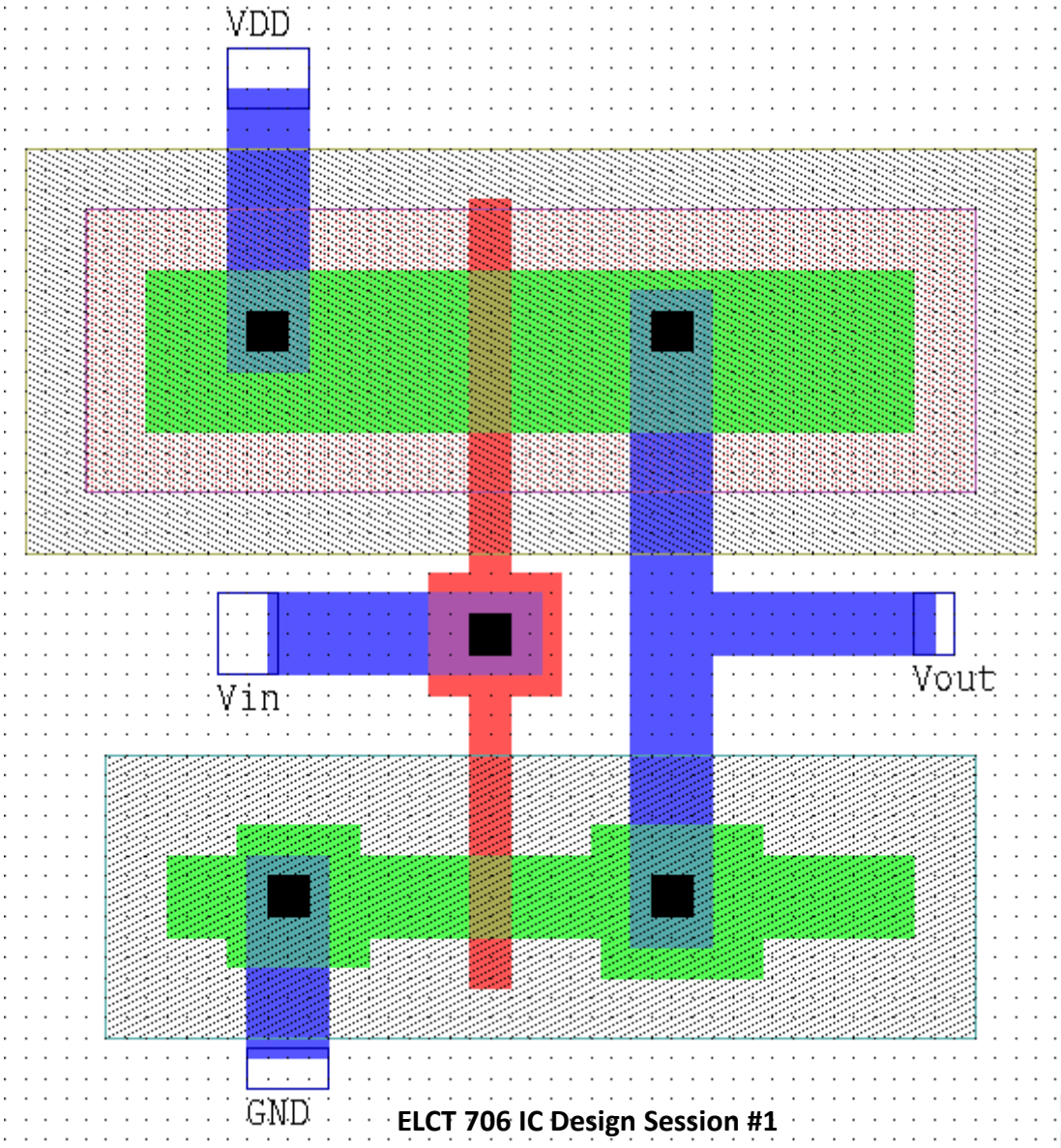


- Add Extra Active Regions
- Press shift and select them all
- Merge them together by pressing the Merge Icon

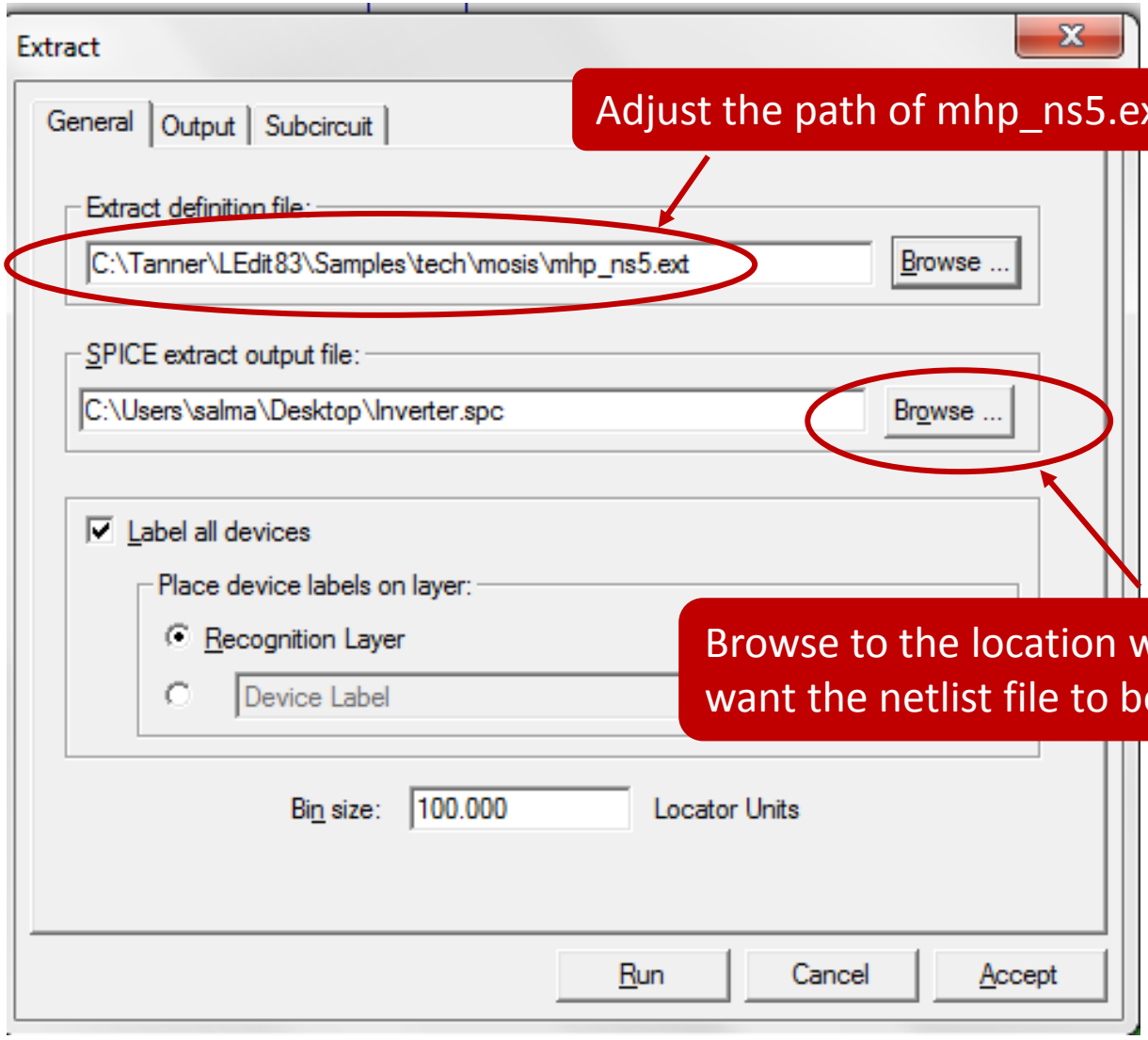
6.6. Poly Contact and Metal Layer for Gate Connections



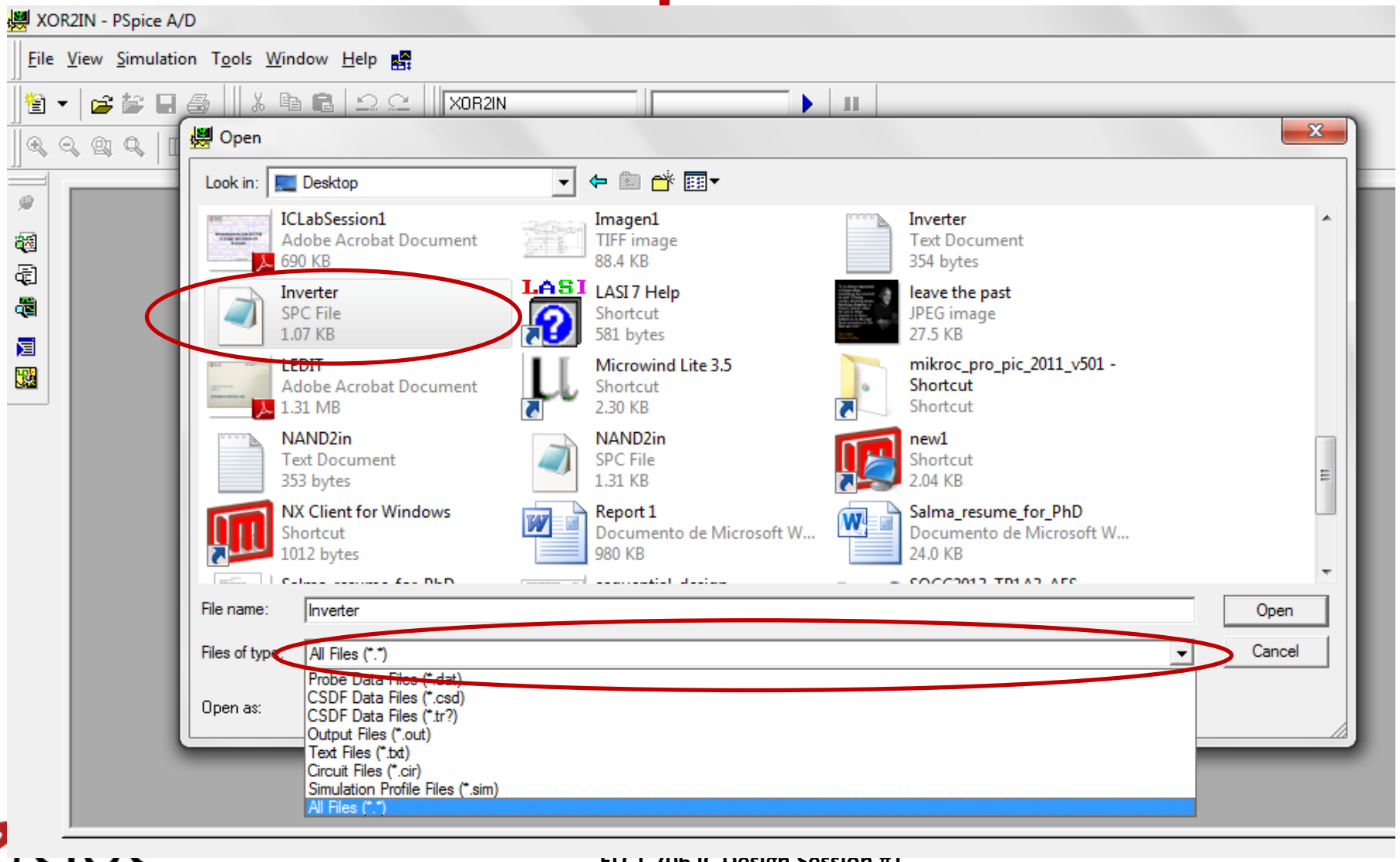
6.7. Add Port Names



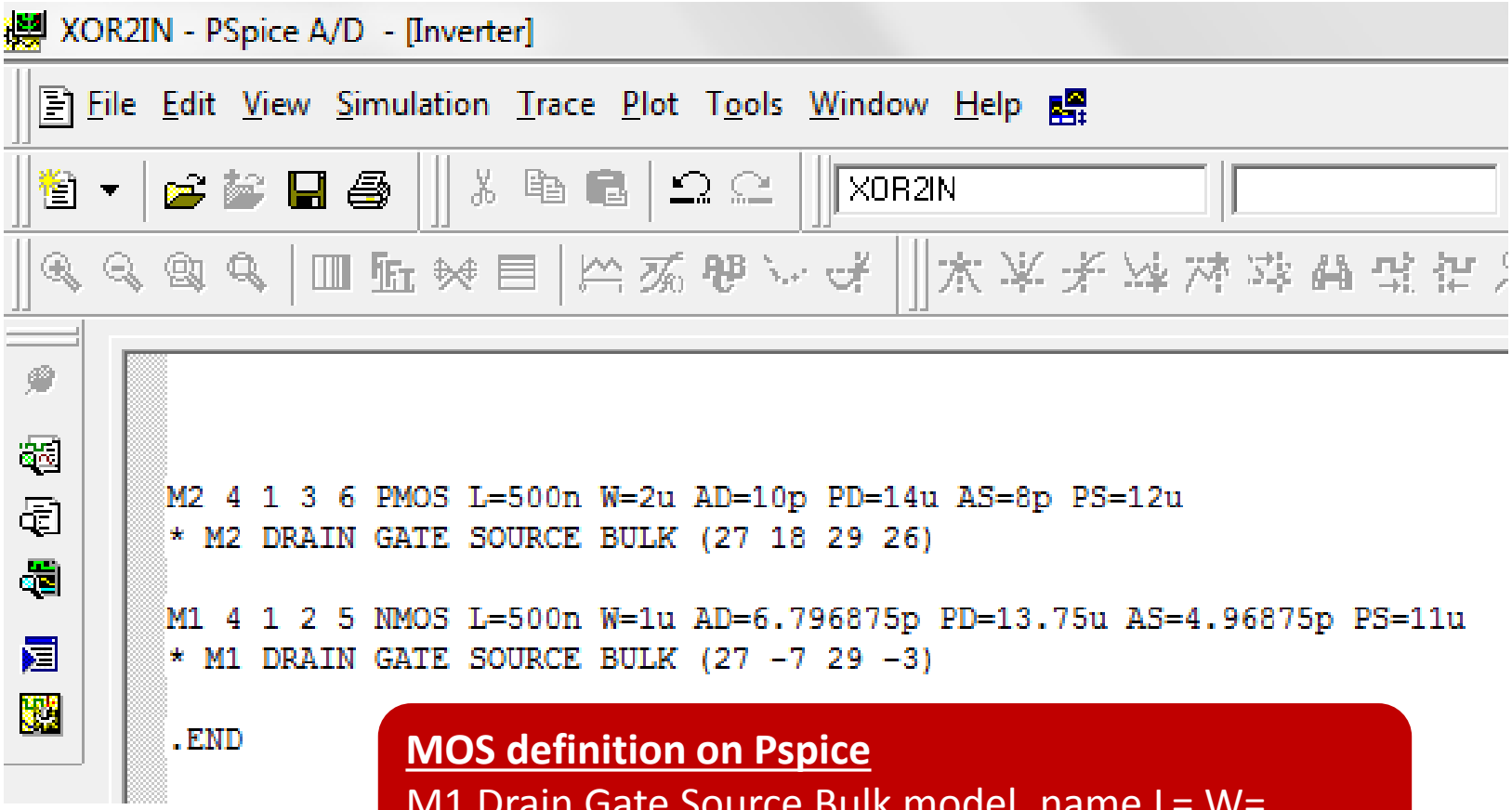
7. Extract the netlist of the layout



8. Open the Generated Netlist file on PSpice



9. Check the generated netlist and Adjust the nodes as required

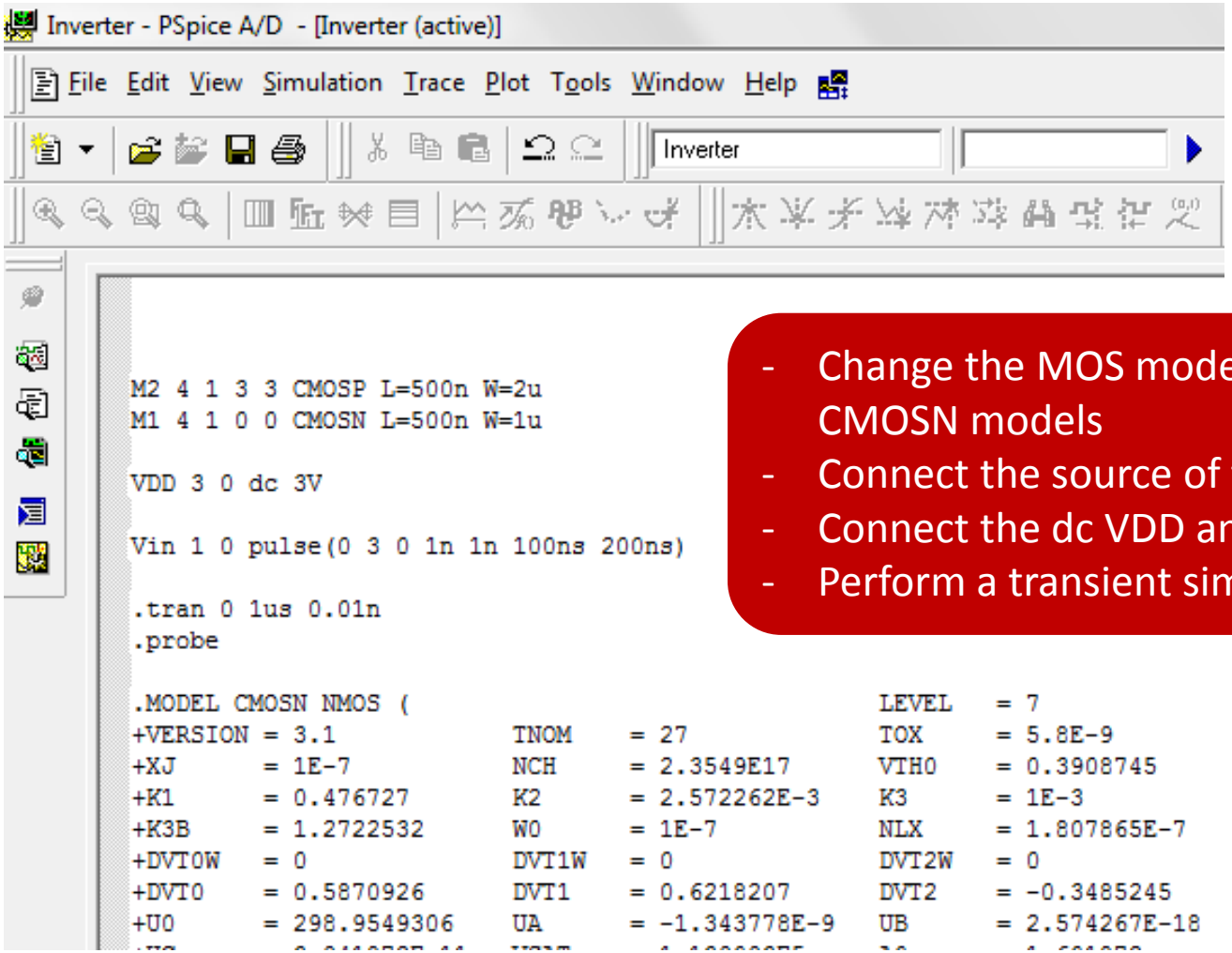


MOS definition on Pspice

M1 Drain Gate Source Bulk model_name L= W=

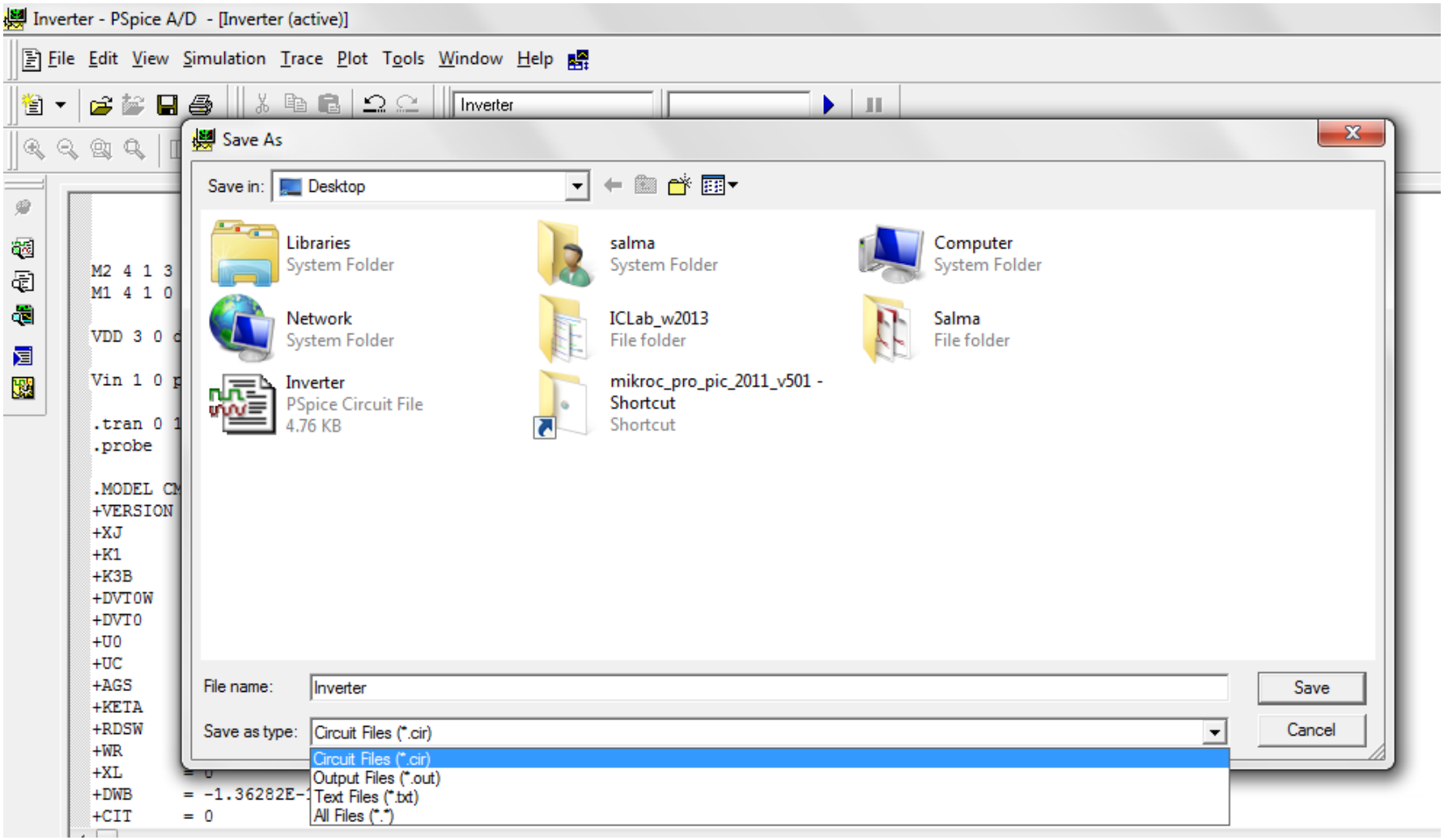
→**N.B.** We will Connect the Source and Bulk together

9. Check the generated netlist and Adjust the nodes as required



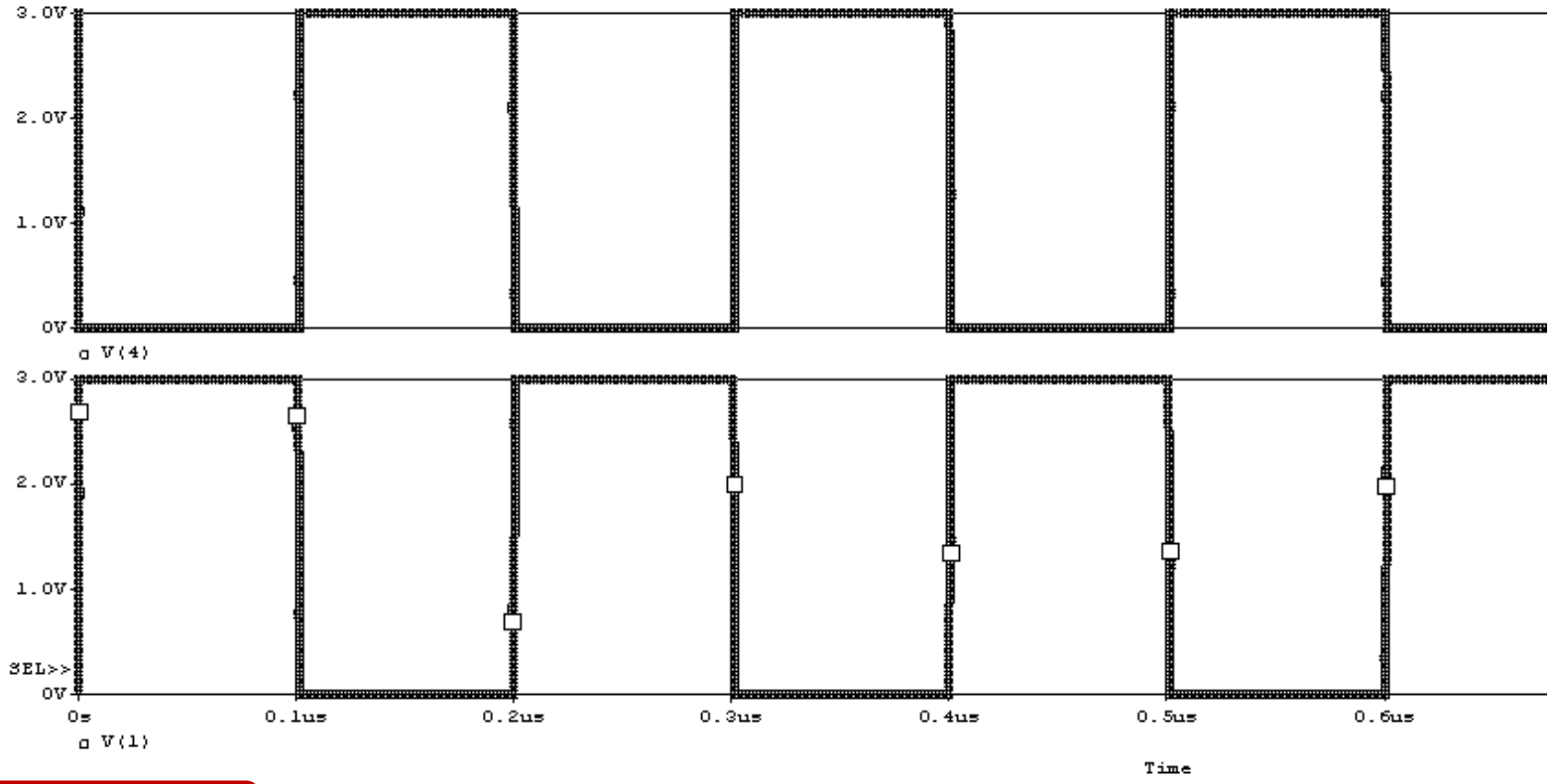
- Change the MOS models to CMOSP and CMOSN models
- Connect the source of the NMOS to GND
- Connect the dc VDD and the pulse Vin
- Perform a transient simulation

10. Save the Netlist as .cir file then Re-open the .cir file



10. Simulate the netlist to test the inverter functionality

Vout = V(4)



Vin = V(1)