SHIFT ADDER AND MULTIPLIER VERILOG CODE

```
module sm(x,y,z,rst, clk, divx);
  input [2:0]x,y;
  input rst, clk;
  output reg [7:0]z;
  output divx;
  reg [2:0]count;
  reg [7:0]Breg;
  reg [3:0]  q;
  reg [7:0] acc;
  wire x1;
  divclk dd (clk,clr,x1);
  assign divx = x1;
  always@(posedge clk)
  begin
  if(rst)
    begin
        acc=0;
      q <= y;
      Breg = x;
      count = 3'b100;
    end
```

```
else if (count>0)
  begin
    if(q[0]==0)
      begin
        Breg=Breg<<1;
        q<=q>>1;
        count=count-1;
      end
    else if(q[0]==1)
      begin
        acc = acc+Breg;
        Breg = Breg<<1;
        q <= q>>1;
        count = count-1;
      end
    end
    z<=acc;
    end
    endmodule

module divclk(clk,rst,z);
input clk,rst;
output reg z;
reg [27:0]sig;
```

```
assign LED=z;
always@(posedge clk)
begin
   if(rst==1)begin
      sig=28'b0;
    end
 else
    begin
      sig=sig+1;
  end
    z=sig[26];
  end
endmodule
```