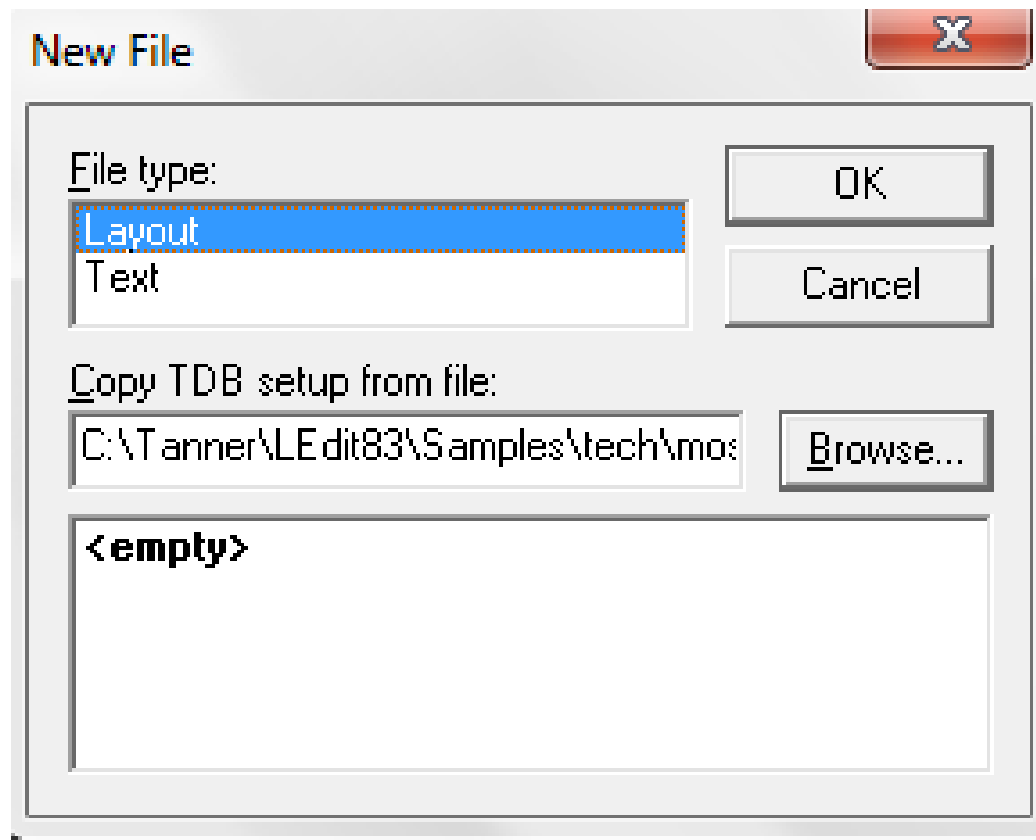


# LEDIT Layout Tool

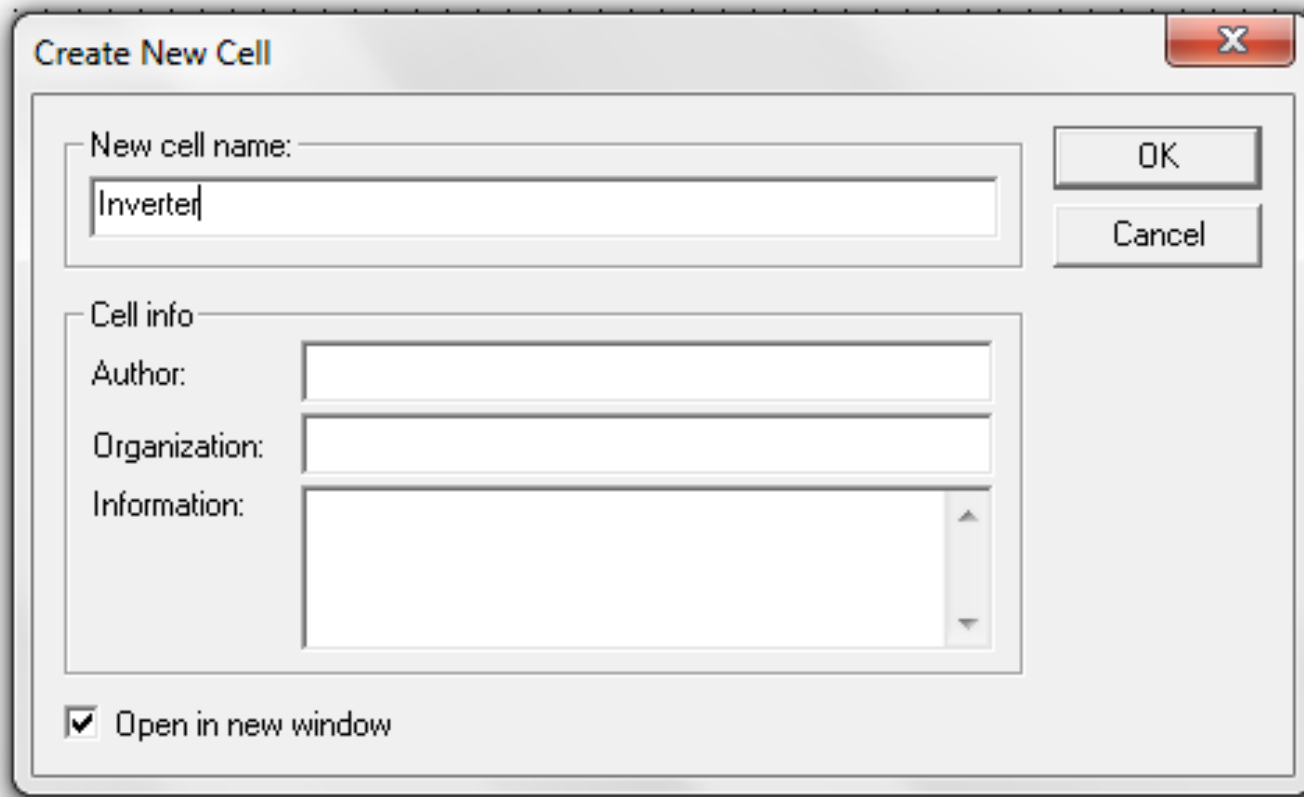
# 1. Create new Layout

- File → New
- Browse:  
LEDIT83→Samples→Tech→mosis→mhp\_ns5.tdb



## 2. Create New Cell

- Menu Bar → Cell → New



Create New Cell

New cell name:

OK Cancel

Cell info

Author:

Organization:

Information:

☒ Open in new window

# 3. Setup Design Technology

- Menu Bar → Setup → Design
- Technology Name: SCN3MSUB
- $1 \text{ Lambda} = 0.25\mu = 1/4$

Setup Design

Technology | Grid | Selection | Drawing | Curves | Xref files

Technology name  
MOSIS/HP 0.5u SCN3M\_SUBM, Sub-Micron

Technology units  
☐ Microns ☐ Millimeters ☐ Centimeters  
☐ Mils ☐ Inches ☒ Other: Lambda

Technology setup  
☐ Maintain physical size of objects ☒ Rescale the design

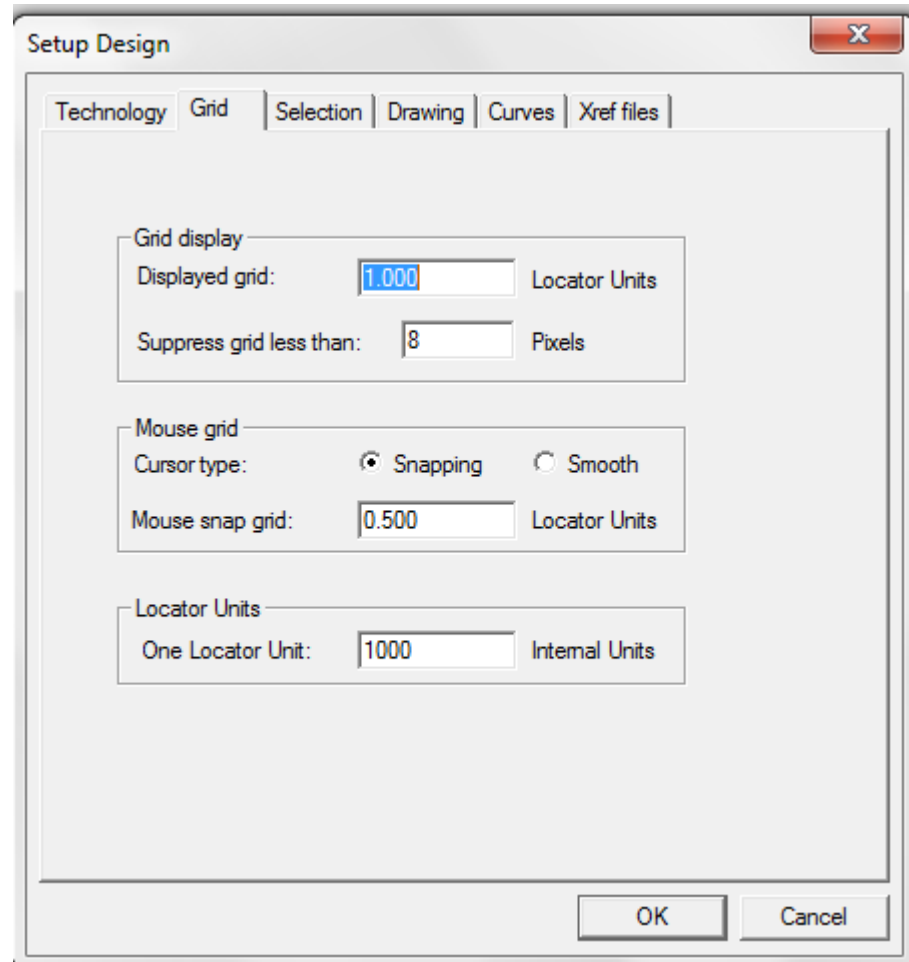
Lambda per Internal Unit  
1 Internal Unit =  $\frac{1}{1000}$  Lambda

Lambda  
1 Lambda =  $\frac{1}{4}$  Microns

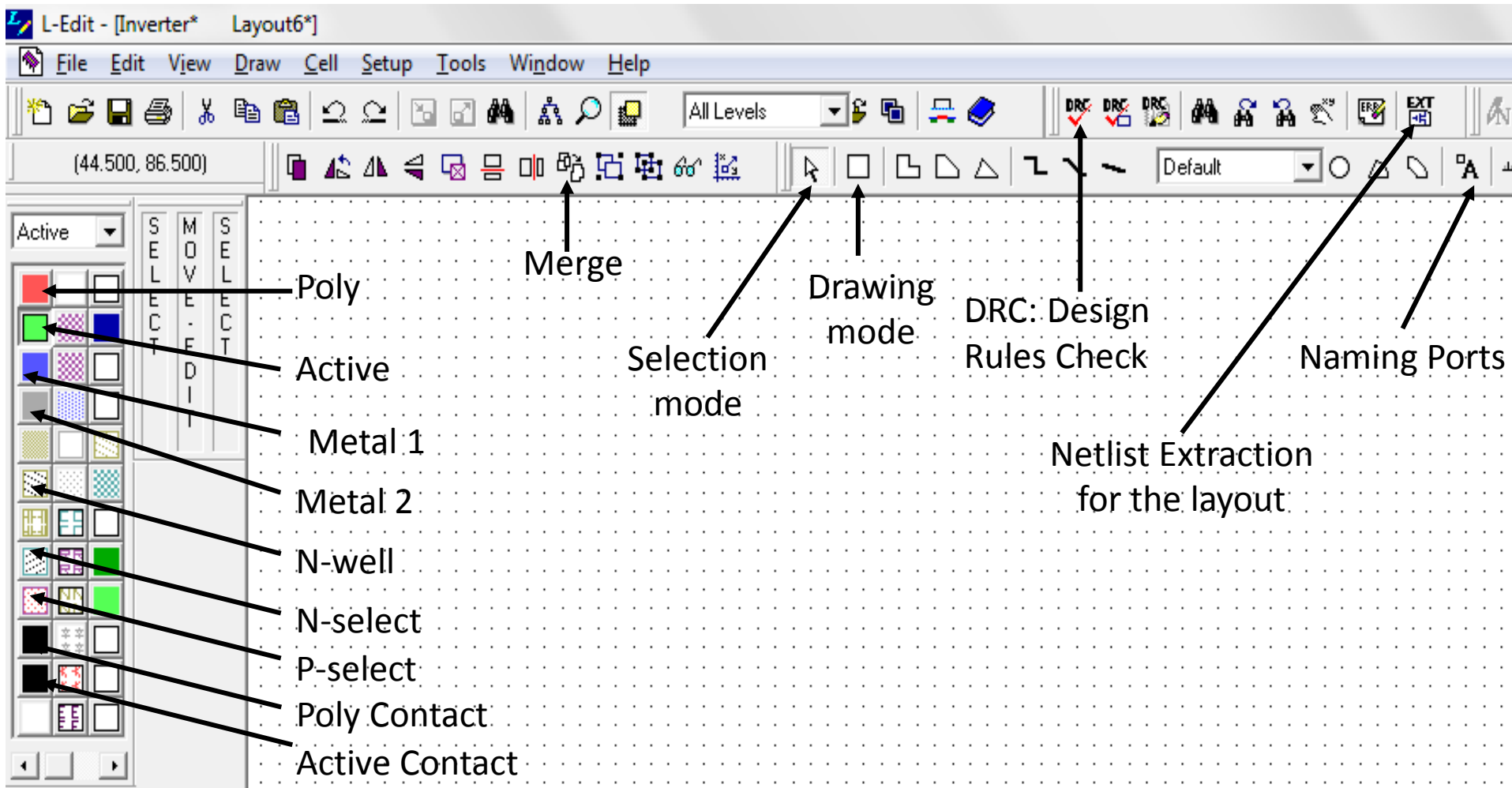
OK Cancel

# 3. Setup Design Technology

- Setup Grid Step = 1 Lambda



# 4. LEDIT Hints



# 5. LEDIT Shortcuts

CTRL + C	Copy
CTRL + V	Paste
CTRL + X	Cut
CTRL + (→, ←, up, down)	move
CTRL + A	Select all
W	Zoom to selection

# 6. CMOS Inverter Layout

- Develop a suitable layout for a CMOS inverter with 0.25um technology using the following aspect ratios:

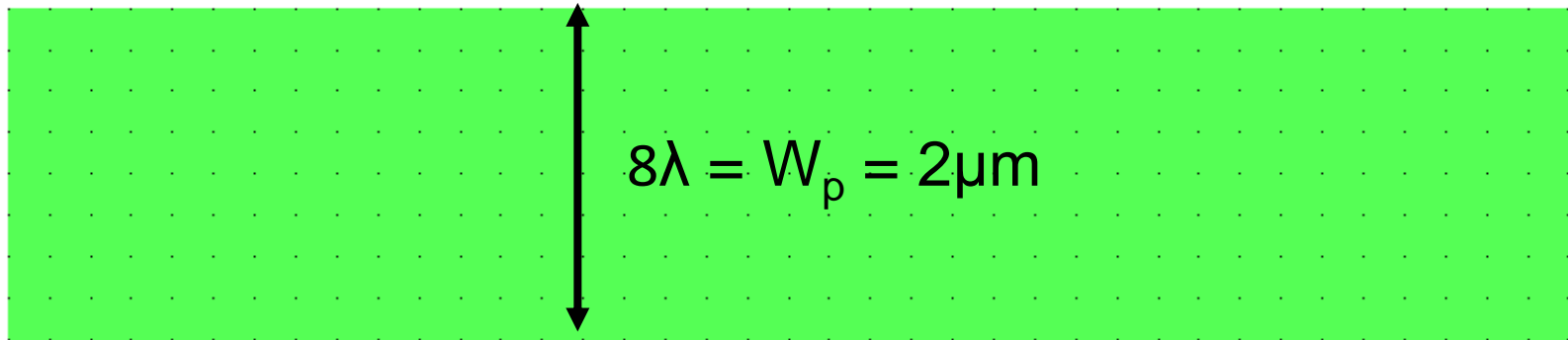
$$(W/L)_n = 1\mu / 0.5\mu$$

$$(W/L)_p = 2\mu / 0.5\mu$$

- For a 0.25um technology
  - $1\mu = 1/0.25 = 4 \text{ Lambda}$
  - $0.5\mu = 2 \text{ Lambda}$
  - $2\mu = 8 \text{ Lambda}$



# 6.1. Active Layer for PMOS



## Hints:

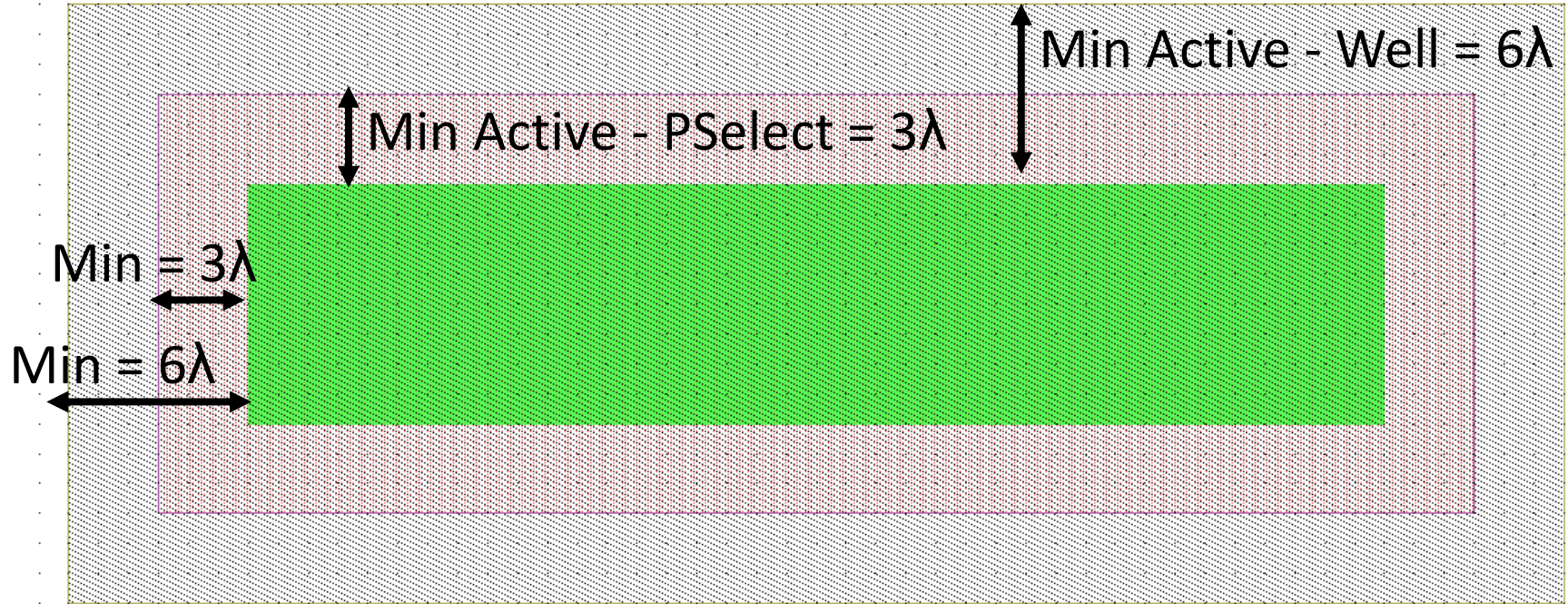
### To move any Layer:

1. Select the layer
2. Press ALT + Click in the middle of the layer and move it.

### To edit the size of any Layer:

1. Select the layer
2. Press ALT + Click on the layer side required to edit.

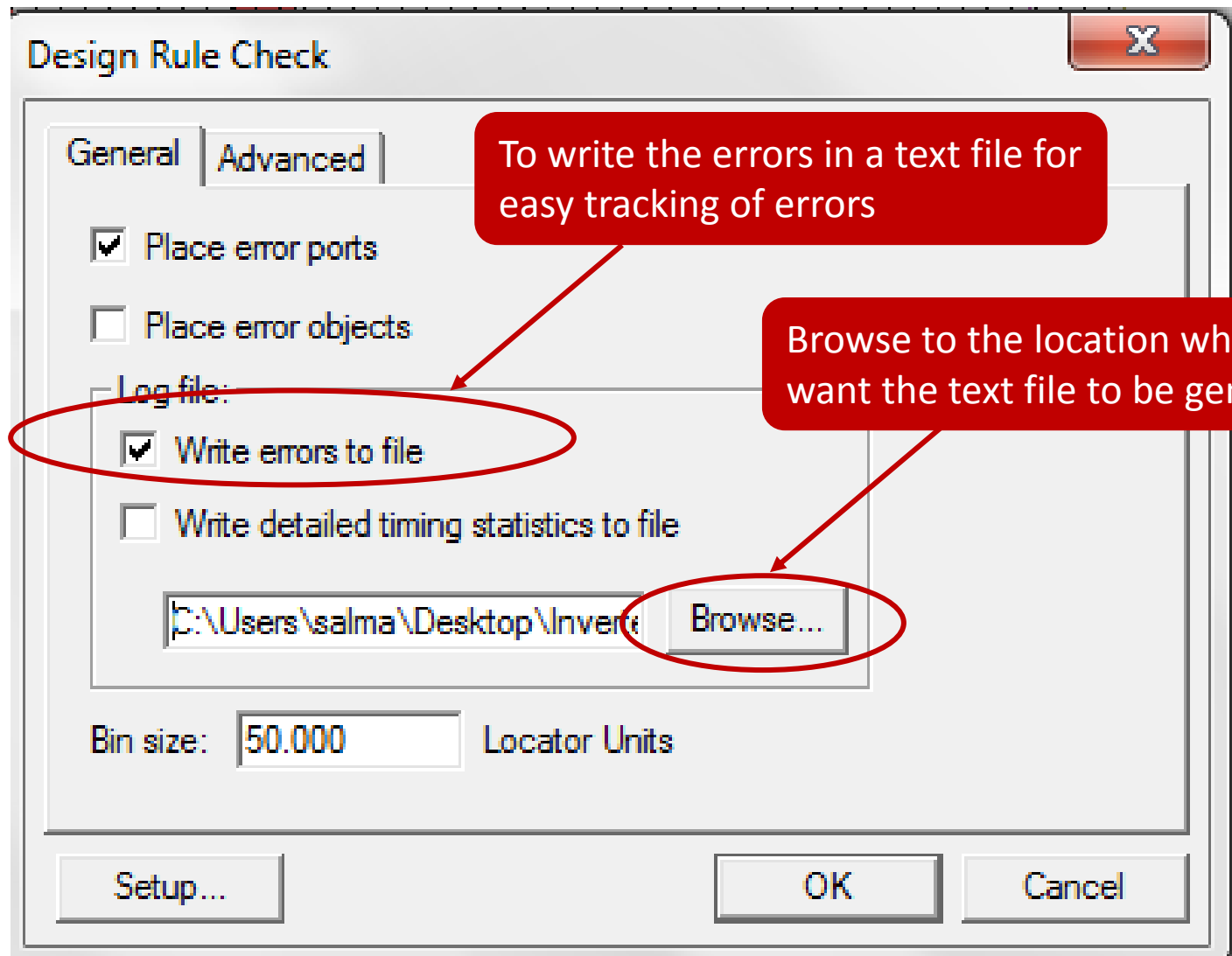
## 6.2. PSelect and N-Well Layer for PMOS



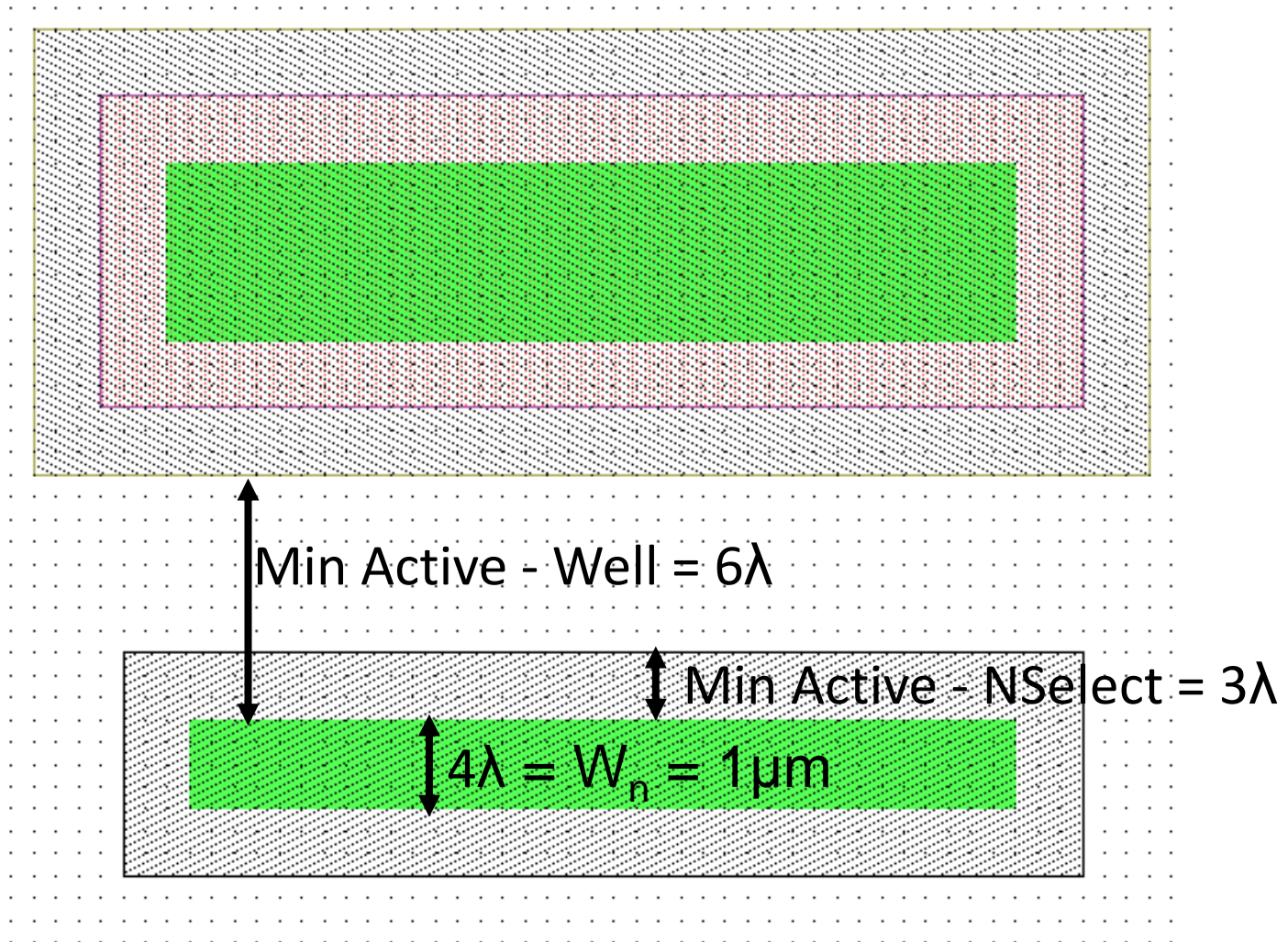
**Hint:**

**Perform a DRC Check after each step**

# Design Rules Check

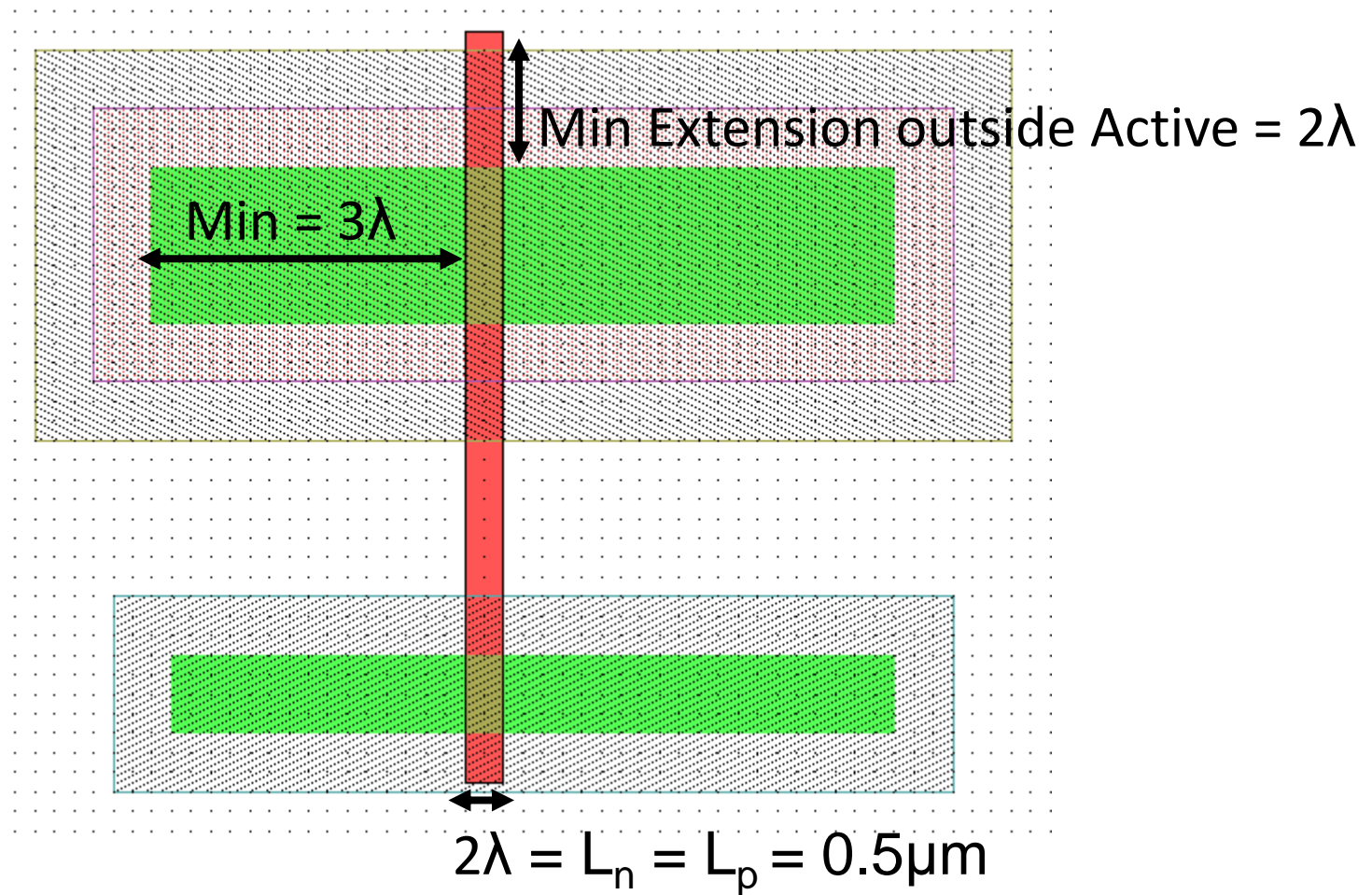


## 6.3. Active and N-Select Layers for NMOS





## 6.4. Poly Layer for NMOS and PMOS Gates



# 6.5. Active Contact and Metal Layer for Drain/Source Connections

Min metal overlap on active contact  $1\lambda$

Min Active overlap on active contact  $1.5\lambda$

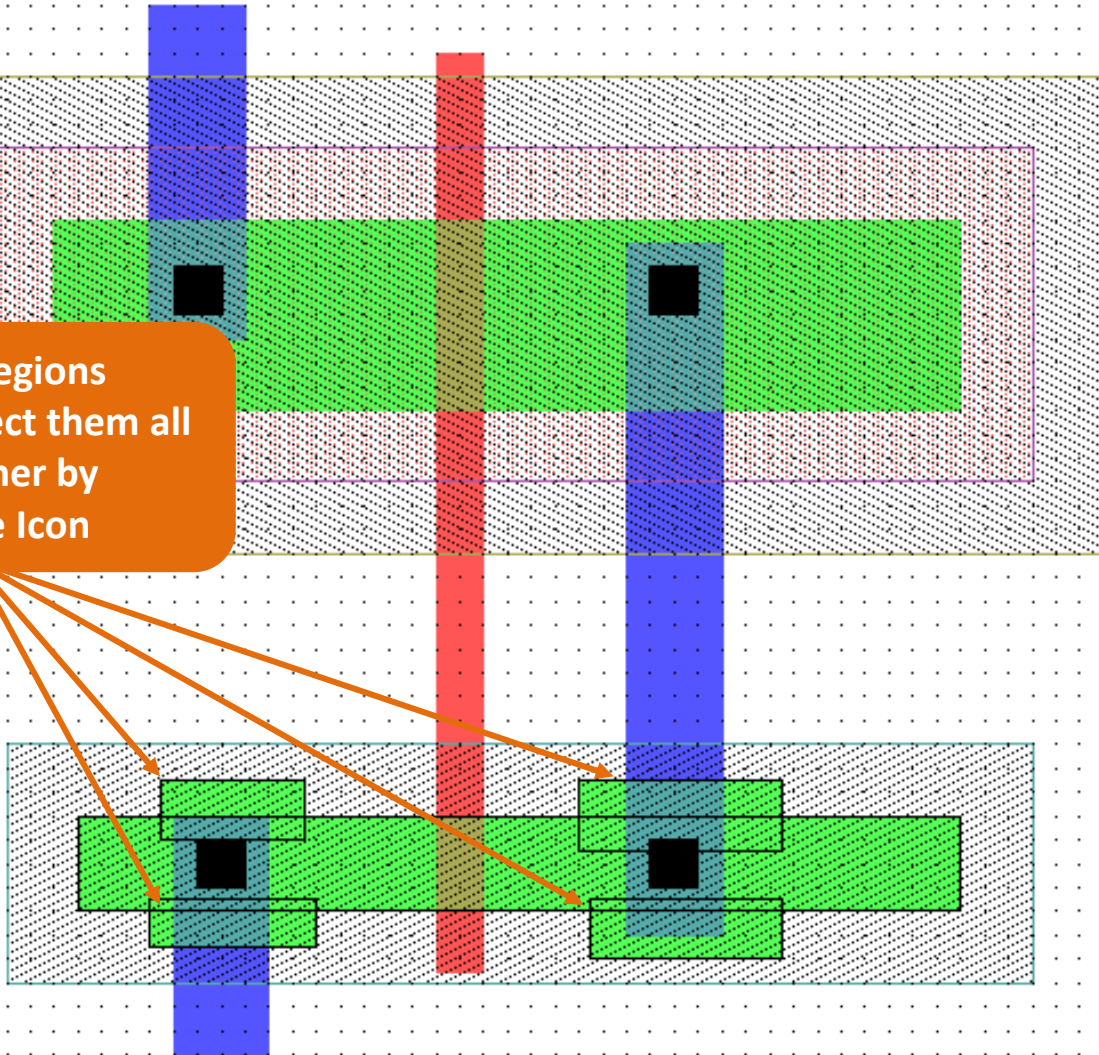
Active Contact Exact Size:  $2\lambda \times 2\lambda$

ERORR!!!

Distance =  $1\lambda < \text{Min } (1.5\lambda)$

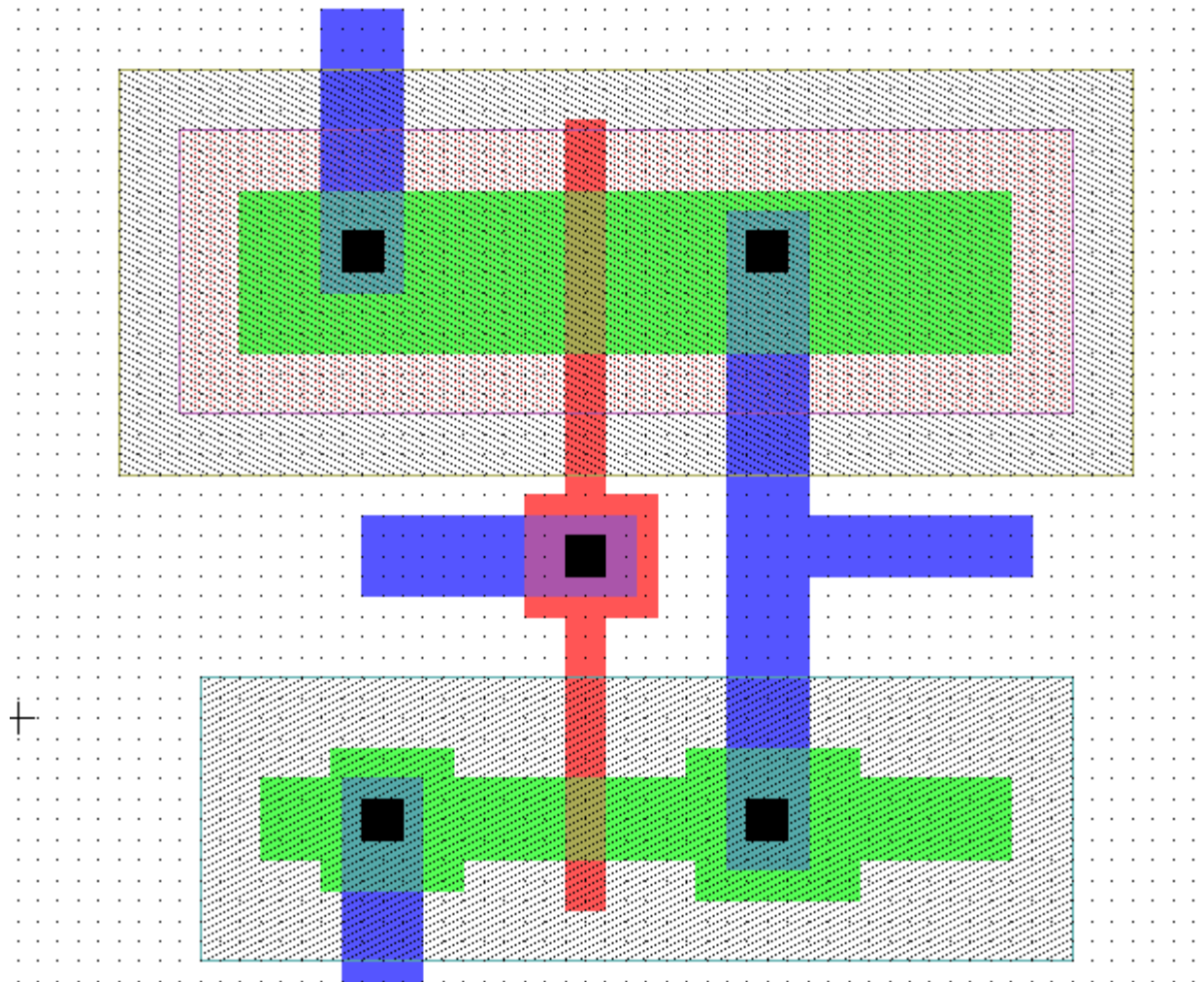
## 6.5. Active Contact and Metal Layer for Drain/Source Connections

- Add Extra Active Regions
- Press shift and select them all
- Merge them together by pressing the Merge Icon



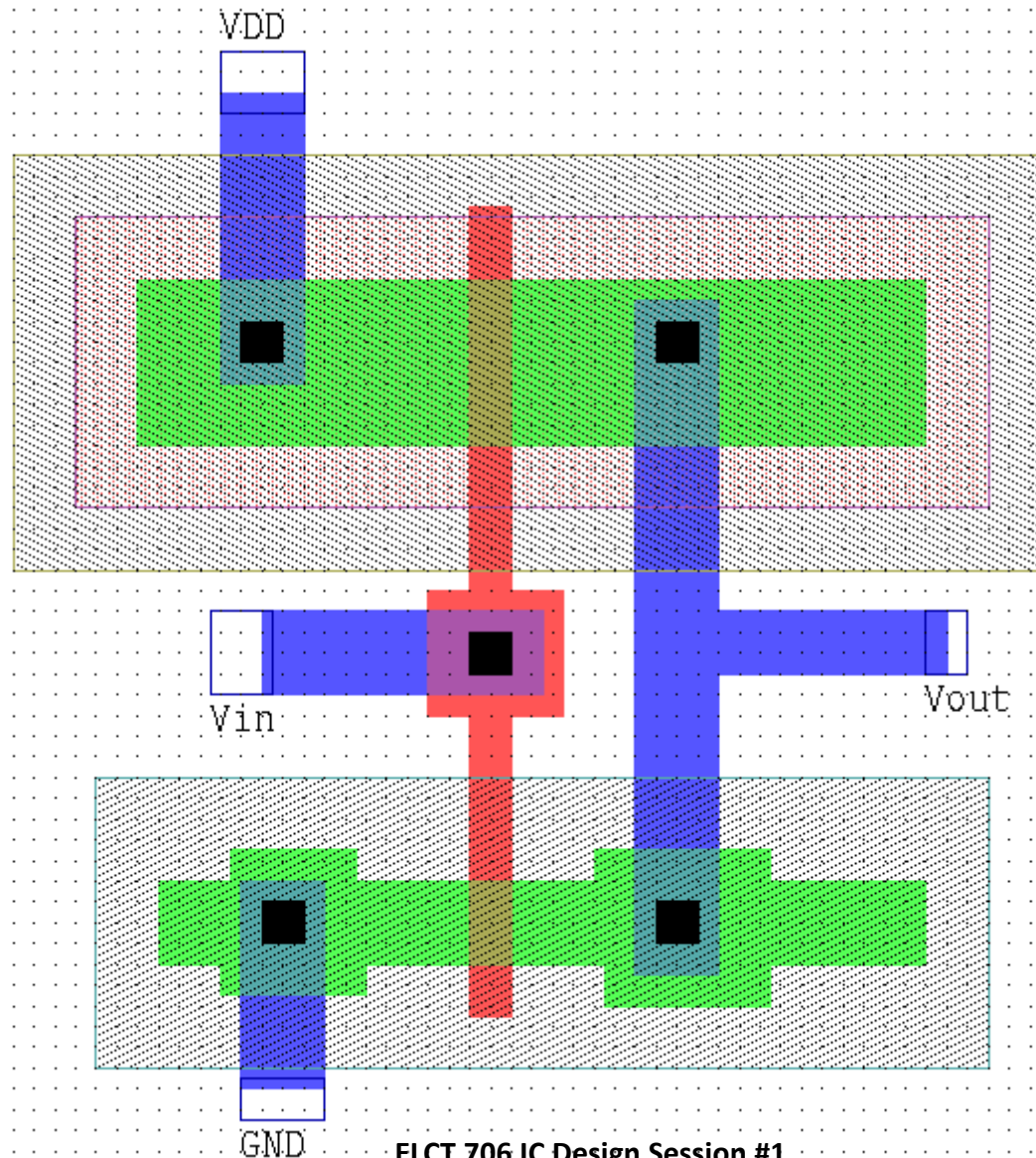


## 6.6. Poly Contact and Metal Layer for Gate Connections

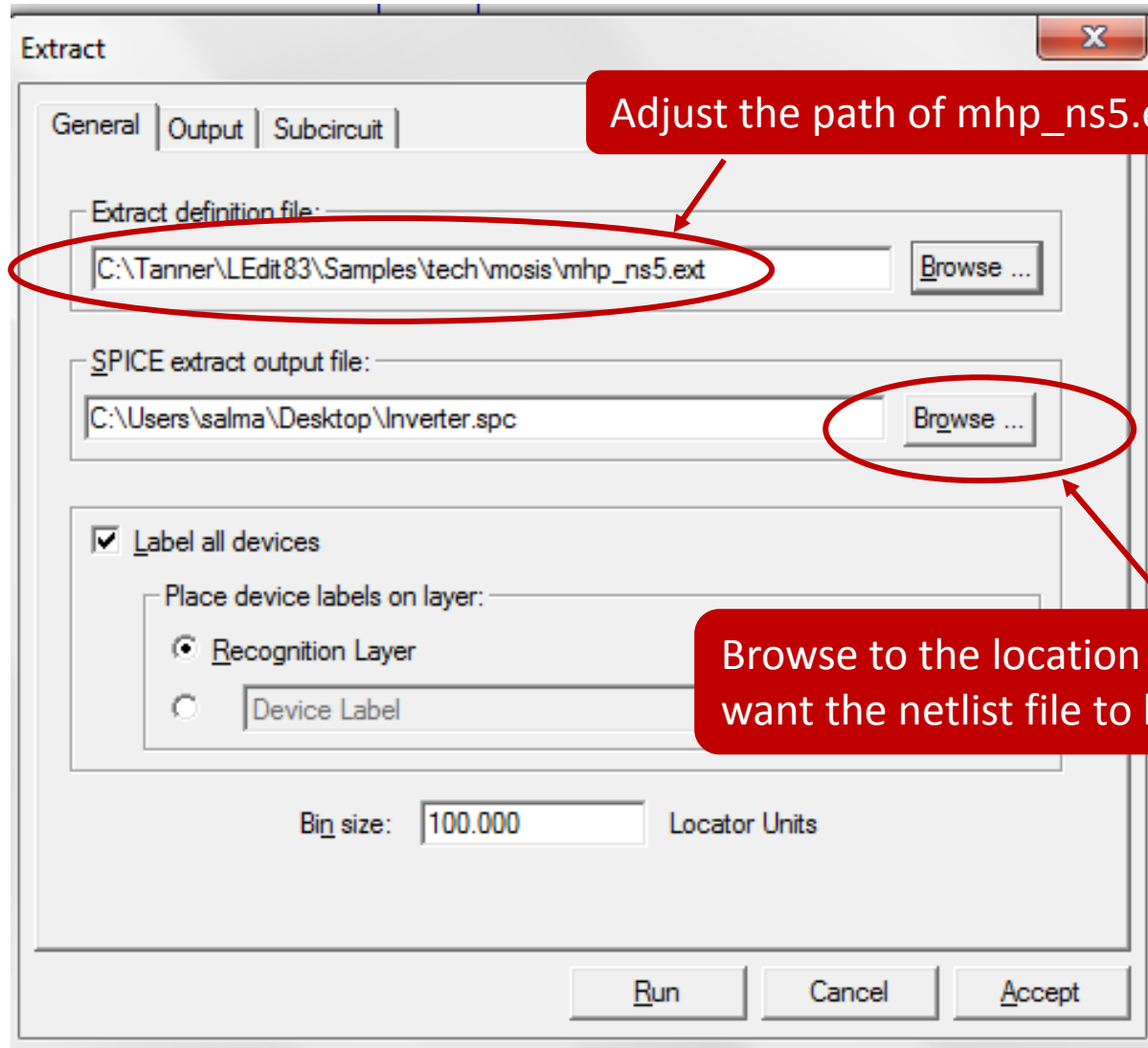




## 6.7. Add Port Names



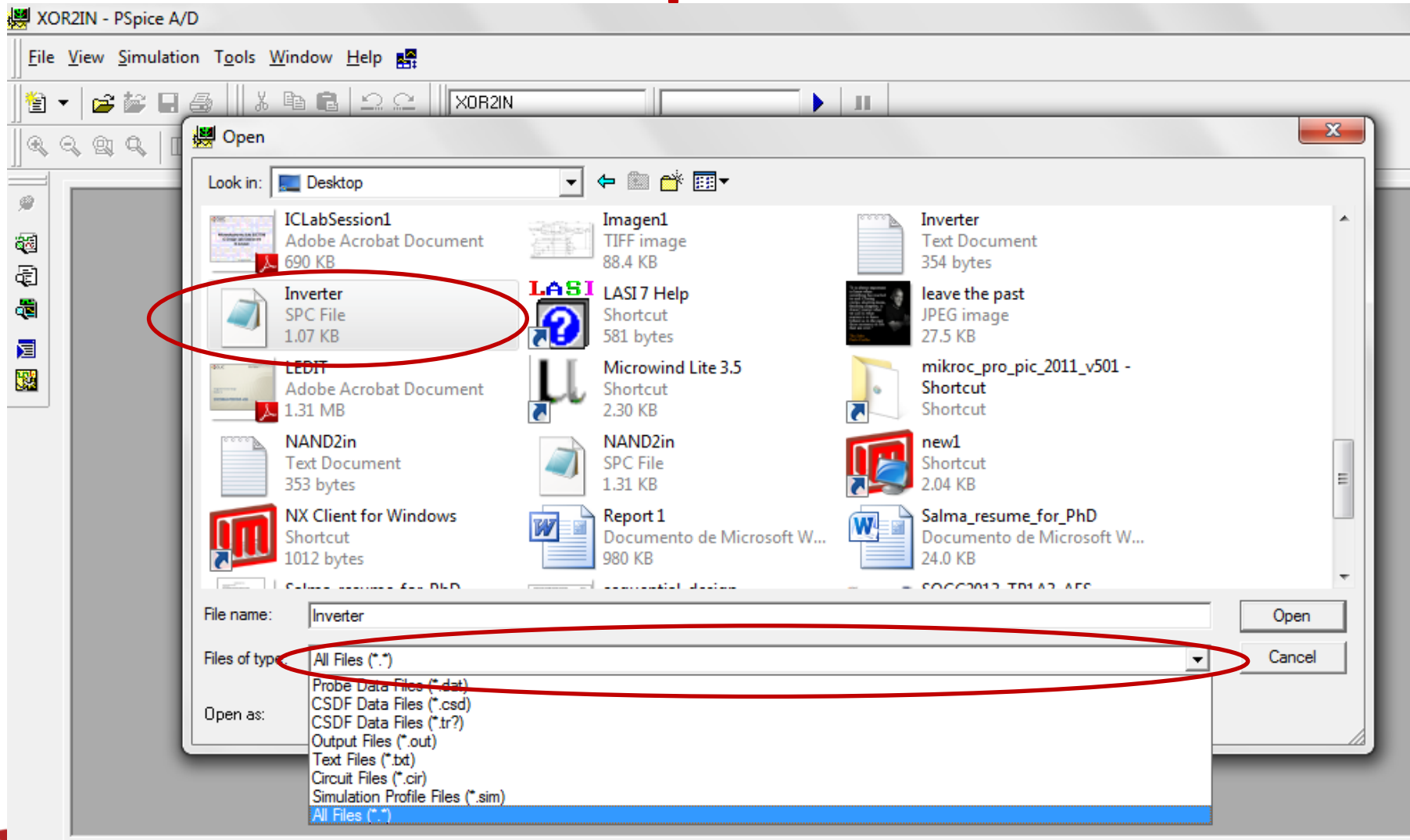
# 7. Extract the netlist of the layout



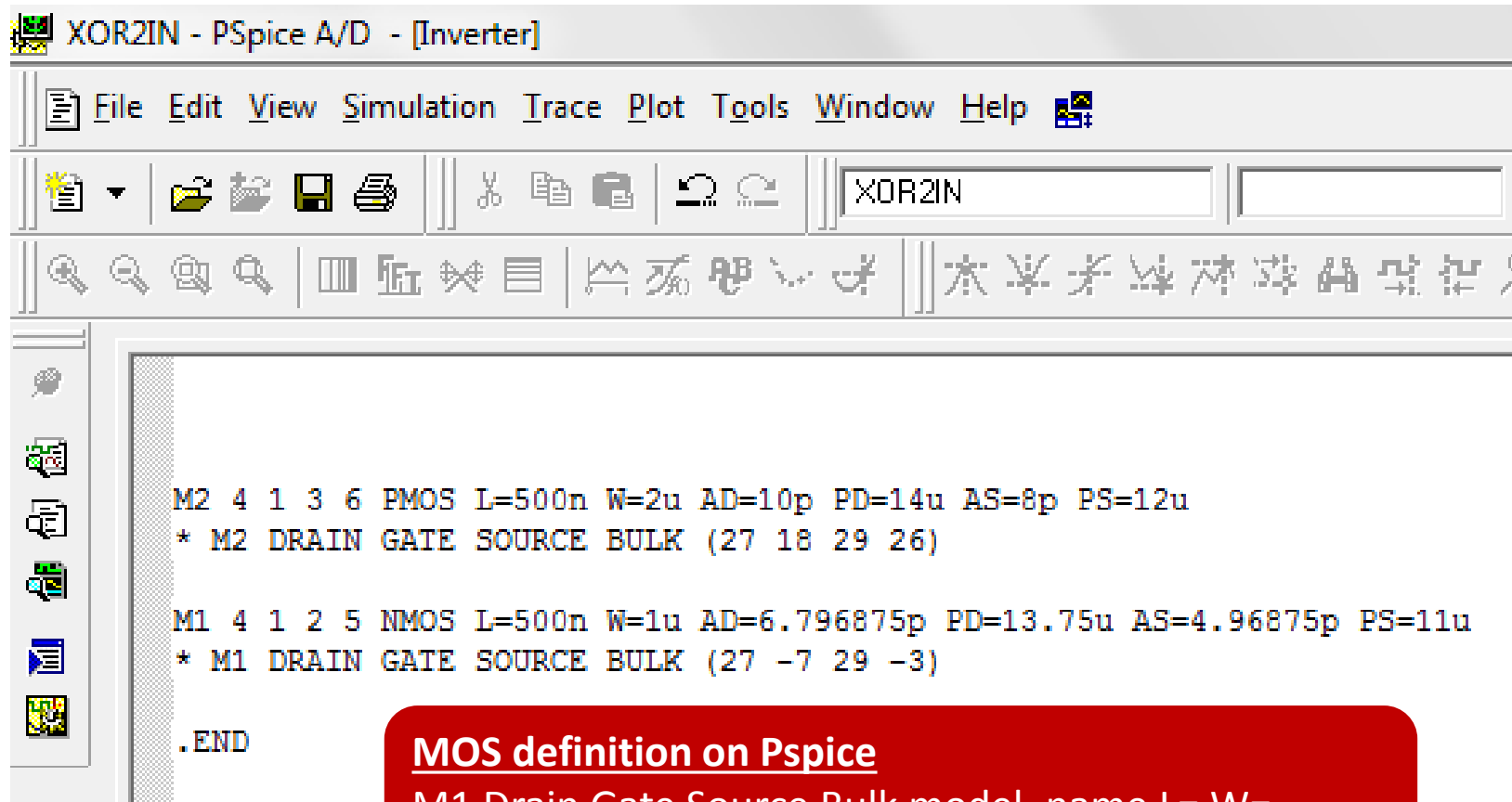
Adjust the path of mhp\_ns5.ext

Browse to the location where you want the netlist file to be generated

# 8. Open the Generated Netlist file on PSpice



# 9. Check the generated netlist and Adjust the nodes as required



The screenshot shows the PSpice A/D software window titled "XOR2IN - PSpice A/D - [Inverter]". The window has a menu bar (File, Edit, View, Simulation, Trace, Plot, Tools, Window, Help) and a toolbar with various icons. The main text area displays the following netlist:

```
M2 4 1 3 6 PMOS L=500n W=2u AD=10p PD=14u AS=8p PS=12u
* M2 DRAIN GATE SOURCE BULK (27 18 29 26)

M1 4 1 2 5 NMOS L=500n W=1u AD=6.796875p PD=13.75u AS=4.96875p PS=11u
* M1 DRAIN GATE SOURCE BULK (27 -7 29 -3)

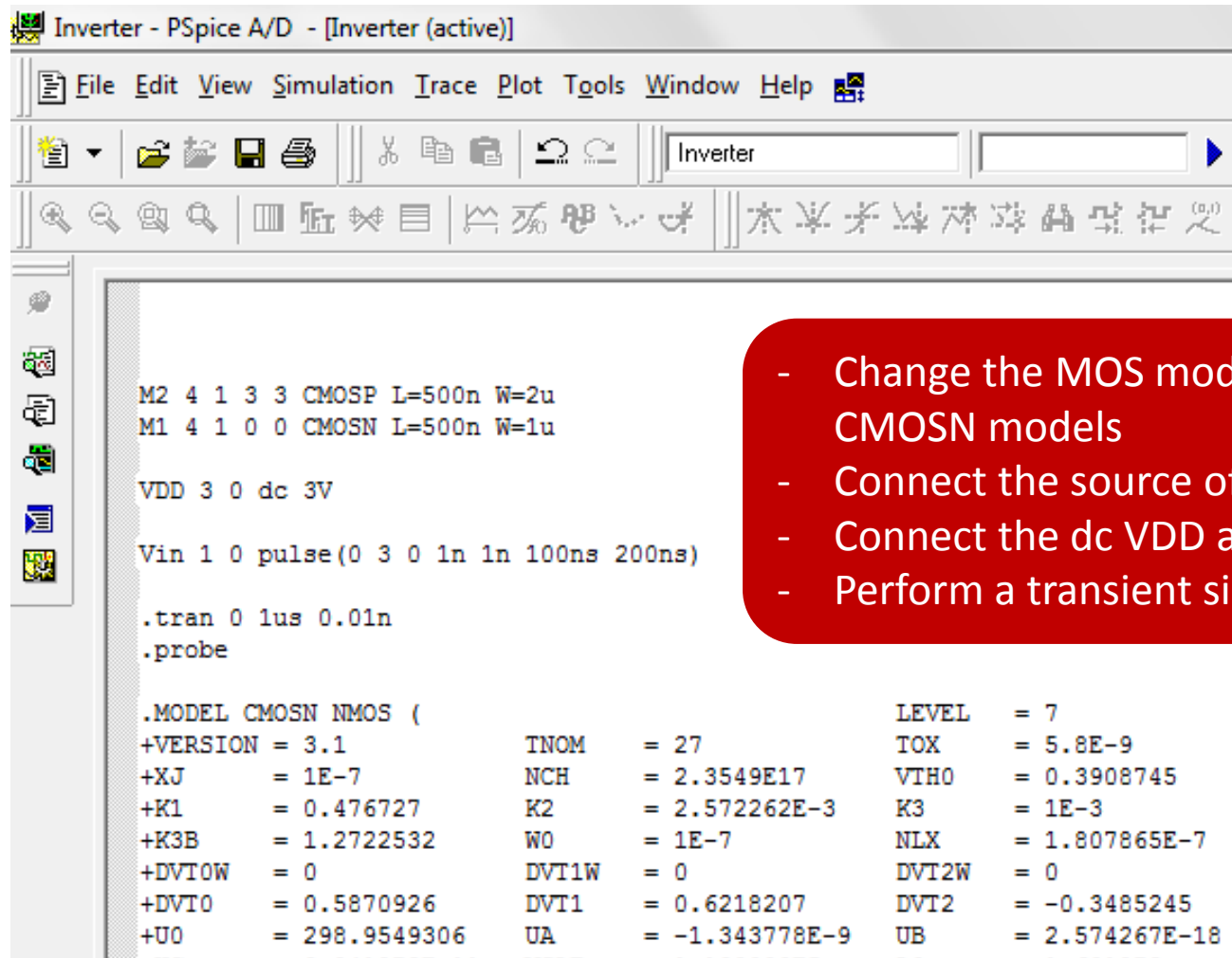
.END
```

## MOS definition on Pspice

M1 Drain Gate Source Bulk model\_name L= W=

→ **N.B.** We will Connect the Source and Bulk together

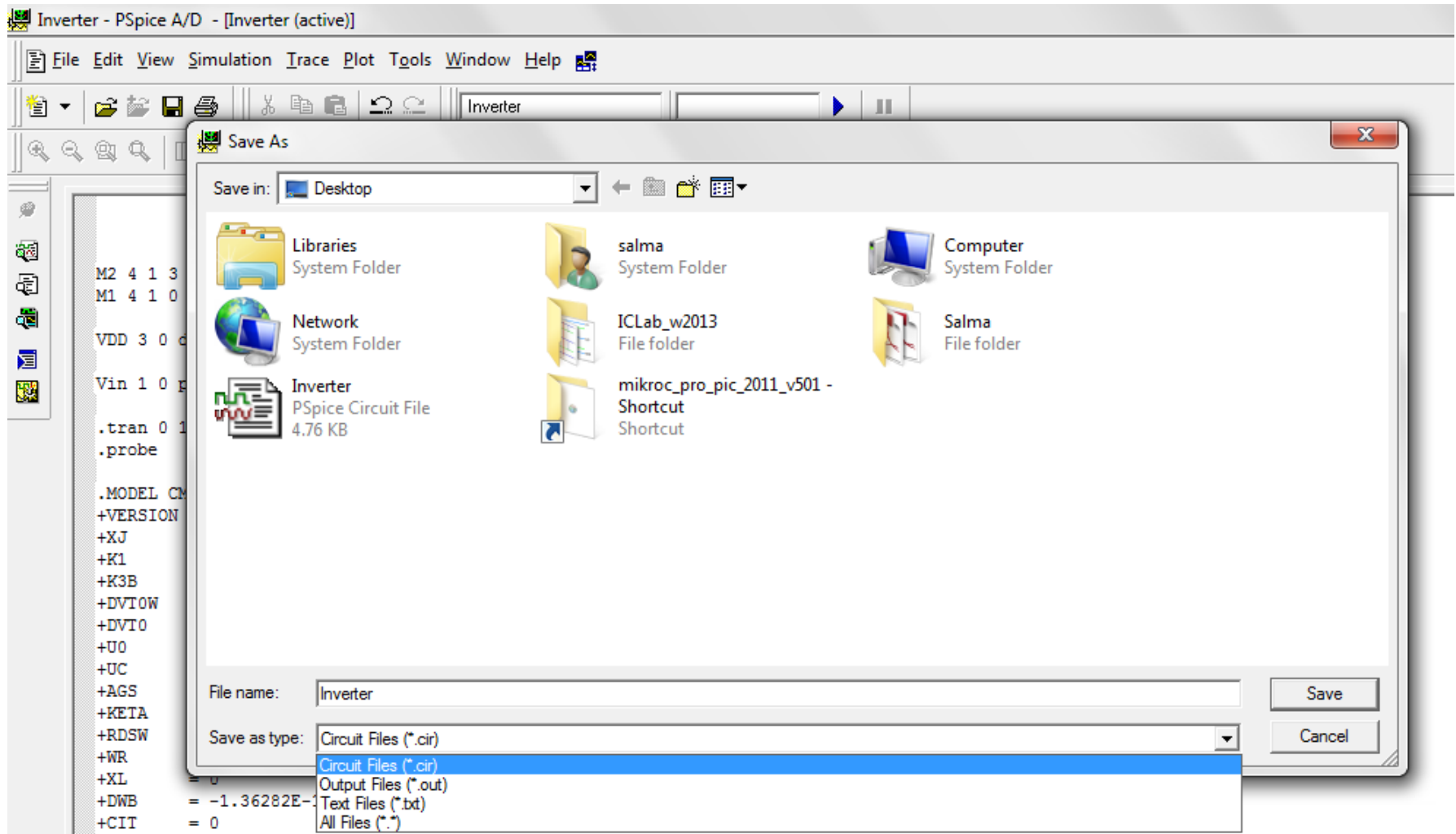
# 9. Check the generated netlist and Adjust the nodes as required



```
Inverter - PSpice A/D - [Inverter (active)]
File Edit View Simulation Trace Plot Tools Window Help
Inverter
M2 4 1 3 3 CMOSF L=500n W=2u
M1 4 1 0 0 CMOSN L=500n W=1u
VDD 3 0 dc 3V
Vin 1 0 pulse(0 3 0 1n 1n 100ns 200ns)
.tran 0 1us 0.01n
.probe
.MODEL CMOSN NMOS (
+VERSION = 3.1          TNOM    = 27          TOX      = 5.8E-9
+XJ         = 1E-7       NCH     = 2.3549E17   VTH0     = 0.3908745
+K1         = 0.476727   K2      = 2.572262E-3  K3       = 1E-3
+K3B        = 1.2722532  W0      = 1E-7       NLX      = 1.807865E-7
+DVT0W      = 0          DVT1W   = 0          DVT2W    = 0
+DVT0       = 0.5870926  DVT1   = 0.6218207   DVT2     = -0.3485245
+U0         = 298.9549306 UA      = -1.343778E-9  UB       = 2.574267E-18
```

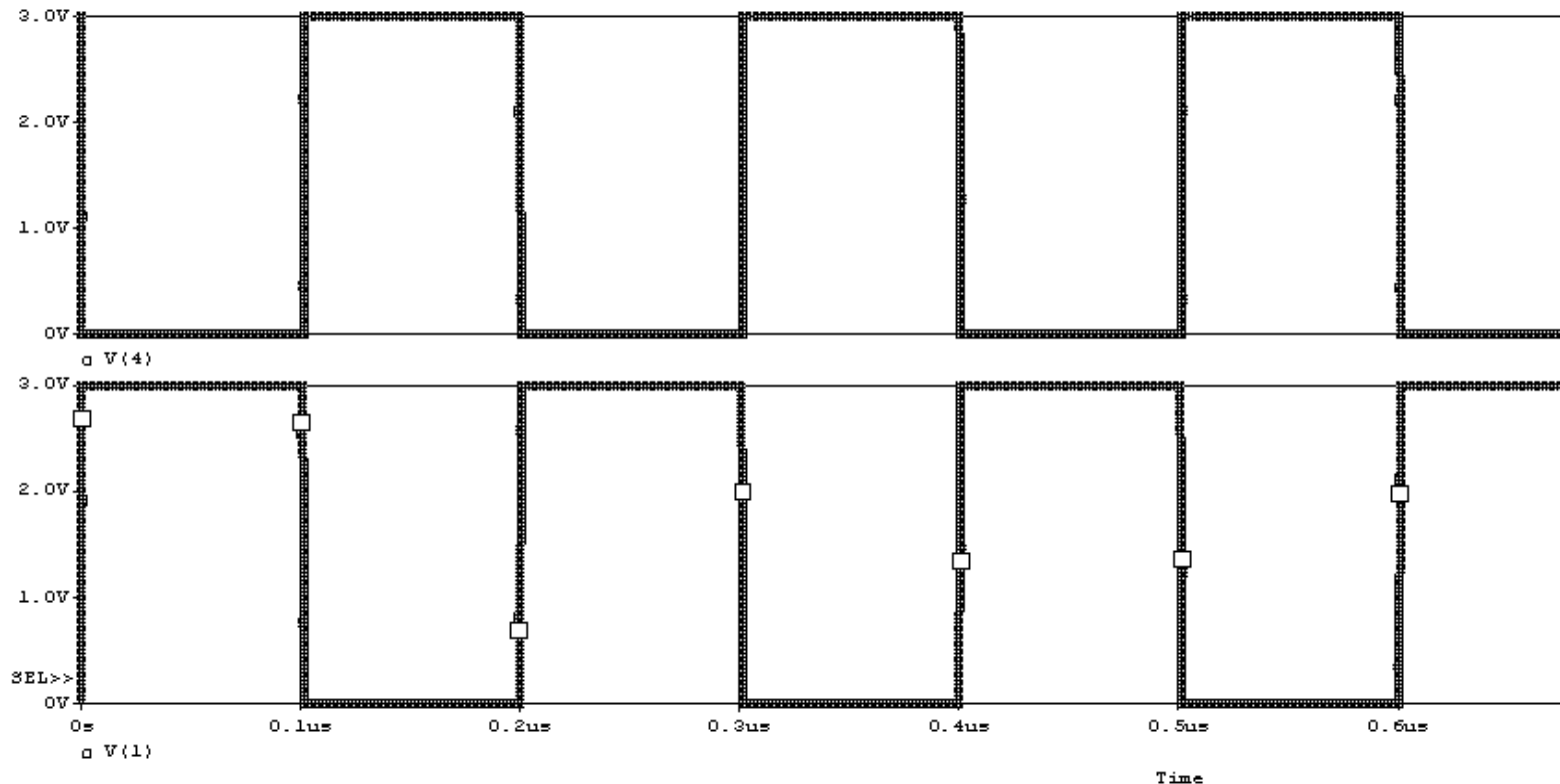
- Change the MOS models to CMOSF and CMOSN models
- Connect the source of the NMOS to GND
- Connect the dc VDD and the pulse Vin
- Perform a transient simulation

# 10. Save the Netlist as .cir file then Re-open the .cir file



# 10. Simulate the netlist to test the inverter functionality

**$V_{out} = V(4)$**



**$V_{in} = V(1)$**