NPTEL ONLINE CERTIFICATION COURSES

DIGITAL CONTROL IN SMPCs AND FPGA-BASED PROTOTYPING

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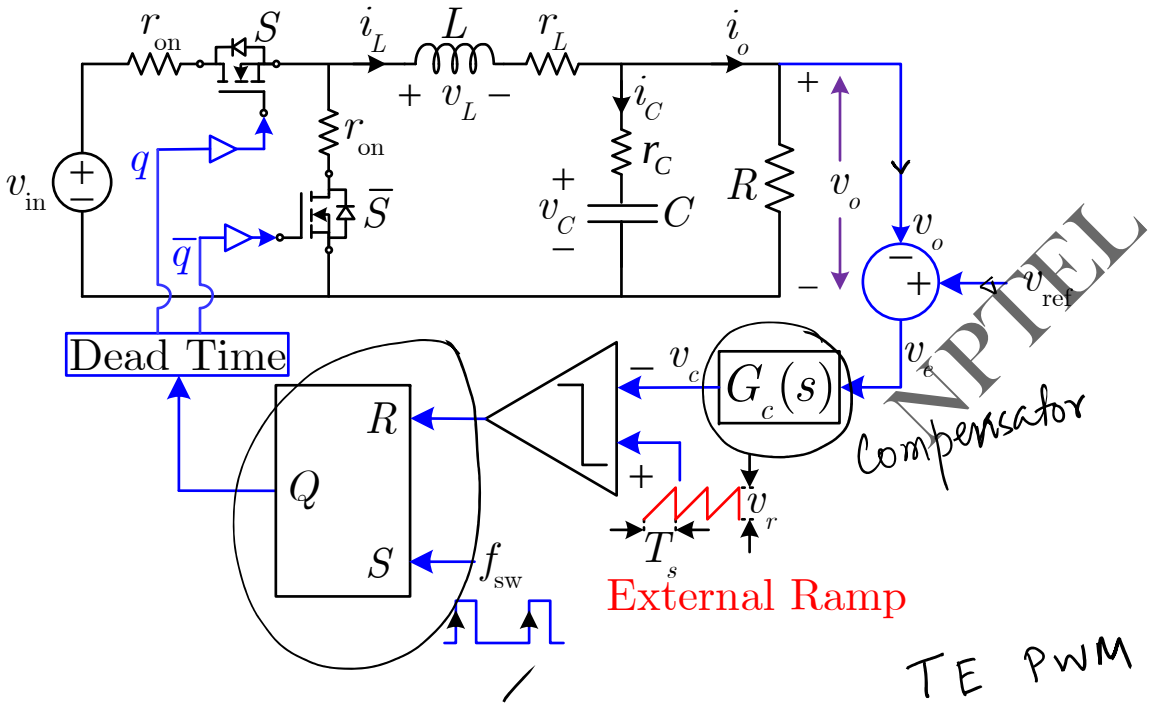
Module 01: Introduction to Digital Control in SMPCs

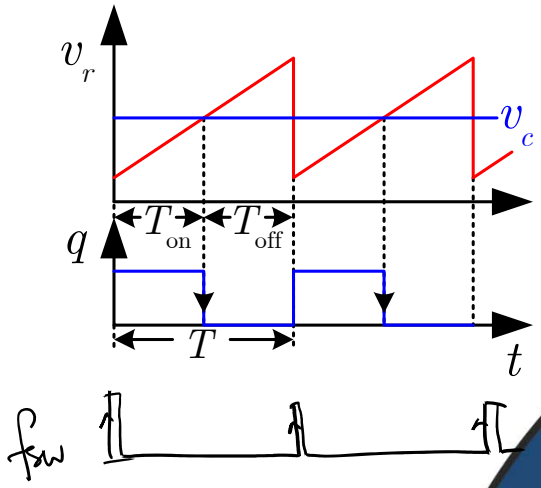
Lecture 08: Levels of Digitization in Single-loop Feedback Control in SMPCs

CONCEPTS COVERED

- Recap of analog voltage mode control
- Digitizing single feedback loop
- Sampling and quantization
- Sampling delay and timing diagrams
- Summary of single-loop digital control

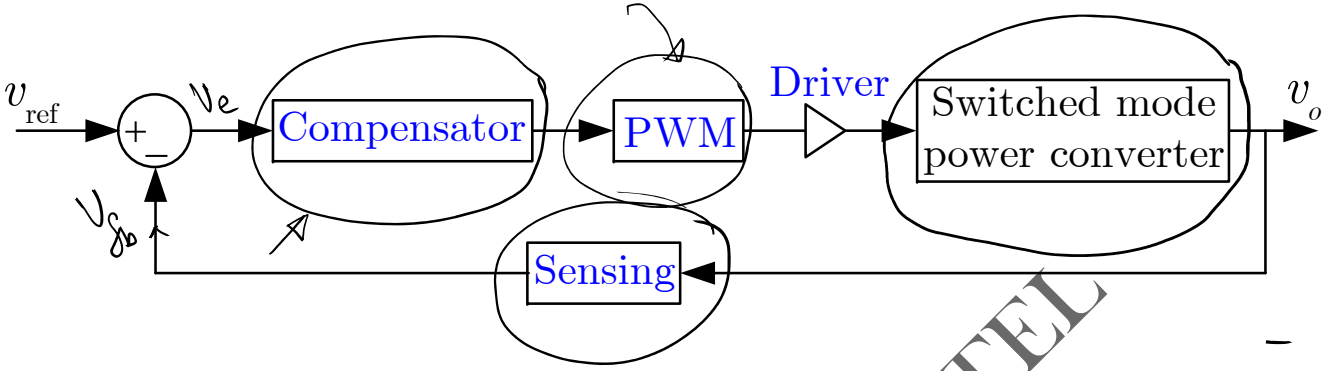
Analog Voltage Mode Control

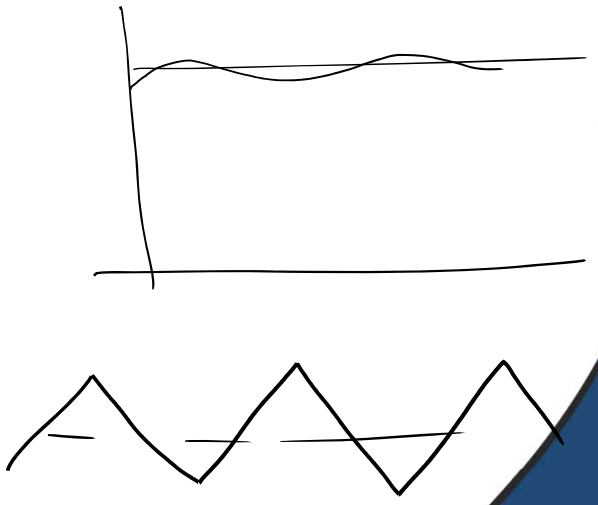




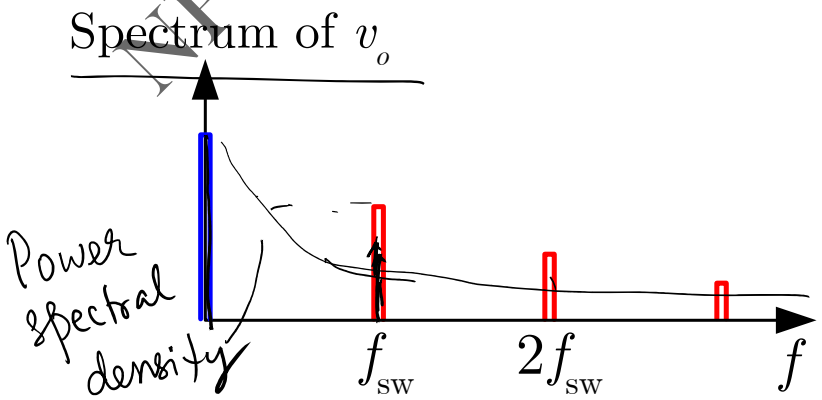
TE PWM

Analog Voltage Mode Control (contd…)

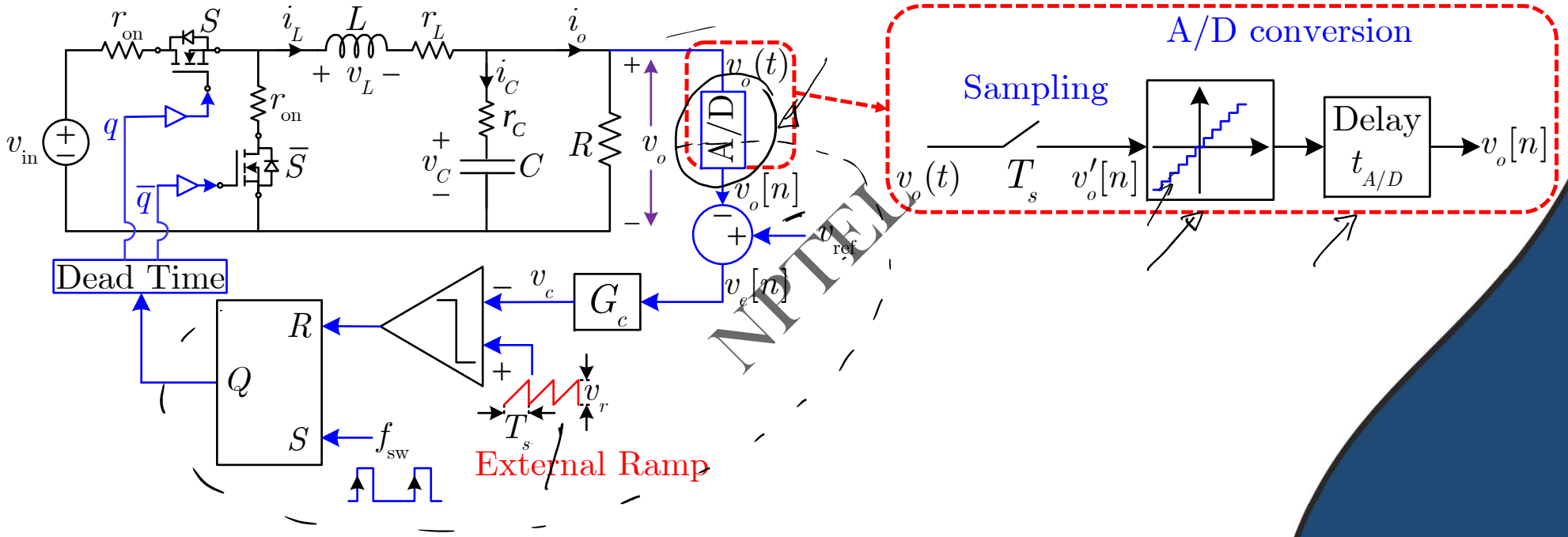




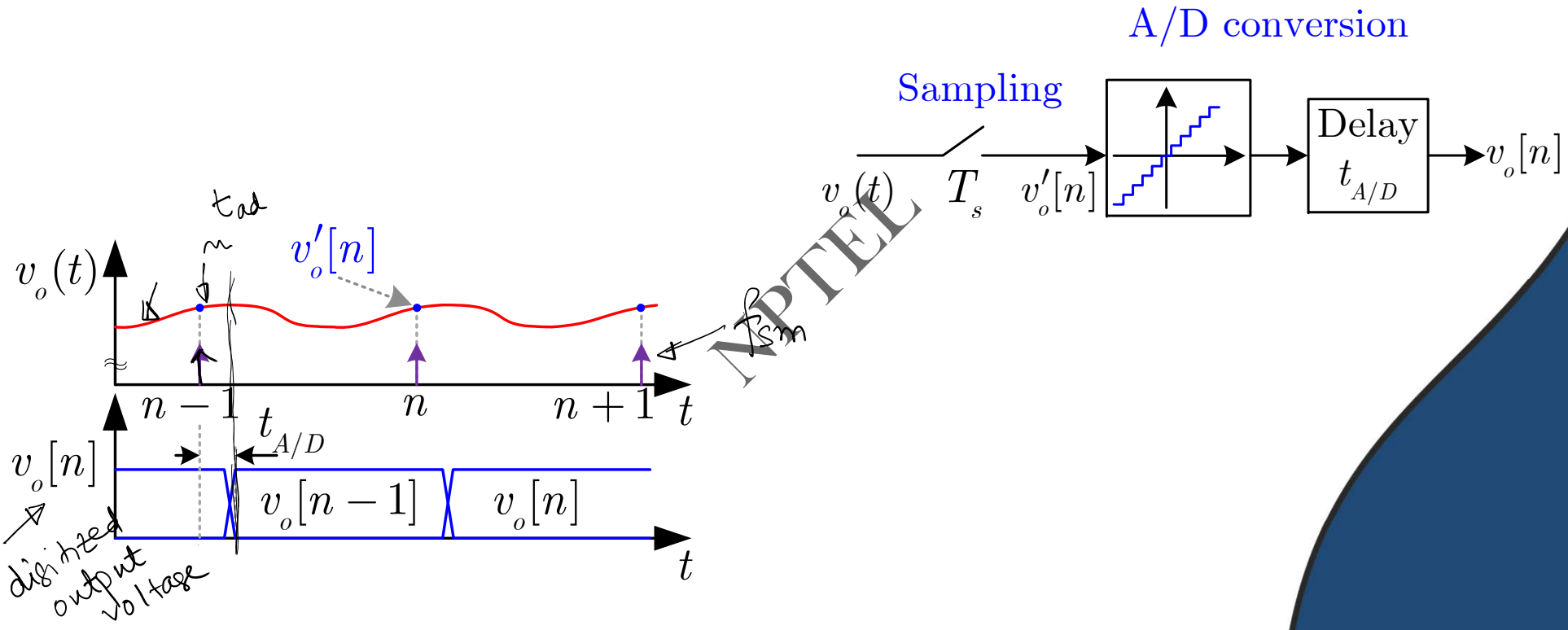
A pole at Nyquist frequency needed to attenuate switching noise in analog feedback voltage loop



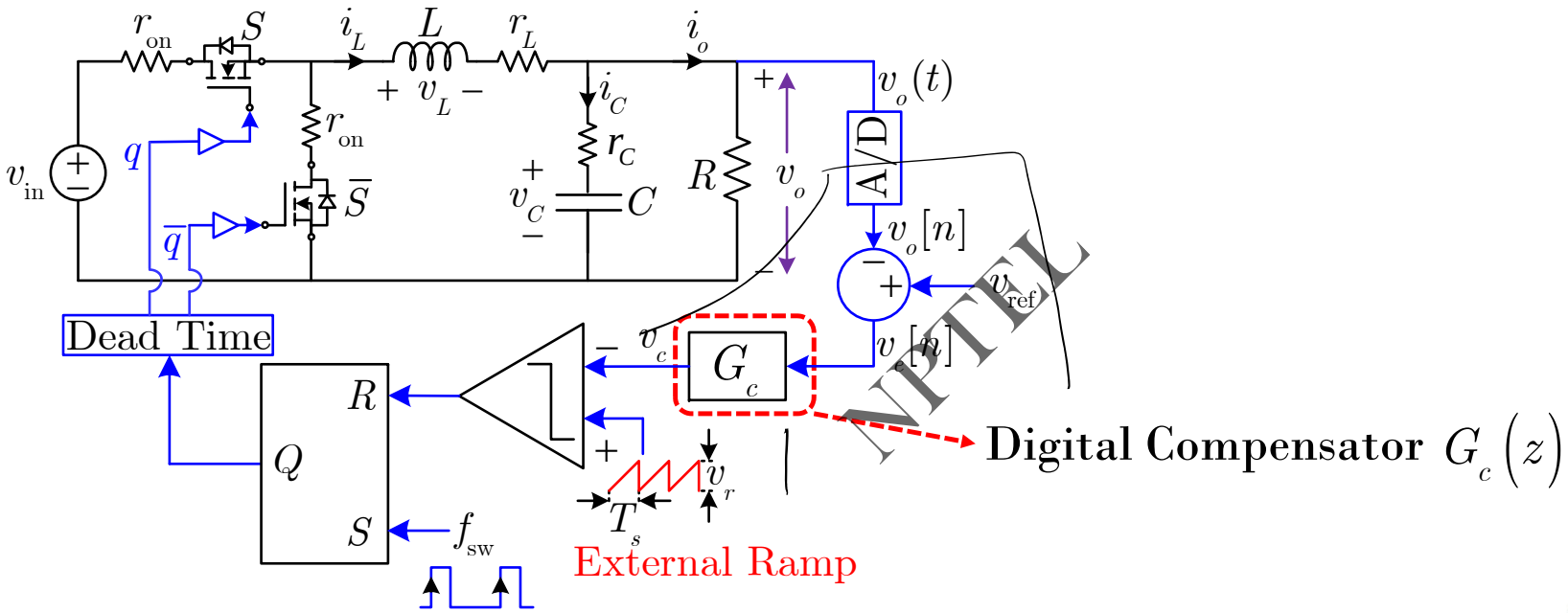
Closing Digital Loop



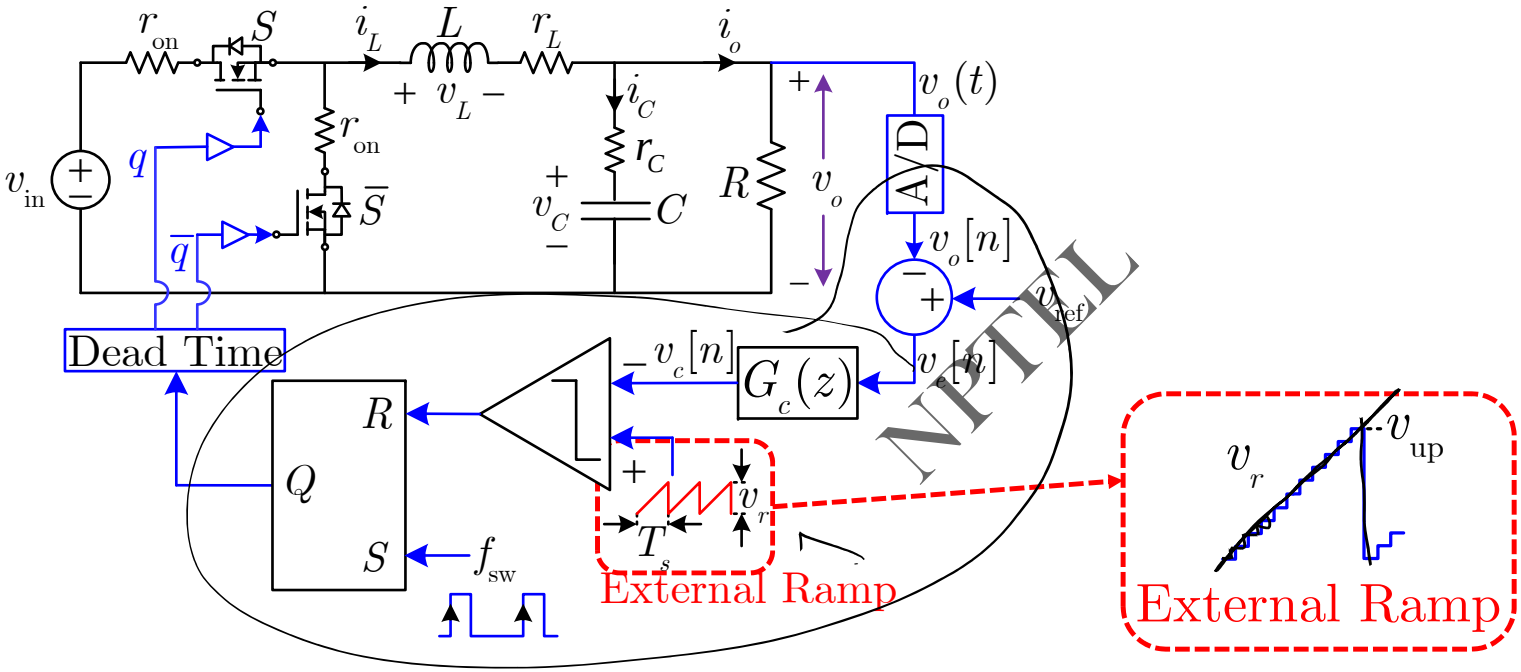
Closing Digital Loop (contd…)



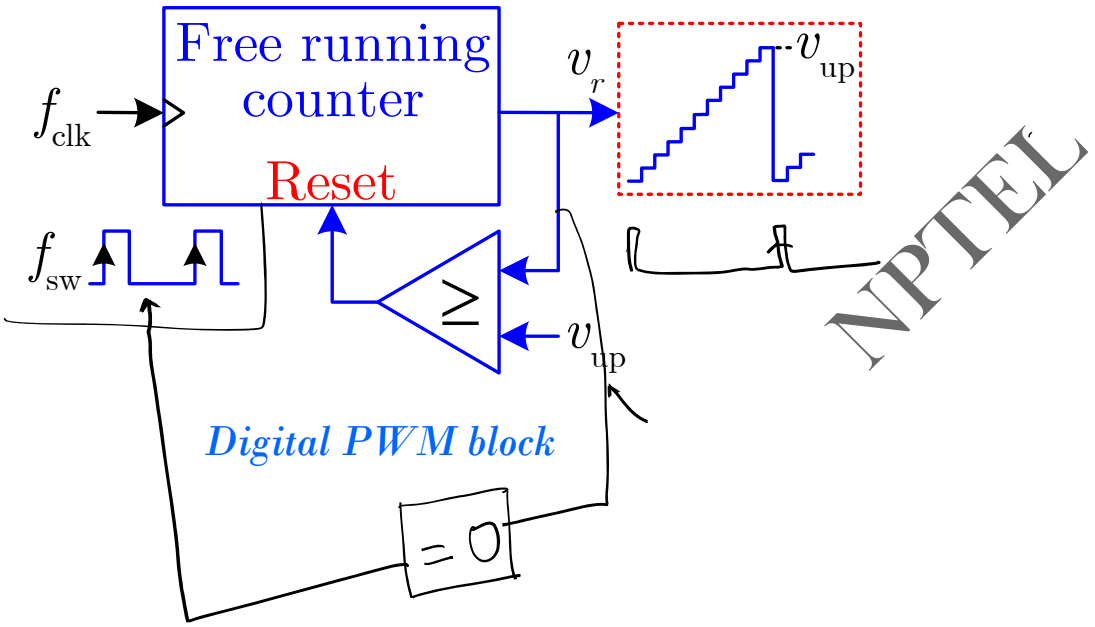
Closing Digital Loop (contd…)

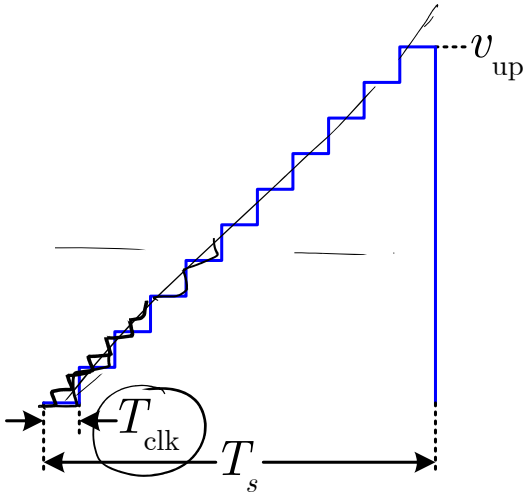


Closing Digital Loop (contd…)



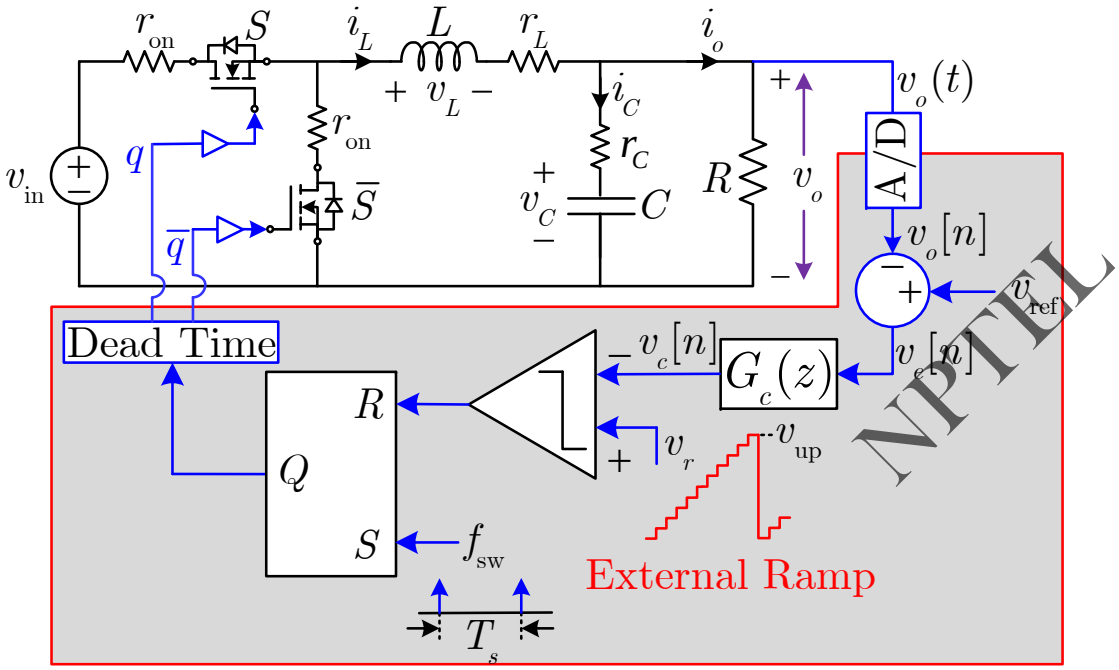
Closing Digital Loop (contd…)





$$T_s = \frac{1}{f_{sw}}$$

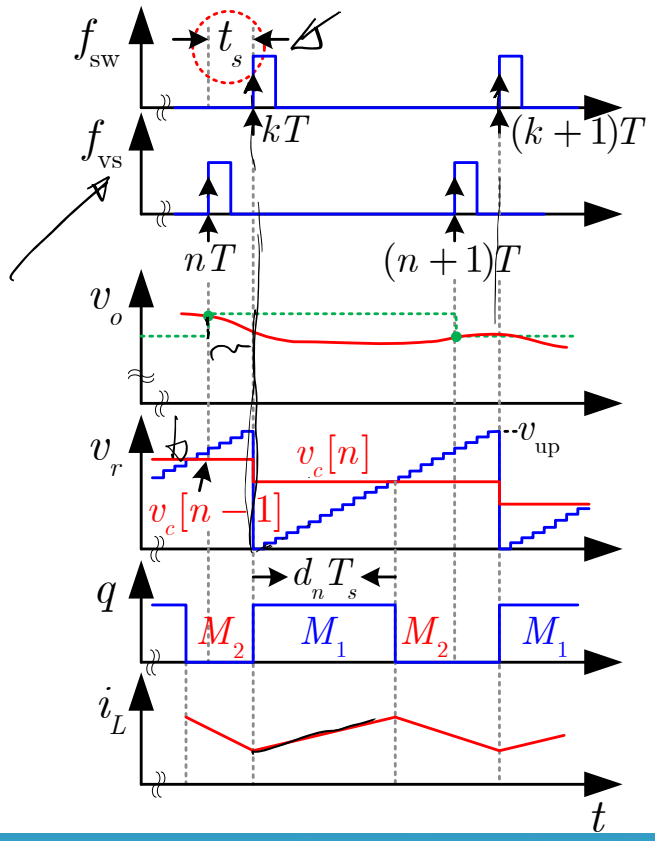
Digital Voltage Mode Control

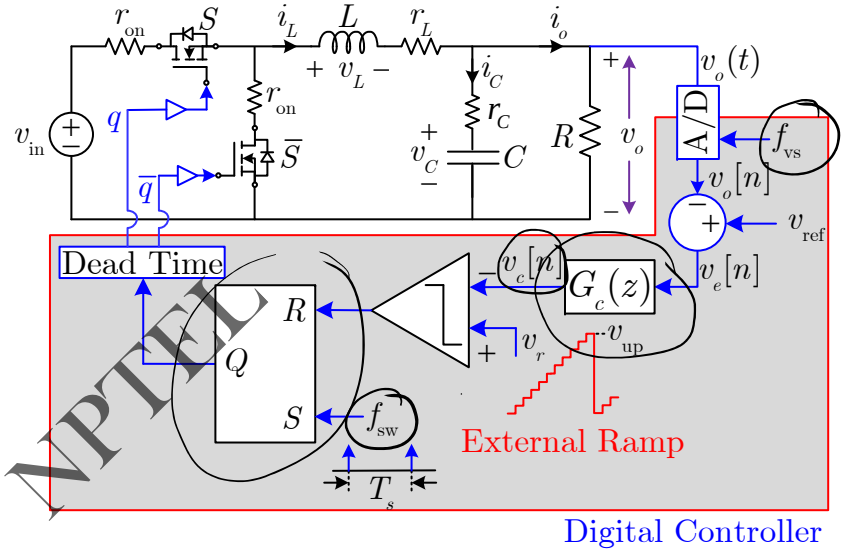


Digital Controller

DPWM voltage-mode control: Buck Converter

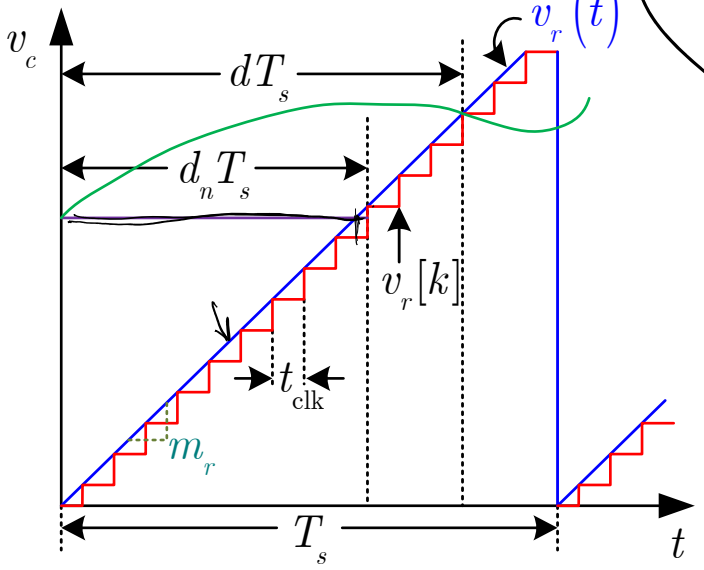
Digital Voltage Mode Control (contd…)

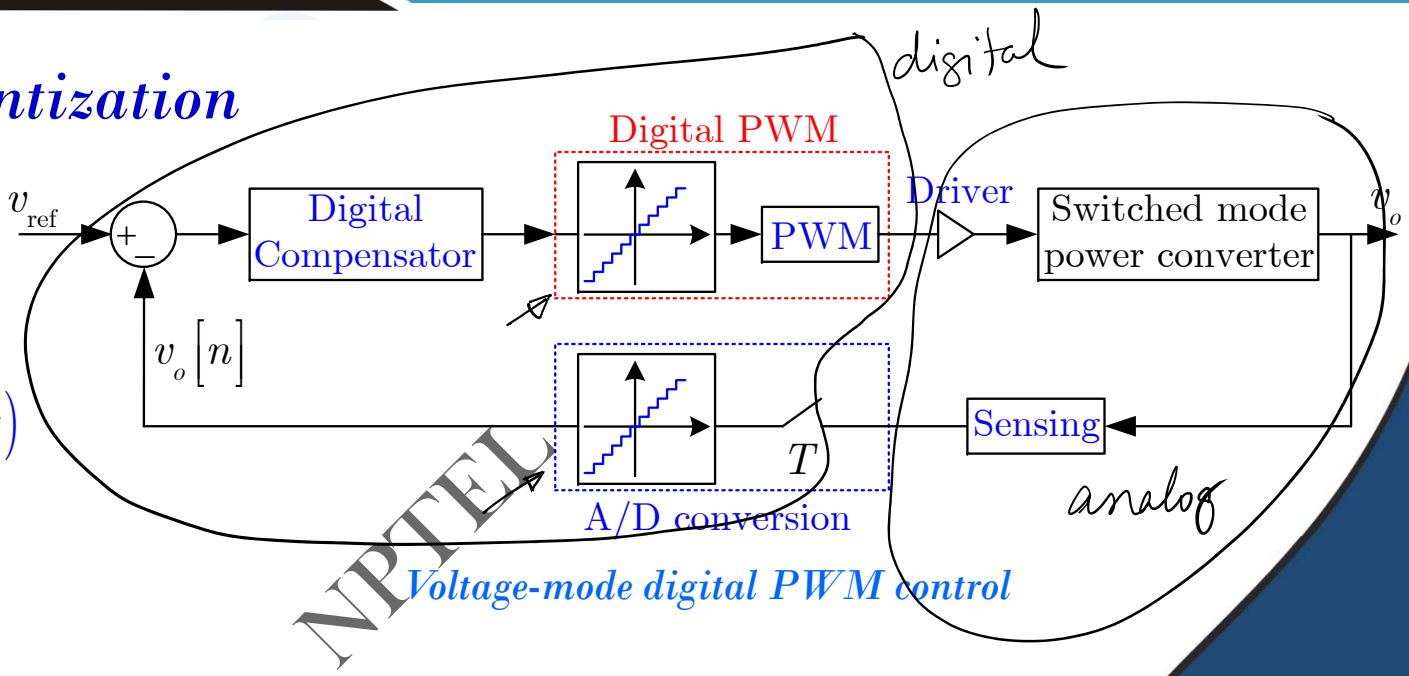




Delay – maybe even larger than switching period !!

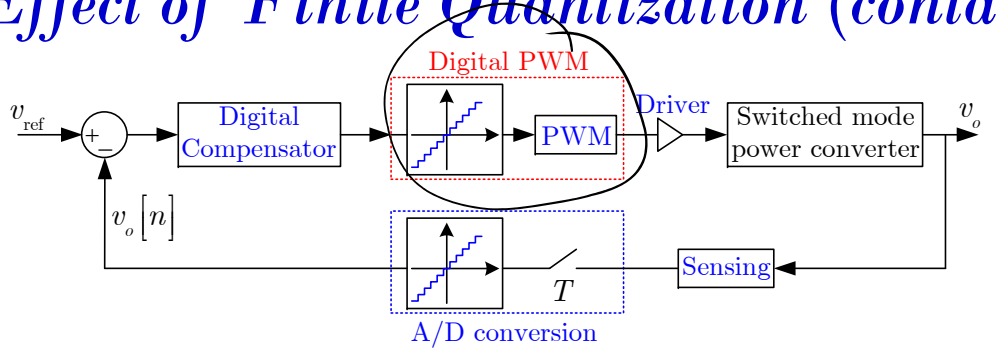
Effect of Finite Quantization



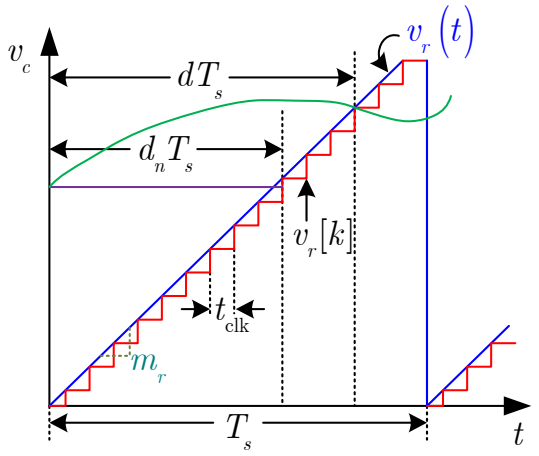


Voltage-mode digital PWM control

Effect of Finite Quantization (contd…)



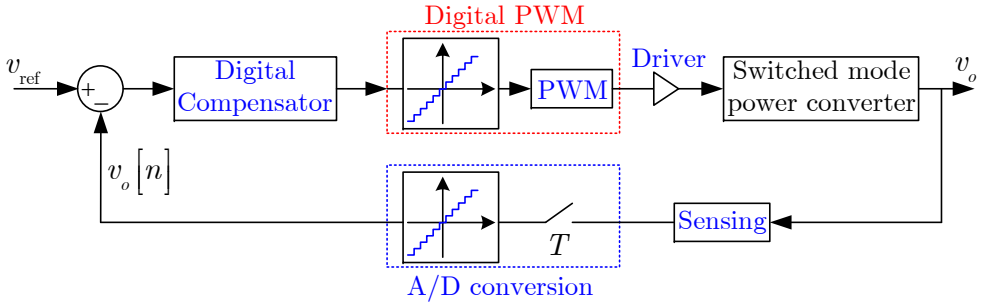
Voltage-mode digital PWM control



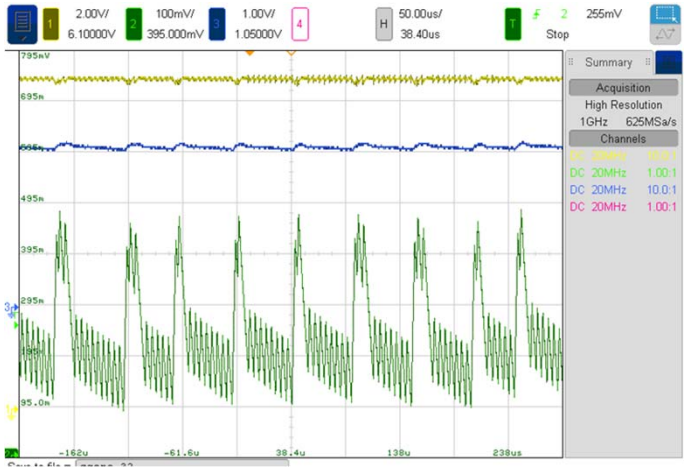
If DPWM resolution poor than ADC

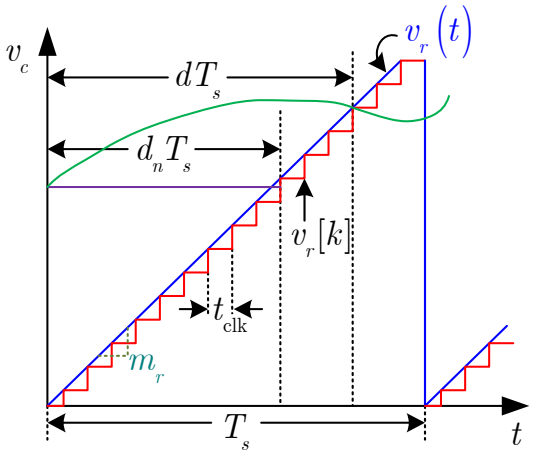
- Quantized voltage may map in between two successive staircase levels
- Exact duty ratio may not be obtained
- This would eventually take error voltage outside the zero-error-bin

Effect of Finite Quantization (contd…)



Voltage-mode digital PWM control





Results in limit cycle oscillation (LCO):

DPWM synchronous buck converter

CONCLUSION

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- Digitizing single feedback loop
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- Sampling delay and timing diagrams
- Summary of single-loop digital control

THANK YOU !