NPTEL ONLINE CERTIFICATION COURSES

DIGITAL CONTROL IN SMPCs AND FPGA-BASED PROTOTYPING

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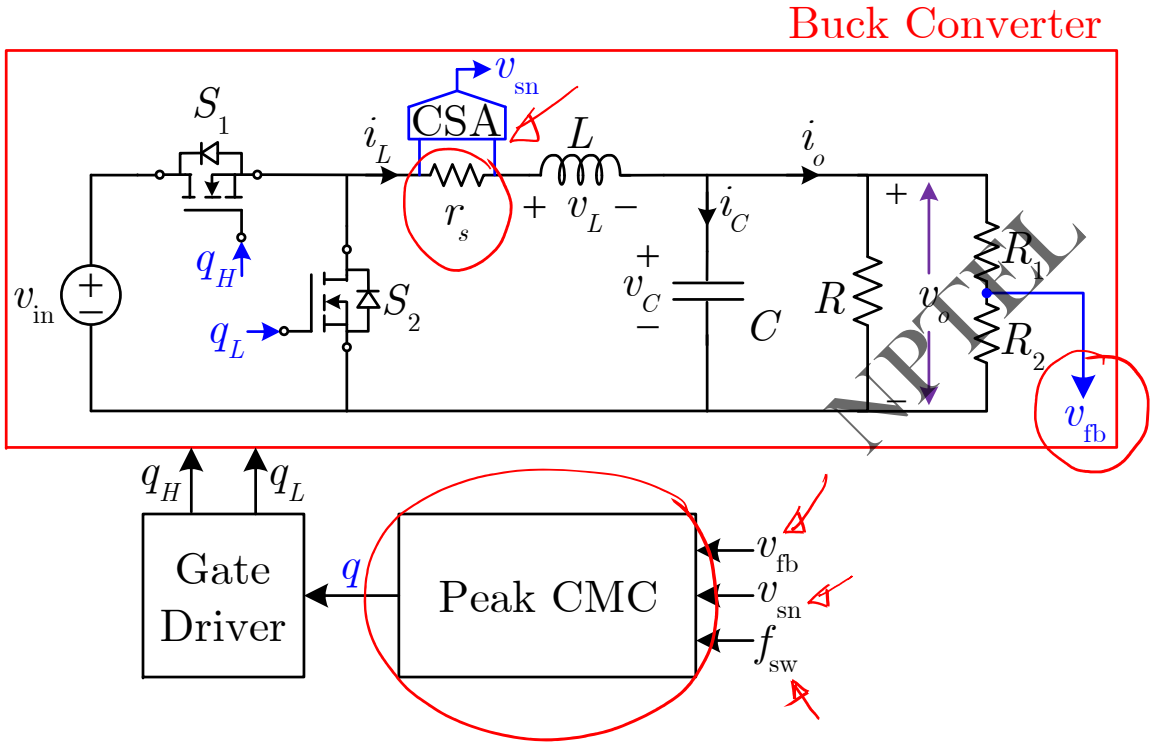
Module 01: Introduction to Digital Control in SMPCs

Lecture 09: Levels of Digitization in Multi-loop Feedback Control in SMPCs

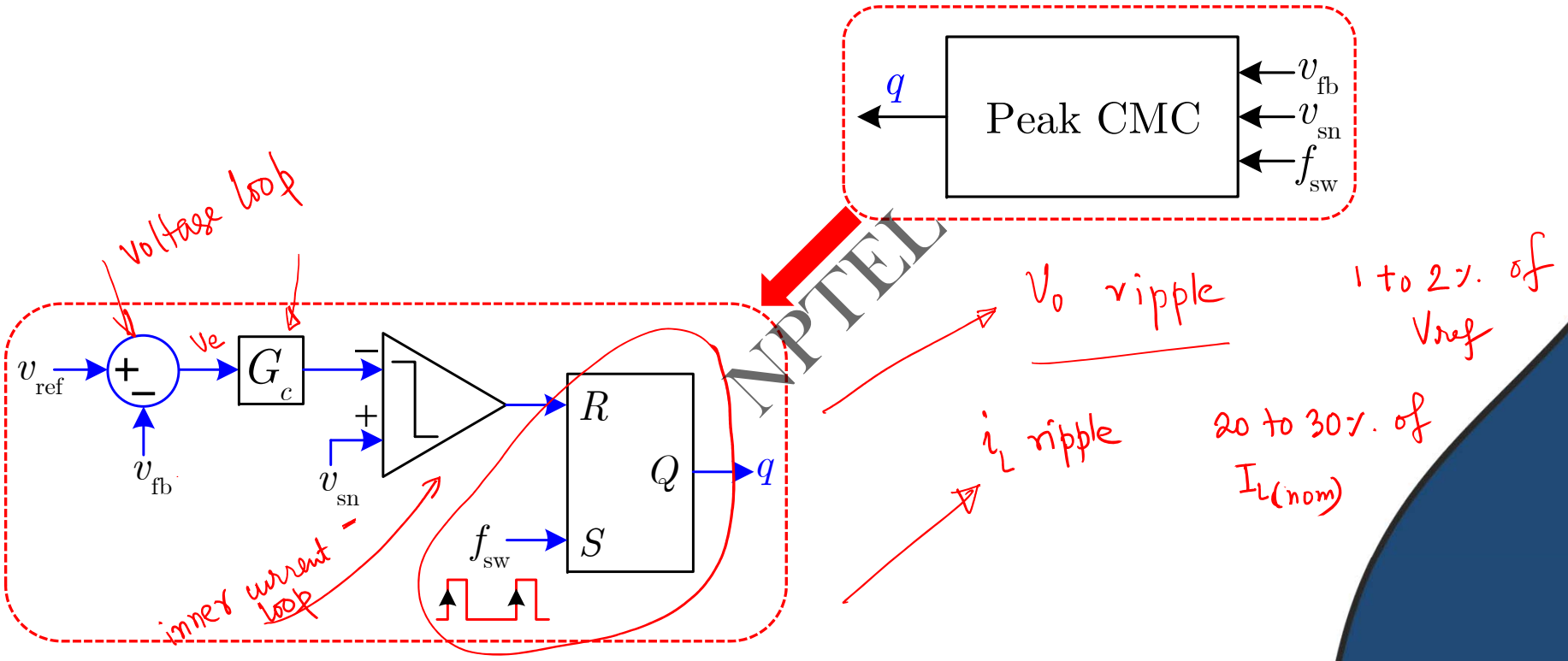
CONCEPTS COVERED

- Recap of analog current mode control
- Digitizing in multi-loop feedback control
- Sampling and quantization
- Summary of multi-loop digital control
- Performance and cost trade-offs

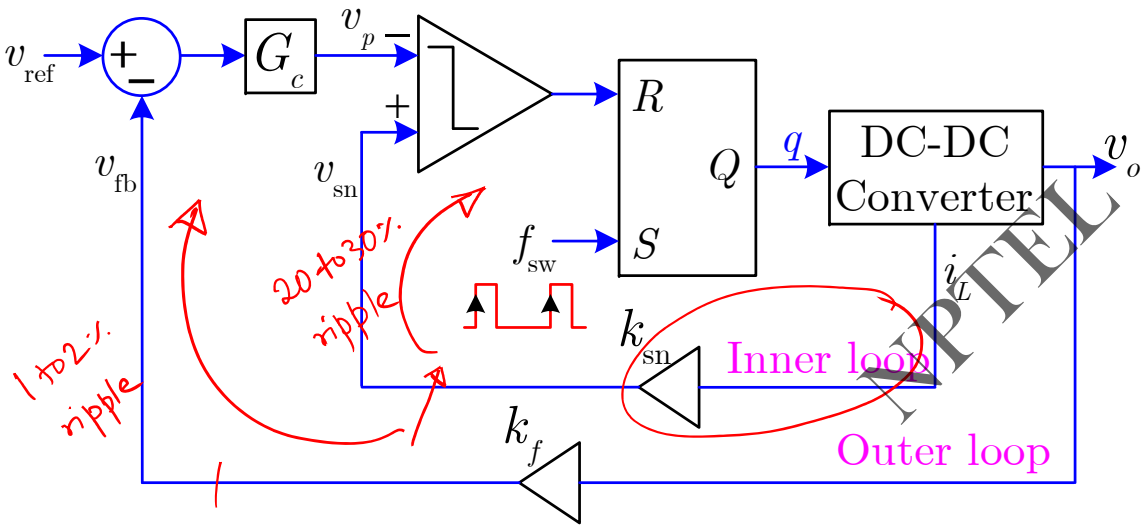
Peak CMC in a Buck Converter



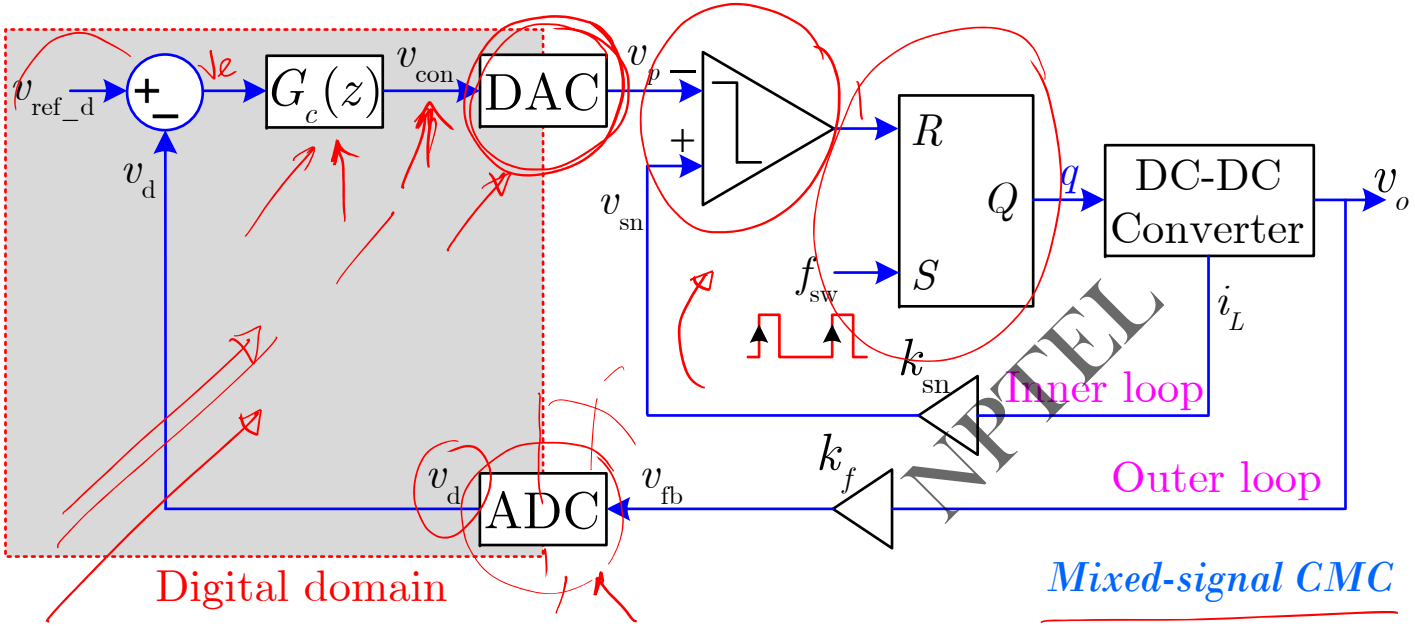
Inside Analog Peak CMC Architecture

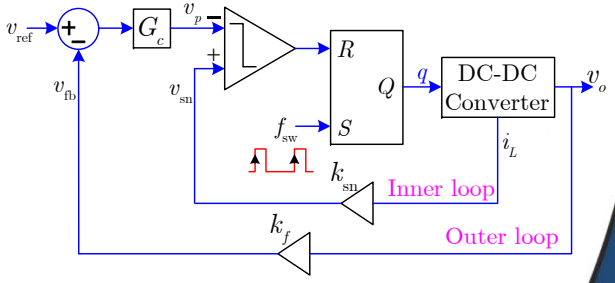


Overall Analog Current Mode Control



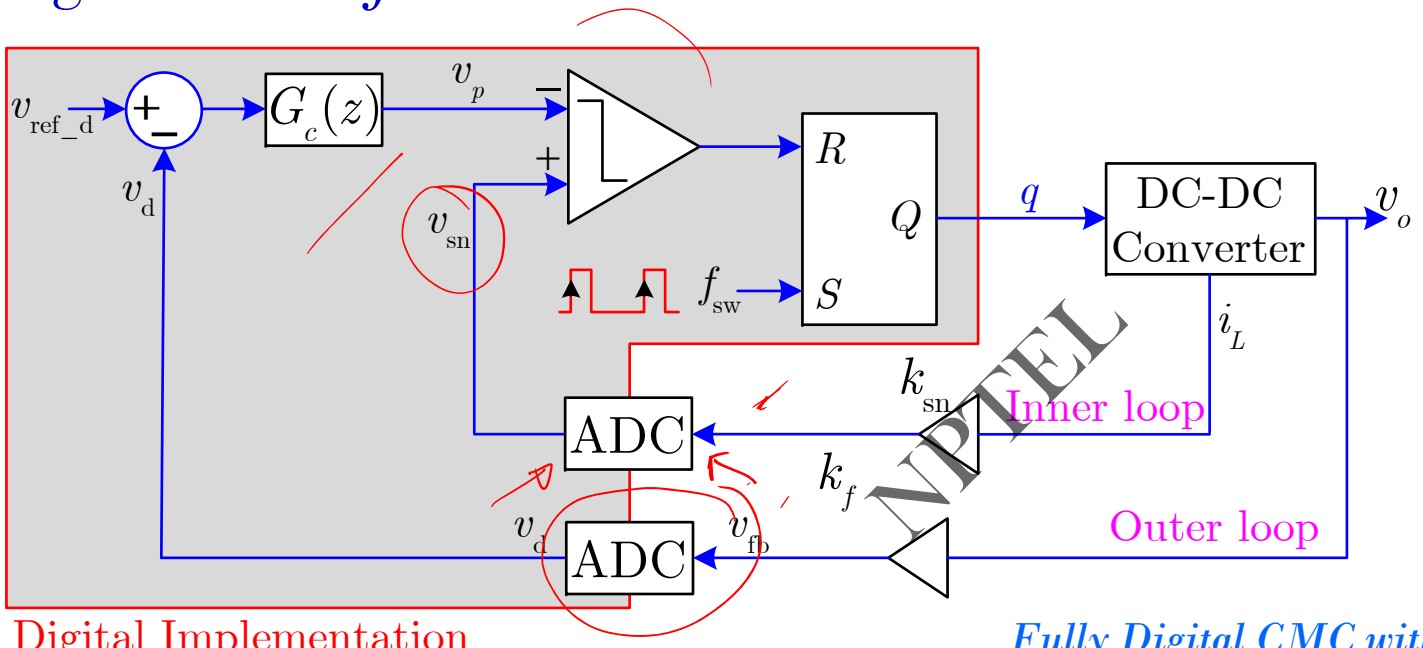
Digitization of CMC: Architecture-I



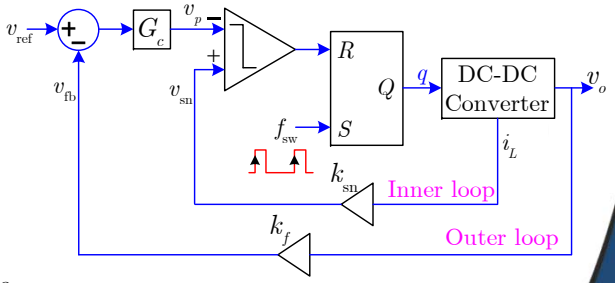


- Current feedback in analog domain
- Voltage feedback in digital domain

Digitization of CMC: Architecture-II



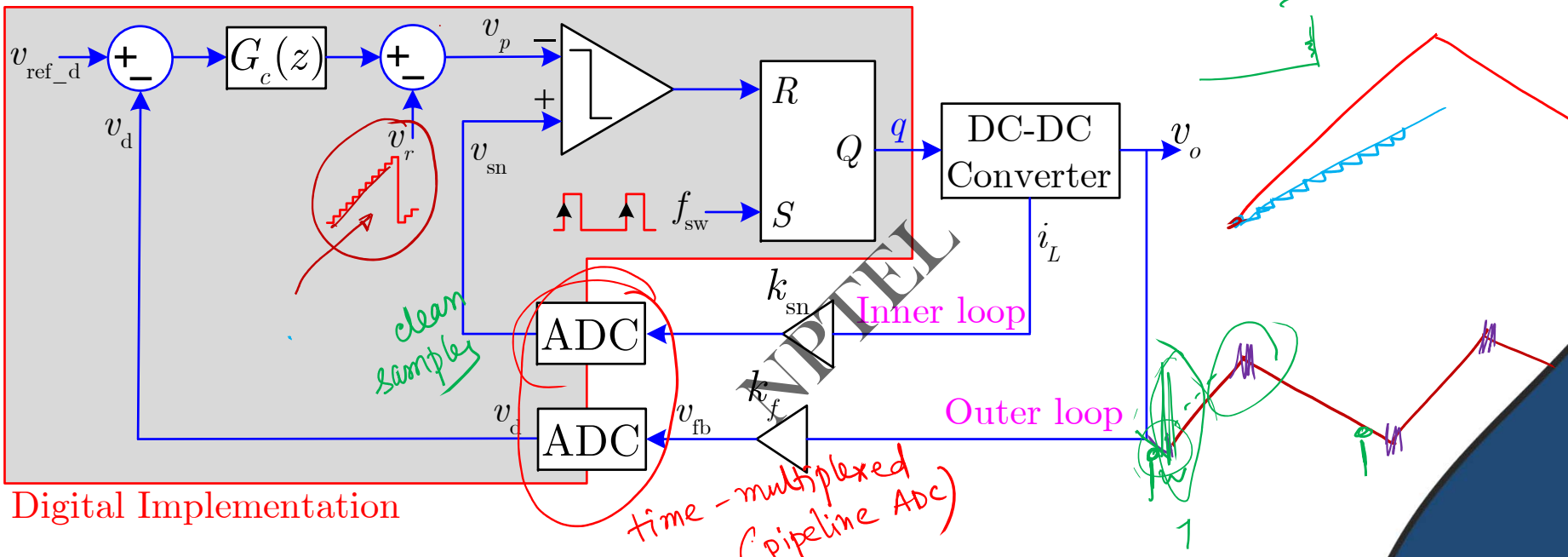
Digital Implementation



Fully Digital CMC with high current loop sampling rate

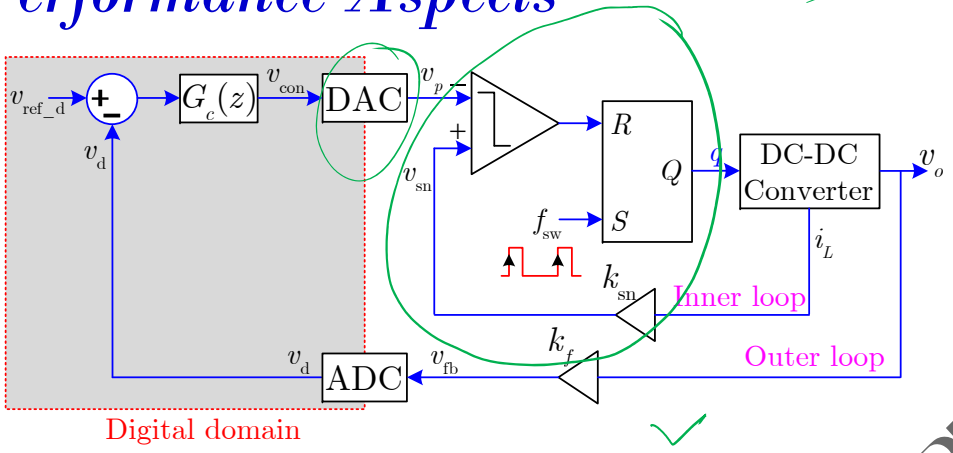
- Current and voltage feedback both are in digital domain

Digitization of CMC: Architecture-II (contd…)

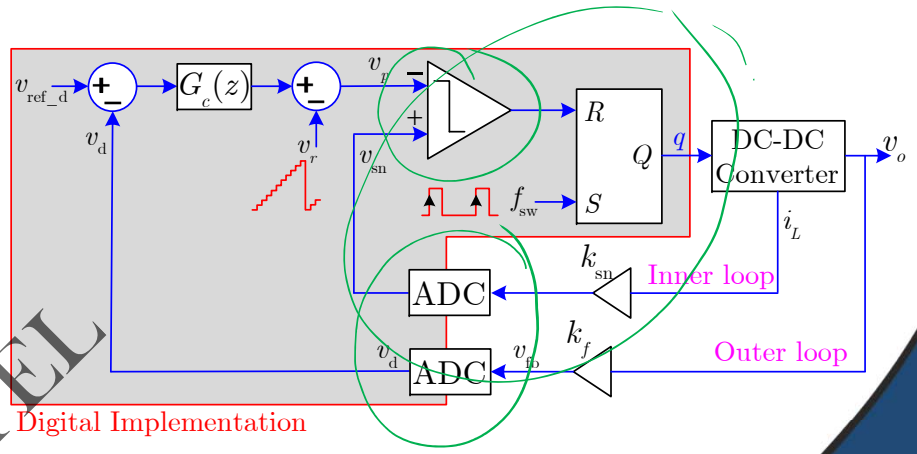


Fully Digital CMC with Ripple Emulation

Performance Aspects

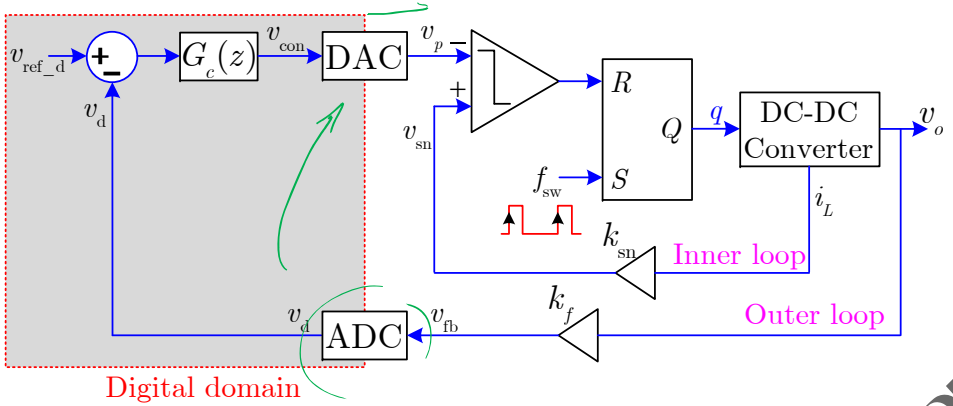


Mixed-signal CMC architecture

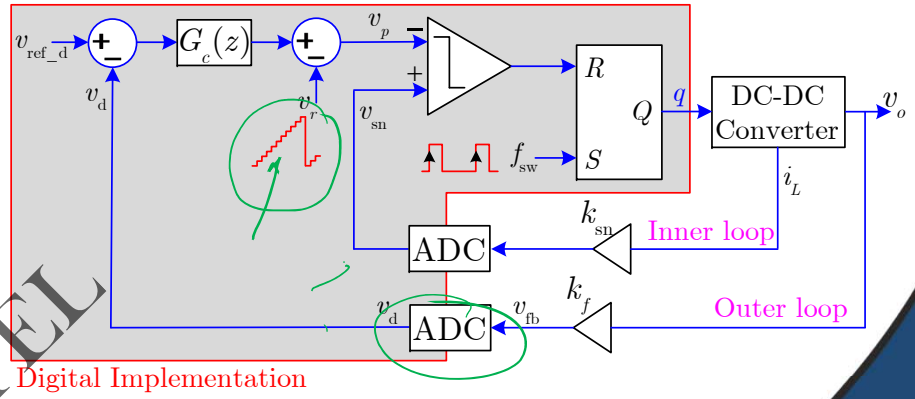


Fully digital CMC architecture

Cost Aspects

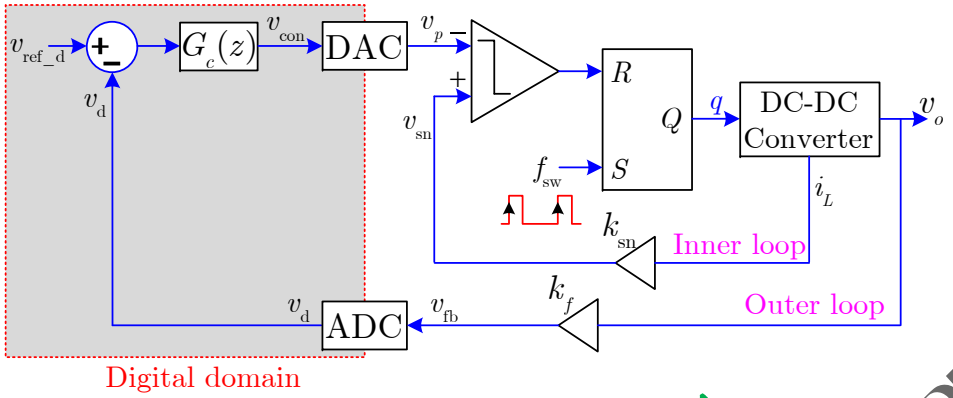


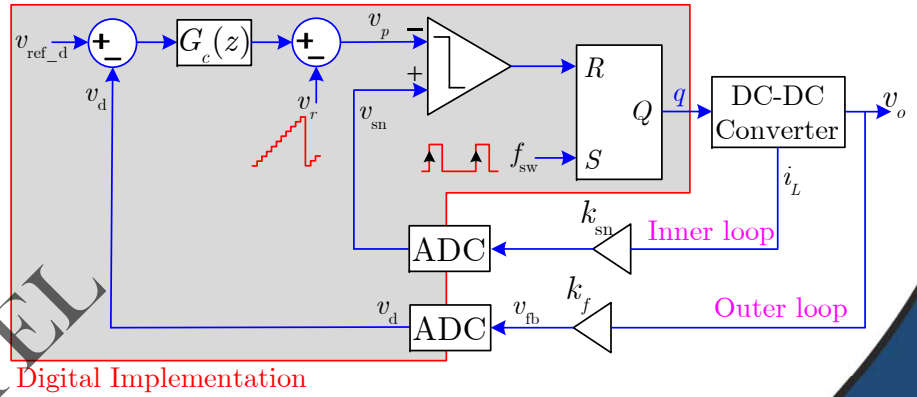
Mixed-signal CMC architecture



Fully digital CMC architecture

Performance/Cost Trade-offs





Mixed-signal CMC architecture

Fully digital CMC architecture

CONCLUSION

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- Digitizing in multi-loop feedback control
- Sampling and quantization
- Summary of multi-loop digital control
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THANK YOU !