NPTEL ONLINE CERTIFICATION COURSES



# DIGITAL CONTROL IN SMPCs AND FPGA-BASED PROTOTYPING

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## Module 01: Introduction to Digital Control in SMPCs

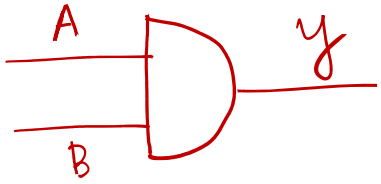
**Lecture 04: Overview of Digital Control Implementation Platforms**

# CONCEPTS COVERED

- Example of CMOS based digital circuit implementation
- Difference between ASIC and LUT based implementation
- Embedded control platforms – ASIC, FPGA, uC
- Digital control platforms in this course
- Why HDL based implementation and FPGA prototyping?

# TWO-input AND Gate – An Example

$$y = AB$$




$$y = AB = \overline{\left(\overline{AB}\right)} = \overline{\overline{A} + \overline{B}} = \overline{x}$$

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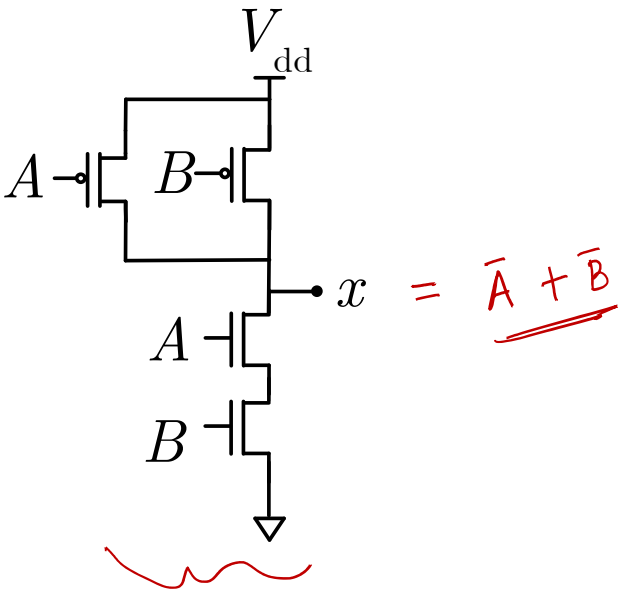
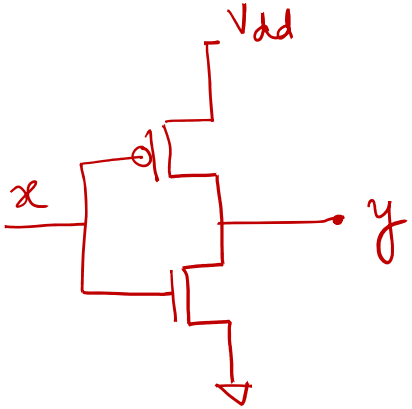
$$x \triangleq \overline{A} + \overline{B}$$

# CMOS Implementation of a TWO-input AND Gate

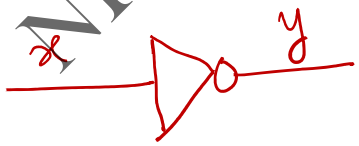
$$y = AB = \overline{\left(\overline{AB}\right)} = \overline{\overline{A} + \overline{B}} = \overline{x}$$



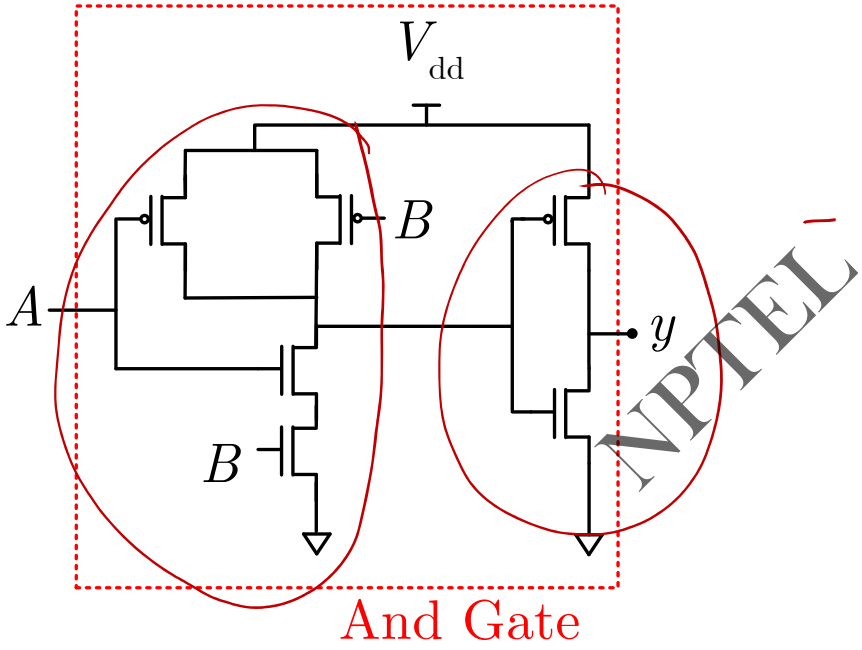

$x = \bar{A} + \bar{B}$




$y = \bar{x}$



# CMOS Implementation of a TWO-input AND Gate



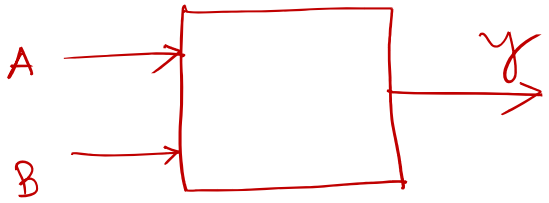

Problems

- Fixed hardware

Number of transistor =6

# *Look-up-table (LUT) of a TWO-input Digital Logic*

| $A$ | $B$ | $y$ |
|---|---|---|
| 0 | 0 | $y_o$ |
| 0 | 1 | $y_1$ |
| 1 | 0 | $y_2$ |
| 1 | 1 | $y_3$ |




Question :

Flexible hardware

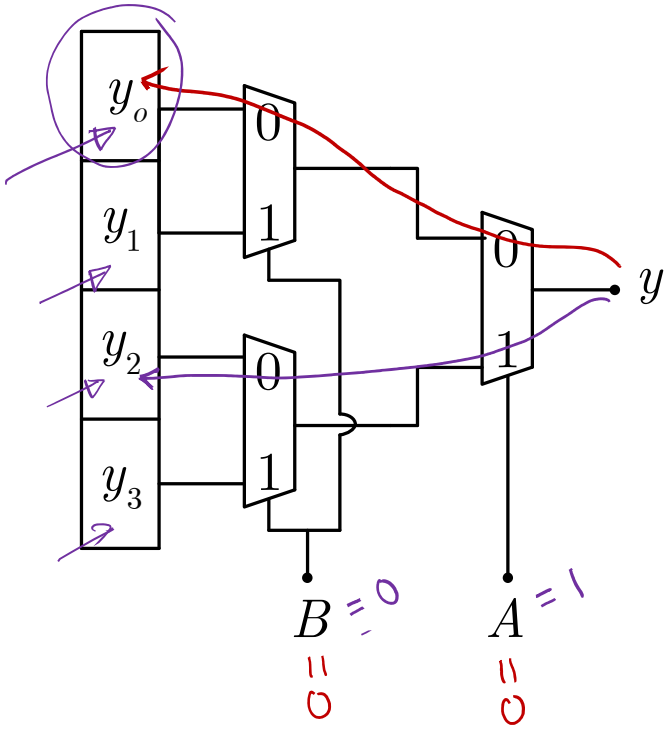


Each $y_K$ can take either '0' or 1

Total number of possible two-input functions $2^4 = 16$

In general = $2^{2^N}$ N= no of input

# LUT based Implementation of a TWO-input Digital Logic




| $A$ | $B$ | $y$ |
|---|---|---|
| 0 | 0 | $y_o$ |
| 0 | 1 | $y_1$ |
| 1 | 0 | $y_2$ |
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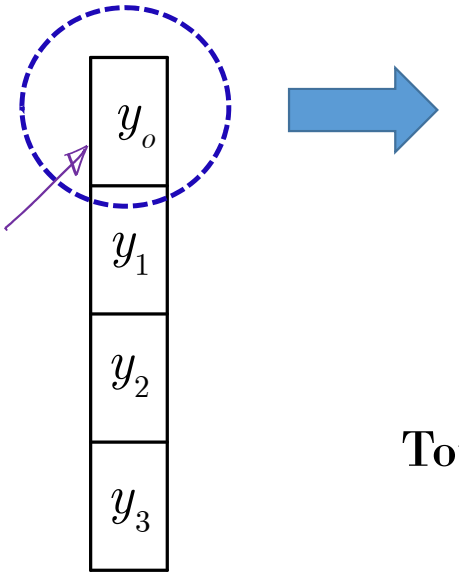
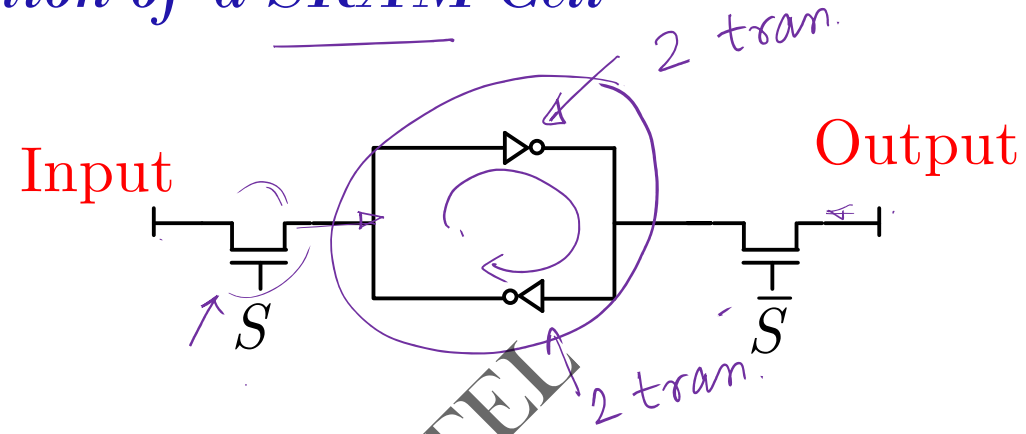
# CMOS Implementation of a SRAM Cell



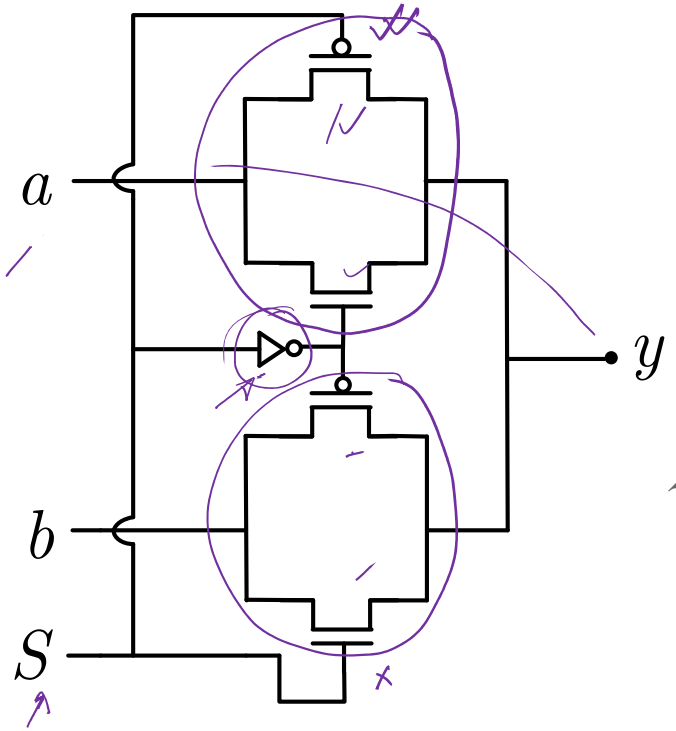



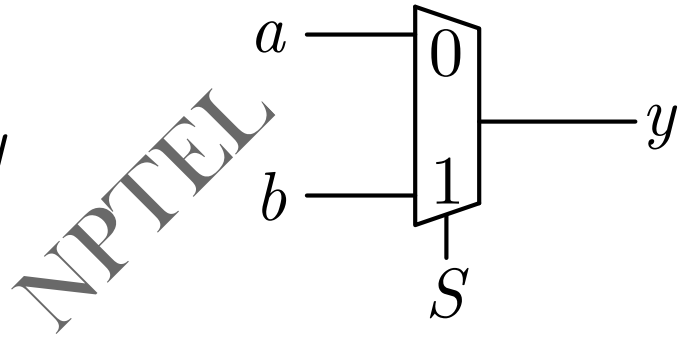



Total transistor for each SRAM cell =6

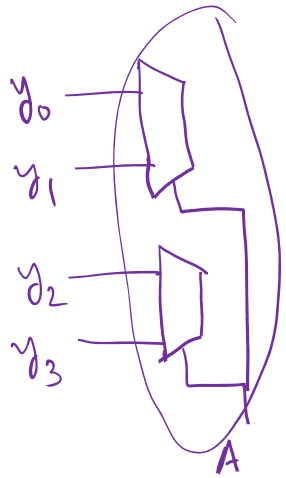
Total transistor for FOUR SRAM cells = 24

# CMOS Implementation of a TWO-input Digital MUX






Total transistor =6 (including inverter)

# *LUT and ASIC Implementation of a TWO-input AND Gate*

## *For 2 Input ASIC AND gate*

Total no of transistor =6

## *For 2 Input LUT based AND gate*

- 4 SRAM cells ⟶ 24 transistors
- 2 2-input (input side) MUX ⟶ (12-2)=10 transistors
- 1 2-input (input side) MUX ⟶ 6 transistors

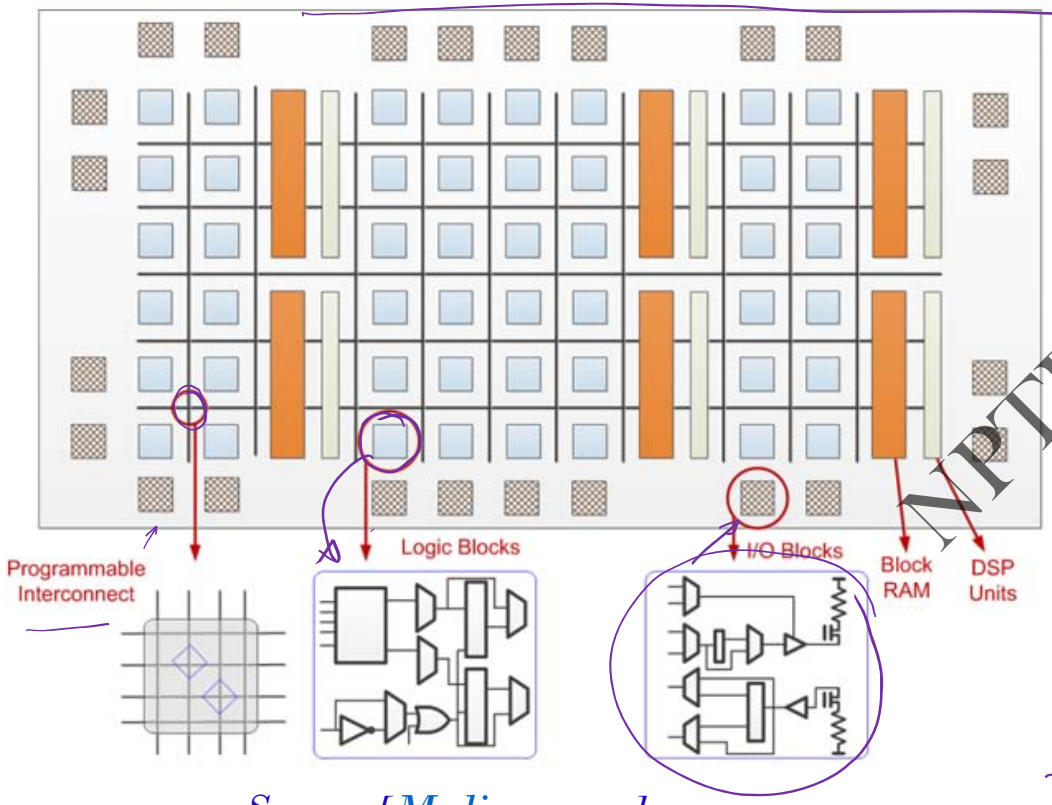
Total no of transistor =40

# TWO-input AND Gate – Comparing LUT and ASIC Implementation

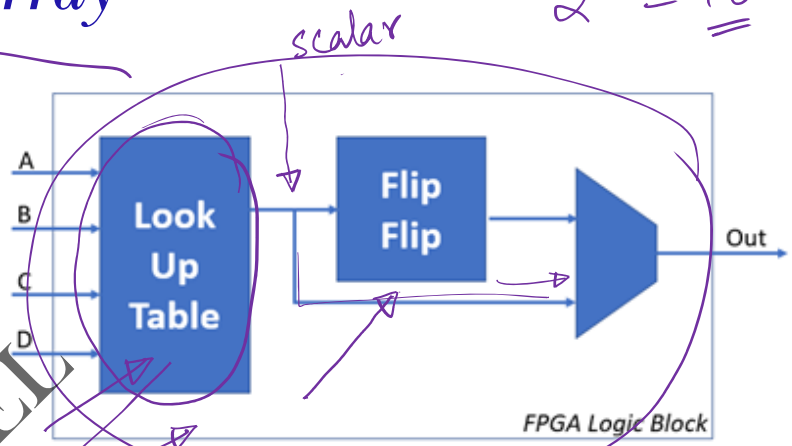
| Method | Description | Benefits | Limitations |
|---|---|---|---|
| ASIC | 6 -Transistors | Hardware optimized, power efficient | Fixed design, high NRE cost, long development time |
| LUT | 40 transistors | Configurable hardware, low NRE cost, short development time | Expensive hardware, power hungry, large component cost |

# FPGA – Field Programmable Gate Array

$2^4 = 16$ SRAM




Source [Medium.com]

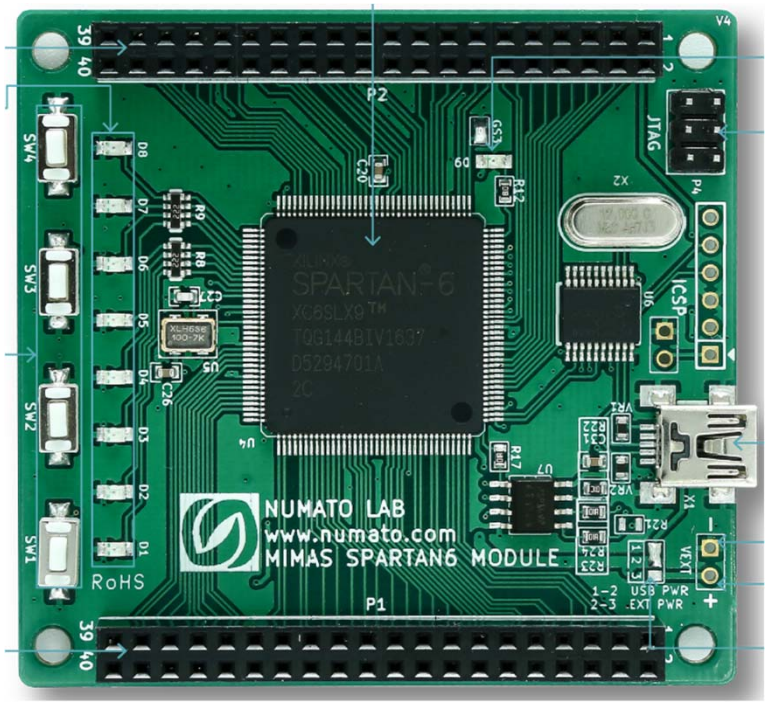



Source [Hardware Bee]

CLB

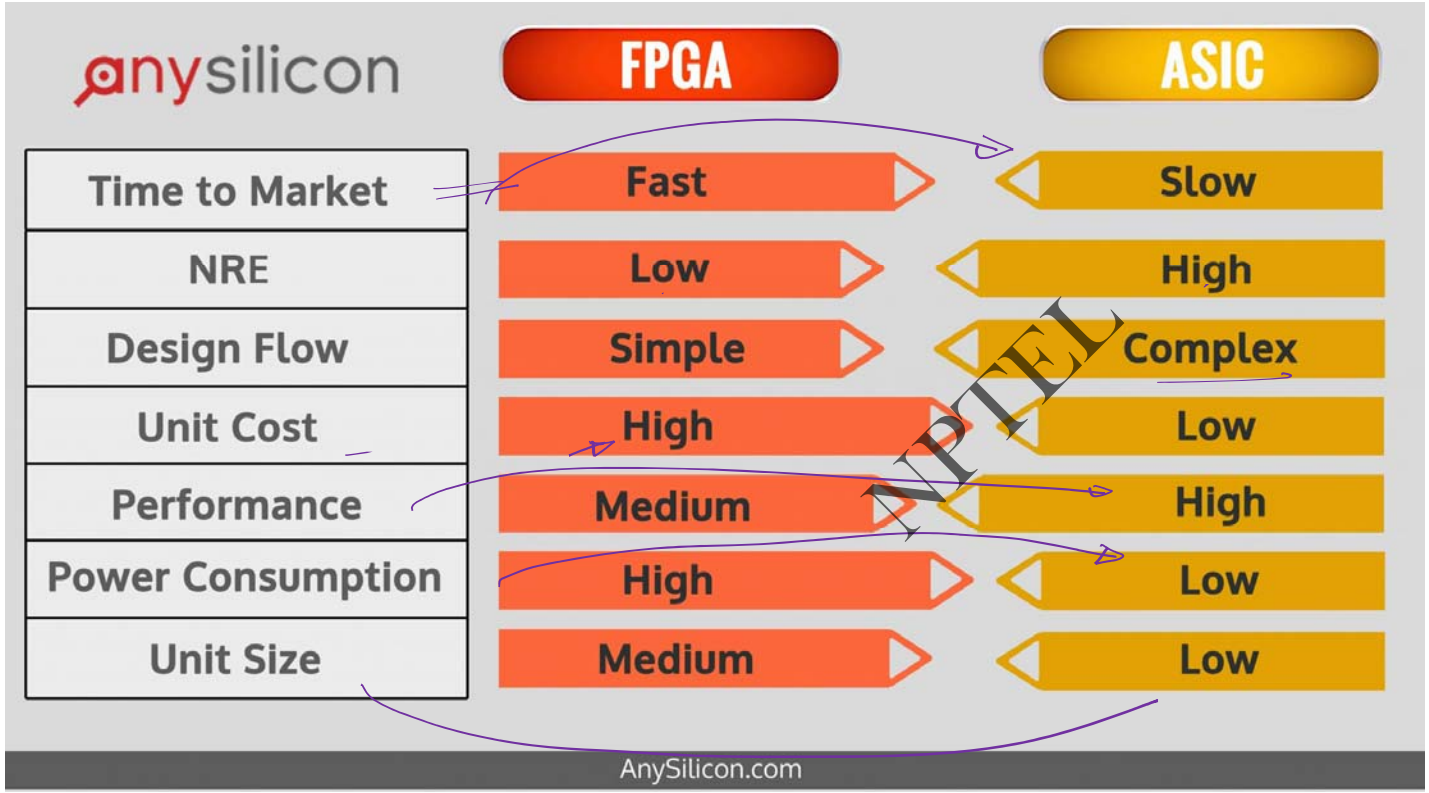
Verilog HDL

# FPGA Kit for This Course




*Xilix FPGA [Numato Lab]*

# FPGA vs ASIC Implementation





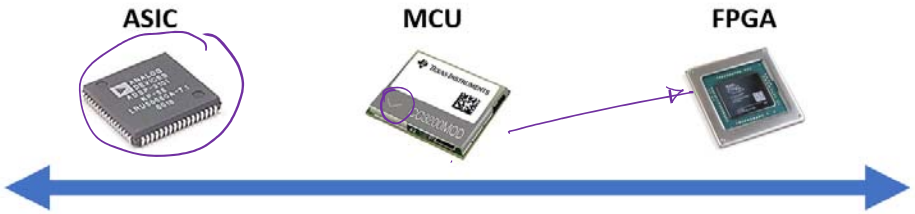

Source – anysilicon.com

# FPGA vs CPLD

| | CPLD | FPGA |
|---|---|---|
| Flexibility | Low | High |
| Price | Low | High |
| Security | High | Low |
| Speed | High | High |
| Capacity | Low | High |
| Application | Simple | Complex |

*Source – Outsourceit.today*

# FPGA vs Microcontroller vs. ASIC Solutions




Source – Octopart.com

| Micro | FPGA |
|---|---|
| Write software. | Design hardware. |
| Typically executes one instruction at a time. | All parts of your circuit can operate independently. |
| Fixed maximum clock speed. | Maximum clock speed is dependent on your design. |
| A handful of I/O pins that can be accessed in small groups (typically eight) at a time. | Many I/O pins that can all be accessed simultaneously. |
| Usually store programs in nonvolatile (persistent) memory. | RAM based and needs to be programed after power on (the Mojo does this automatically). |
| Often very power efficient with advanced sleep modes. | Power usage depends on your design but typically requires more than a microcontroller. |
| Fixed peripherals that limit the devices you can connect. | Can interface with virtually any digital device. |

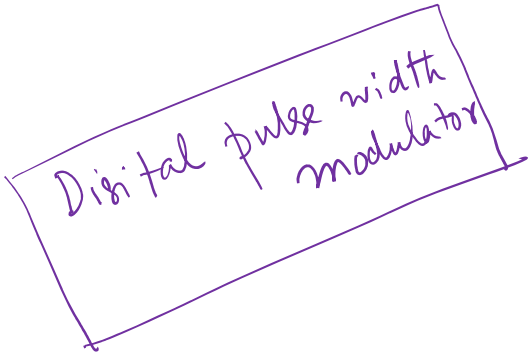
Source – fpgakey.com

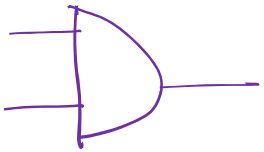
# *FPGA and Microcontrollers in This Course*

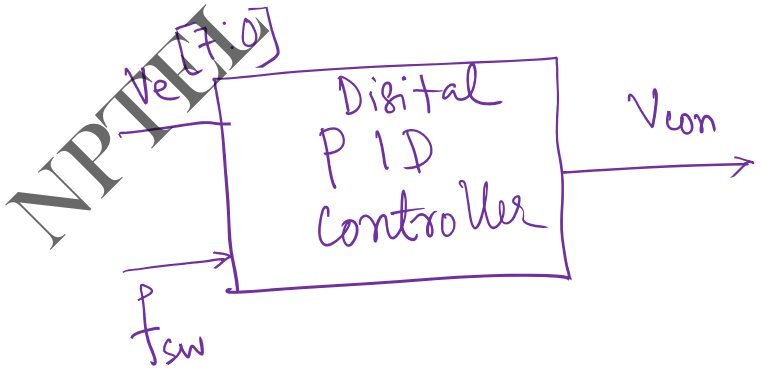
- Verilog HDL based implementation and Xilinx Spartan 6 FPGA prototyping
- Introduction to STM32 microcontroller and selected hardware demonstrations
- Introduction to C2000 microcontroller and selected hardware demonstrations

# Why Verilog HDL based Implementation?

Hardware descriptive language





# CONCLUSION

- Example of CMOS based digital circuit implementation
- Difference between ASIC and LUT based implementation
- Embedded control platforms – ASIC, FPGA, uC
- Digital control platforms in this course
- Why HDL based implementation and FPGA prototyping?



# THANK YOU !