



NPTEL ONLINE CERTIFICATION COURSES

DIGITAL CONTROL IN SMPCs AND FPGA-BASED PROTOTYPING

Dr. Santanu Kapat

Electrical Engineering Department, IIT KHARAGPUR

Module 02: Fixed and Variable Frequency Digital Control Architectures

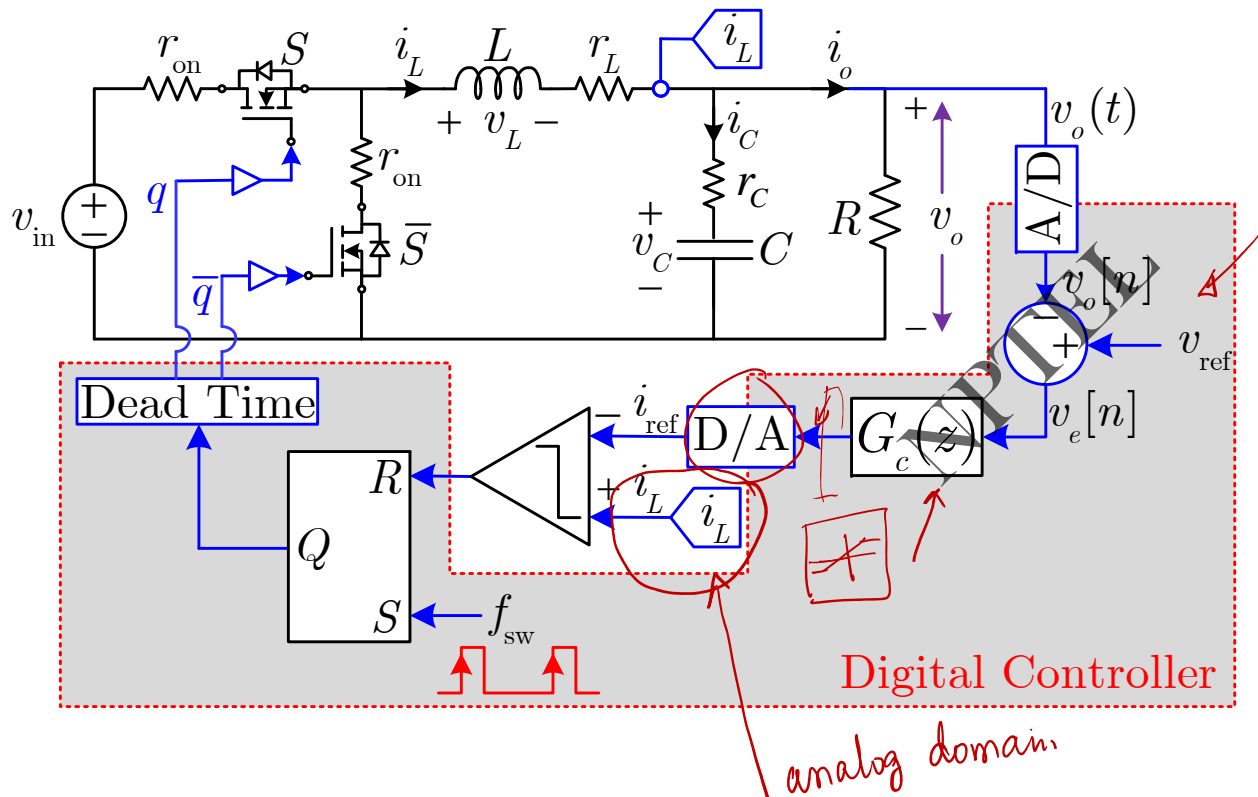
Lecture 14: Sampling Methods under Fixed Frequency Current Mode Control



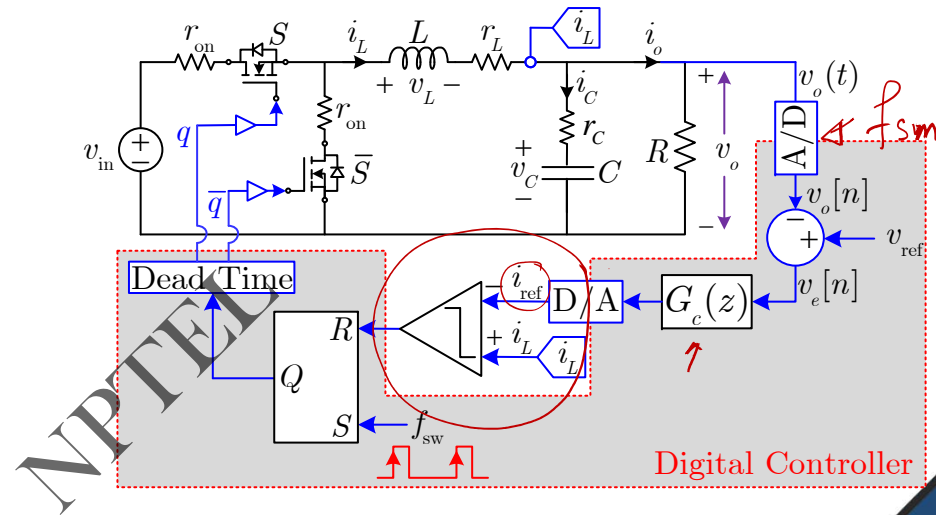
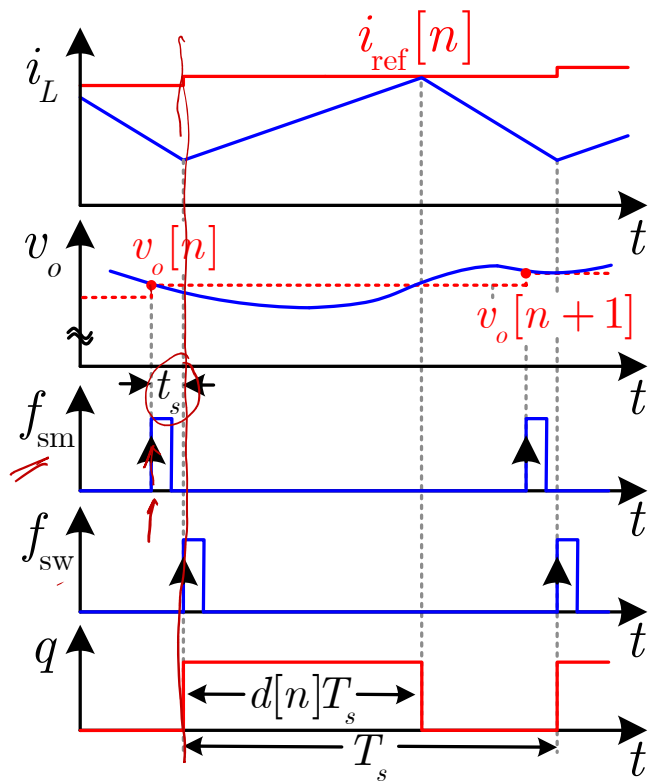
CONCEPTS COVERED

- Overview of sampling methods in digital current mode control
- Mixed-signal current mode control and control waveforms
- Fully digital current mode control and control waveforms

Mixed-Signal Peak CMC Architecture

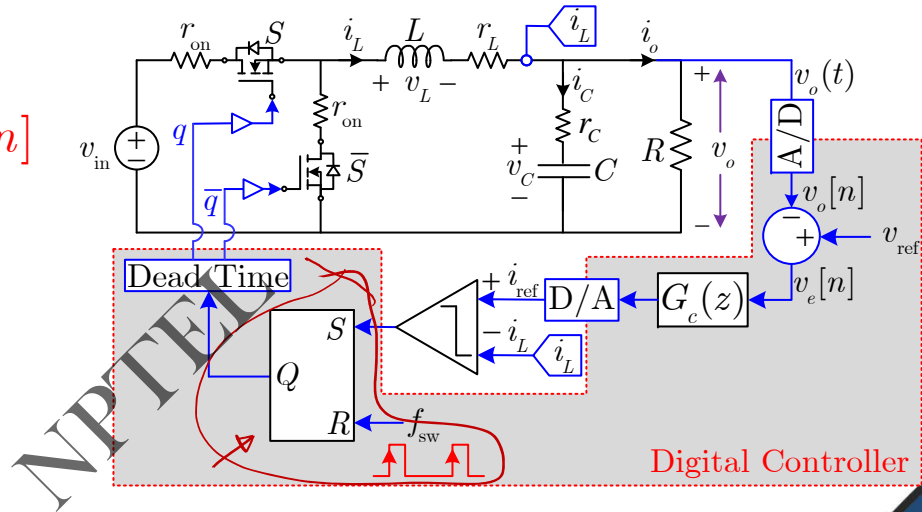
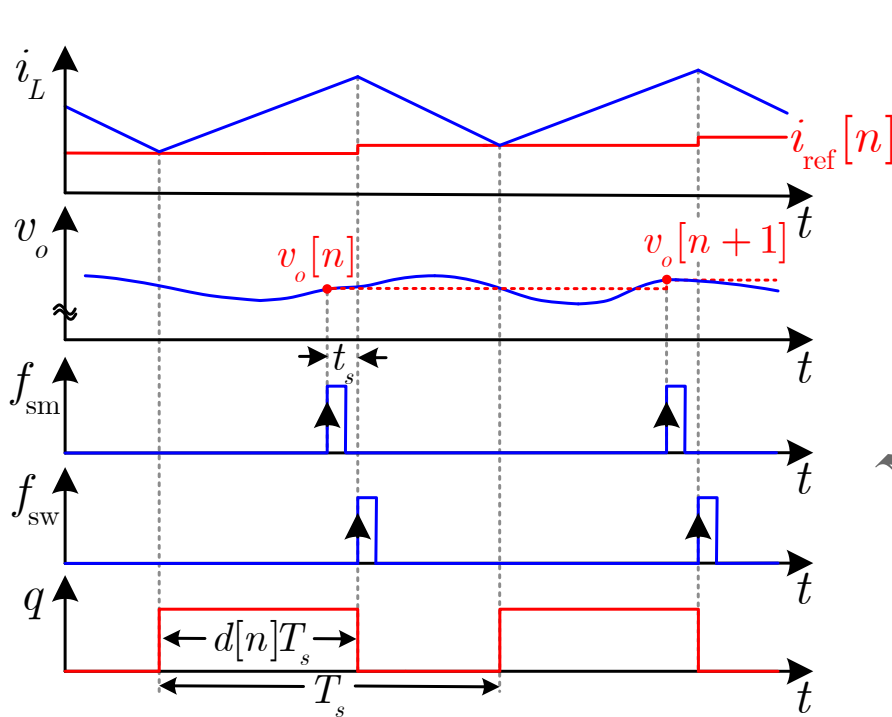


Mixed-Signal Peak CMC Architecture



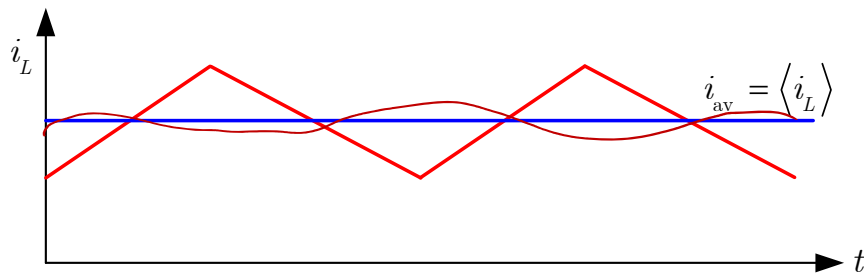
- Trailing-edge modulation with
interval-2 sampling

Mixed-Signal Valley CMC Architecture



- Leading-edge modulation with interval-1 sampling

Mixed-Signal Average CMC Architecture

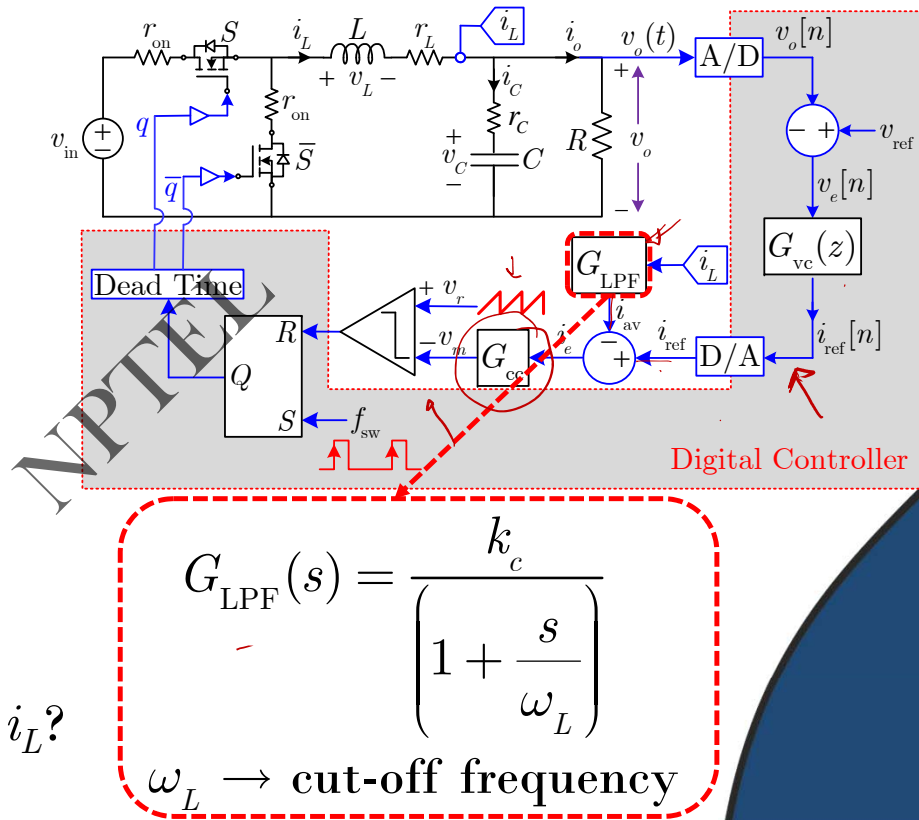


Objective:

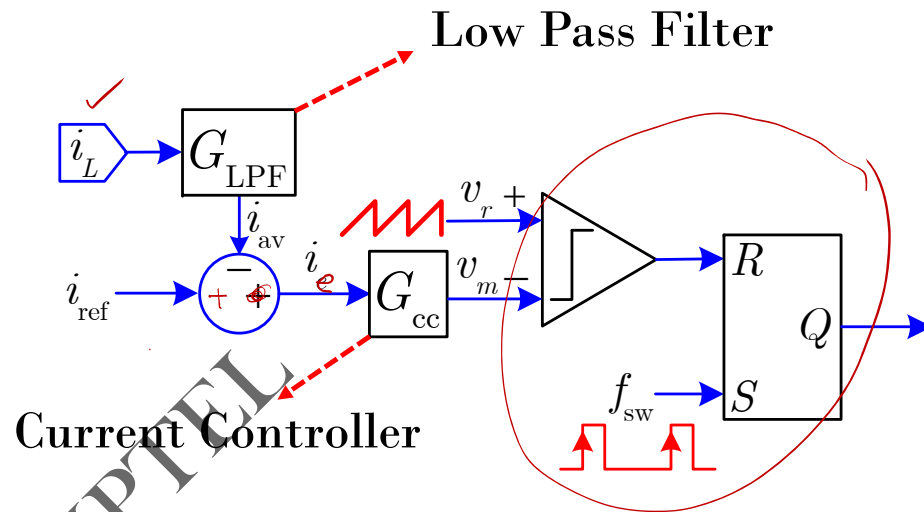
- To control average value of i_L

Question:

- How to extract average value of i_L ?



Average CMC – Current Loop

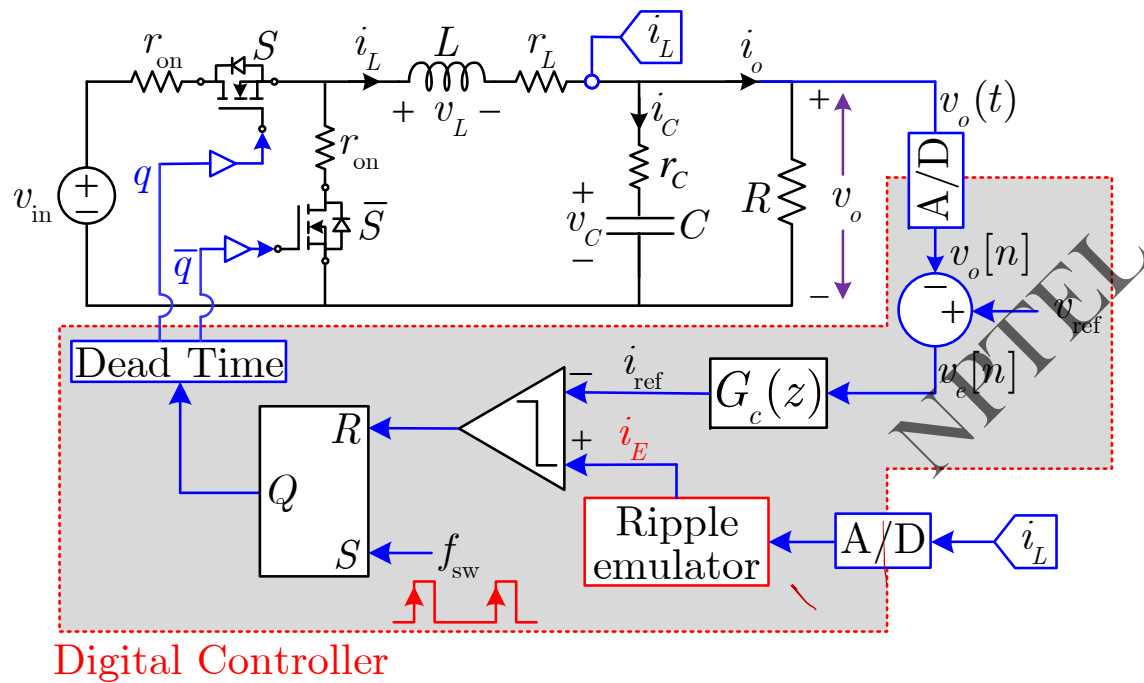


$G_{\text{LPF}} \rightarrow$ LPF is used to extract average inductor current

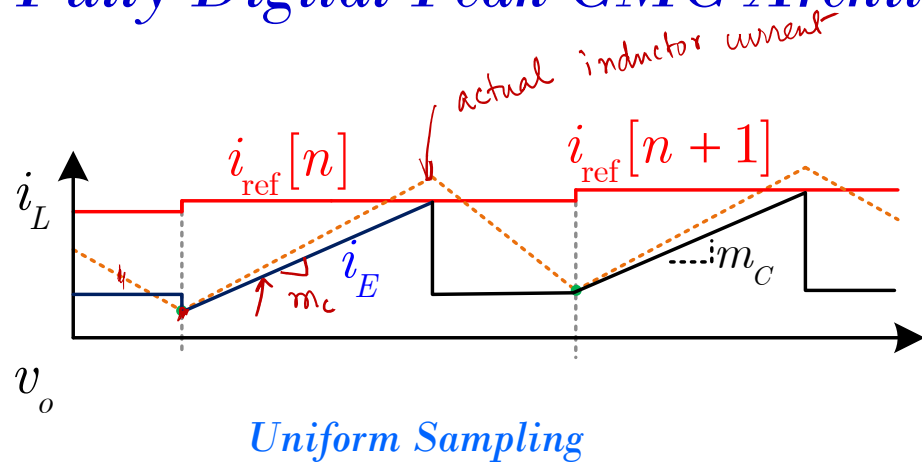
$G_{\text{cc}} \rightarrow$ Current controller
(Generally PI)

$$G_{\text{LPF}} = \frac{k_c}{\left(1 + \frac{s}{\omega_L}\right)} \quad \begin{matrix} w_L \ll 2\pi f_{\text{sw}} \\ w_L \approx \frac{2\pi f_{\text{sw}}}{10} \end{matrix} \quad (\text{Thumb rule})$$

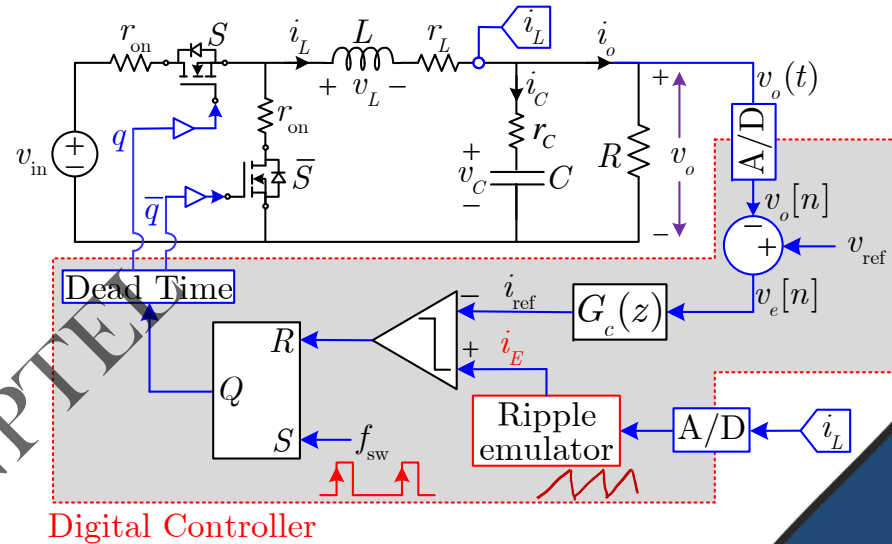
Fully Digital Peak CMC Architecture



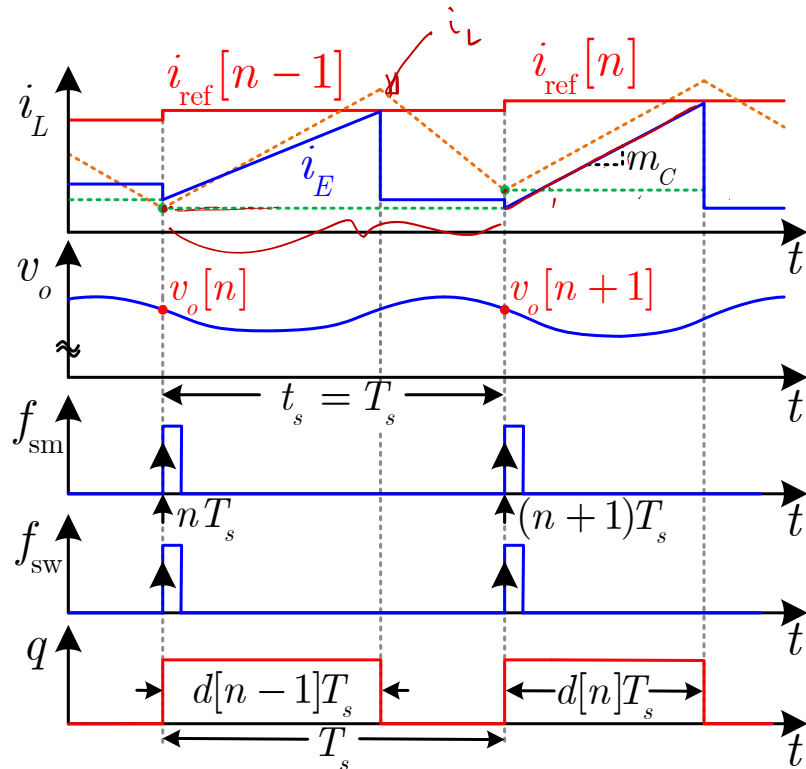
Fully Digital Peak CMC Architecture



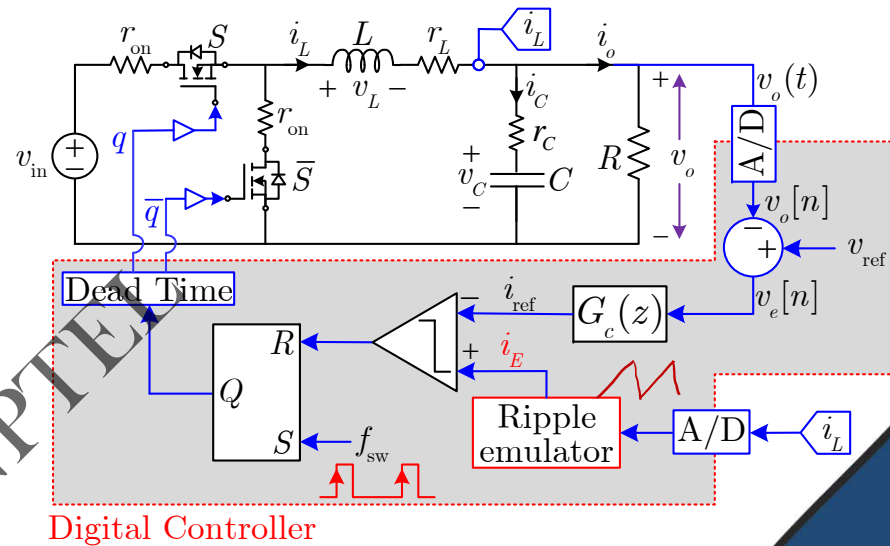
- Infeasible sampling – why?



Fully Digital Peak CMC Architecture (contd...)



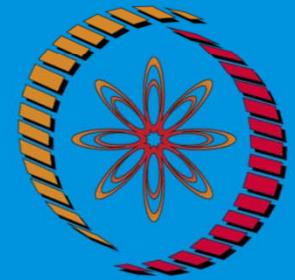
Uniform Sampling with one cycle delay



- Feasible sampling

CONCLUSION

- Overview of sampling methods in digital current mode control
- Mixed-signal current mode control and control waveforms
- Fully digital current mode control and control waveforms



**THANK
YOU !**