NPTEL ONLINE CERTIFICATION COURSES

DIGITAL CONTROL IN SMPCs AND FPGA-BASED PROTOTYPING

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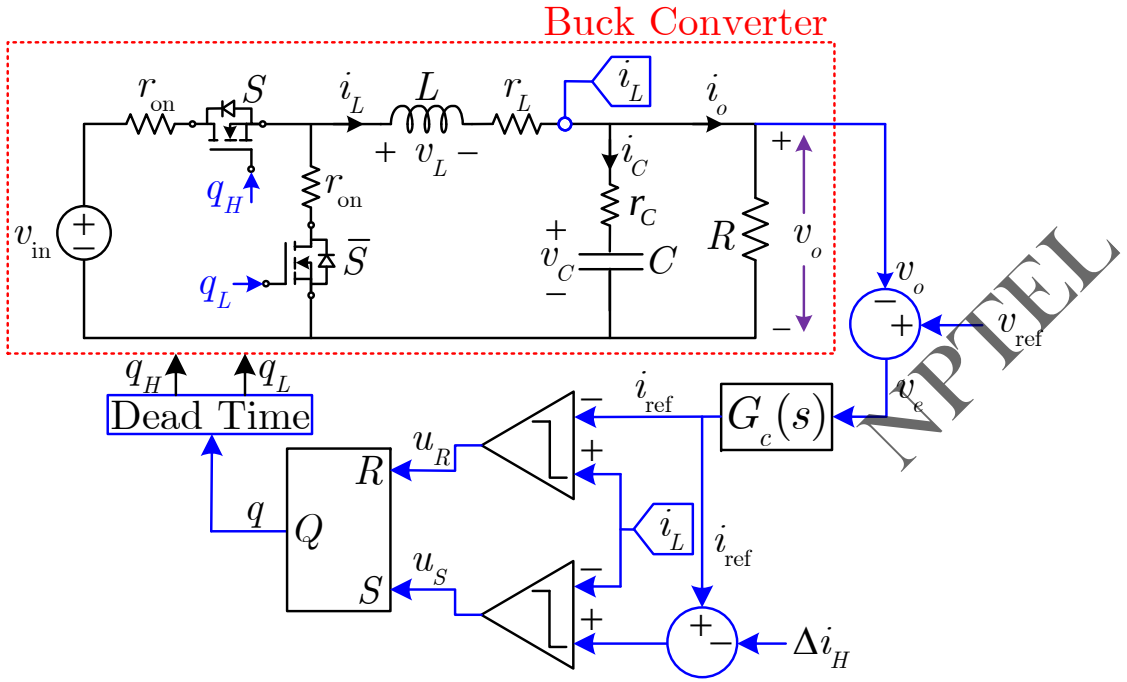
Module 02: Fixed and Variable Frequency Digital Control Architectures

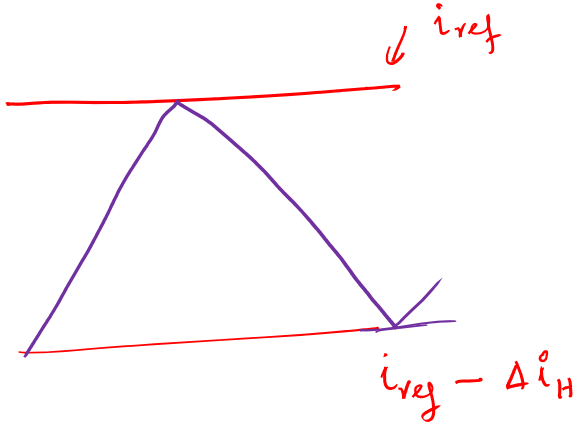
Lecture 19: Overview of Digital Hysteresis Control Architectures

CONCEPTS COVERED

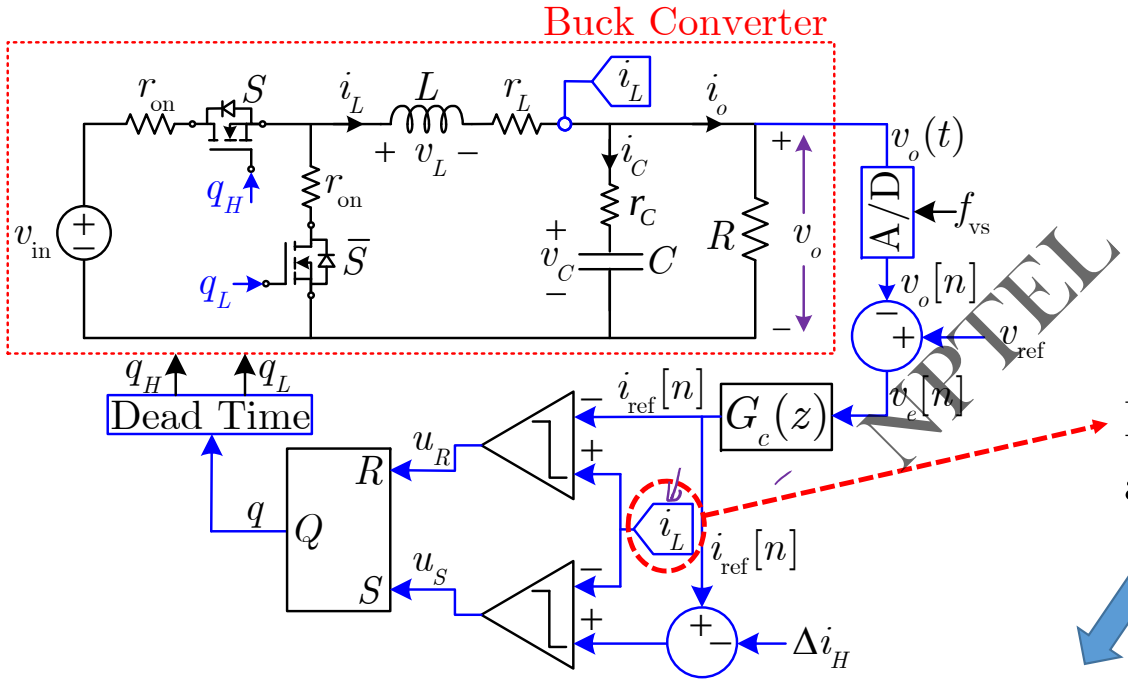
- Current hysteresis control with analog current loop
- Mixed-signal current hysteresis control and control waveforms
- Benefits of mixed-signal current hysteresis control

Analog Hysteresis CMC in a Buck Converter





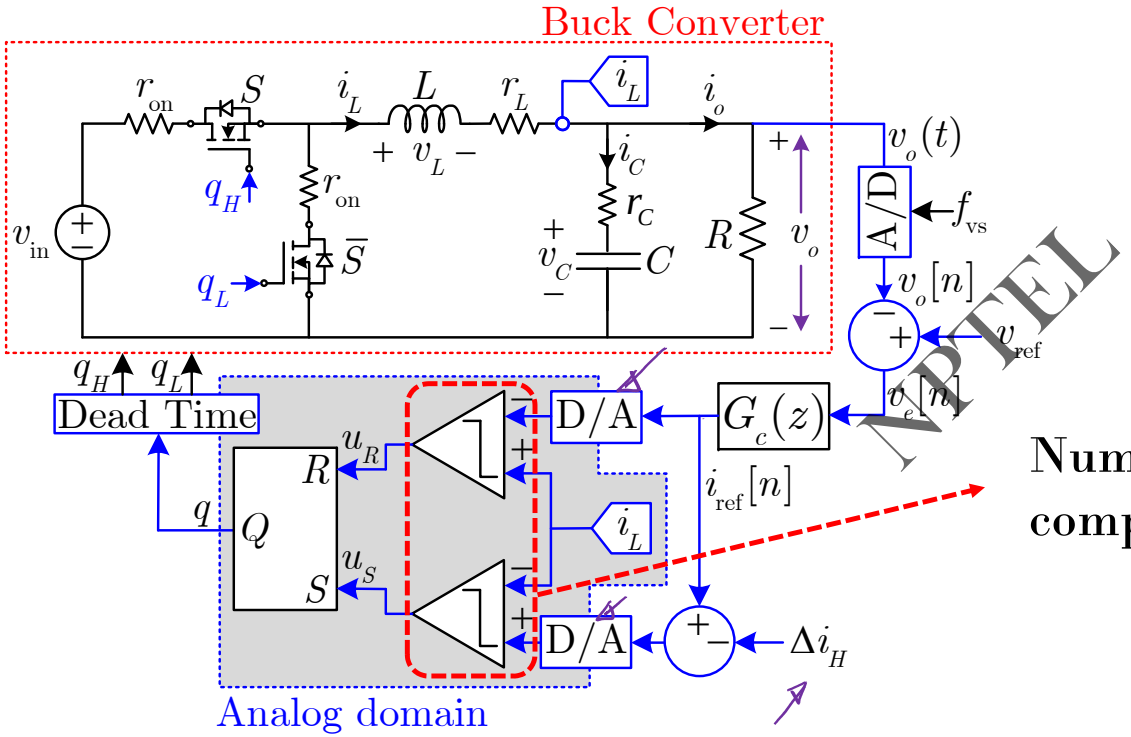
Closing Digital Loop



Inductor current is in analog domain

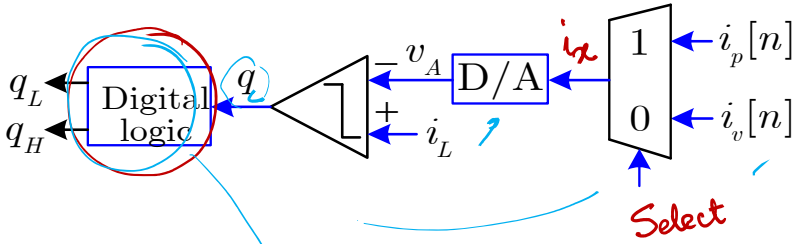
DAC converter is needed to generate analog current reference

Closing Digital Loop (contd…)

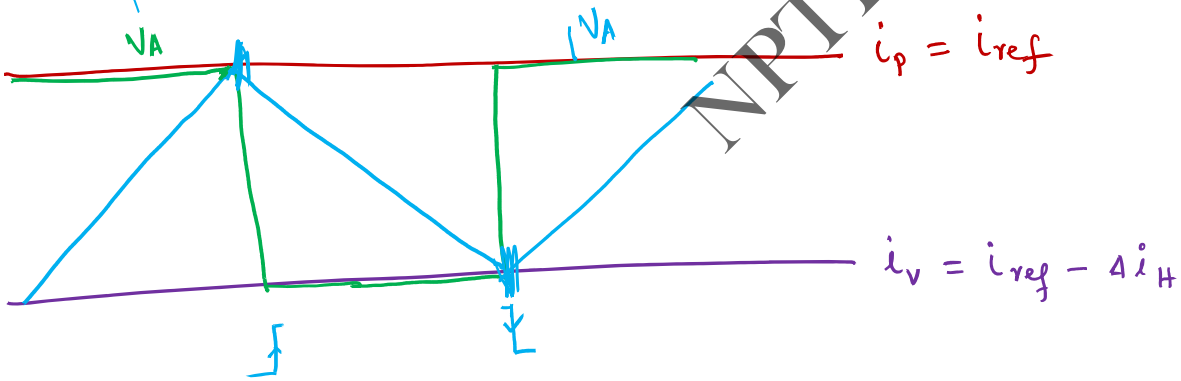


Number of DACs and analog comparator increases

Closing Digital Loop (contd…)

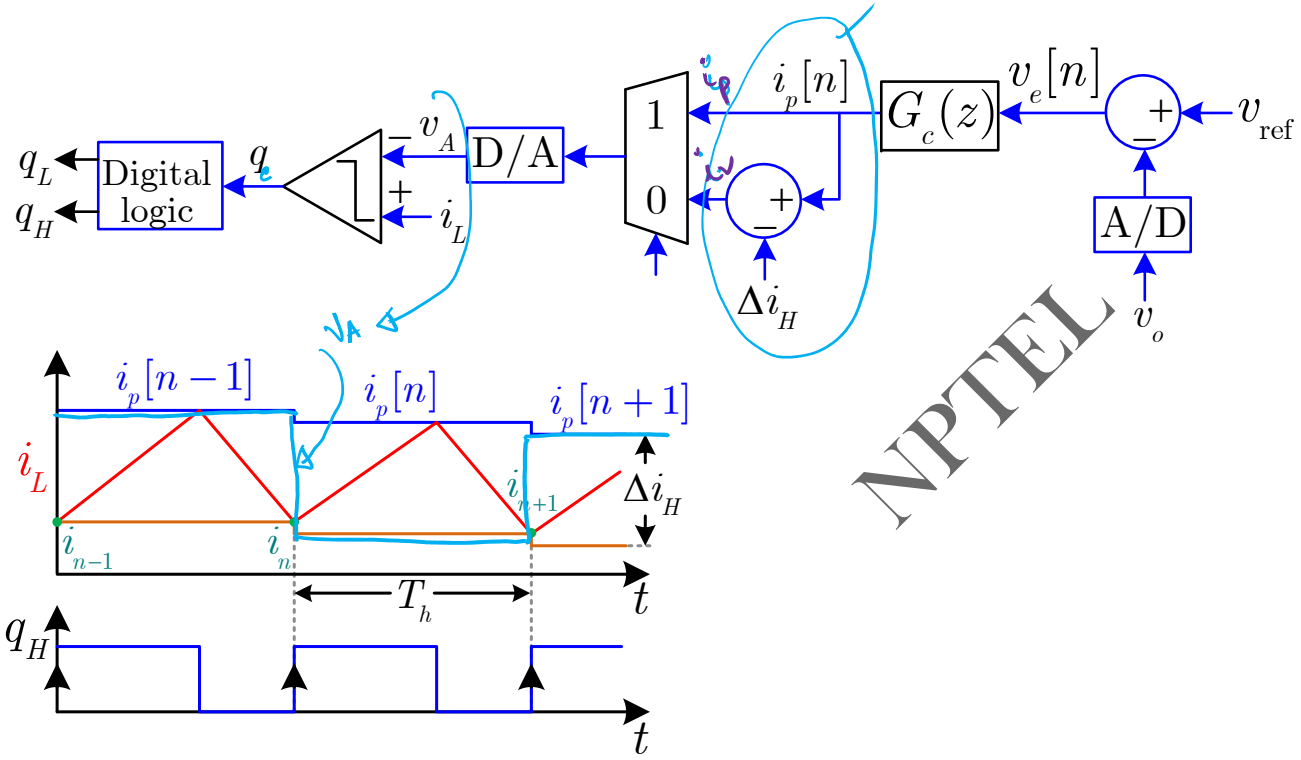


Mixed signal hysteresis current controller block



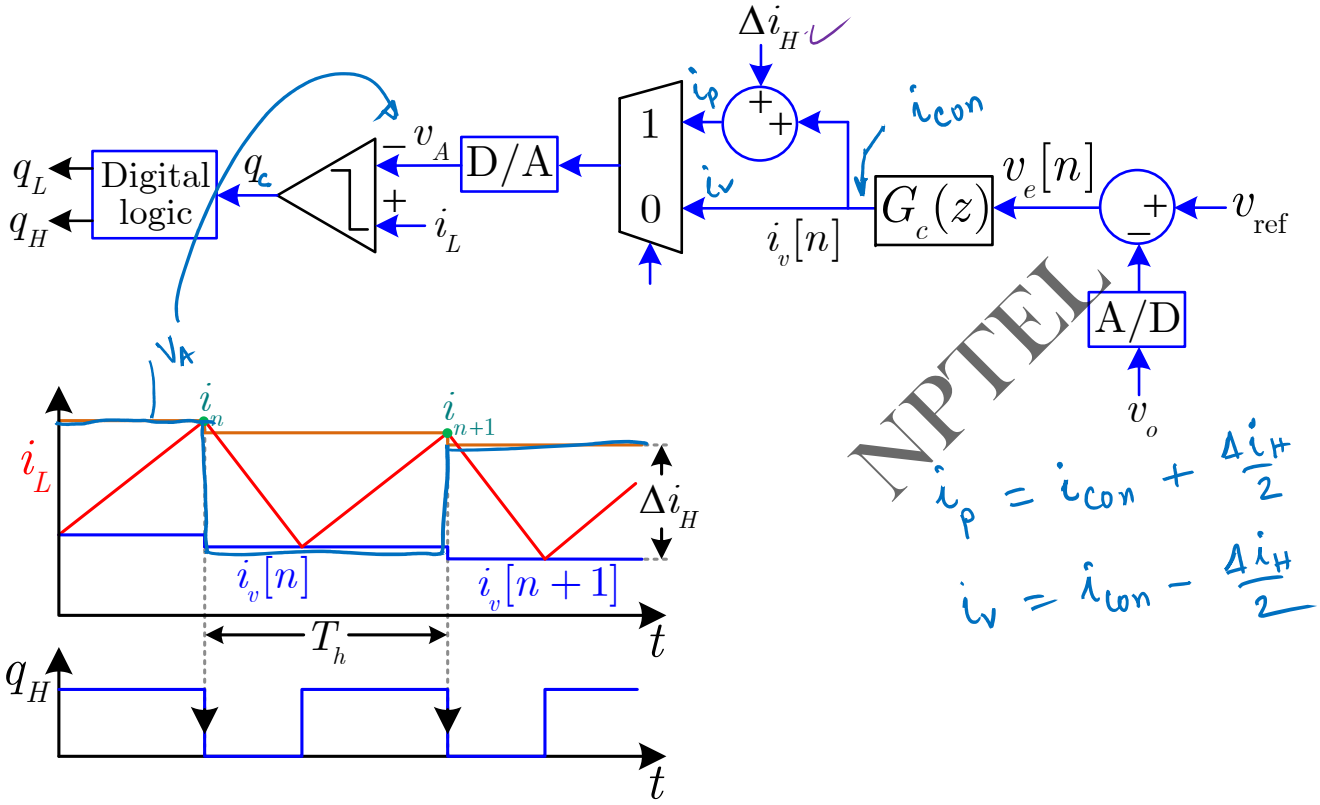
[S. Kapat, "Parameter-Insensitive Mixed-Signal Hysteresis-Band … ", *IEEE TPEL*, 2017]

Control Waveforms of Peak Current-mode MSHCC



[S. Kapat, "Parameter-Insensitive Mixed-Signal Hysteresis-Band … ", *IEEE TPEL*, 2017]

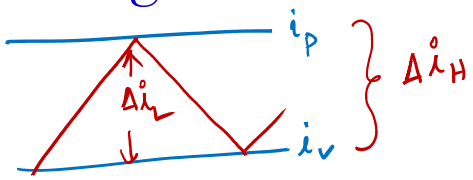
Control Waveforms of Valley Current-mode MSHCC

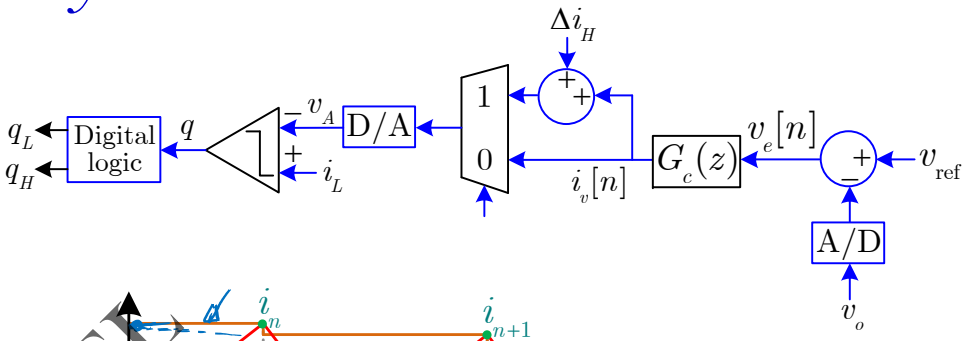


$i_p = i_{con} + \frac{\Delta i_H}{2}$

$i_v = i_{con} - \frac{\Delta i_H}{2}$

Benefits of Mixed-Signal Current Hysteresis Control





- $\Delta i_L \approx \Delta i_H$
- Programmable f_{sw}
- Very fast transient
- Trajectory based control

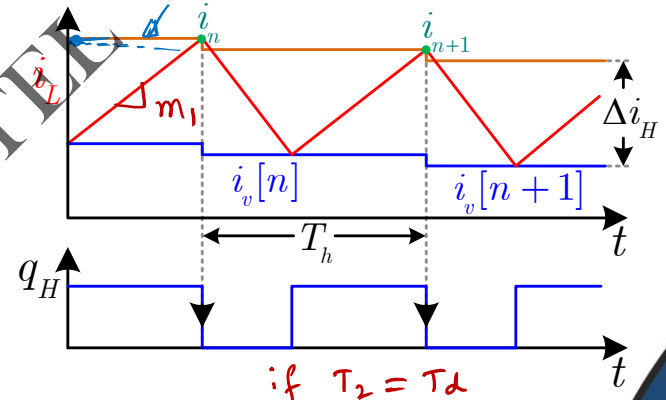
$\Delta i_L = m_1 t_{on} = \Delta i_H$

$t_{on} = \frac{\Delta i_H}{m_1}$

$= m_1 dT$

$\propto \Delta i_{H_1} \rightarrow T_1$

$\Delta i_{H_2} \rightarrow T_2$



if $T_2 = T_d$

$\frac{\Delta i_{H_2}}{\Delta i_{H_1}} = \frac{T_2}{T_1}$

$\Delta i_{H_2} = \frac{\Delta i_{H_1}}{T_1} \propto T_d$

CONCLUSION

- Current hysteresis control with analog current loop
- Mixed-signal current hysteresis control and control waveforms
- Benefits of mixed-signal current hysteresis control

THANK YOU !