NPTEL ONLINE CERTIFICATION COURSES

DIGITAL CONTROL IN SMPCs AND FPGA-BASED PROTOTYPING

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Module 02: Fixed and Variable Frequency Digital Control Architectures

Lecture 13: Overview of Digital Pulse Width Modulator Architectures

CONCEPTS COVERED

- Digital Pulse Width Modulation (DPWM) – Requirements and Challenges
- Counter-based DPWM Architecture
- Other DPWM Architectures
- Delay-line DPWM Architecture
- Hybrid DPWM Architecture

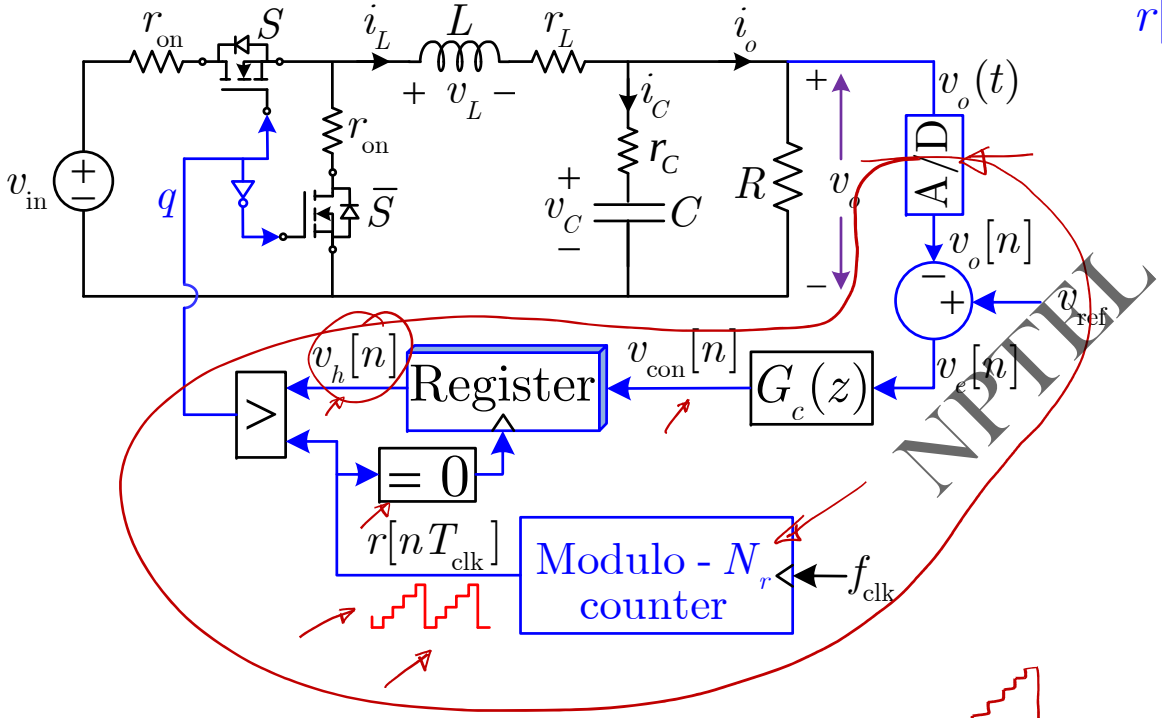
Digital Pulse Width Modulator (DPWM) Architectures

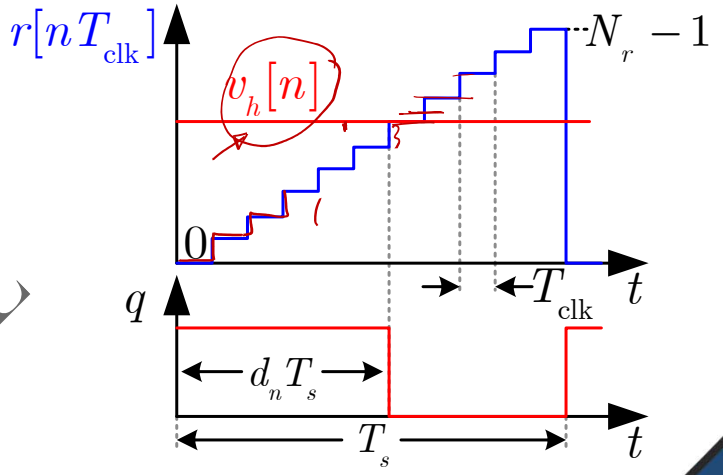
(1) Counter-based DPWM

(2) Delay Line-based DPWM

(3) Hybrid DPWM

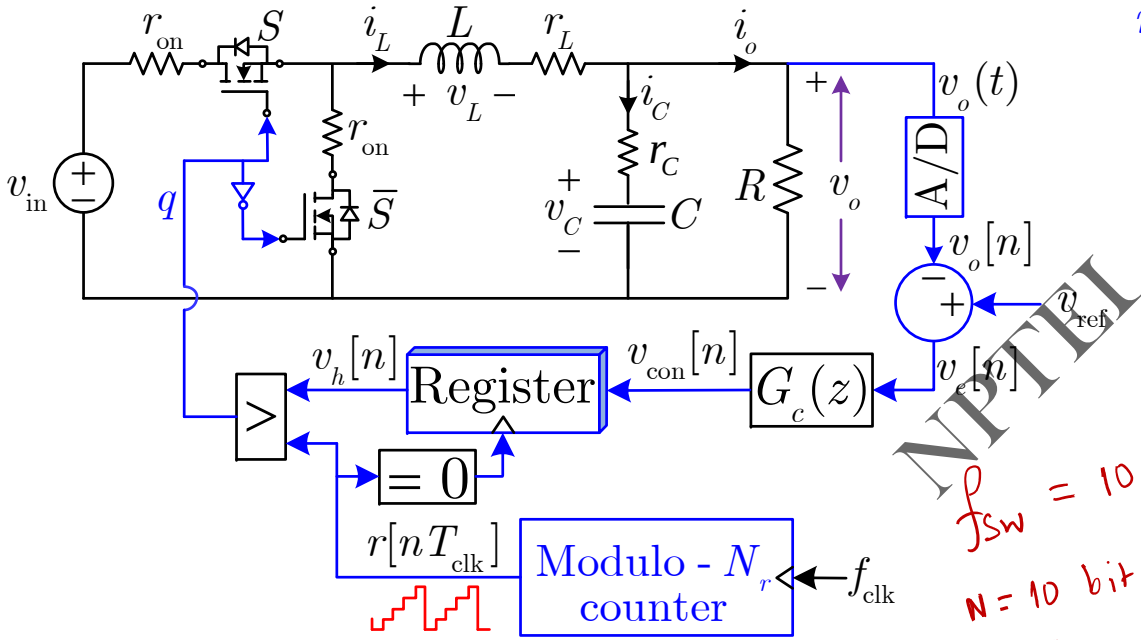
Counter-based DPWM

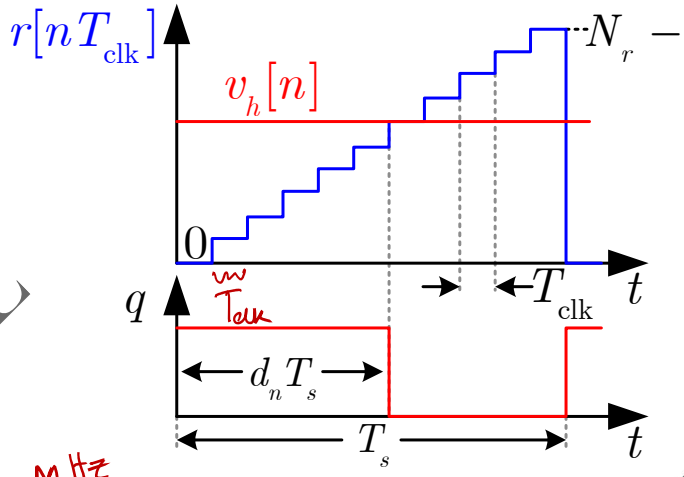




[For details, refer to '*Digital Control of High-frequency Switched …', Wiley-IEEE Press, 2015*]

Counter-based DPWM



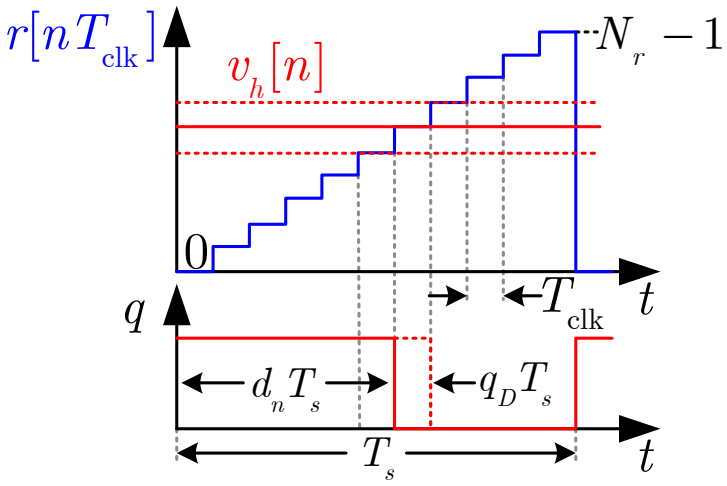


- For N-bit counter

$$f_{clk} = 2^N \times f_{sw}$$

[For details, refer to '*Digital Control of High-frequency Switched …', Wiley-IEEE Press, 2015*]

Counter-based DPWM – Requirements



- **Modulator duty cycle resolution**

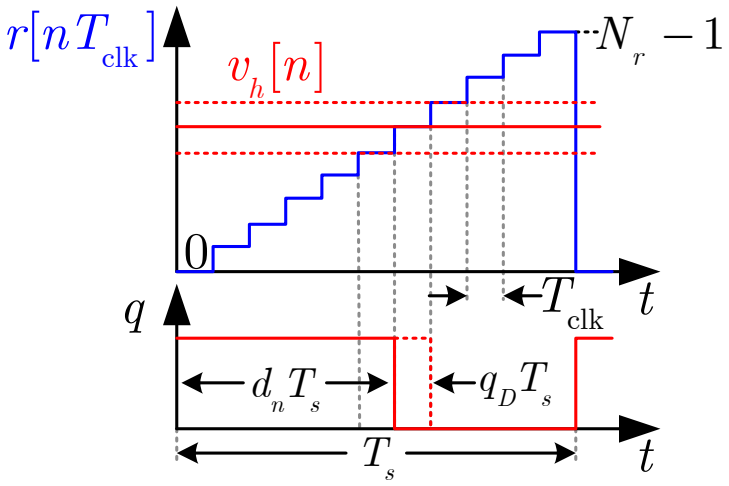
$$q_D \triangleq \frac{\Delta t_{\text{DPWM}}}{T_s}$$

- **For counter based DPWM**

$$\Delta t_{\text{DPWM}} = T_{\text{clk}}$$

$$\Rightarrow q_D = \frac{T_{\text{clk}}}{T_s} = \frac{1}{N_r}$$

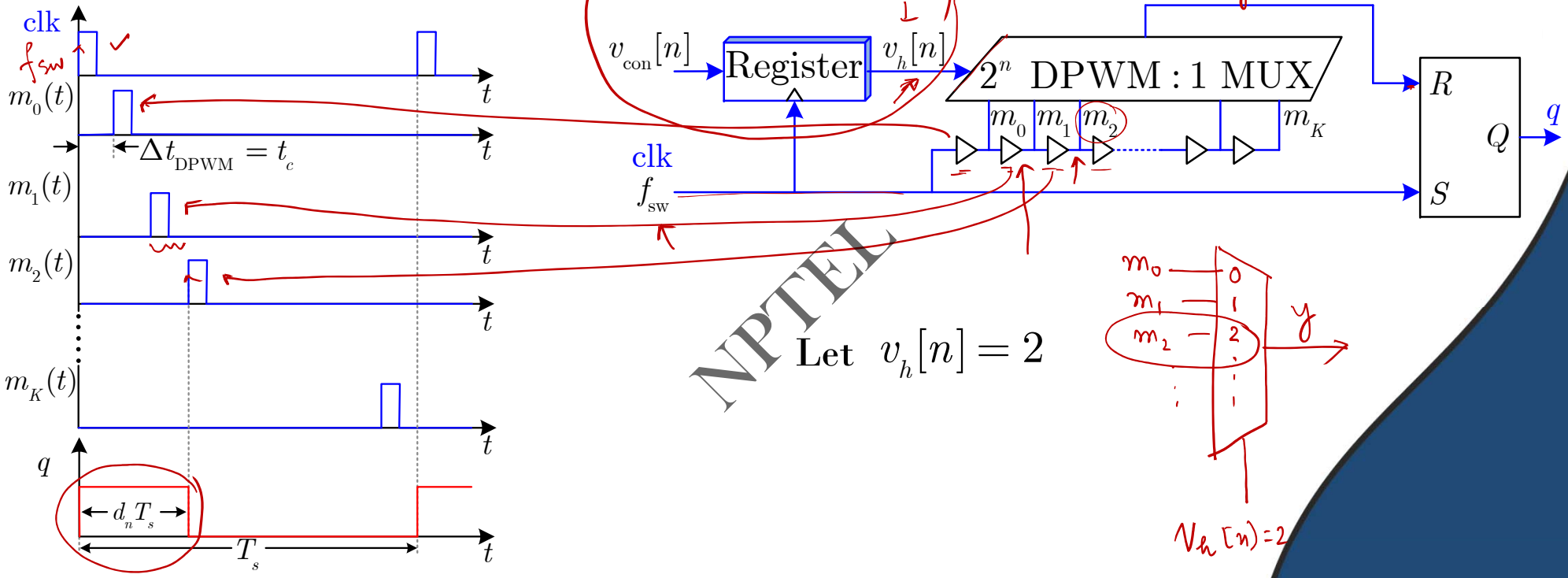
Counter-based DPWM – Requirements and Challenges



$$q_D = \frac{T_{clk}}{T_s} = \frac{1}{N_r}$$

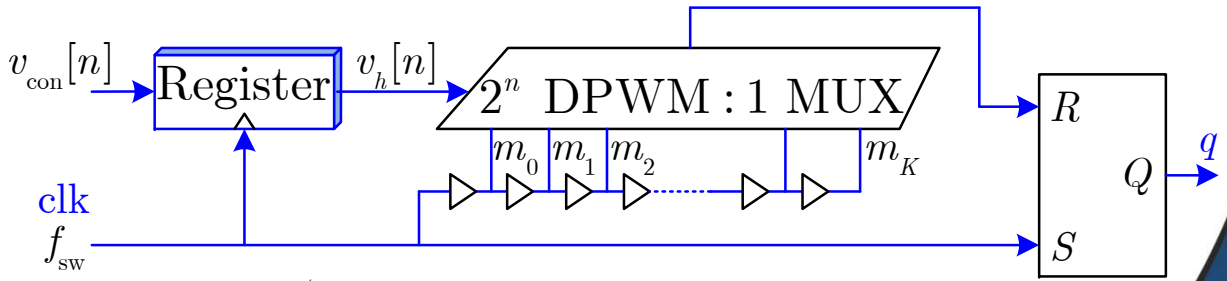
f_{clk} too high for high freq + high duty resolution application ?

Delay Line-based DPWM



A. P. Dancy, A. P. Chandrakasan, "Ultra low power control circuits …," *IEEE PESC*, 1991

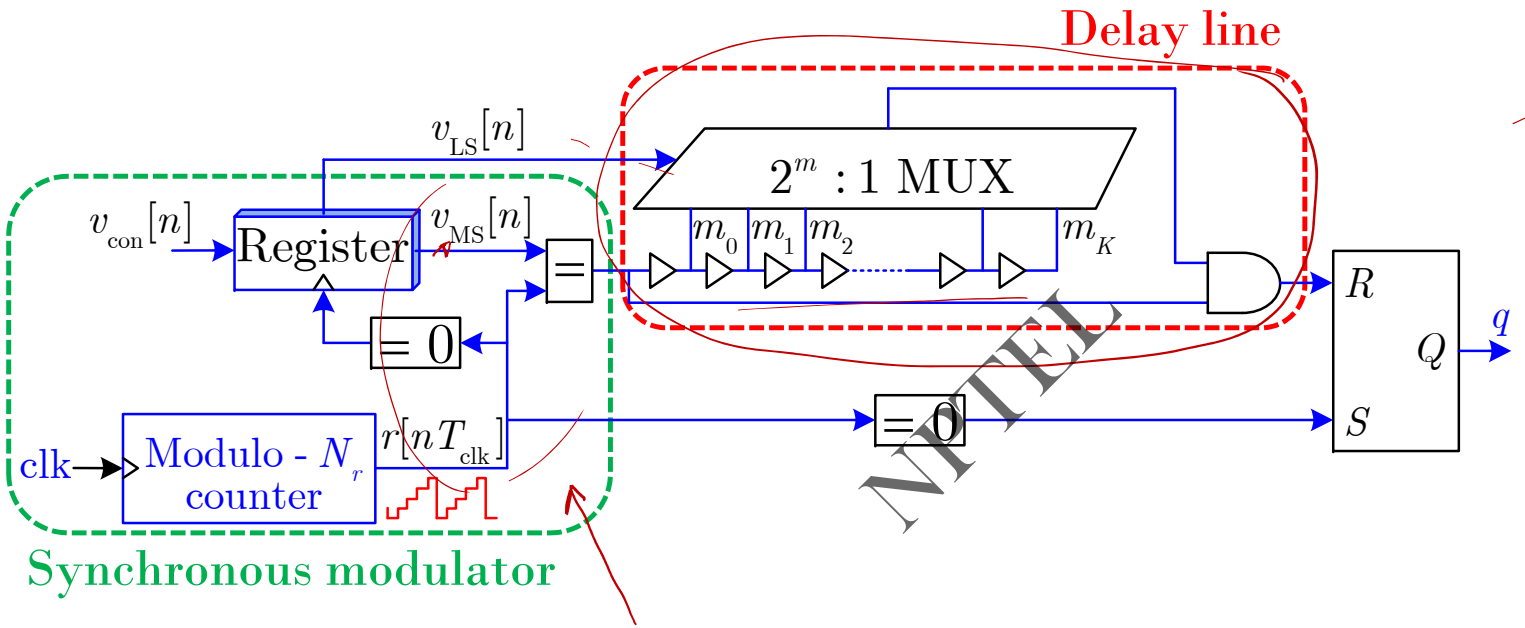
Delay Line-based DPWM (contd…)



- Disadvantage:

  The length of the delay line and the size of the multiplexed grow exponentially with the number of bits n_{DPWM}

Hybrid DPWM



8-bit DPWM

3-bit counter-based

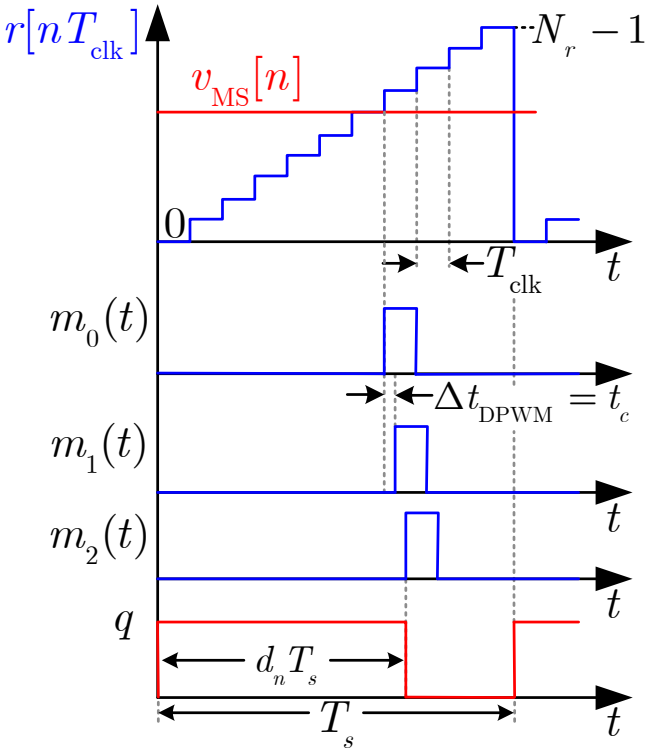
$f_{sw} = 2^3 \times f_{sw}$

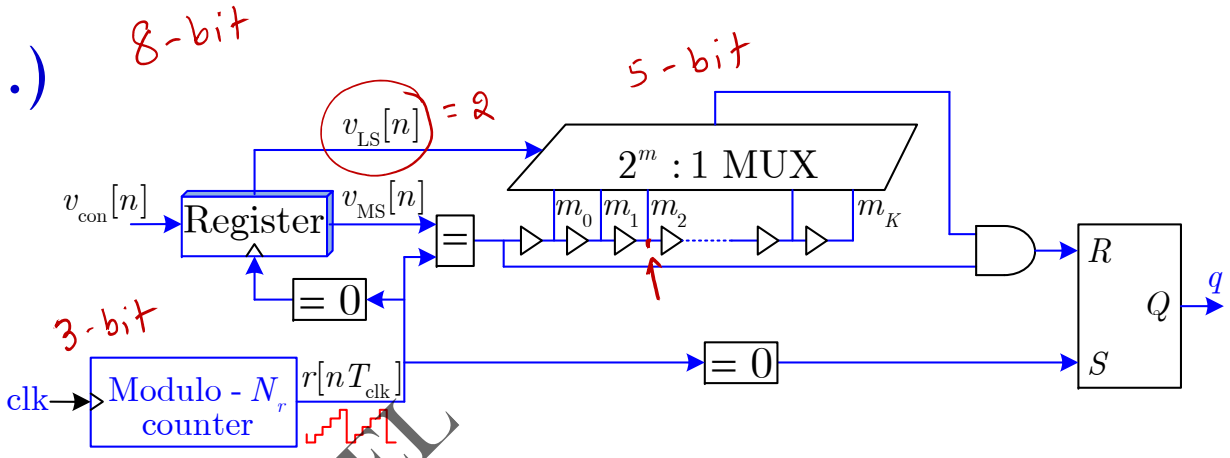
5-bit delay line

2^5 no. delays (buffers)

[A. P. Dancy, et Al., "High-efficiency multiple-output DC-DC … " *IEEE Trans. VLSI*, June 2000]

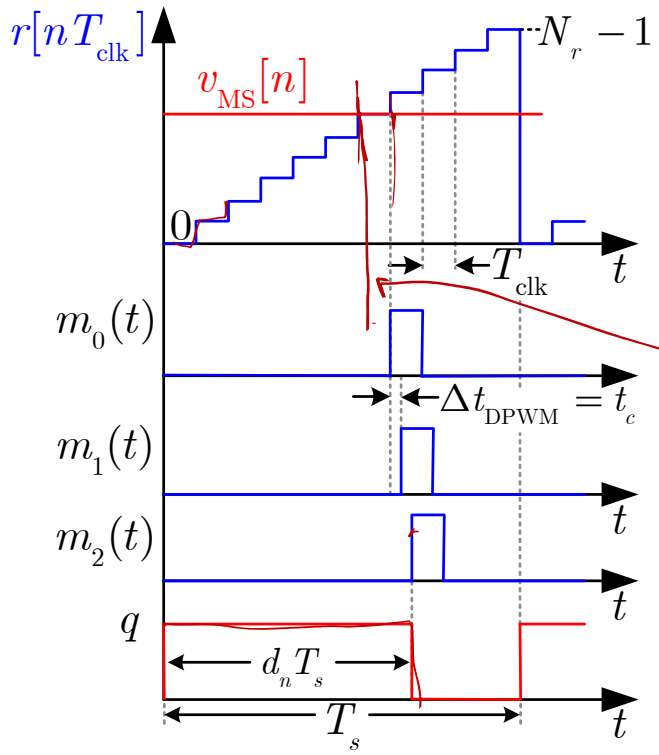
Hybrid DPWM (contd…)

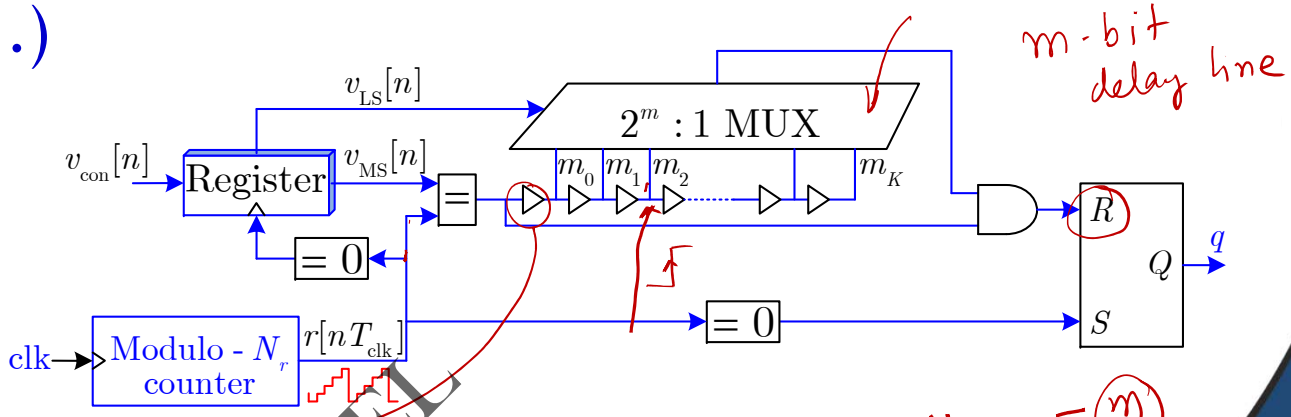




- Let $v_{LS}[n] = 2$

Hybrid DPWM (contd…)





m-bit delay line

- Let $v_{LS}[n] = 2$

$$\Rightarrow \frac{T_{clk}}{T_s} = \frac{f_s}{f_{clk}} = \frac{1}{2^{(n_{DPWM} - m)}}$$

$N_{dpwm} - m$

$f_{sw} = 2$ × few

[For details, refer to *'Digital Control of High-frequency Switched …', Wiley-IEEE Press, 2015*]

CONCLUSION

- Digital Pulse Width Modulation – Requirements and Challenges
- Counter-based DPWM Architecture
- Delay-line DPWM Architecture
- Hybrid DPWM Architecture

THANK YOU !