NPTEL ONLINE CERTIFICATION COURSES

DIGITAL CONTROL IN SMPCs AND FPGA-BASED PROTOTYPING

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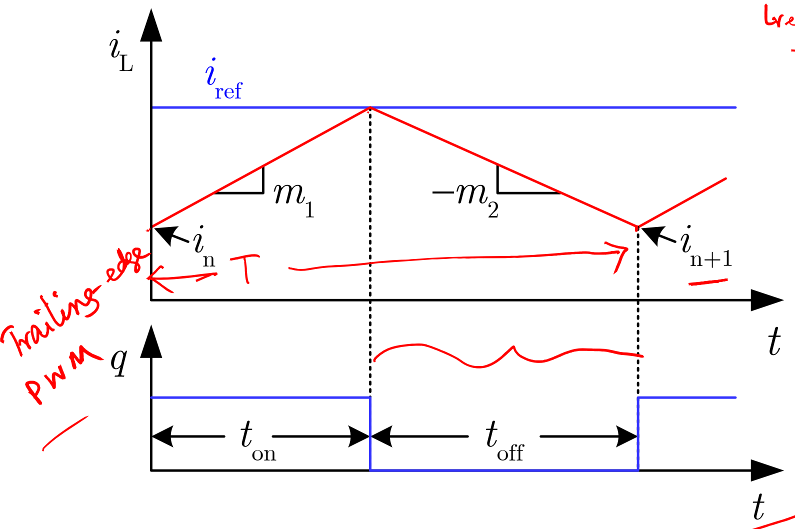
Module 04: Modeling Techniques and Mode Validation using MATLAB

Lecture 32: Discrete Time Modeling with Closed Current Loop

CONCEPTS COVERED

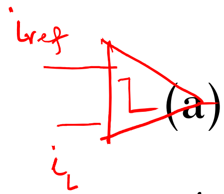
- Discrete-time modeling analog current loop
- Current loop stability under mixed-signal CMC
- Current-loop stability under fully digital CMC
- Need for going closed-loop stability analysis

Fixed Frequency Analog Peak CMC – Current Loop Stability



$$i_{n+1} = i_{ref} - m_2 t_{off}$$

$$i_n = i_{ref} - m_1 t_{on}$$



$t_{on} = dT$

(a) Under fixed-frequency modulation

$$t_{on} = dT; \quad t_{off} = (1-d)T$$

$$i_{n+1} = i_{ref} - m_2 (1-d)T$$

$$i_n = i_{ref} - m_1 dT$$

$$\Rightarrow dT = \left(\frac{i_{ref} - i_n}{m_1}\right)$$

[For details, refer to Lecture~23, NPTEL "Control and Tuning Methods ..." course (Link)

Current Loop Stability Analysis (contd...)

$$dT = \frac{i_{ref} - i_n}{m_1}$$

Thus, $i_{n+1} = i_{ref} + m_2\left(\frac{i_{ref} - i_n}{m_1}\right) - m_2 T \;= -\left(\frac{m_2}{m_1}\right) i_n + \left(1 + \frac{m_2}{m_1}\right) i_{ref} - m_2 T$

Perturbed current dynamics becomes

$$\boxed{\tilde{i}_{n+1} = -\left(\frac{m_2}{m_1}\right)\tilde{i}_n + \left(1 + \frac{m_2}{m_1}\right)\tilde{i}_{ref}}$$

① Zero-input stability

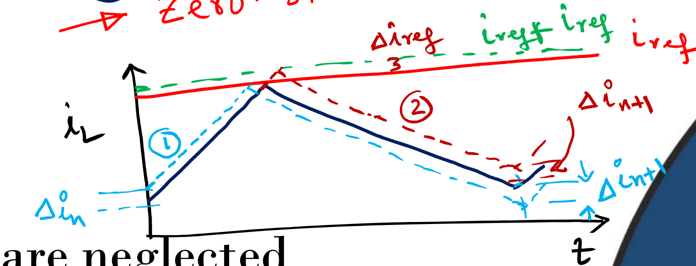
$\tilde{i}_{ref} = 0$ but $\tilde{i}_n \neq 0$

② Zero-state stability

- <u>Assumptions</u>:

  1. Perturbations in slopes are neglected

  2. Nonlinear perturbed (product) terms are neglected



[For details, refer to Lecture~23, NPTEL "Control and Tuning Methods ..." course (<u>Link</u>)

Current Loop Stability Analysis (contd...)

inner current-loop stability due to the perturbation in i_n

For constant reference, $\tilde{i}_{\text{ref}} = 0;$

Thus, $\tilde{i}_{\text{n+1}} = -\left(\dfrac{m_2}{m_1}\right)\tilde{i}_{\text{n}}$

$\tilde{i}_L(z)\left(z + \dfrac{m_2}{m_1}\right) = 0$

$z = -\dfrac{m_2}{m_1}$

For inner loop stability,

$$\boxed{\left|\frac{m_2}{m_1}\right| < 1}$$

Slope	Buck Converter	Boost Converter
m_1 ✓	$\dfrac{V_{\text{in}} - V_{\text{o}}}{L}$	$\dfrac{V_{\text{in}}}{L}$
m_2	$\dfrac{V_{\text{o}}}{L}$	$\dfrac{V_{\text{o}} - V_{\text{in}}}{L}$

[For details, refer to Lecture~23, NPTEL "Control and Tuning Methods ..." course (Link)

Current Loop Stability Analysis (contd...)

- **Buck Converter:**

$$\left|\frac{m_2}{m_1}\right| = \left|\frac{V_o}{V_{in} - V_o}\right| = \frac{V_o}{V_{in} - V_o} \quad \text{(Since } 0 < V_o < V_{in}\text{)}$$

$$\therefore \frac{V_o}{V_{in} - V_o} < 1$$

$$\Rightarrow \frac{V_o}{V_{in}} < \frac{1}{2}$$

$$\boxed{\Rightarrow D < 0.5}$$

[For details, refer to Lecture~23, NPTEL "Control and Tuning Methods ..." course (Link)

Current Loop Stability Analysis (contd…)

- <u>Boost Converter</u>:

$$\frac{m_2}{m_1} = \frac{V_o - V_{\text{in}}}{V_{\text{in}}}$$

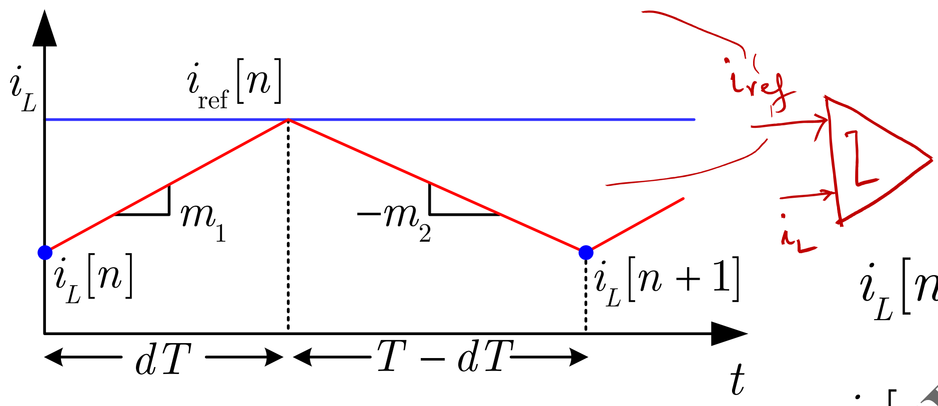
$$\therefore \frac{V_o - V_{\text{in}}}{V_{\text{in}}} < 1$$

$$\Rightarrow V_o < 2V_{\text{in}}$$

$$\boxed{\Rightarrow D < 0.5}$$

[For details, refer to Lecture~23, NPTEL "Control and Tuning Methods …" course (Link)

Fixed Frequency Mixed Signal Peak CMC – Current Loop Stability



$$i_{\text{ref}}[n] = i_L[n] + m_1 dT$$

$$i_L[n+1] = i_{\text{ref}}[n] - m_2\left(1-d\right)T$$

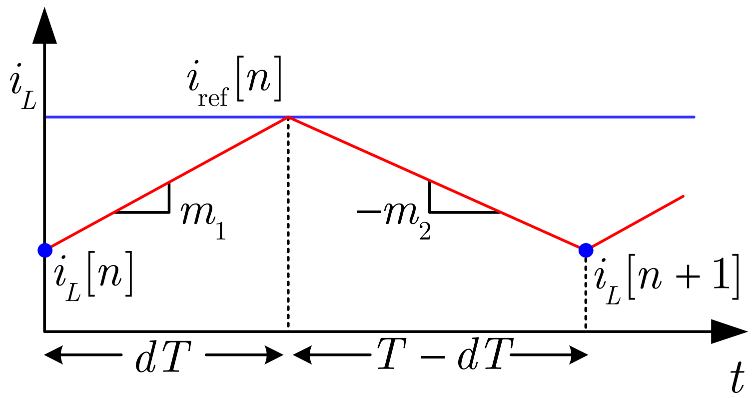
$$i_L[n+1] = i_L[n] + m_1 dT - m_2\left(1-d\right)T$$

$$i_L[n+1] = i_L[n] + (m_1 + m_2)dT - m_2 T$$

$$dT = \frac{i_{\text{ref}}[n] - i_L[n]}{m_1}$$

$$\Rightarrow i_L[n+1] = i_L[n] + \frac{m_1+m_2}{m_1}\left(i_{\text{ref}}[n] - i_L[n]\right) - m_2 T$$

Fixed Frequency Mixed Signal Peak CMC – Current Loop Stability



$$i_L[n+1] = i_L[n] + \frac{m_1+m_2}{m_1}(i_{ref}[n] - i_L[n]) - m_2 T$$

Perturbed dynamics

$$\tilde{i}_L[n+1] = \tilde{i}_L[n] + \frac{m_1+m_2}{m_1}(\tilde{i}_{ref}[n] - \tilde{i}_L[n])$$

Z transform

$$\frac{\tilde{i}_L(z)}{\tilde{i}_{ref}(z)} = \frac{1+\dfrac{m_2}{m_1}}{z+\dfrac{m_2}{m_1}} \quad \Rightarrow \left|\frac{m_2}{m_1}\right| < 1 \quad \Rightarrow D < 0.5$$

$0 < \frac{m_2}{m_1} < 1$

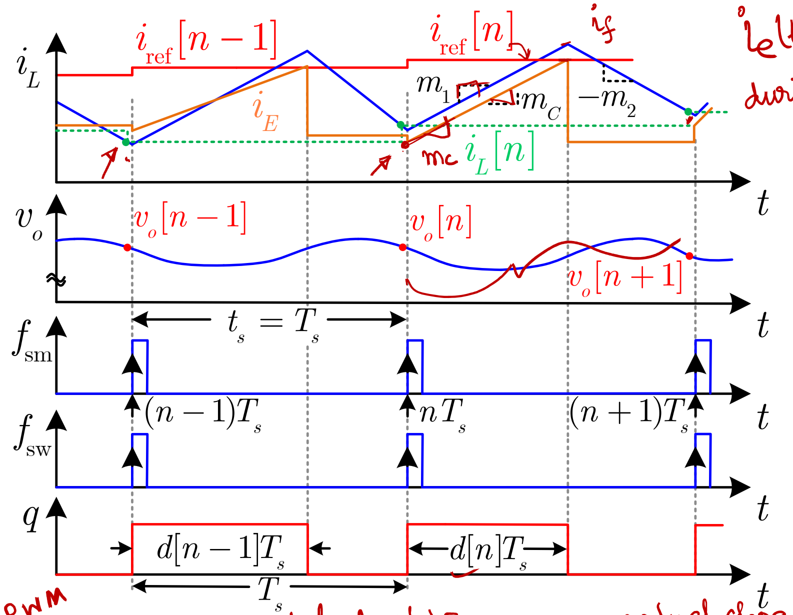
zero-input stability $(\tilde{i}_{ref} = 0)$

Same as analog CMC!!

Fixed reference current i_{ref}

Fixed Frequency Fully Digital Peak CMC – Current Loop Stability

$m_1 = \frac{v_{in} - v_o}{L}$



$i_e(t) = i_L[n-1] + m_c t$ during n^{th} clock cycle

$$i_L[n+1] = i_L[n] + m_1 d[n]T - m_2\big(1 - d[n]\big)T$$

$$i_L[n+1] = i_L[n] + (m_1 + m_2)d[n]T - m_2 T$$

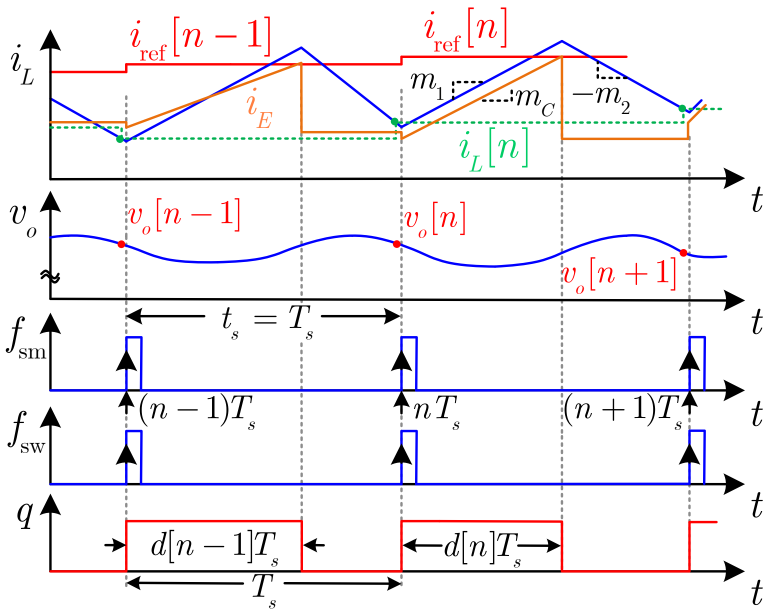
$$d[n]T = \frac{i_{ref}[n] - i_L[n-1]}{m_c}$$

$m_c \rightarrow$ emulated slope , $m_1 -$ actual slope

say : $a = \frac{m_1 + m_2}{m_c}$

$$\Rightarrow i_L[n+1] = i_L[n] + \frac{m_1 + m_2}{m_c}\left(i_{ref}[n] - i_L[n-1]\right) - m_2 T$$

Fixed Frequency Fully Digital Peak CMC – Current Loop Stability



$$i_L[n+1] = i_L[n] + \frac{m_1+m_2}{m_c}\left(i_{\text{ref}}[n] - i_L[n-1]\right) - m_2 T$$

Perturbed dynamics

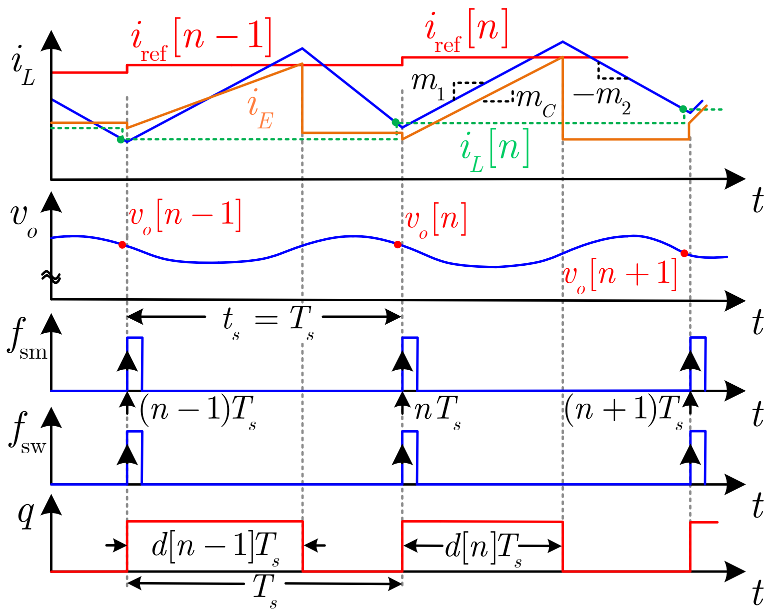
$$\tilde{i}_L[n+1] = \tilde{i}_L[n] + \frac{m_1+m_2}{m_c}\left(\tilde{i}_{\text{ref}}[n] - \tilde{i}_L[n-1]\right)$$

$= a$

Apply Z transform

$$z\tilde{i}_L(z) = \tilde{i}_L(z) + a\tilde{i}_{\text{ref}}(z) - az^{-1}\tilde{i}_L(z)$$

Fixed Frequency Fully Digital Peak CMC – Current Loop Stability



Z transform

$$z\tilde{i}_L(z) = \tilde{i}_L(z) + a\tilde{i}_{ref}(z) - az^{-1}\tilde{i}_L(z)$$

$$\tilde{i}_L(z)\left[z - 1 + az^{-1}\right] = \tilde{i}_{ref}(z)\,a$$

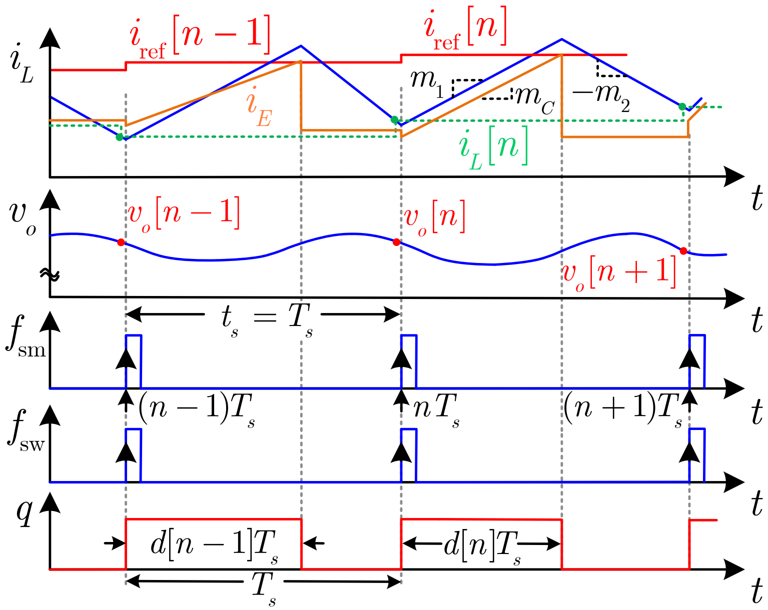
$\tilde{i}_L(z)\left[z^2 - z + a\right] = 0$ if $\tilde{i}_{ref}(z) = 0$

zero-input stability

roots of z must lie inside the unit circle

$$\frac{\tilde{i}_L(z)}{\tilde{i}_{ref}(z)} = \frac{az}{z^2 - z + a} \quad \text{where} \quad a = \frac{m_1 + m_2}{m_c}$$

Fixed Frequency Fully Digital Peak CMC – Current Loop Stability



$a>0$

$$\frac{\tilde{i}_L(z)}{\tilde{i}_{\text{ref}}(z)} = \frac{az}{z^2 - z + a} \quad \text{where} \quad a = \frac{m_1 + m_2}{m_c}$$

$z^2 - z + a = 0$

$\left(z - \frac{1}{2}\right)^2 = \left(\frac{1}{2}\right)^2 - a$

$z = \frac{1}{2} \pm \frac{1}{2}\sqrt{1-4a}$

For current-loop stability

$$a < 1 \Rightarrow \frac{m_1 + m_2}{m_c} < 1$$

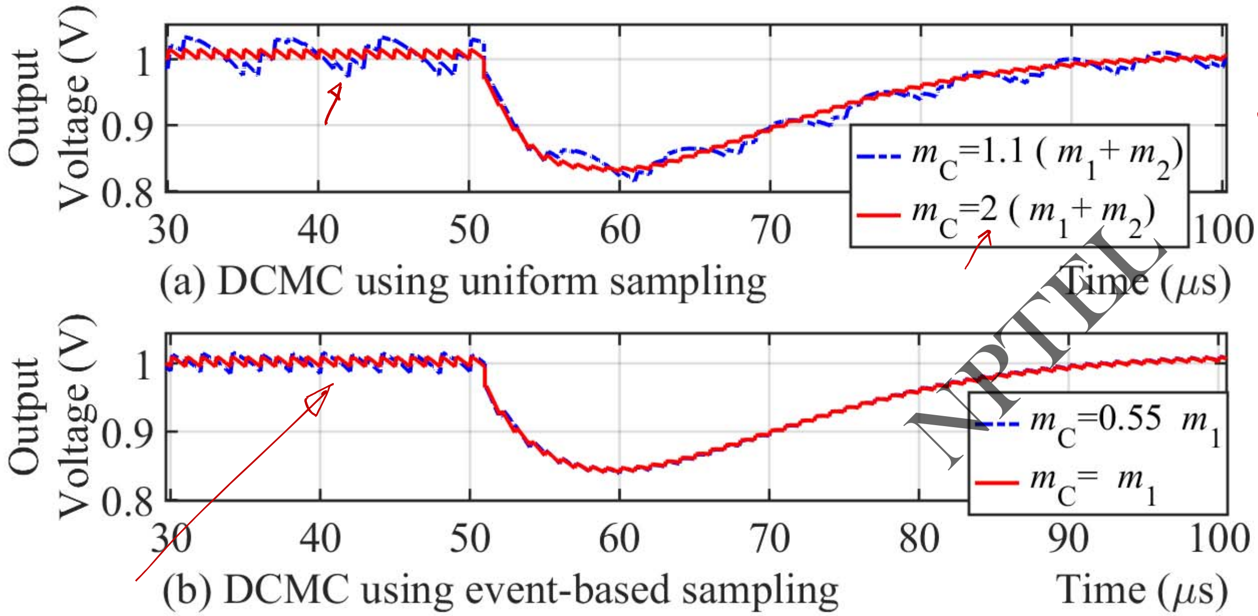
$$\Downarrow$$

$$m_c > m_1 + m_2$$

$m_c > m_1 + m_2$

[S. Kapat, “Beyond Stability and Performance Limits in Digital Current Mode Control …”, *IEEE APEC*, 2021]

Fixed Frequency Fully Digital Peak CMC – Closed-Loop Stability



[S. Kapat, "Beyond Stability and Performance Limits in Digital Current Mode Control …", *IEEE APEC*, 2021]

$$m_c > m_1 + m_2$$

- Need to study closed-loop stability!!
- Detailed system model needed

CONCLUSION

- Discrete-time modeling analog current loop
- Current loop stability under mixed-signal CMC
- Current-loop stability under fully digital CMC
- Need for going closed-loop stability analysis

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THANK YOU !