



**NPTEL ONLINE CERTIFICATION COURSES**

# **DIGITAL CONTROL IN SMPCs AND FPGA-BASED PROTOTYPING**

**Dr. Santanu Kapat**

**Electrical Engineering Department, IIT KHARAGPUR**

**Module 02: Fixed and Variable Frequency Digital Control Architectures**

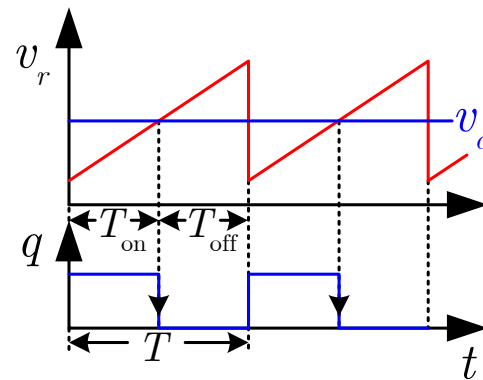
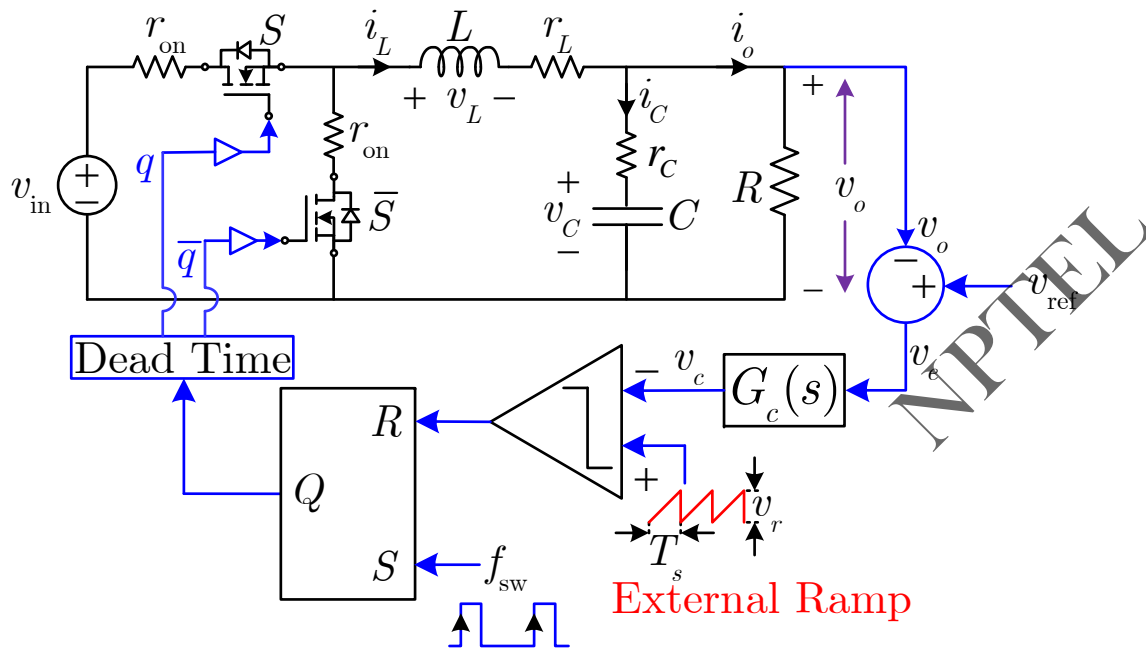
**Lecture 12: Voltage Mode Digital Pulse Width Modulators and Sampling Methods**



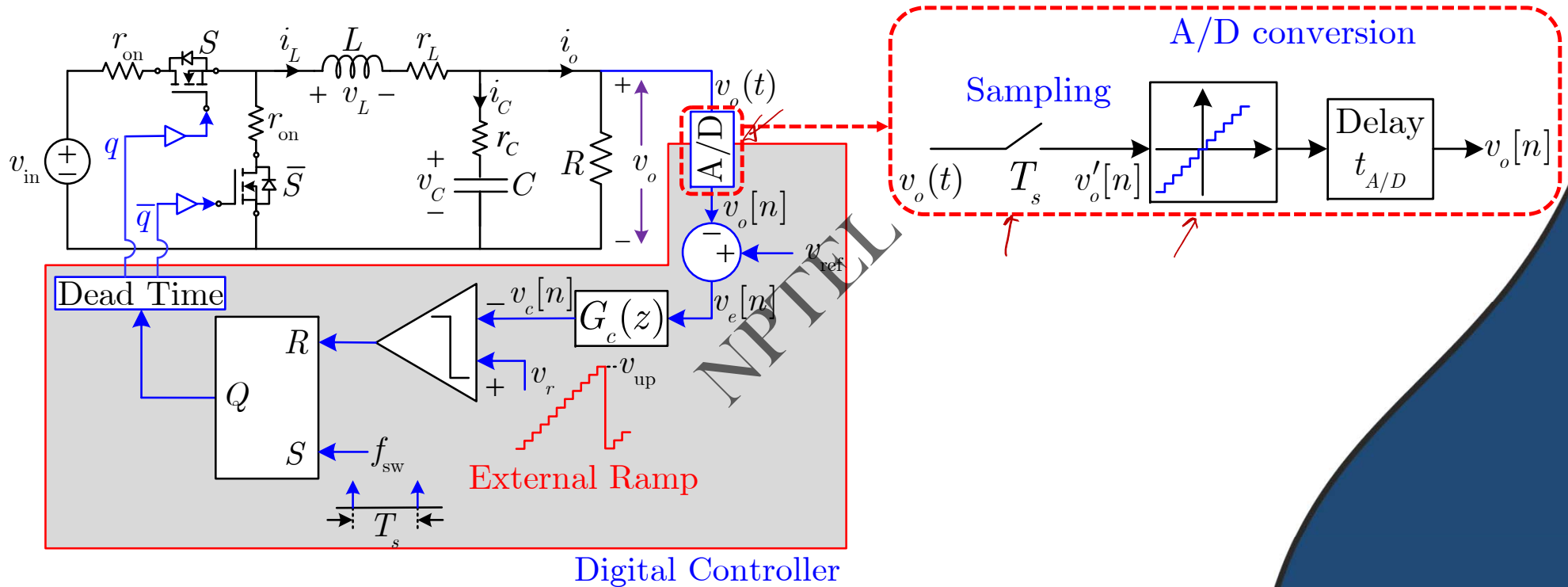
## CONCEPTS COVERED

- Trailing-edge PWM and digital voltage mode control
- Sampling delay and control waveforms
- Leading-edge PWM and digital voltage mode control
- Digital voltage mode control architectures

# Analog Voltage Mode Control



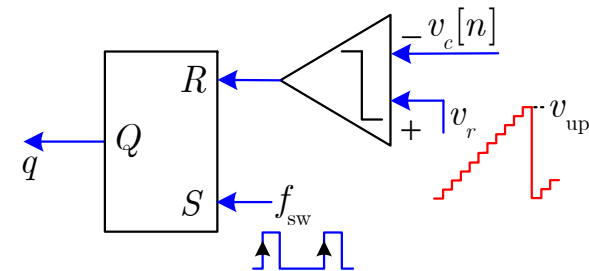
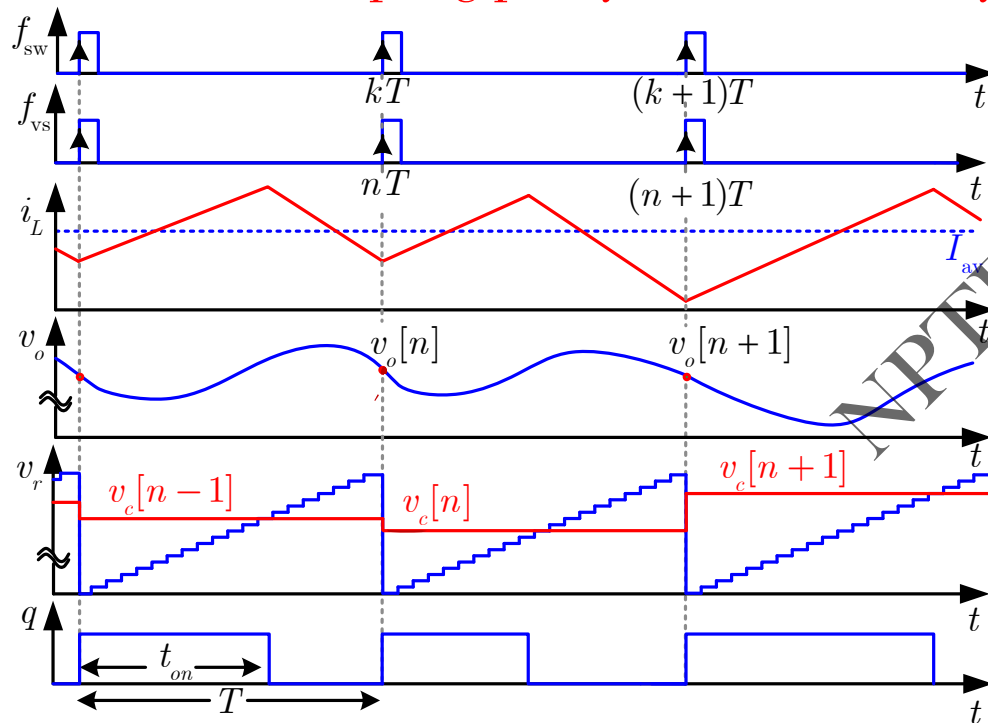
# Digital Voltage Mode Control



DPWM voltage-mode control: Buck Converter

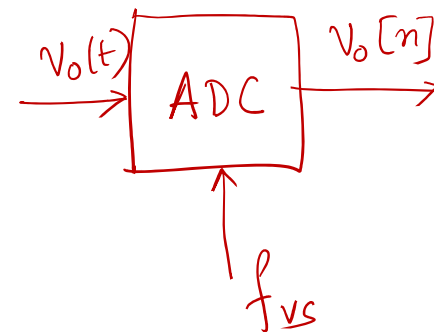
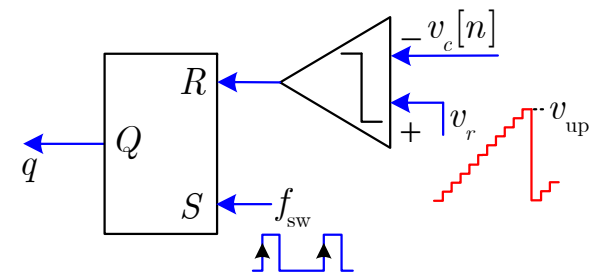
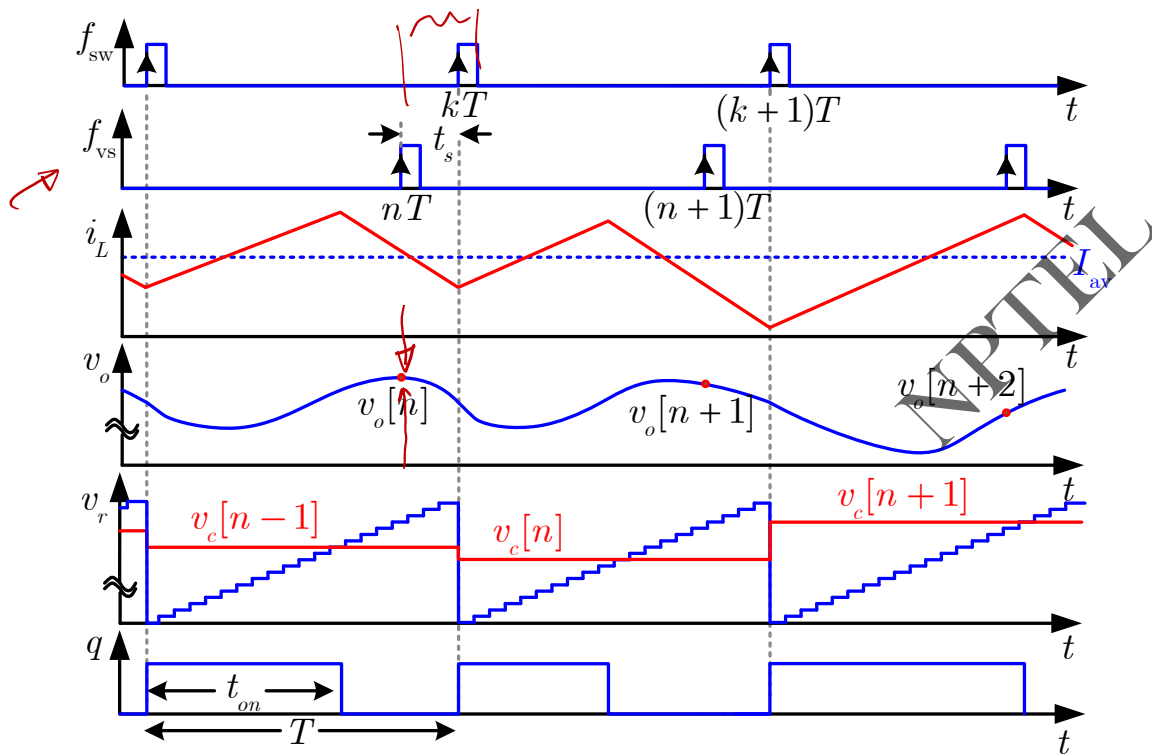
# Trailing-edge Modulation : Uniform Sampling

## Case 1: One sampling per cycle without delay



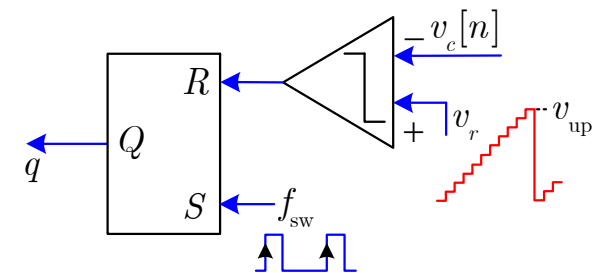
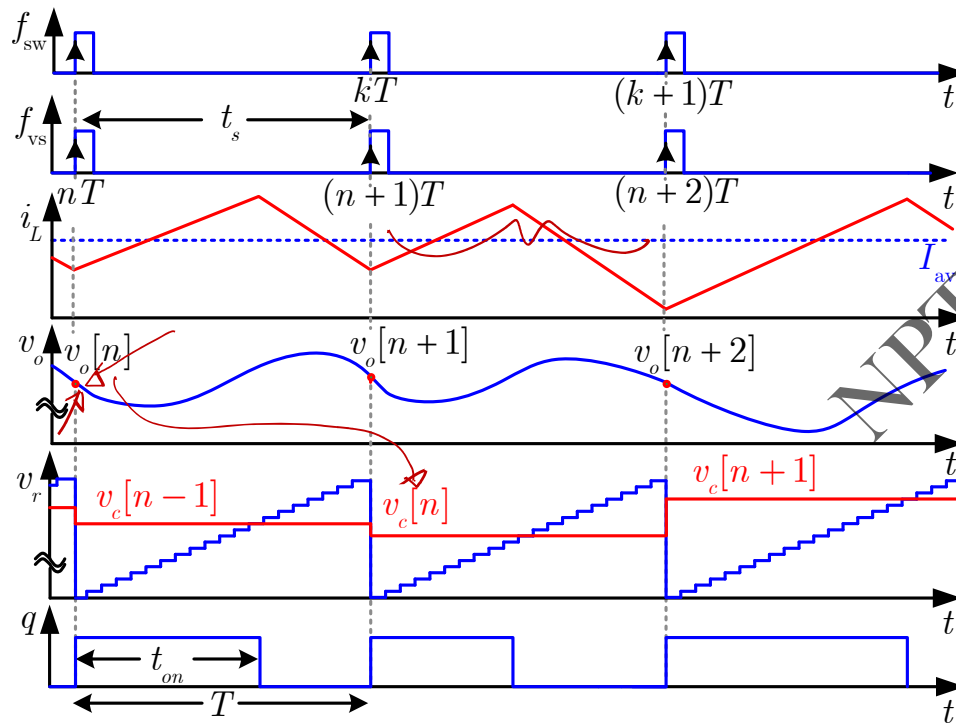
## Trailing-edge Modulation : Uniform Sampling (contd...)

Case 2: Interval 2 sampling ( $t_s$  time delay)



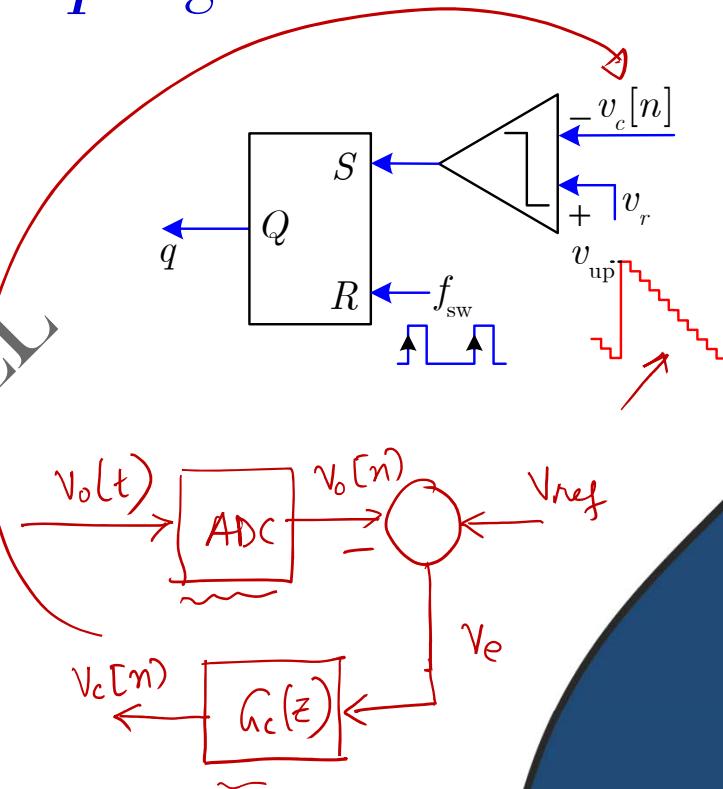
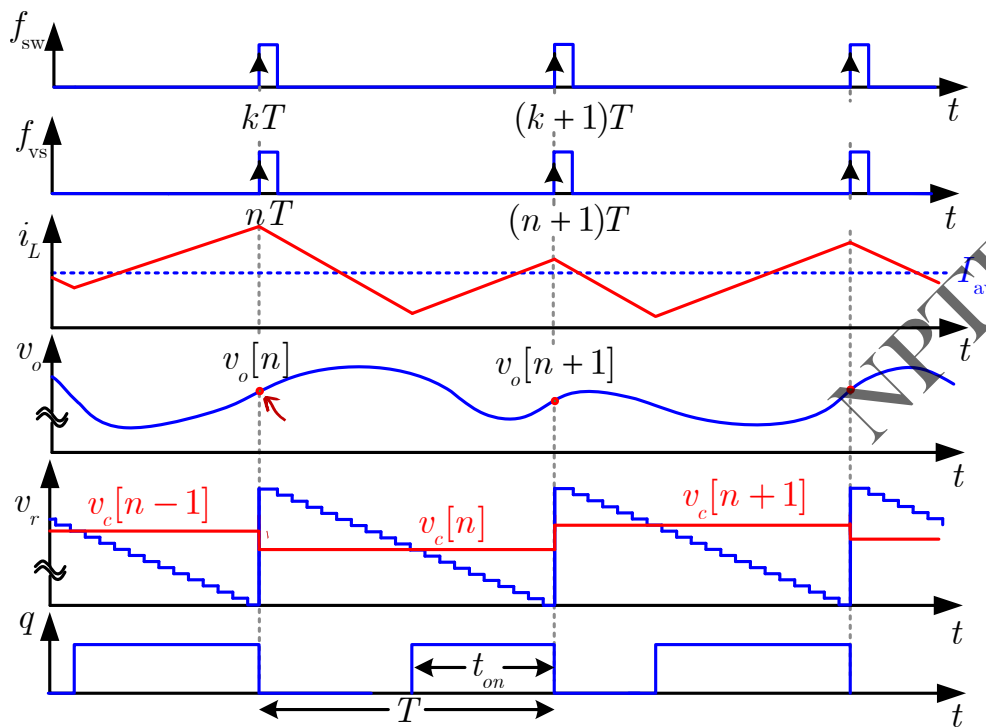
## Trailing-edge Modulation : Uniform Sampling (contd...)

### Case 3: Interval 2 sampling (one cycle delay)



# Leading-edge Modulation : Uniform Sampling

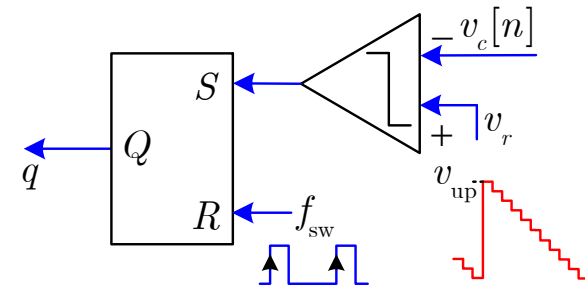
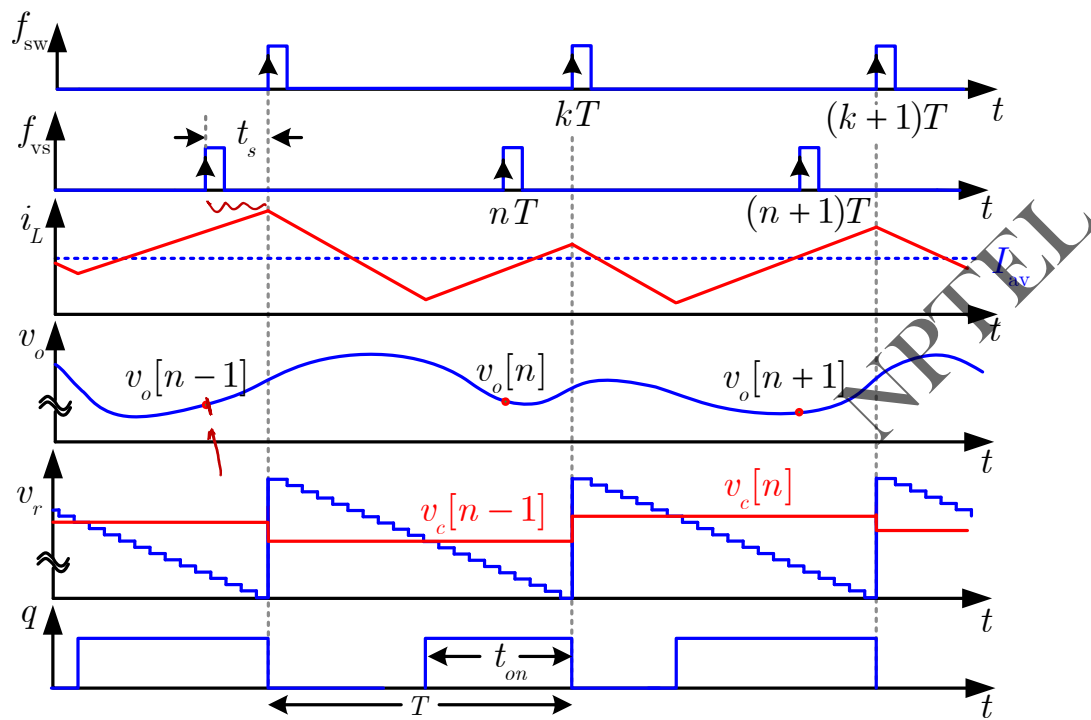
Case 1: One sampling per cycle without delay





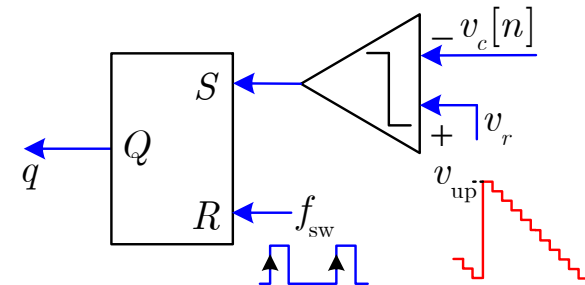
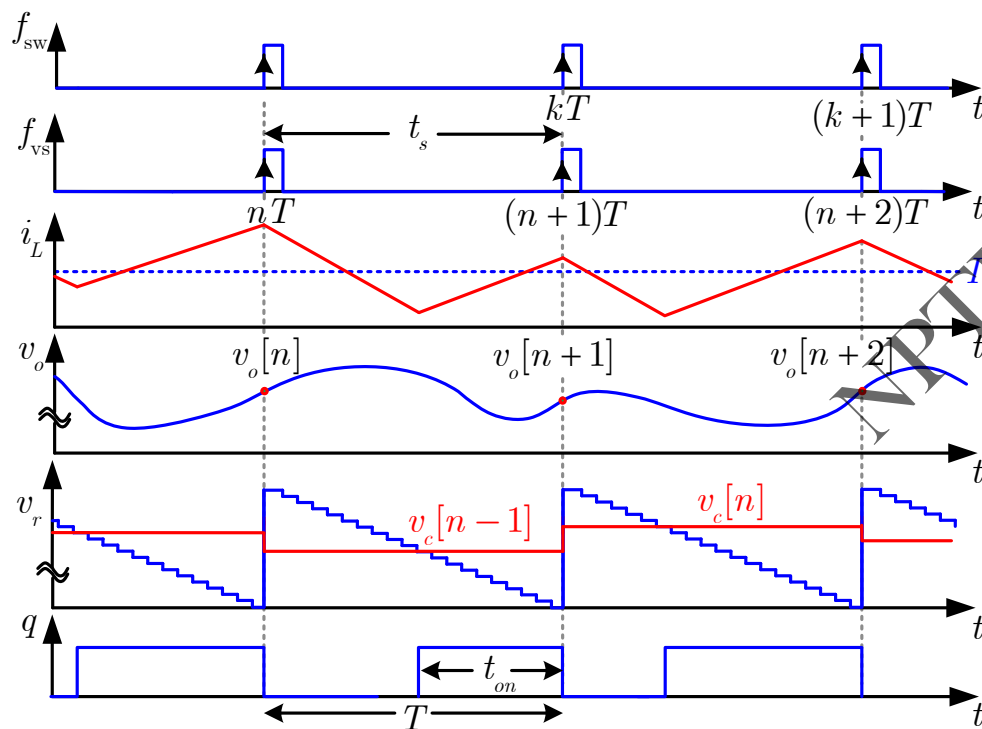
## Leading-edge Modulation : Uniform Sampling (contd...)

Case 2: Interval 1 sampling ( $t_s$  time delay)



# Leading edge modulation : Uniform sampling

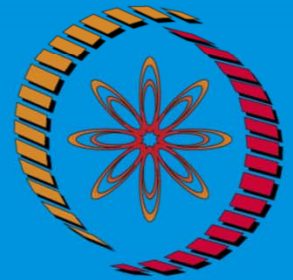
## Case 3: Interval 1 sampling (one cycle delay)



$v_o(t)$  Pipeline ADC  $v_o[n]$

## CONCLUSION

- Trailing-edge PWM and digital voltage mode control
- Sampling delay and control waveforms
- Leading-edge PWM and digital voltage mode control
- Digital voltage mode control architectures



**THANK  
YOU !**