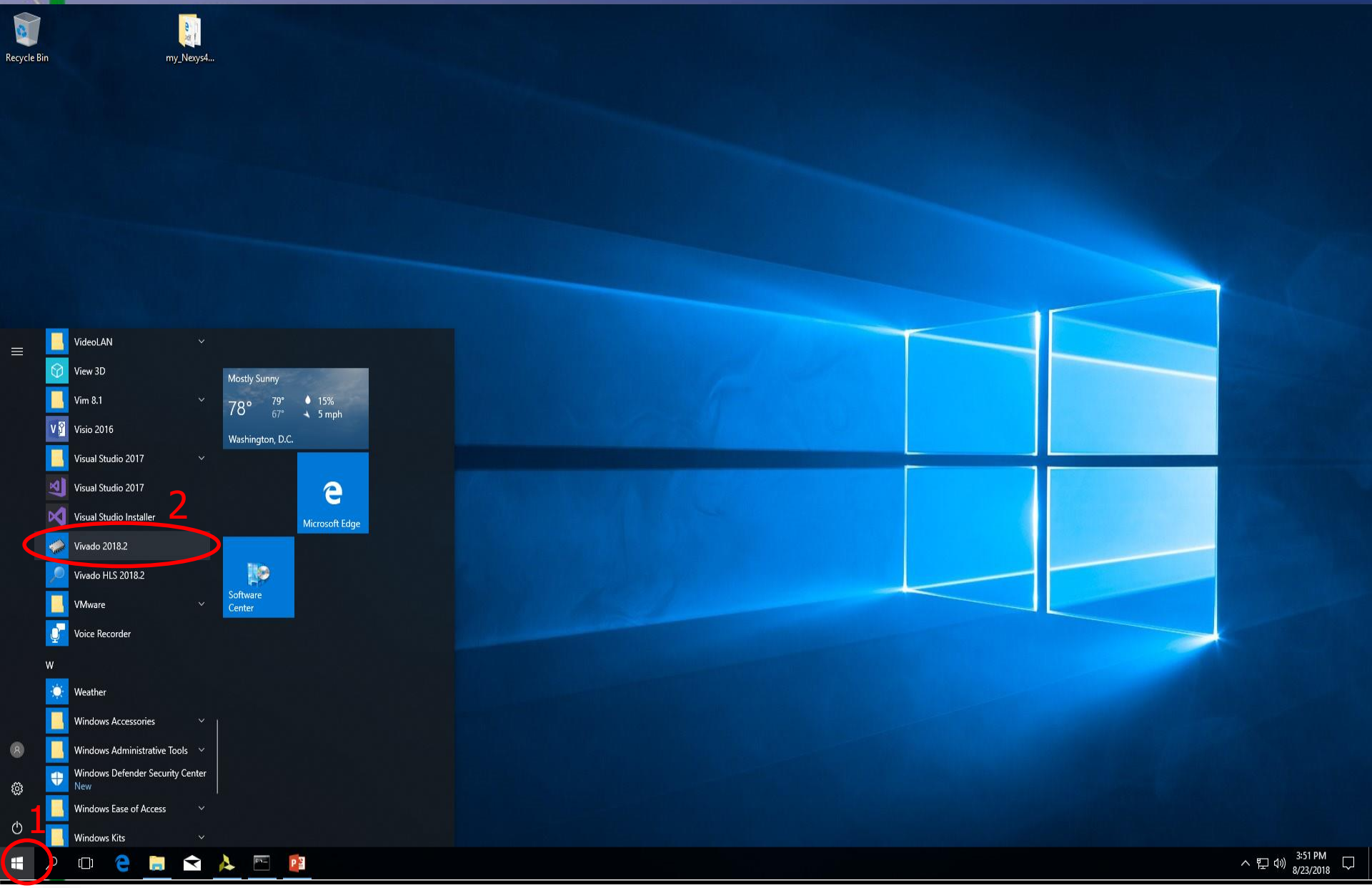
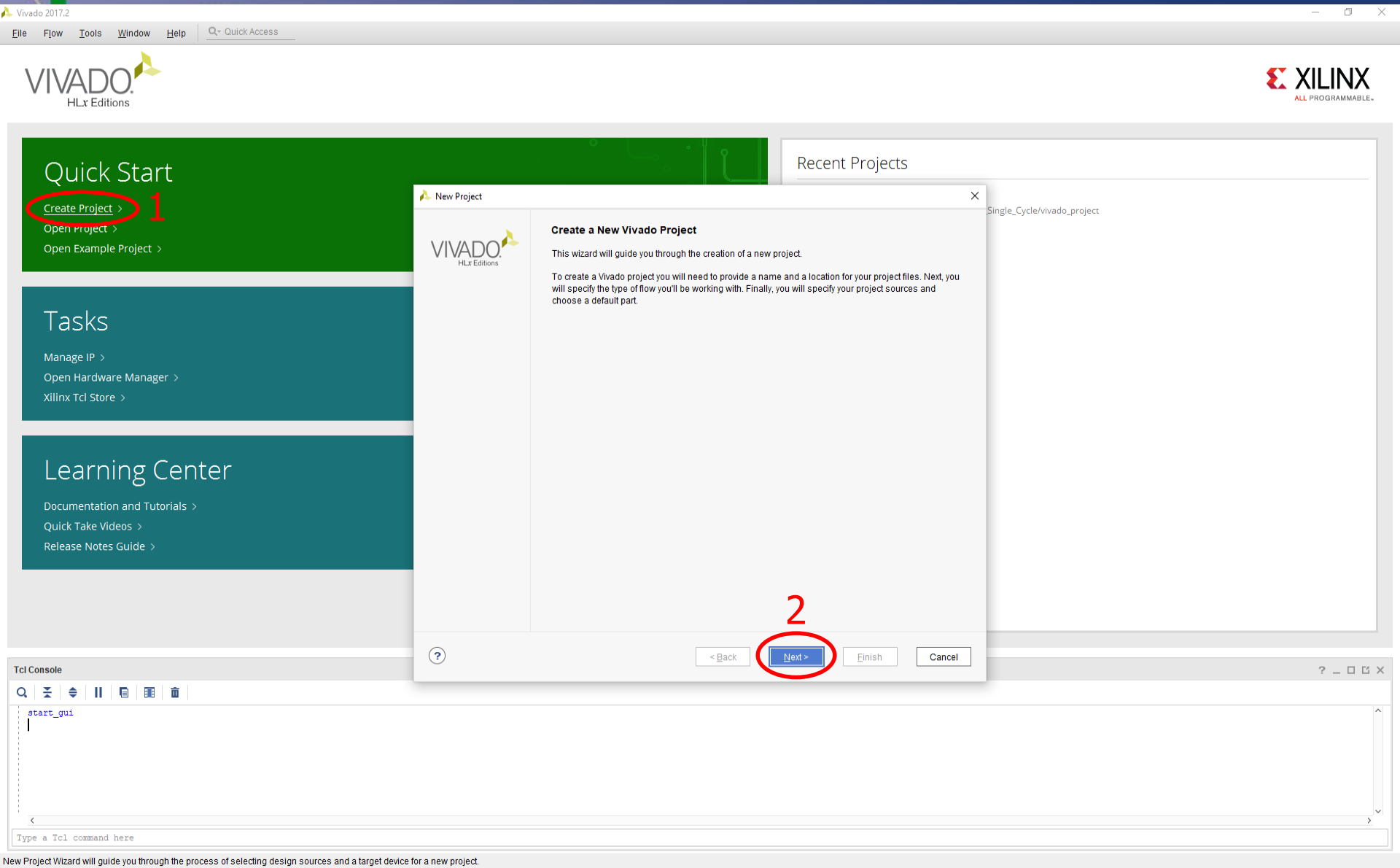
Functional Simulation using Xilinx Vivado 2019.2

1) Create a blank Vivado project
   - Project name
   - Project destination folder
   - Choose default settings
2) Add source files
   - Design file(s)
   - Simulation files
     - Testbench
     - Waveform configuration
3) Run behavioral/functional simulation
   - Simulation settings, e.g., simulation time
   - Edit waveform configuration, e.g., waveform style (digital, analog), add signals, add dividers, signal radix, etc.

Xilinx Vivado 2019.2 – (1) Create Project



Xilinx Vivado 2019.2 – (1) Create Project



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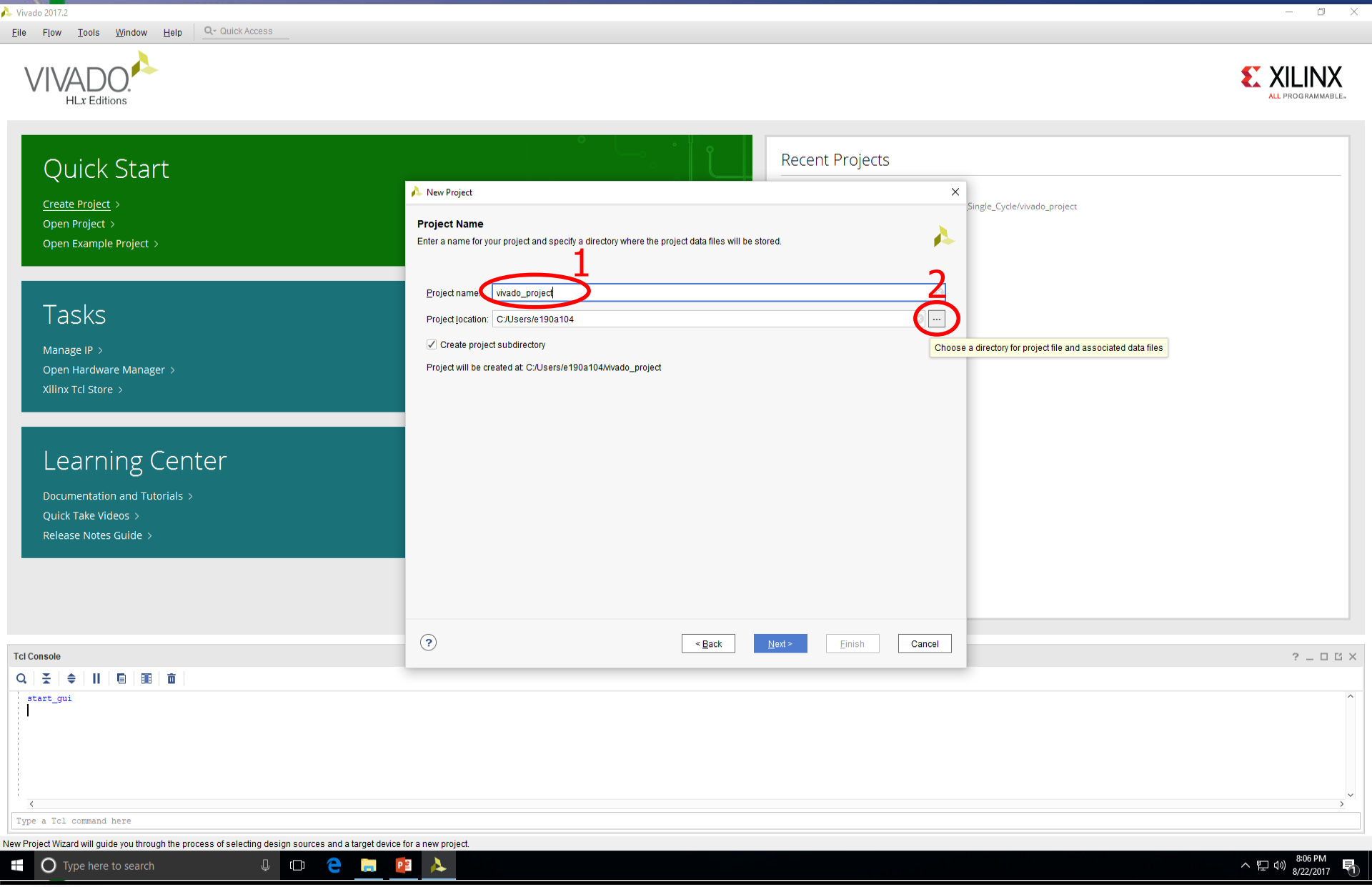
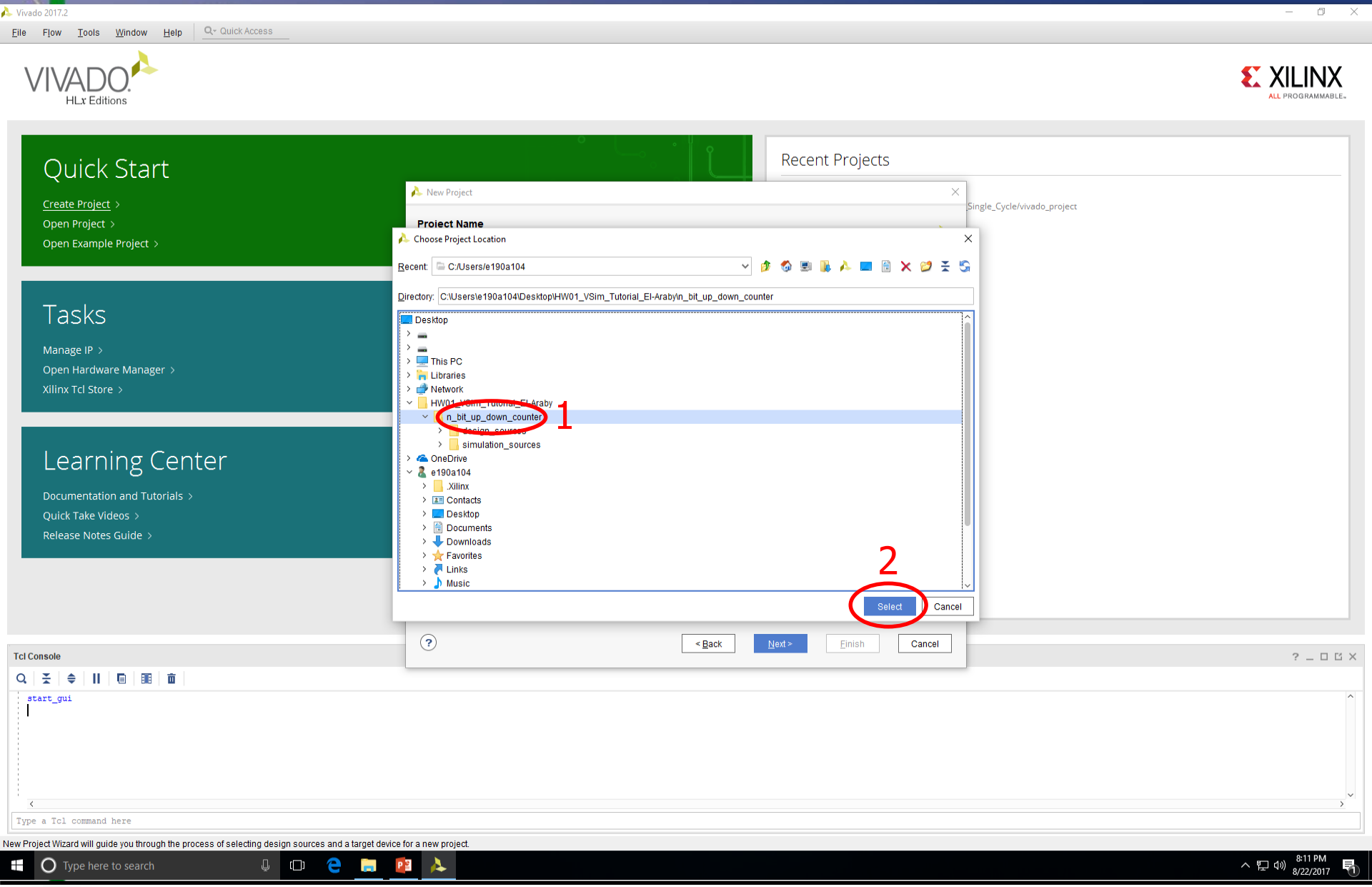


Xilinx Vivado 2019.2 – (1) Create Project



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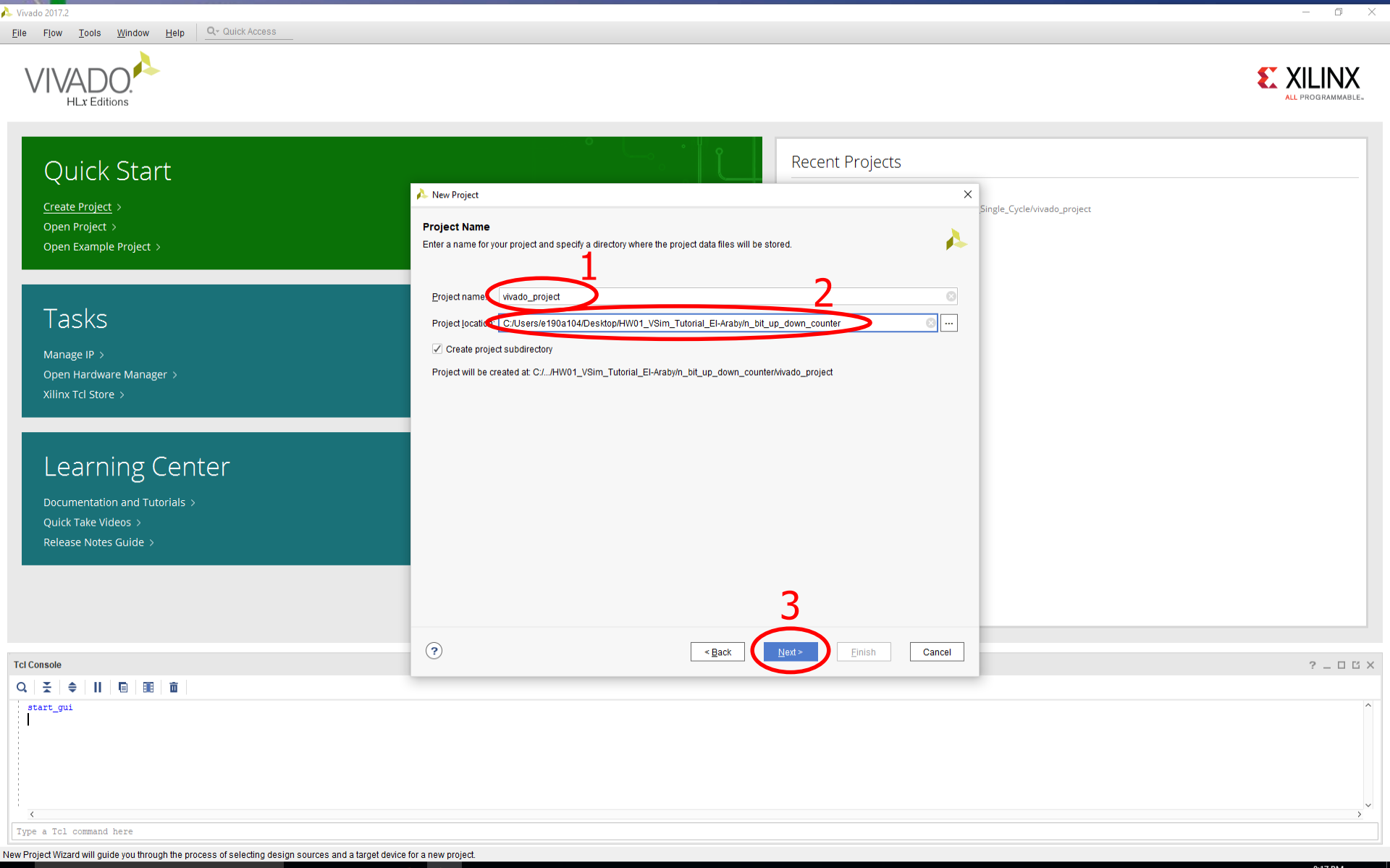

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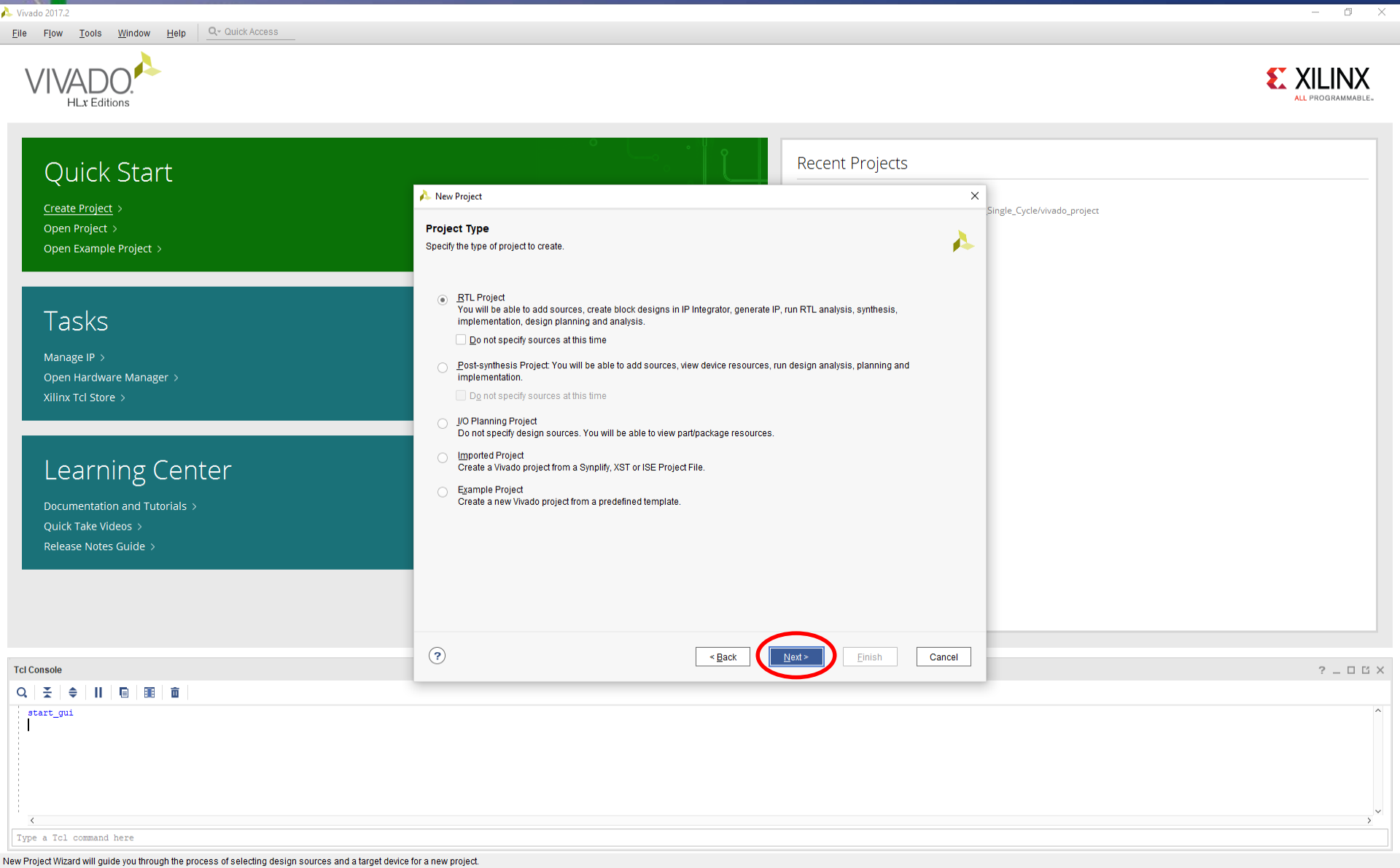

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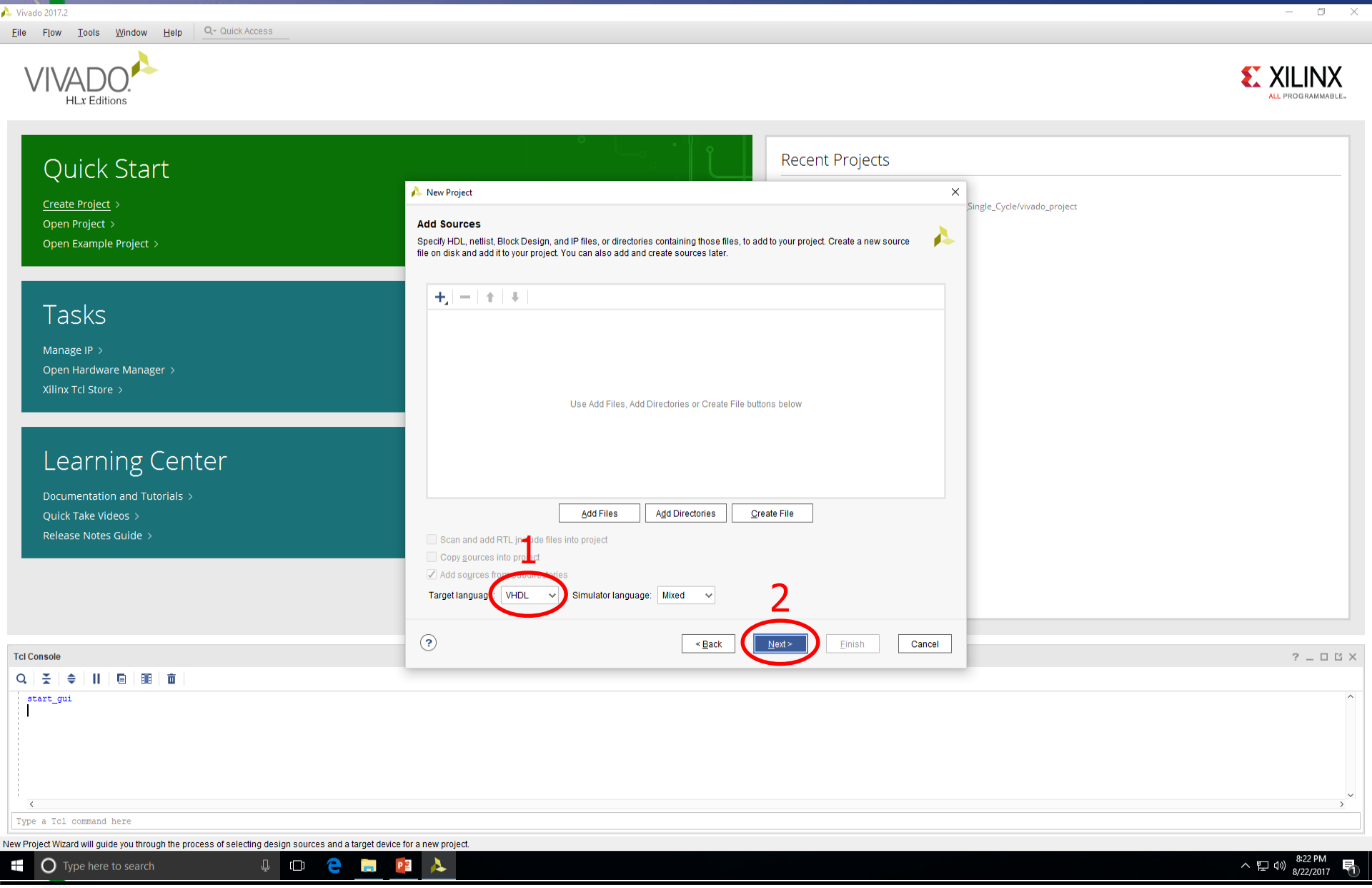

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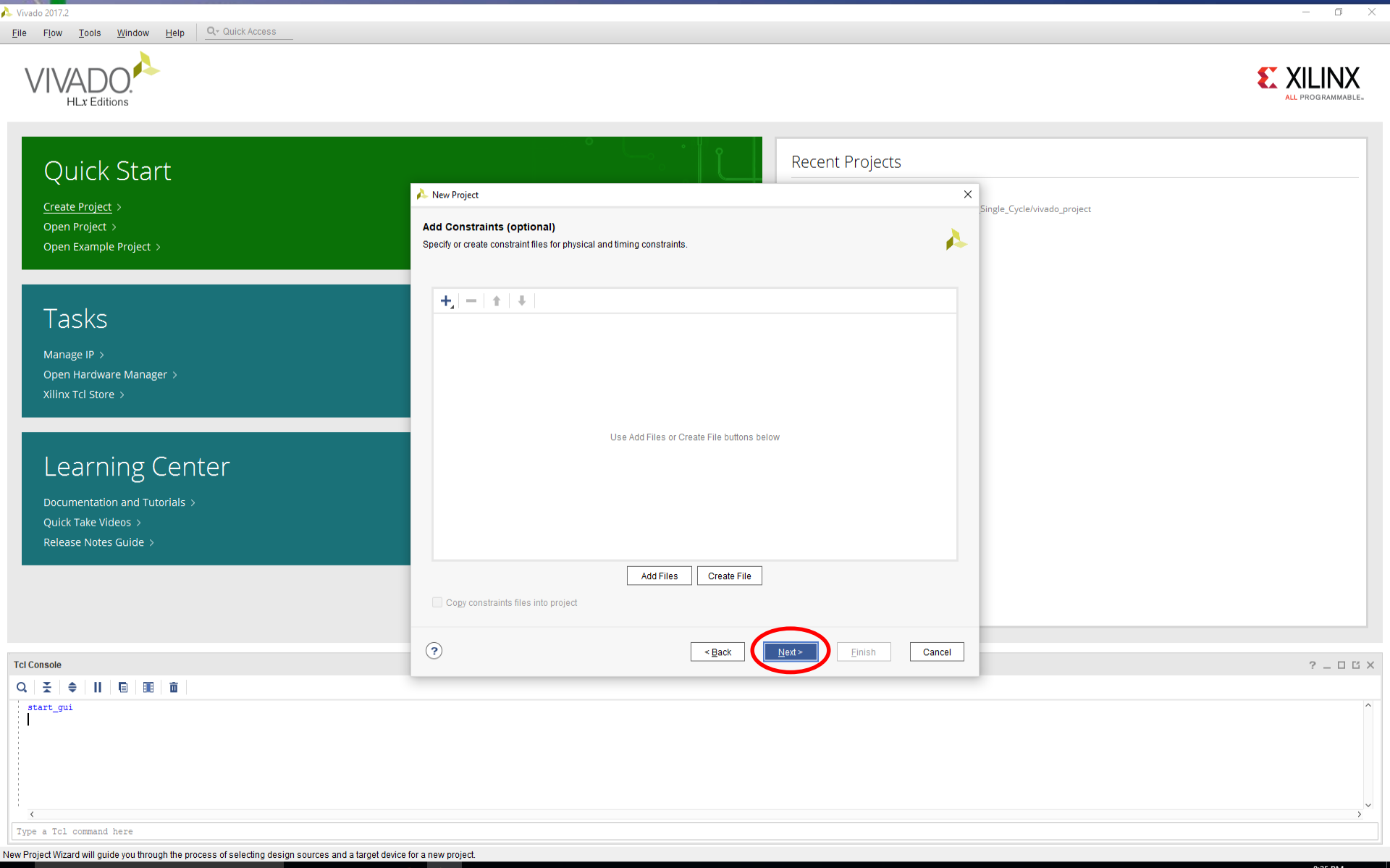

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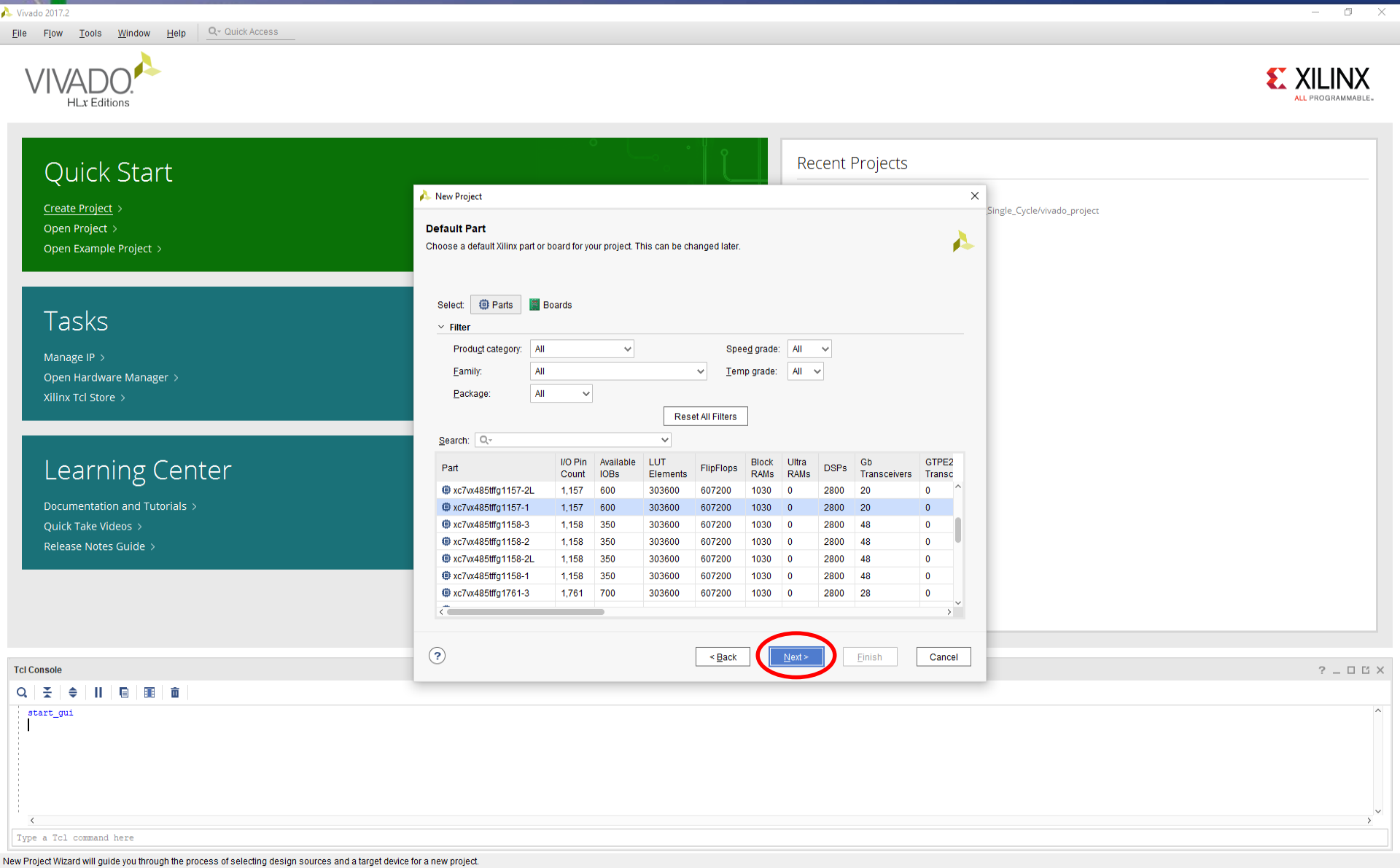

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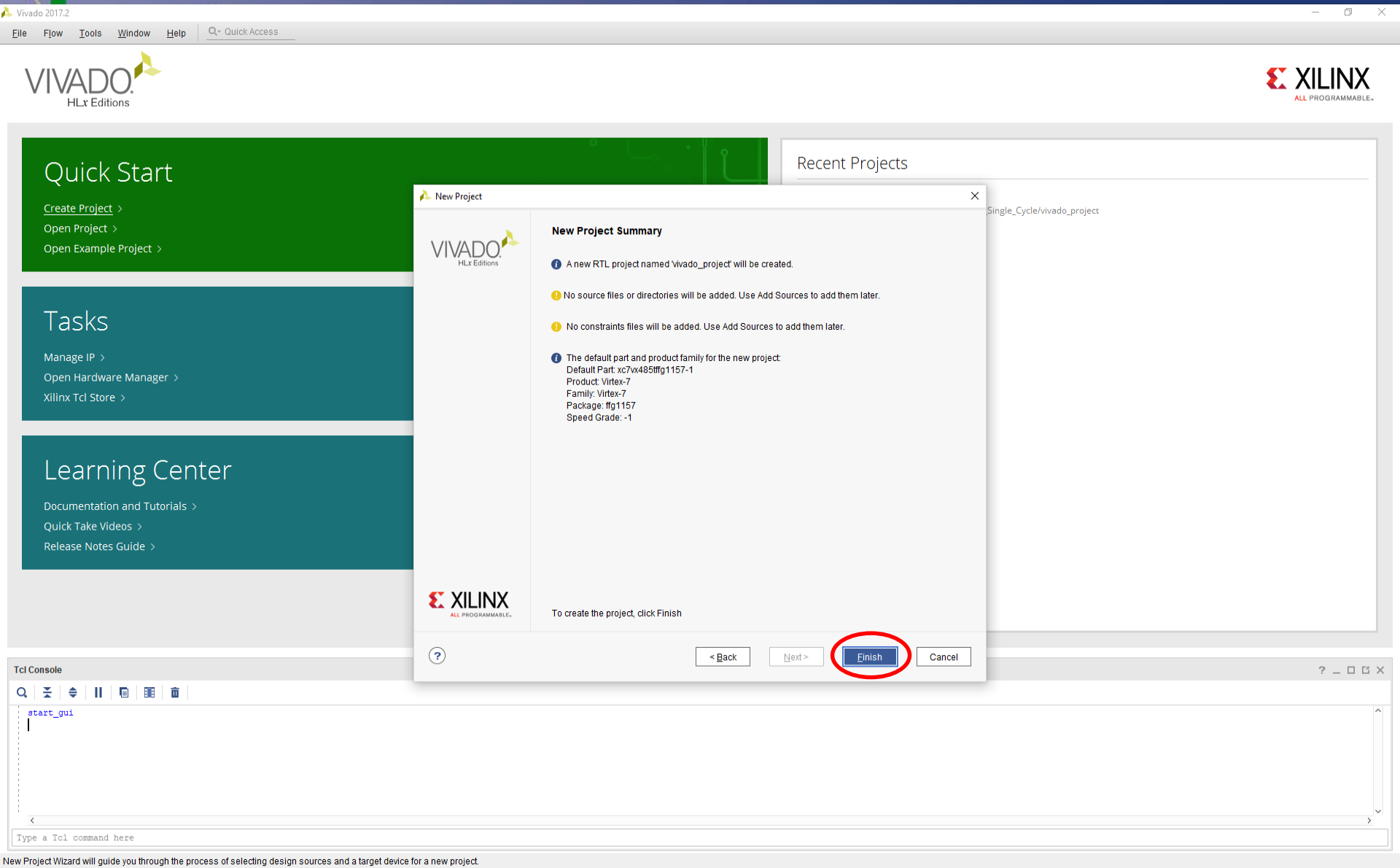
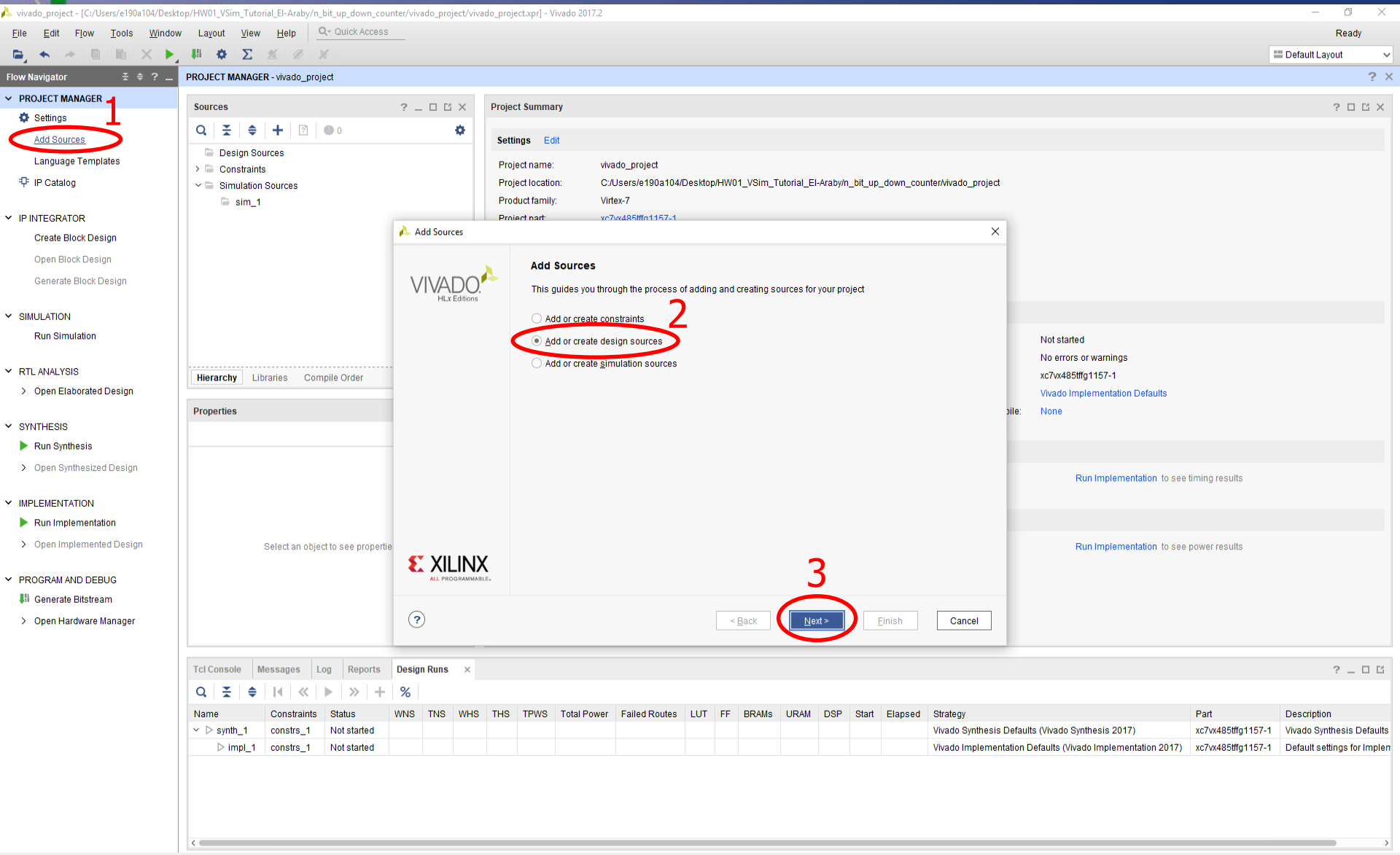


Xilinx Vivado 2019.2 – (2) Add Sources



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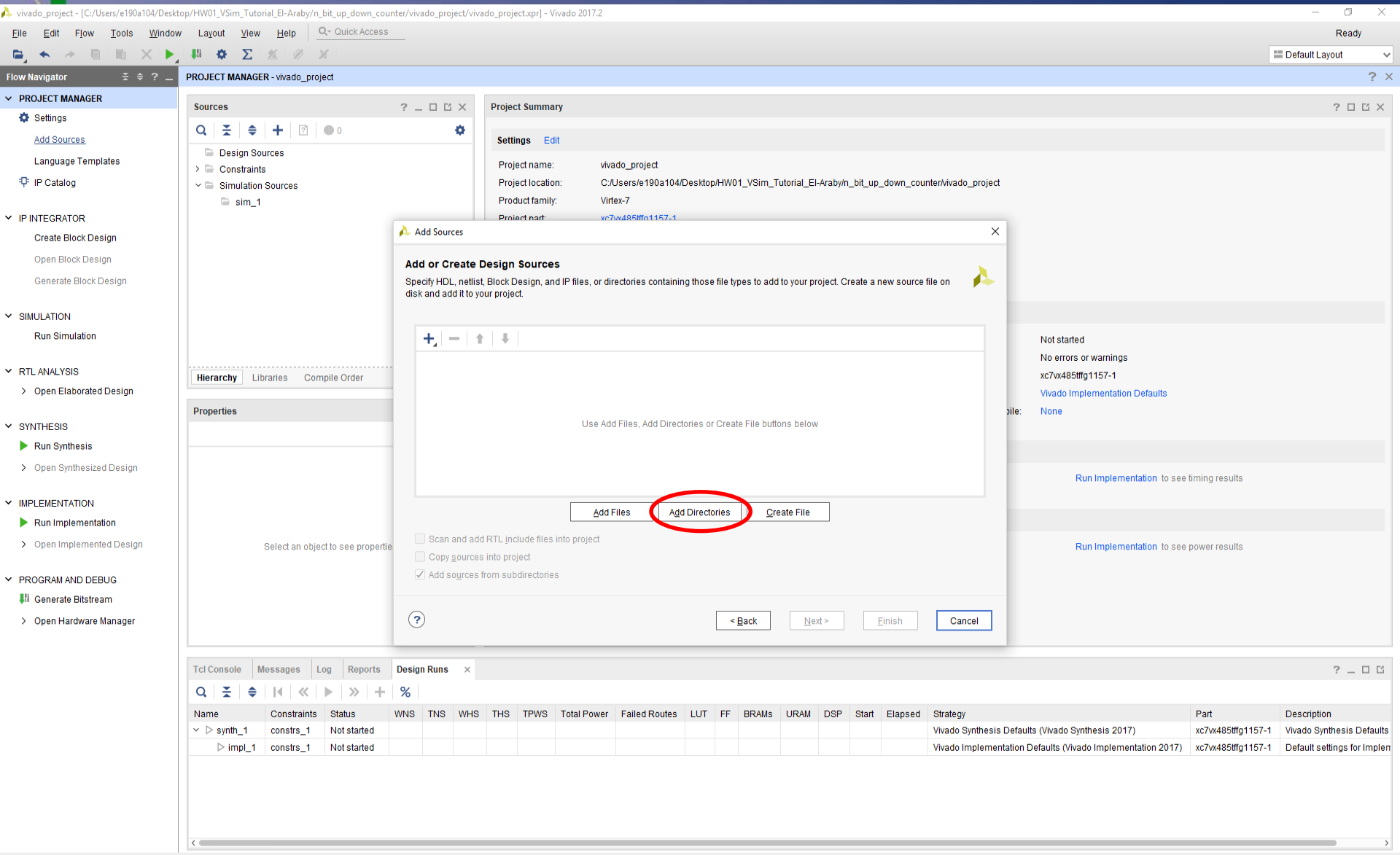

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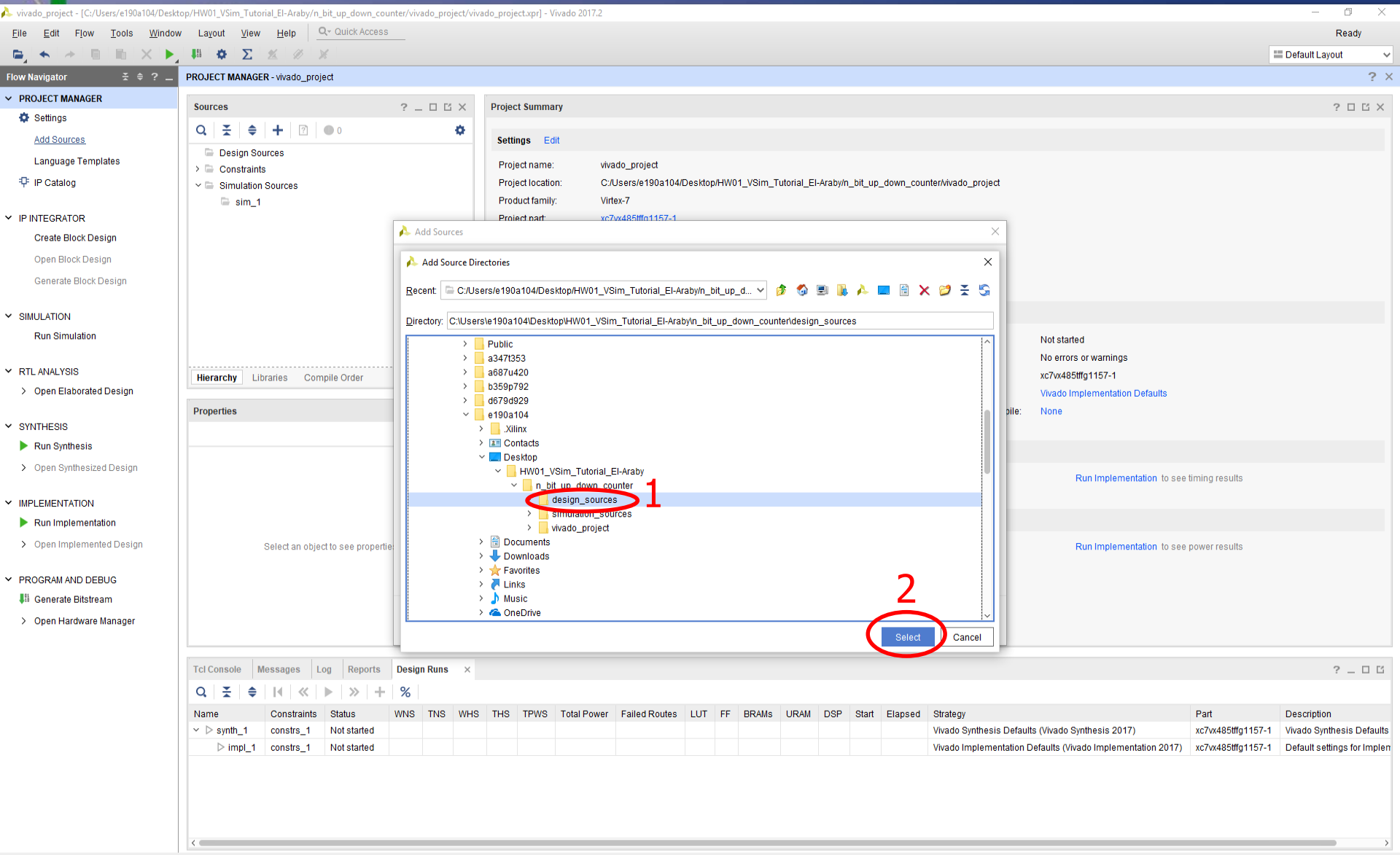

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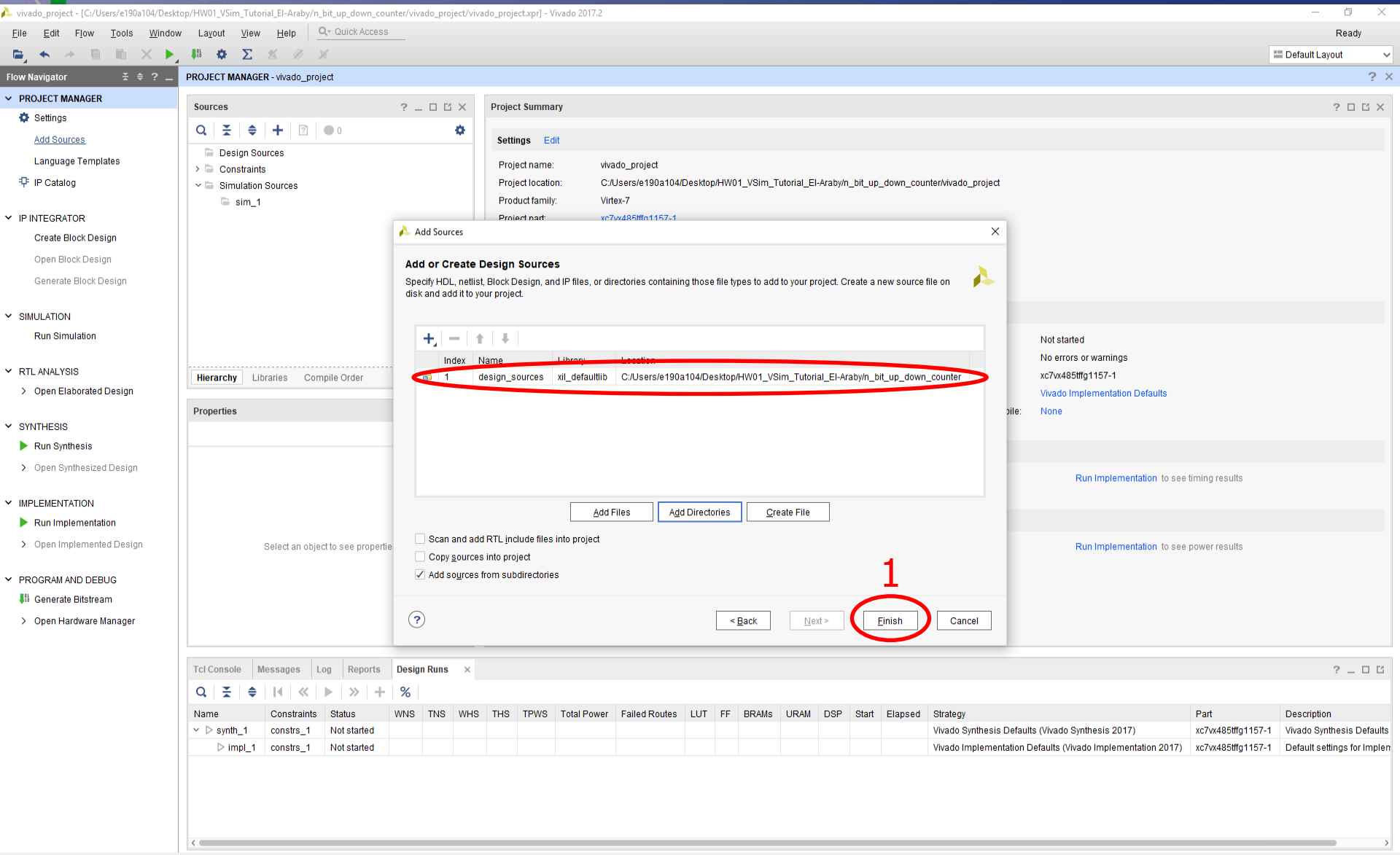
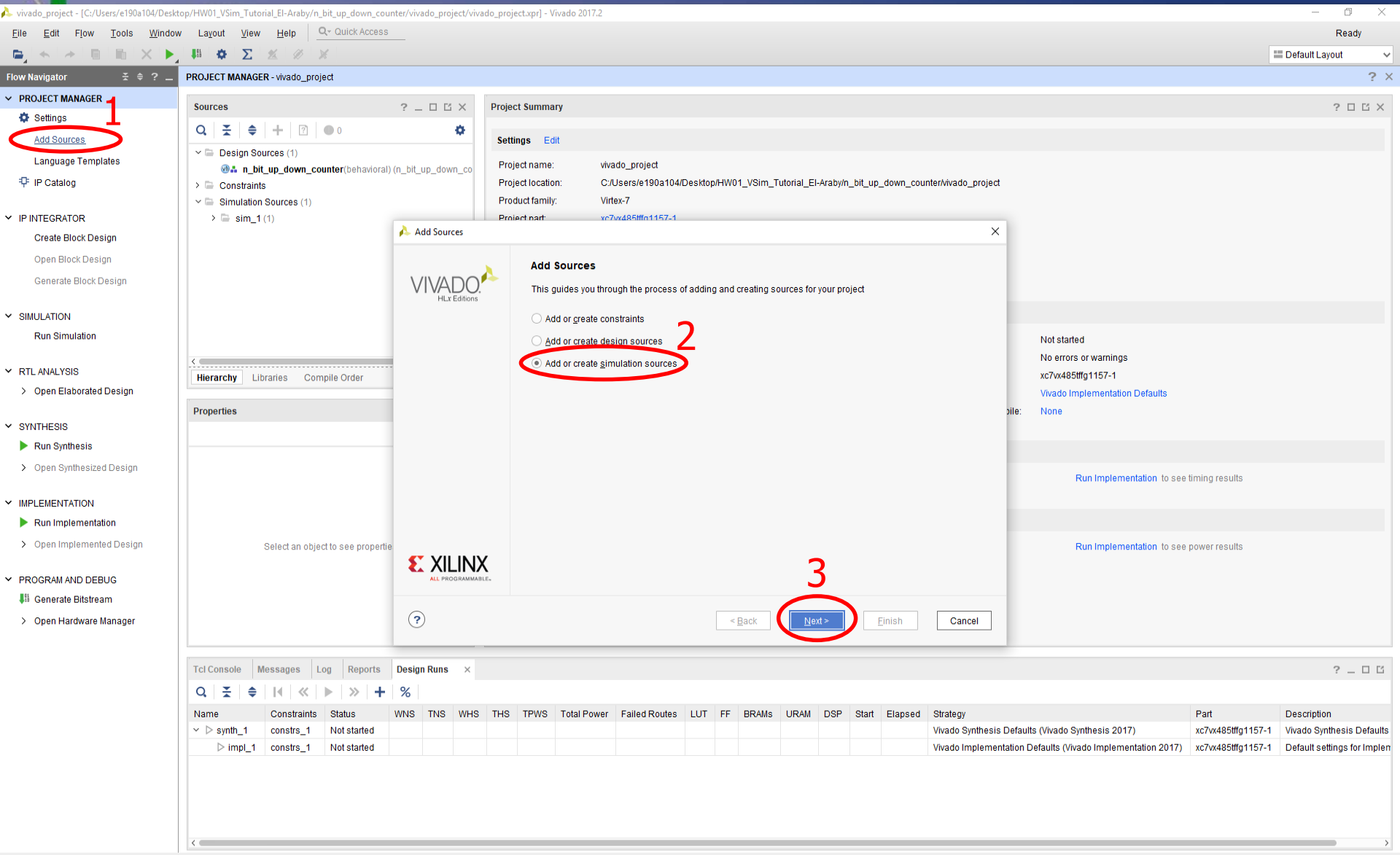


Xilinx Vivado 2019.2 – (2) Add Sources



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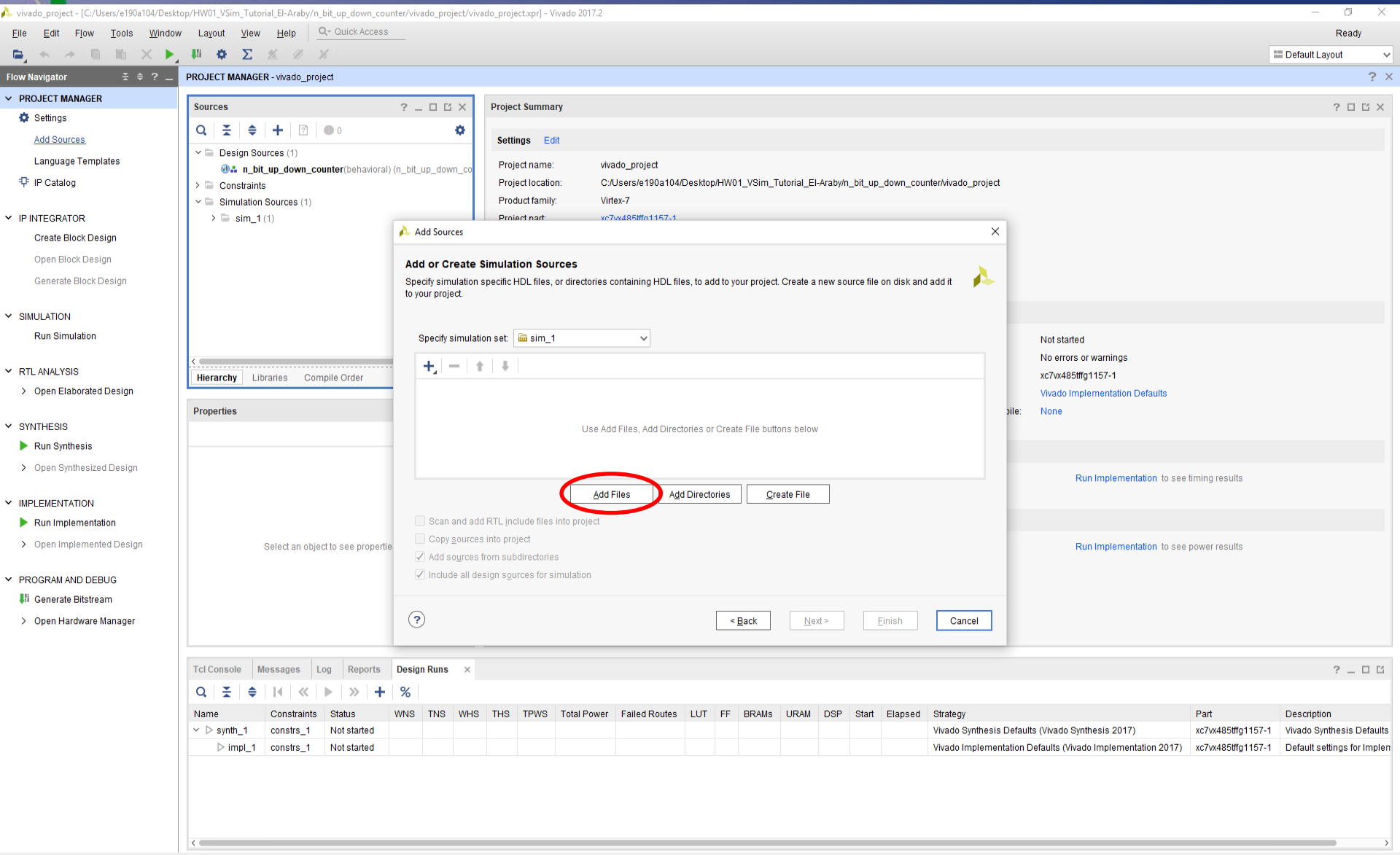

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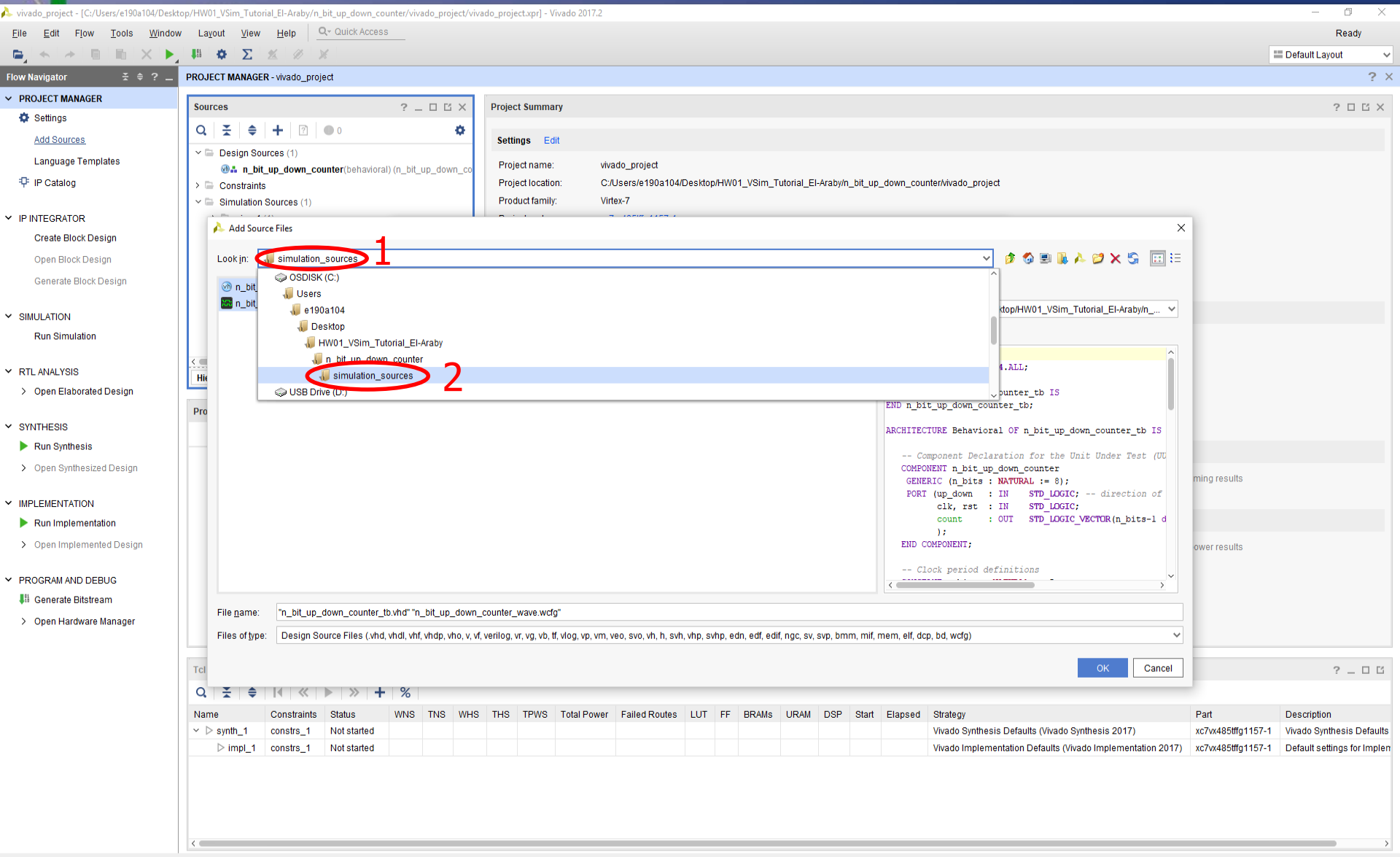

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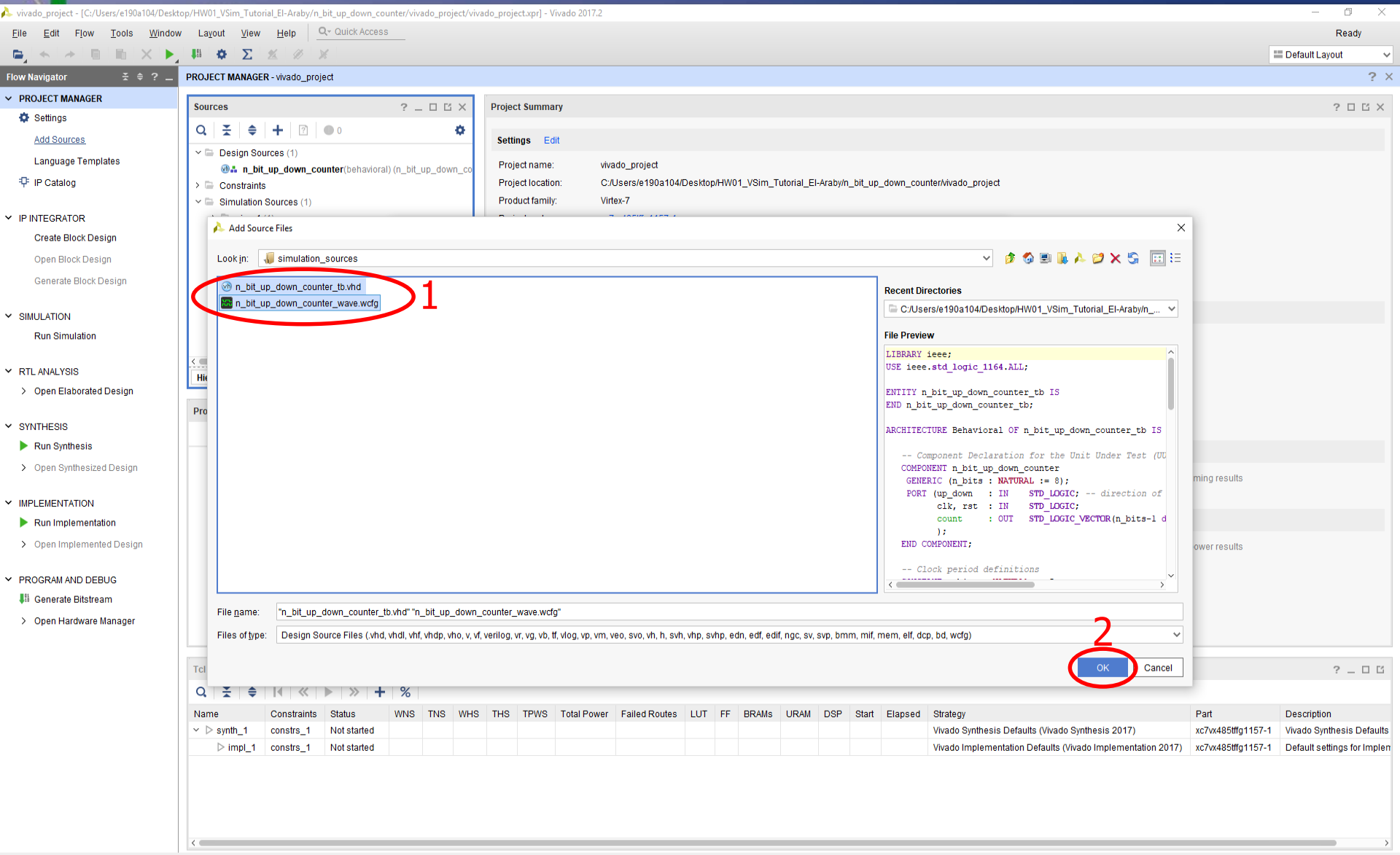

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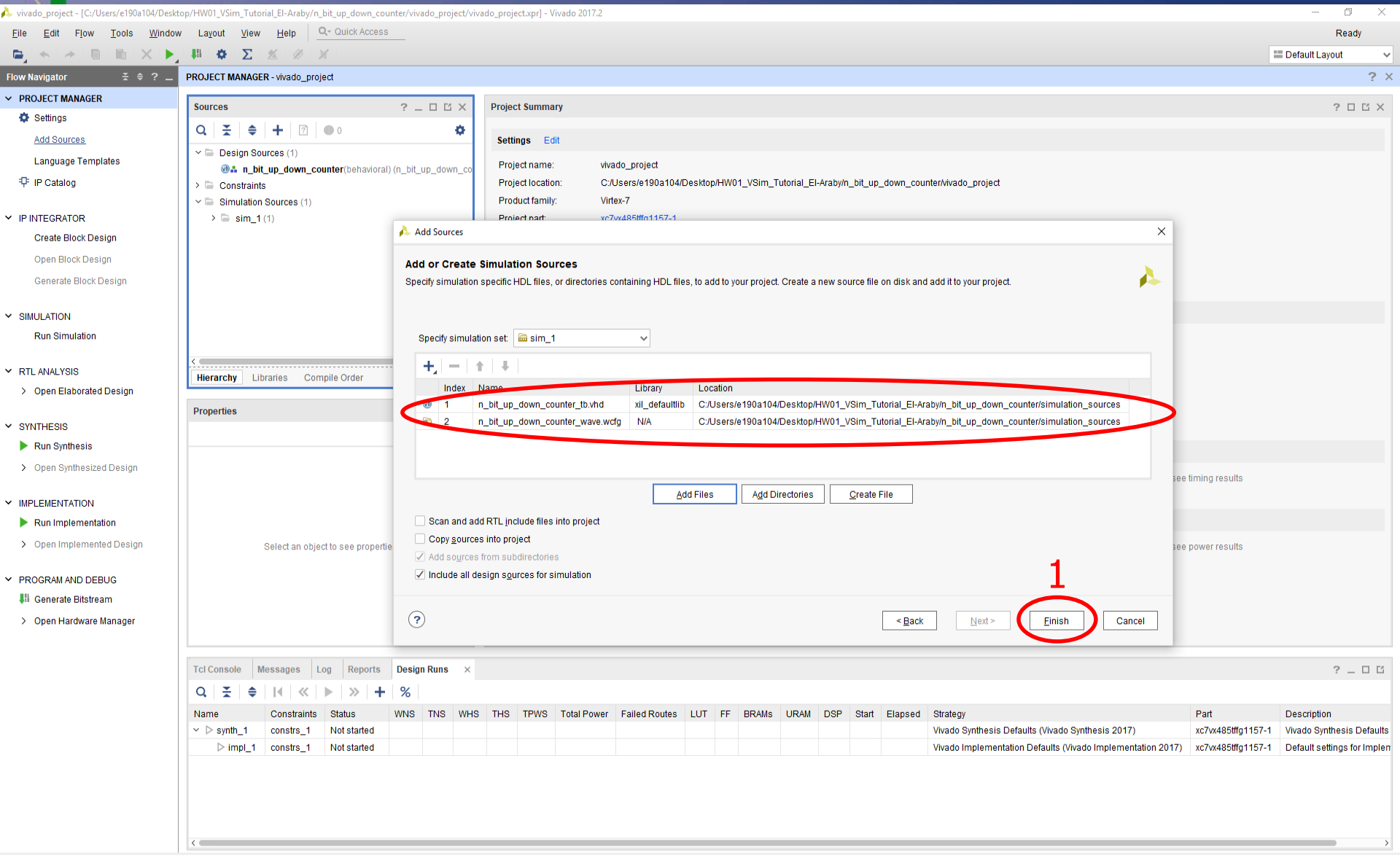

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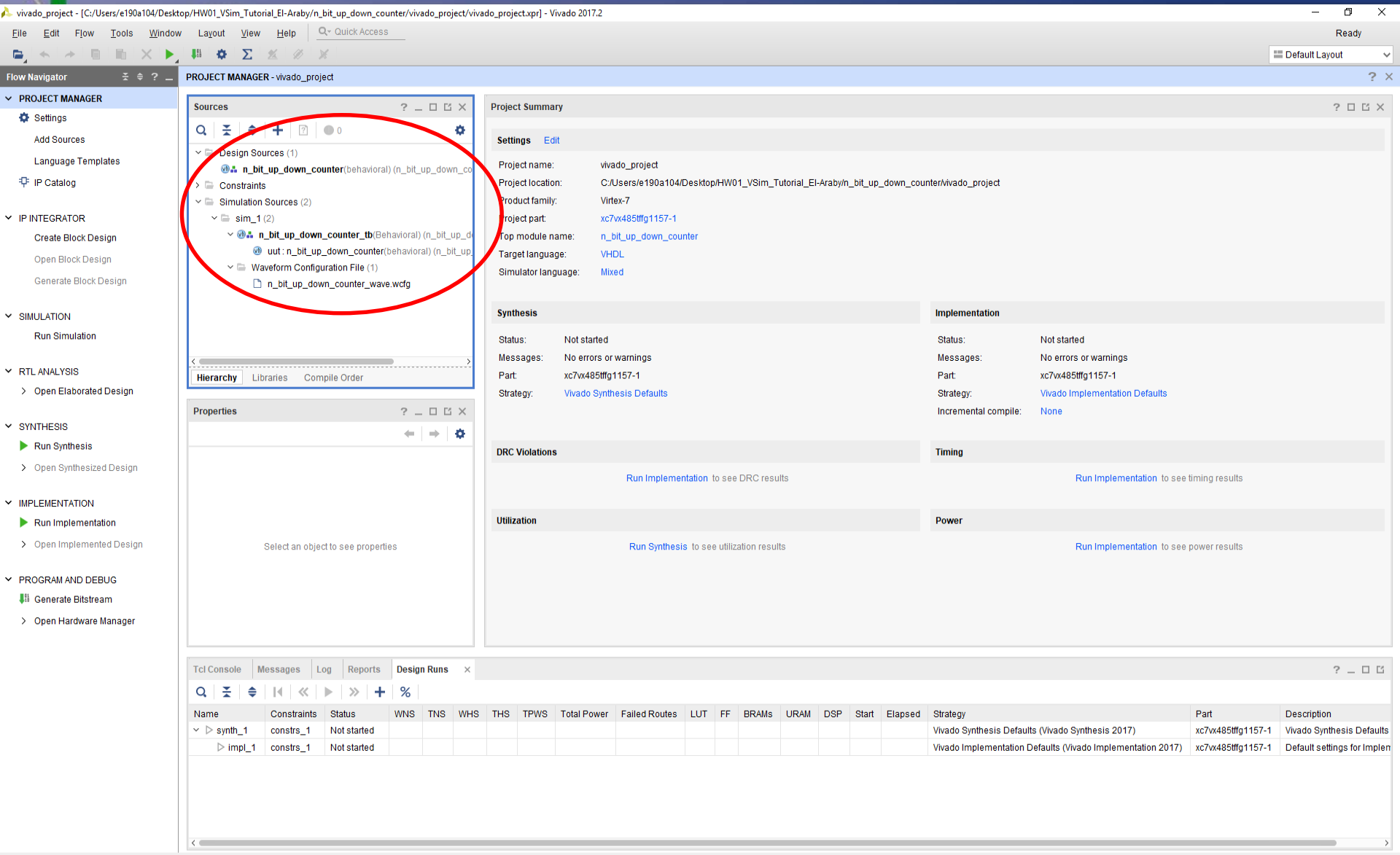

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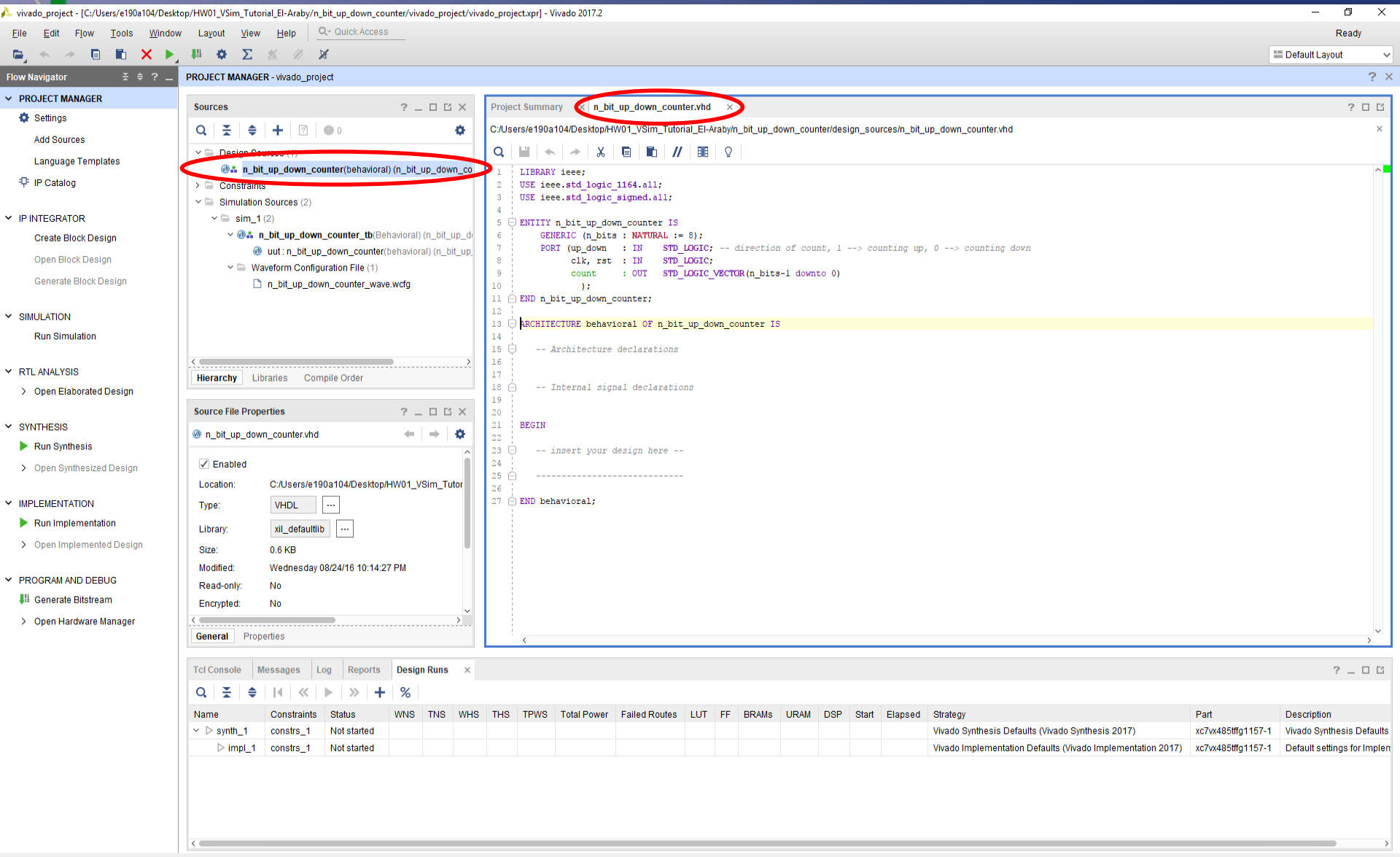

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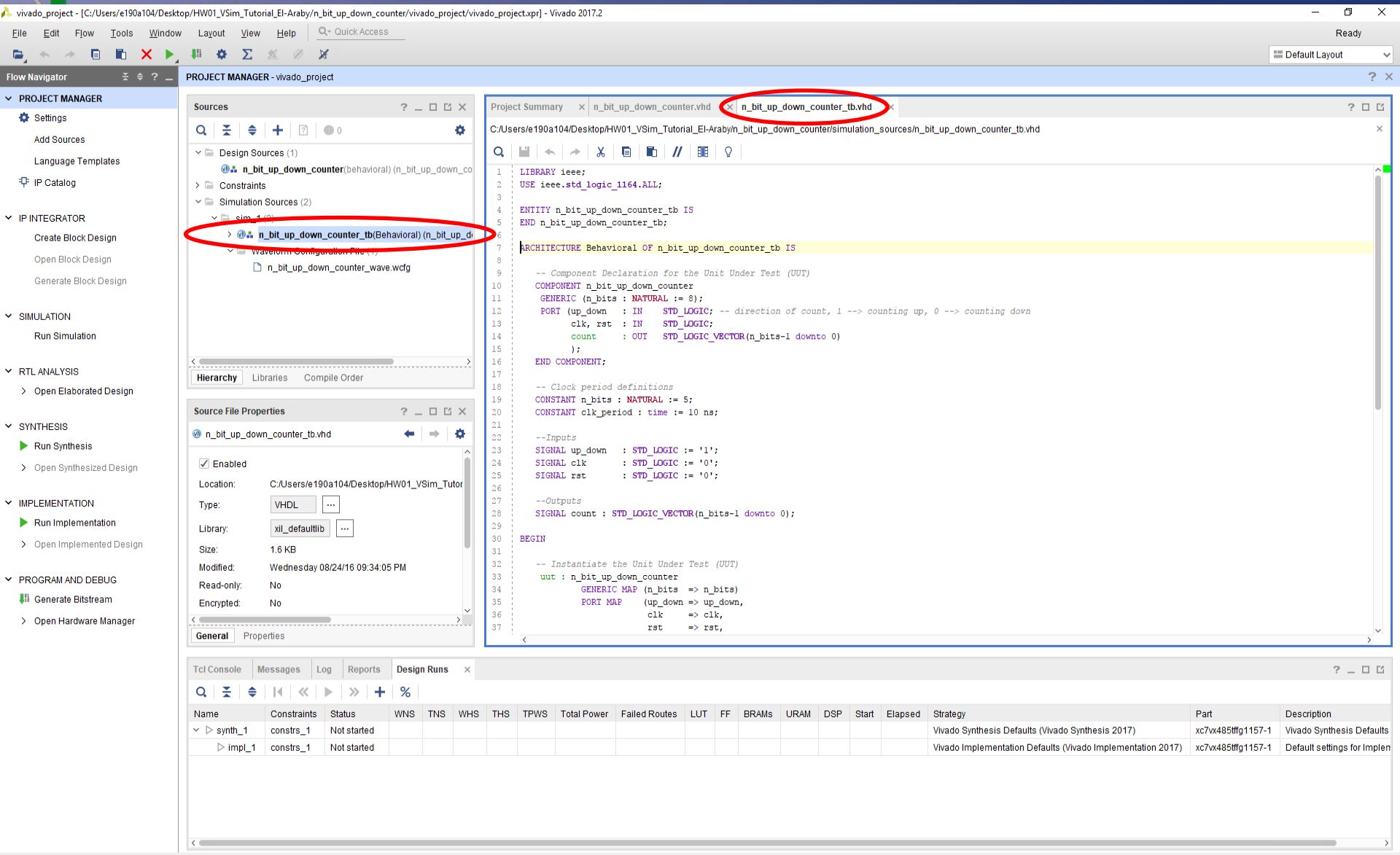
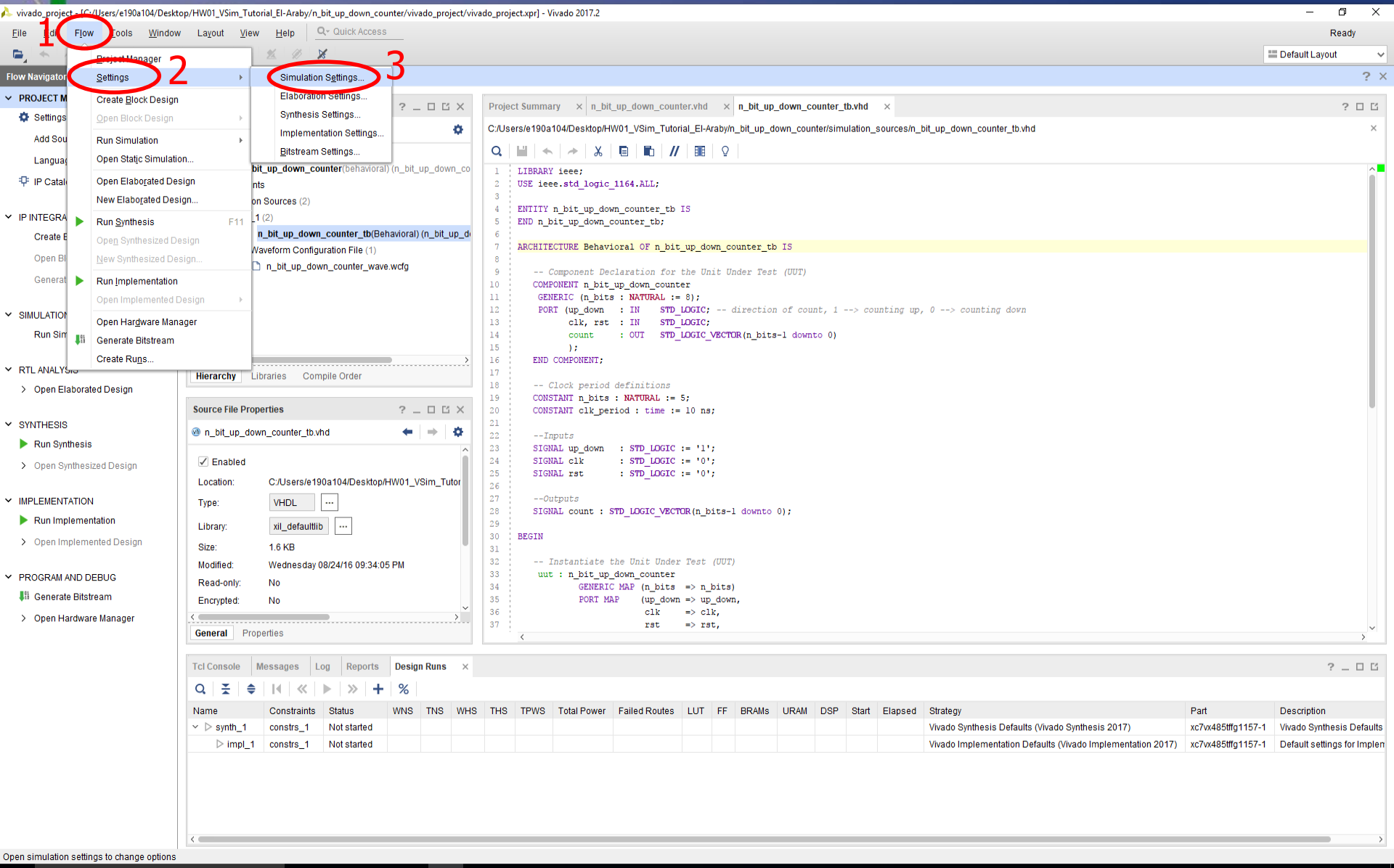
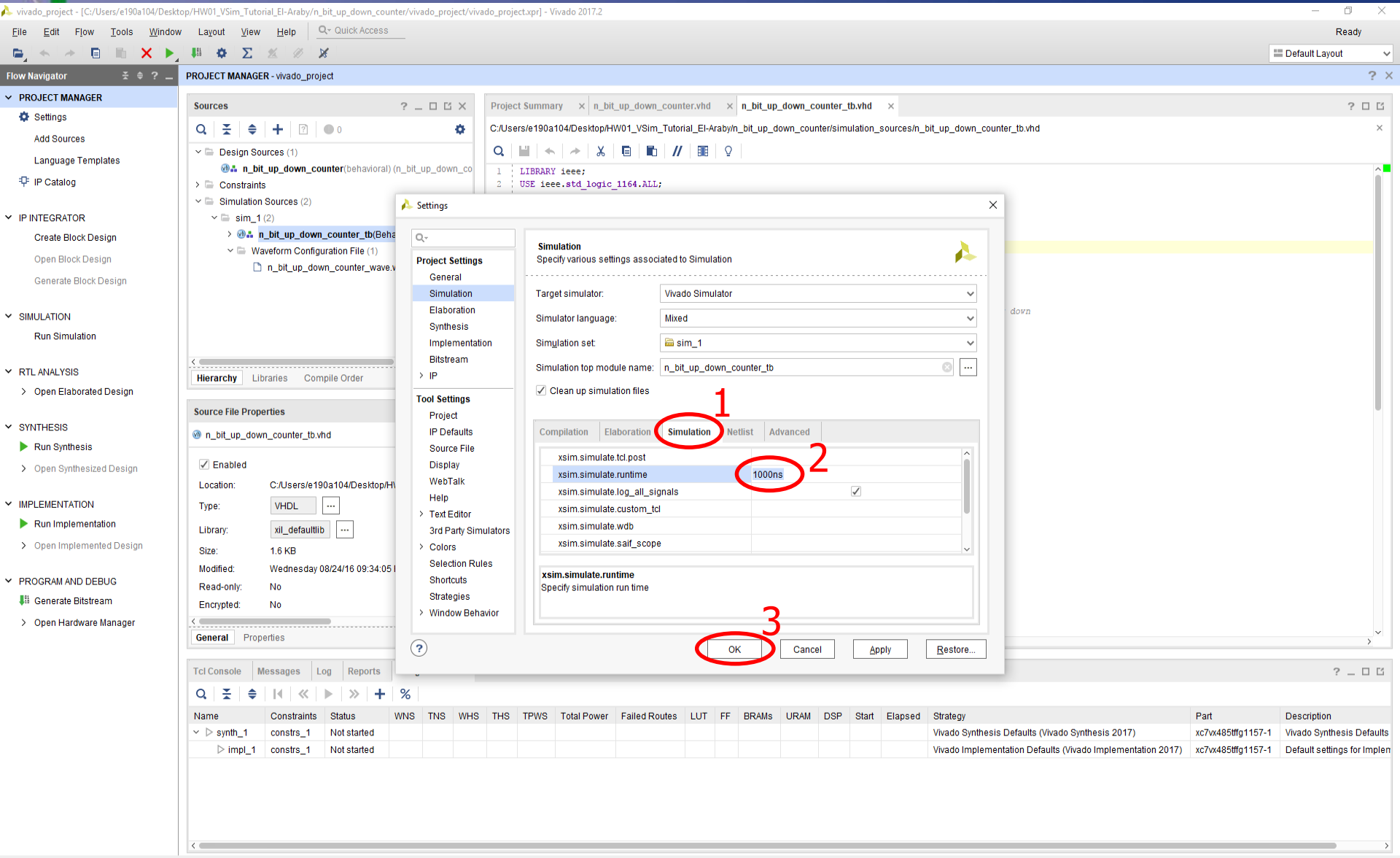


Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation



Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation



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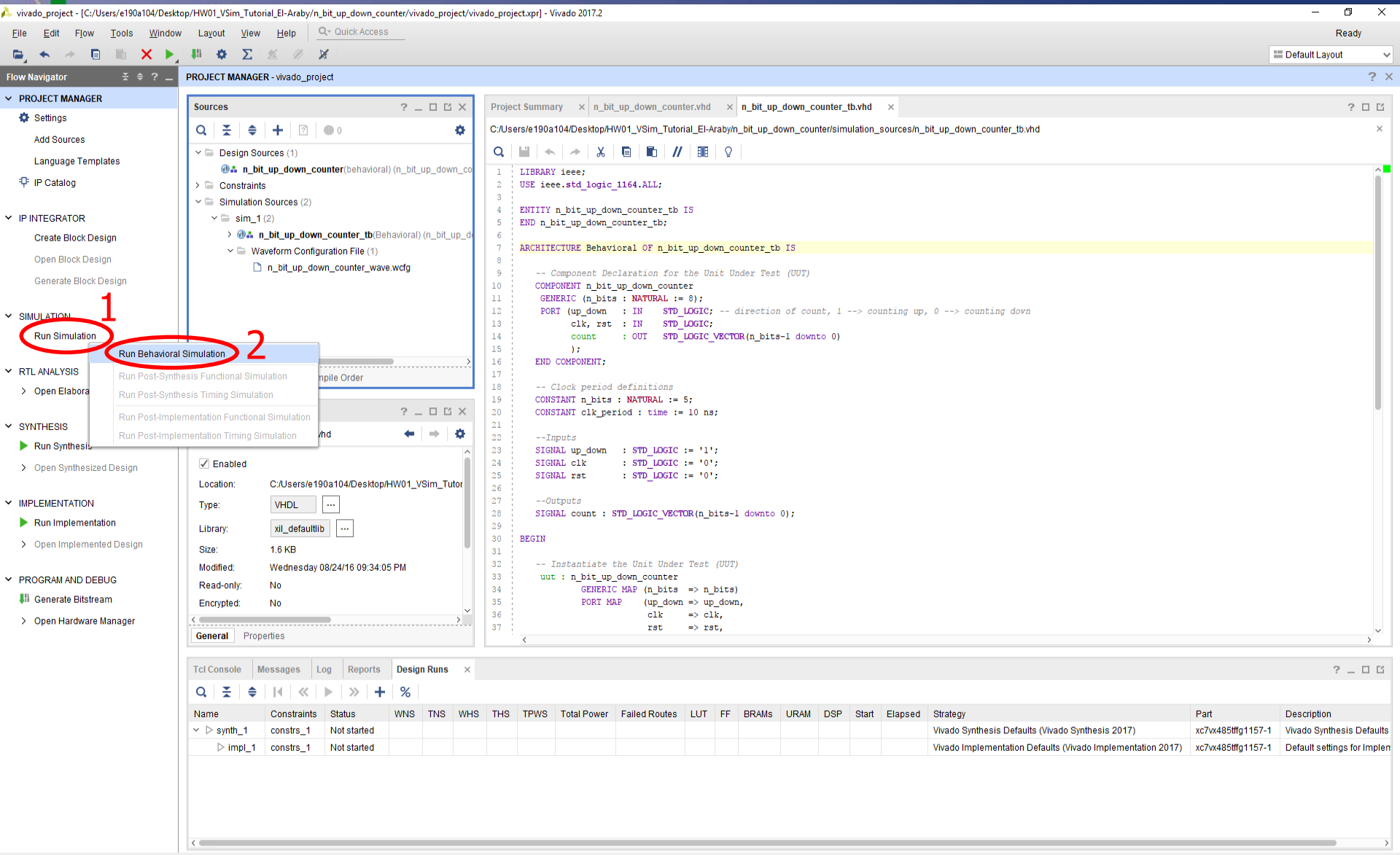

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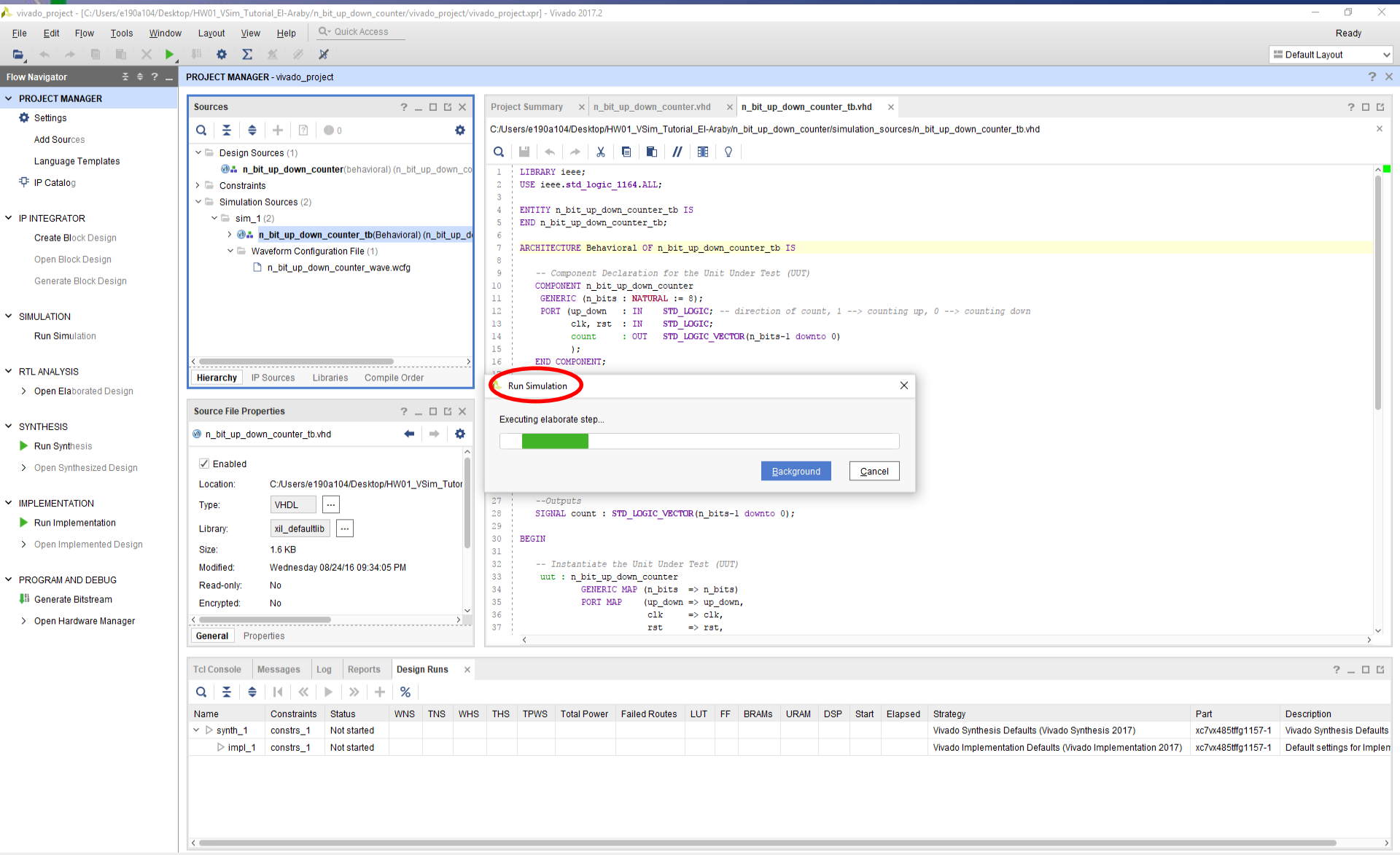
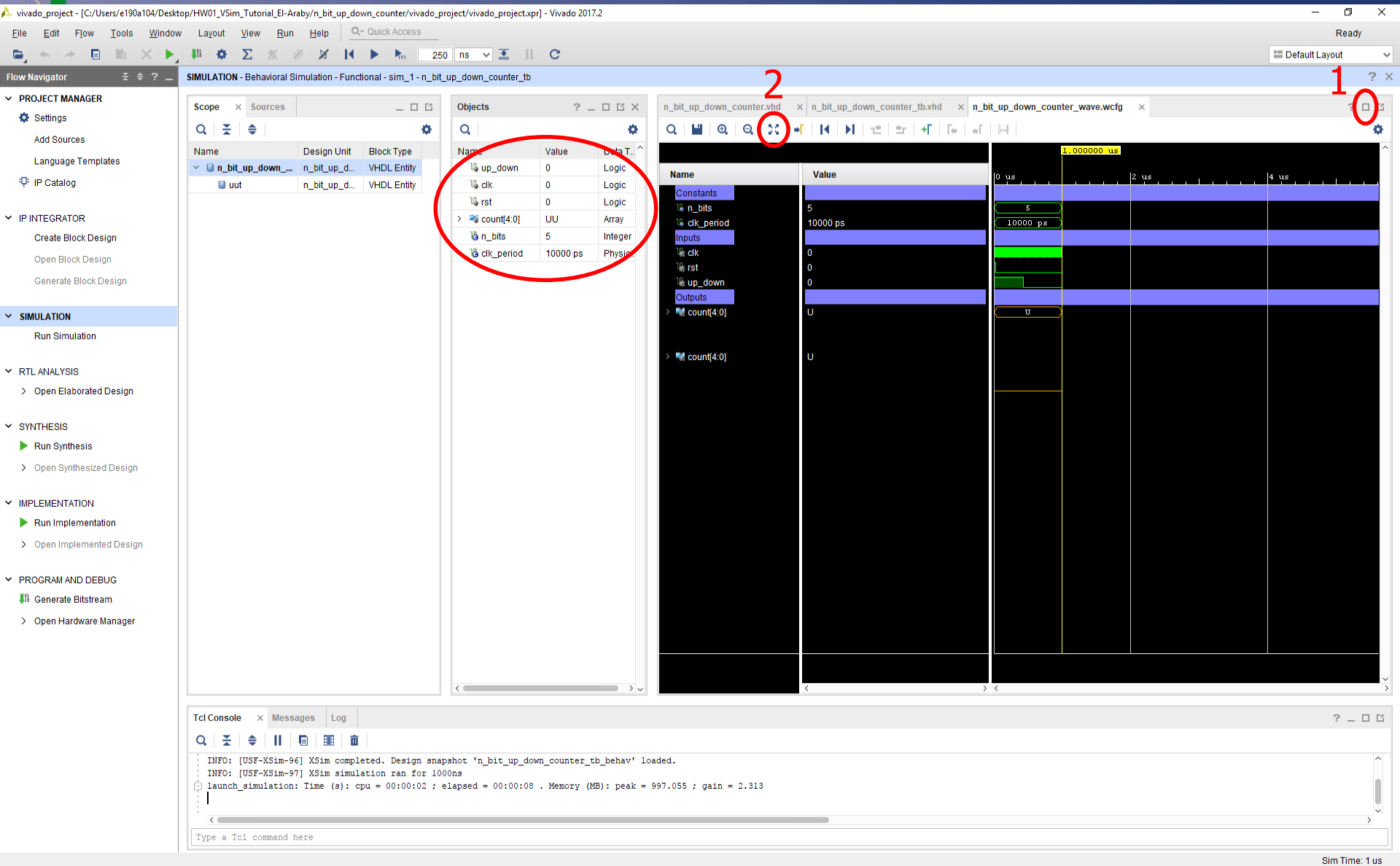


Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation



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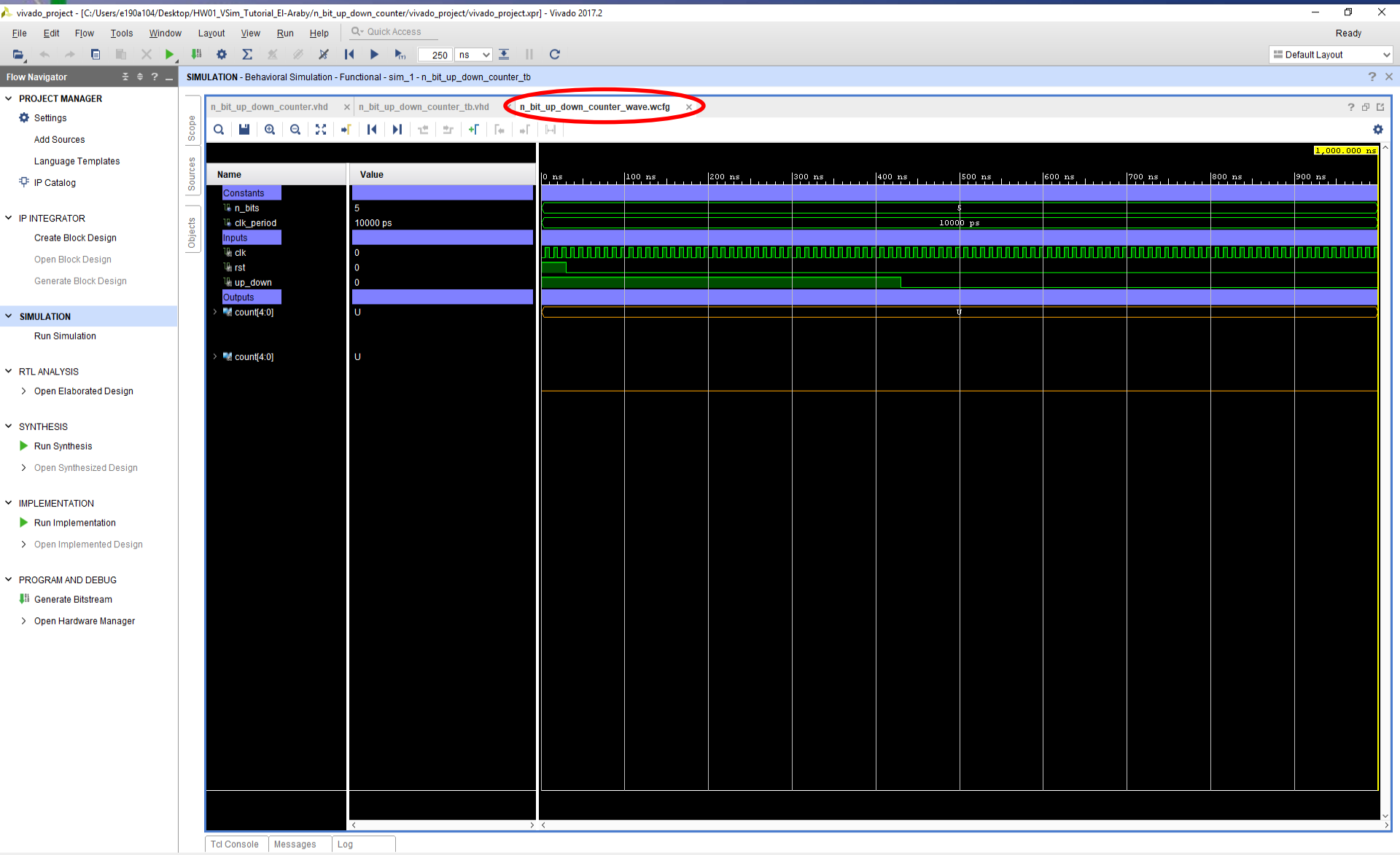
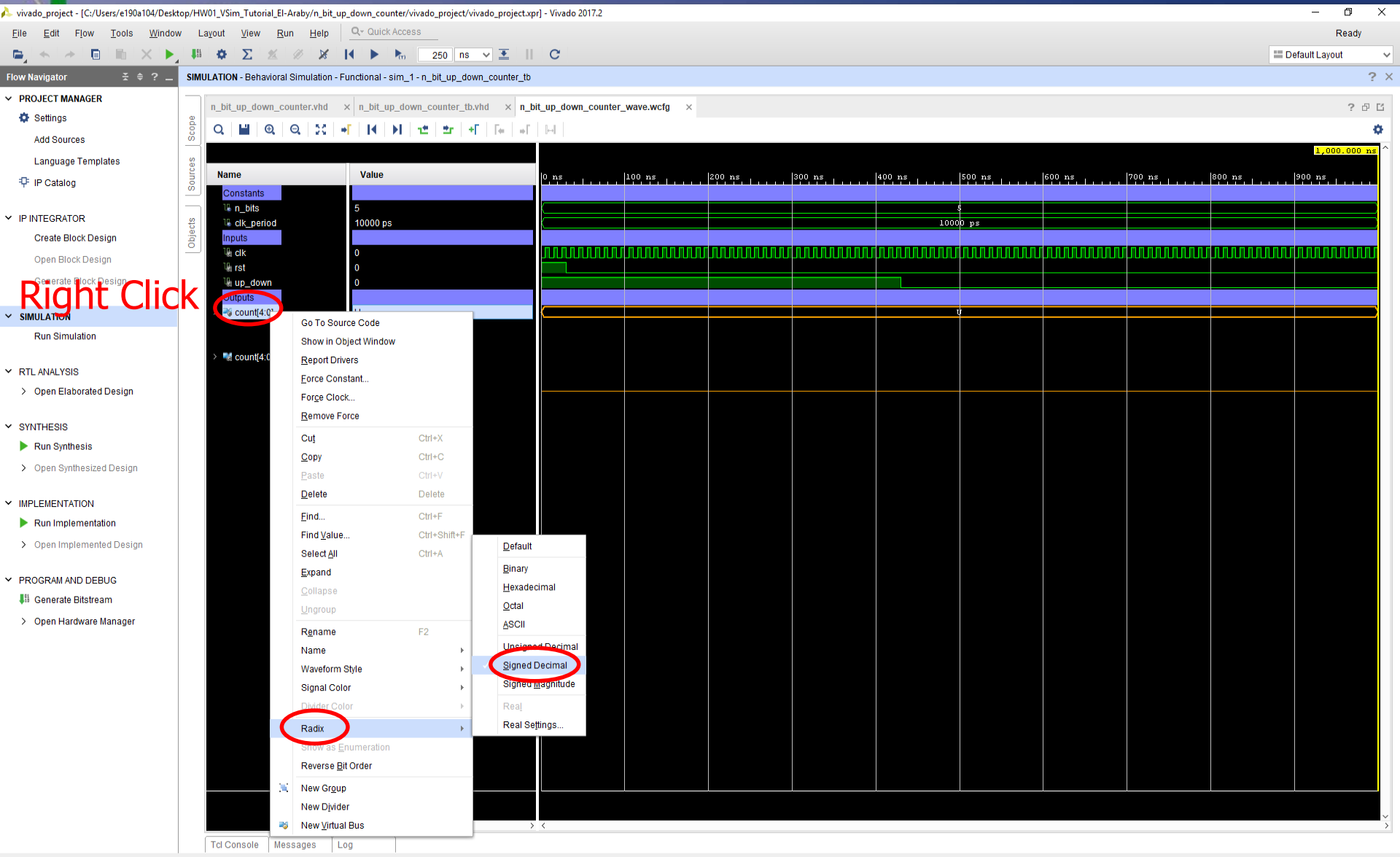
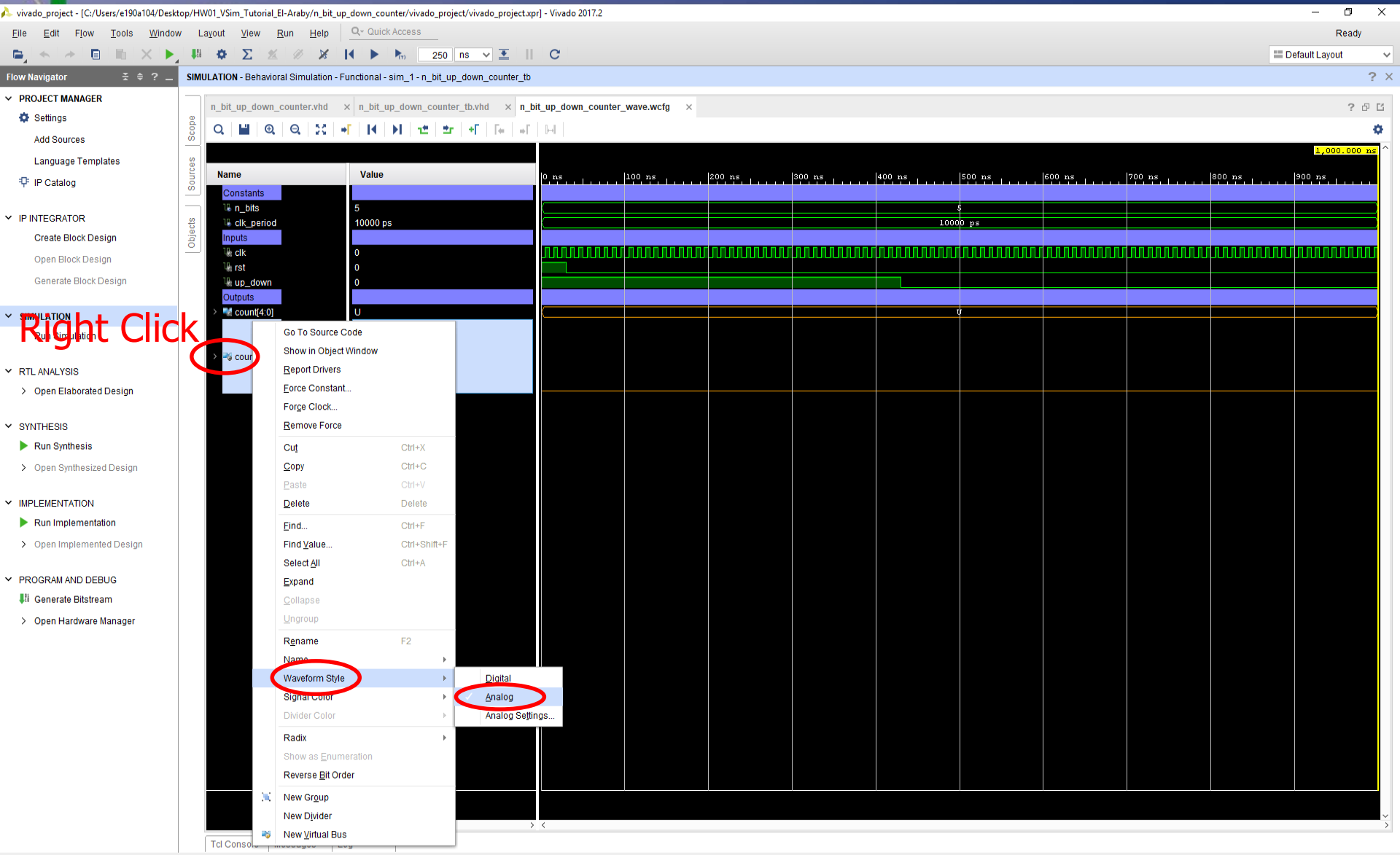


Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation



Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation



Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation