# Final Project Proposal

**Project Title**: Five stage 32-bit pipelined MIPS CPU Design using System Verilog

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**Description:**

5 stage 32-bit microprocessor which can perform load, store and Arithmetic instructions. Using a pipelined type of approach to perform individual operations from one instruction to the next and executing it one after the other.

We are designing a pipelined datapath which for 5 cycles and is different from the “Computer Organization and Design” (Davis A. Patterson and John L. Hennessy) 4 th edition diagram 4.33: The single cycle datapath. The data path created should support the instruction set. Implementing 32 bit MIPS design architecture.

**Starting point**

We are designing a module for single-cycle MIPS datapath using System Verilog and then continue on the design the ALU of the MIPS processor.

**Team contribution**

Individual contribution: Each one of us is working on one topic as given below

The topics are:

1. single cycle MIPS data path 2).set and instructions 3). data path and control

4. Complete pipelined MIPS

As a team, we are working together and assisting each other.

Source : ” Computer Organization and Design” (Davis A. Patterson and John L. Hennessy) 4 th edition diagram 4.33: The single cycle datapath.