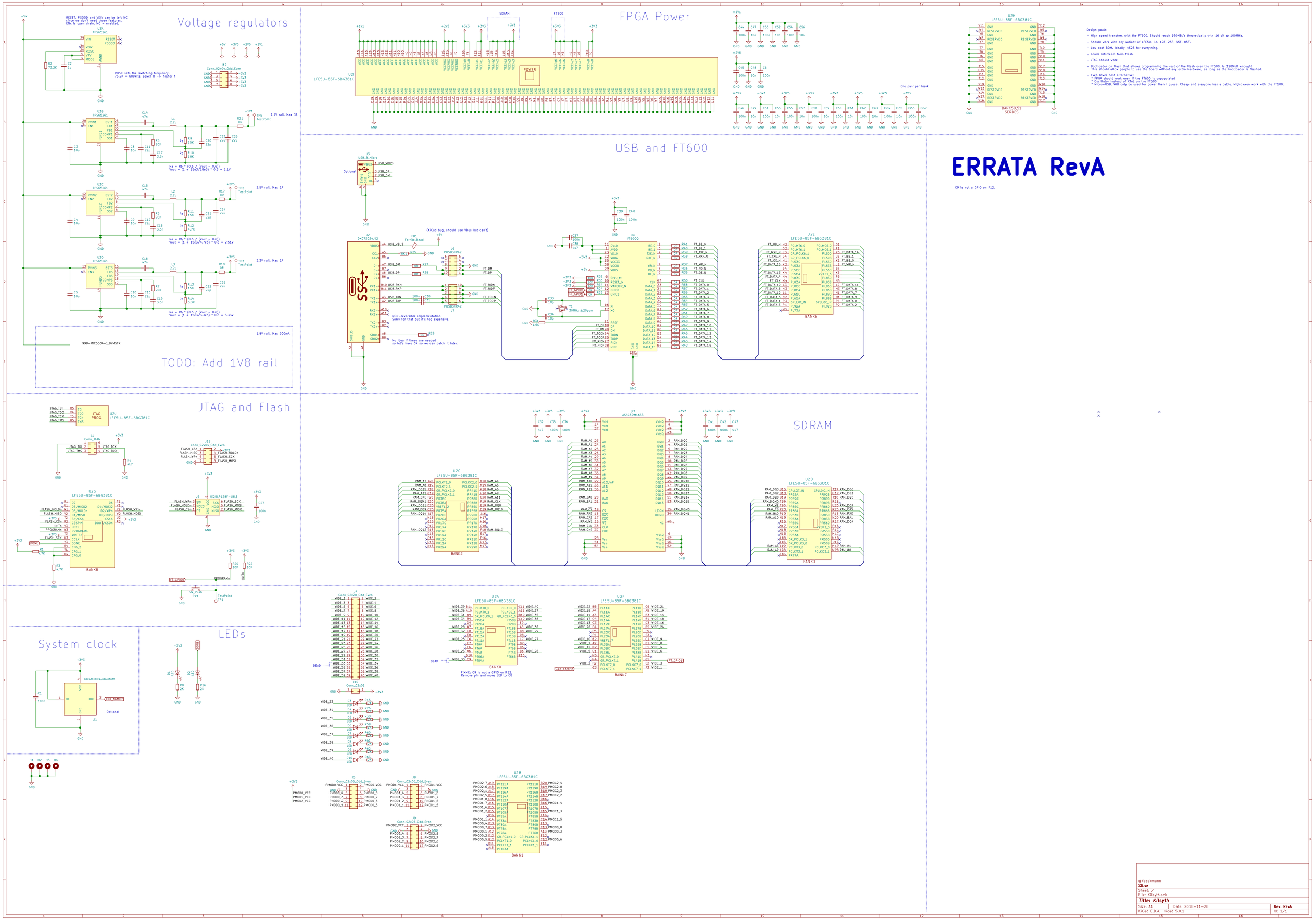
Voltage regulators
RESET, PGOOD and VDIV can be left NC since we don't need those features. ENx is open drain, NC = enabled.
ROSC sets the switching frequency. 73.2K = 600kHz. Lower R -> higher f
1.1V rail, Max 3A
Ra = Rb * (0.6 / (Vout - 0.6))
Vout = (1 + 15e3/18e3) * 0.6 = 1.1V
2.5V rail, Max 2A
Vout = (1 + 15e3/4.7e3) * 0.6 = 2.51V
3.3V rail, Max 2A
Vout = (1 + 15e3/3.3e3) * 0.6 = 3.33V
1.8V rail, Max 300mA
998-MIC5504-1.8YM5TR
TODO: Add 1V8 rail
FPGA Power
SDRAM
FT600
POWER
One pair per bank
USB and FT600
(KiCad bug, should use VBus but can't)
NON-reversible implementation. Sorry for that but it's too expensive.
No idea if these are needed so let's have OR so we can patch it later.
ERRATA RevA
C9 is not a GPIO on F12.
Design goals:
- High speed transfers with the FT600. Should reach 190MB/s theoretically with 16 bit @ 100MHz.
- Should work with any variant of LFE5U. i.e. 12F, 25F, 45F, 85F.
- Low cost BOM. Ideally <$25 for everything.
- Loads bitstream from flash
- JTAG should work
- Bootloader on flash that allows programming the rest of the flash over the FT600. Is 128Mbit enough? This should allow people to use the board without any extra hardware, as long as the bootloader is flashed.
- Even lower cost alternative:
  * FPGA should work even if the FT600 is unpopulated
  * Oscillator instead of XTAL on the FT600
  * Micro-USB. Will only be used for power then i guess. Cheap and everyone has a cable. Might even work with the FT600.
JTAG and Flash
SDRAM
System clock
LEDs
Optional
DEAD
FIXME: C9 is not a GPIO on f12. Remove pin and move LED to C8
BANK0
BANK2
BANK3
BANK6
BANK7
BANK8
BANK1
BANKS0,51 SERDES
LFE5U-85F-6BG381C
TP6500
TP6501
TP6502
TP6503
TP6504
TP6505
TP6506
TP6507
TP6508
TP6509
TP6510
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