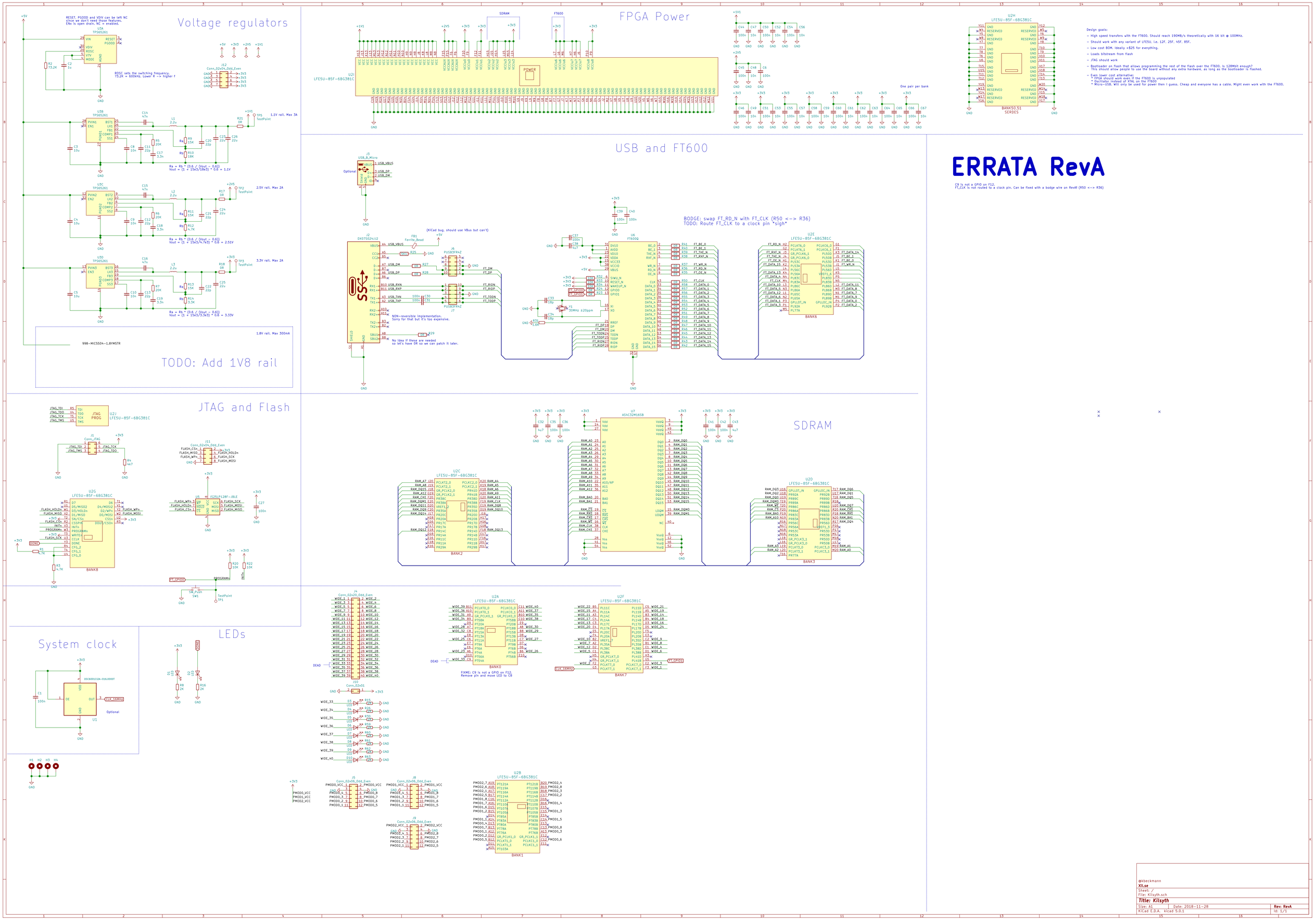
Voltage regulators
RESET, PGOOD and VDIV can be left NC since we don't need those features. ENx is open drain, NC = enabled.
ROSC sets the switching frequency. 73.2K = 600kHz. Lower R -> higher f
1.1V rail, Max 3A
Ra = Rb * (0.6 / (Vout - 0.6))
Vout = (1 + 15e3/18e3) * 0.6 = 1.1V
2.5V rail, Max 2A
Vout = (1 + 15e3/4.7e3) * 0.6 = 2.51V
3.3V rail, Max 2A
Vout = (1 + 15e3/3.3e3) * 0.6 = 3.33V
1.8V rail, Max 300mA
998-MIC5504-1.8YM5TR
TODO: Add 1V8 rail
FPGA Power
SDRAM
FT600
One pair per bank
BANK50,51 SERDES
Design goals:
- High speed transfers with the FT600. Should reach 190MB/s theoretically with 16 bit @ 100MHz.
- Should work with any variant of LFE5U. i.e. 12F, 25F, 45F, 85F.
- Low cost BOM. Ideally <$25 for everything.
- Loads bitstream from flash
- JTAG should work
- Bootloader on flash that allows programming the rest of the flash over the FT600. Is 128Mbit enough? This should allow people to use the board without any extra hardware, as long as the bootloader is flashed.
- Even lower cost alternative:
  * FPGA should work even if the FT600 is unpopulated
  * Oscillator instead of XTAL on the FT600
  * Micro-USB. Will only be used for power then i guess. Cheap and everyone has a cable. Might even work with the FT600.
USB and FT600
(KICad bug, should use VBus but can't)
NON-reversible implementation. Sorry for that but it's too expensive.
No idea if these are needed so let's have OR so we can patch it later.
BODGE: swap FT_RD_N with FT_CLK (R50 <-> R36)
TODO: Route FT_CLK to a clock pin *sigh*
ERRATA RevA
C9 is not a GPIO on F12.
FT_CLK is not routed to a clock pin. Can be fixed with a bodge wire on RevA (R50 <-> R36)
JTAG and Flash
System clock
LEDs
SDRAM
FIXME: C9 is not a GPIO on f12. Remove pin and move LED to C8
Optional
BANK0
BANK1
BANK2
BANK3
BANK6
BANK7
BANK8
okbeckmann
XILse
Sheet: /
File: Kilsyth.sch
Title: Kilsyth
Size: A1
Date: 2018-11-28
Rev: RevA
KiCad E.D.A. kicad 5.0.1
Id: 1/1