

Laplace Transform

Laboratory III

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1 Goal of the exercise

2 Laplace Transform

3 Course of measurements

First we tested two circuits: low-pass and high-pass configuration of RC circuit and RLC circuits. After connecting oscilloscope to the wave generator and prototype board, we generated square wave with $V_{p2p} = 1V$, offset = .5V, frequency of 100Hz and duty cycle of 50%. Then we read from the oscilloscope Voltage value at times $1t$, $5t$ and $10t$ (where $10t$ is just as failsafe) and time when voltage reaches 10% and 90% of the highest value.

For RLC circuits we tested ho different resistances before RC circuit influence output charactristic. We measured response for 2 cases: Generator out resistance (50 Ohm) + resistance selected by jumper wire. In our case we tested jumper on 1.1k Ohm resistance path and 3.3k Ohm. After that we checked response of the circuit: if response was sinusoid with decreasing amplitude - resustance was smaller then RC if response was exp. decay if R was higher if response was aperiodic critical waveform if resistance was equal RC

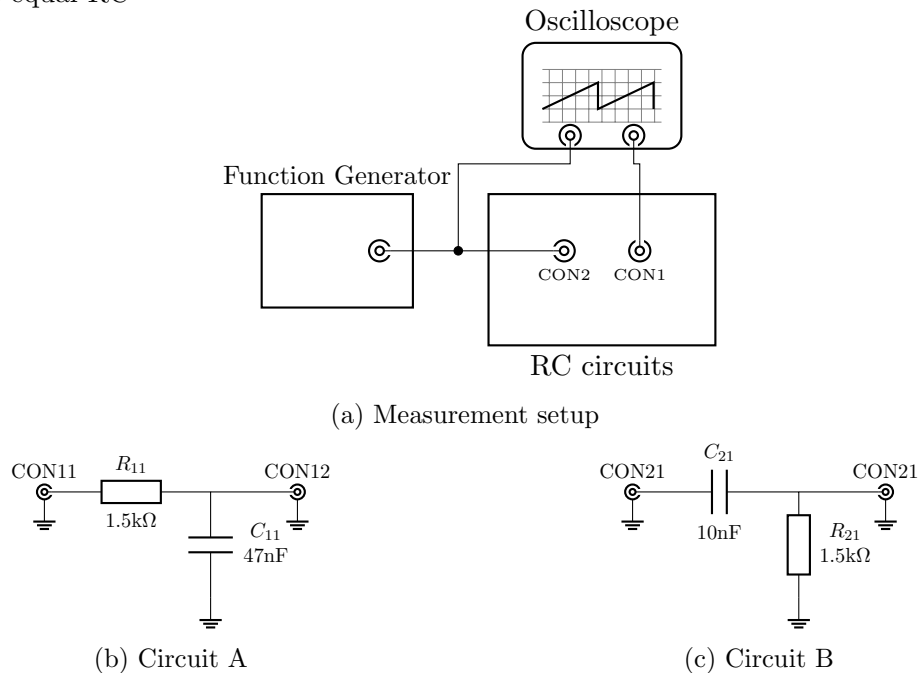


Figure 1: RC Circuits

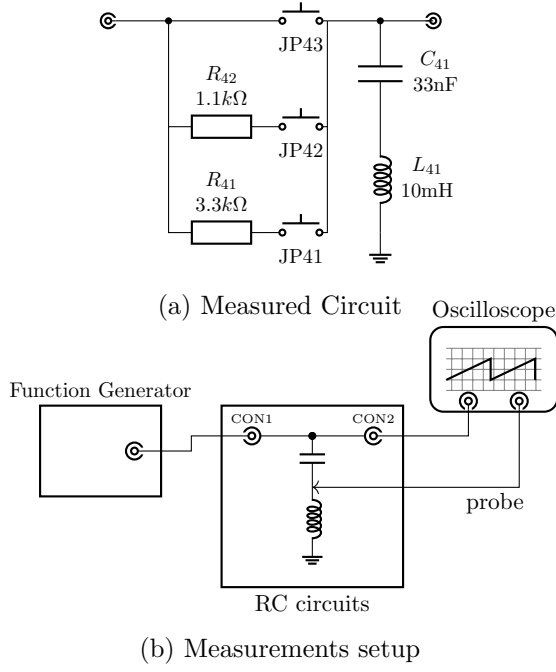


Figure 2: RLC circuit

4 Theoretical calculations

For all calculations we used Matlab with Symbolic Math Toolbox. Source code can be found in Appendix. A

In all three circuit input voltage was square wave with 50% duty cycle which can be described in time domain by

$$v_{in}(t) = V_{offset}\mathbf{1}(t) + V_{pp}\mathbf{1}(t - \frac{T}{2}) - V_{pp}\mathbf{1}(t - T) \quad (1)$$

and after Laplace transform into frequency domain

$$V_{in}(s) = \mathcal{L}[v_{in}(t)] = \frac{V_{offset}}{s} + \frac{e^{-\frac{T}{2}s}}{s} - \frac{e^{-Ts}}{s} \quad (2)$$

4.1 Circuit A

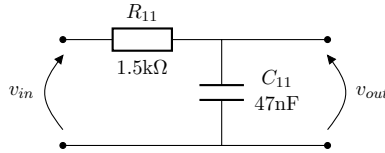


Figure 3: Circuit A schematics

v_{out} of circuit A can be described using simple voltage divider

$$v_{out}(s) = v_{in}(s) \frac{\frac{1}{sC_{11}}}{R_{11} + \frac{1}{sC_{11}}} \quad (3)$$

after applying inverse Laplace transform to $V_{out}(s)$ we obtain below plot.

Figure 4: Circuit A output voltage

4.2 Circuit B

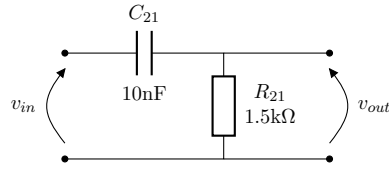
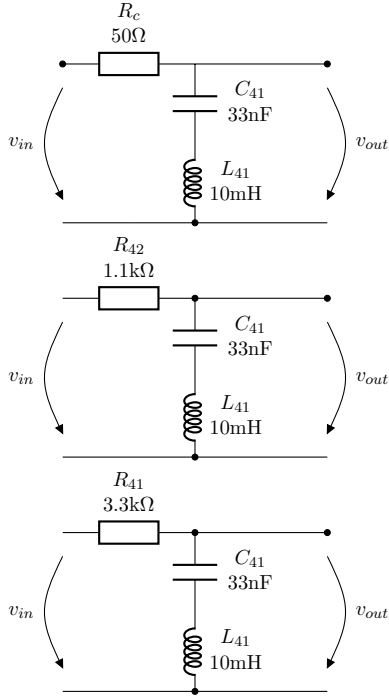


Figure 5: Circuit B schematics

4.3 Circuit C



5 Comparison

6 Conclusions

A Appendix