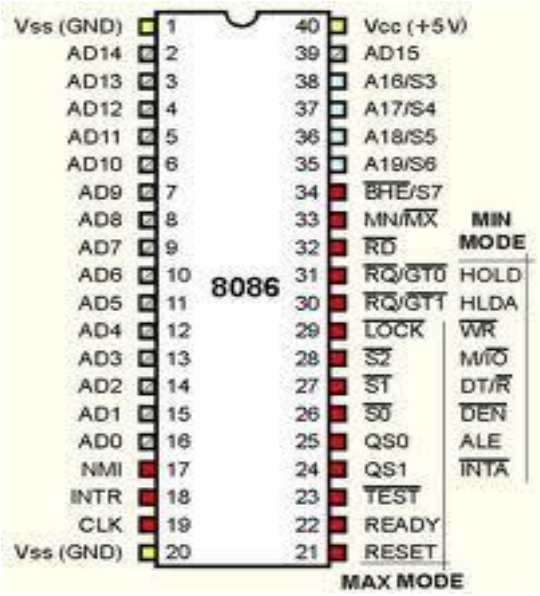
UNIT-II

Hardware Features of 8086

Pin Diagram of 8086: -



Pin Description of 8086: - The 8086 Microprocessor has 40 pins. By usingthese pins 8086 communicate with external devices. These 40 pins are also called as 40 signals of 8086. The 40 signals are divided as follows:

1. Common Signals
2. Minimum Mode Signals
3. Maximum Mode Signals

In above classification 32-pins are common pins these pins perform same operation in both Minimum Mode as well as in Maximum Mode operations of 8086. But remaining 8-pins perform different functions in Minimum Mode and in Maximum Mode.

1. Common Signals(32): -

The functionality of these pins can't change in any Mode of operation of 8086.

Address/Data signals (AD15-AD0): - [AD_0-AD_{15}]=[A_0-A_{15}]+[D_0-D_{15}]

These 16 signals are the Multiplexed Address &Data lines. These lines are bidirectional in nature. These are used to transmit Address &Data.The multiplexed Address & Data lines **AD15-AD0** act as Address Bus**(A15-A0)** in the 1st clock cycle (T_1)of any machine cycle and for the remaining clock cycles in the machine cycle the multiplexed address and data bus act as Data Bus **(D15-D0).**

Address/Status Signals (A_{16}/S_3-A_{19}/S_6): -[A_{16}/S_3-A_{19}/S_6] = [A_{16}-A_{19}]+[S_3-S_6]: -

The multiplexed address and status lines act as Address Bus (A19-A16) in the 1st clock cycle of any machine cycle;for the remaining clock cycles in the machine cycle,the multiplexed address and status lines act as status lines.If the processor is communicating with the memory locations in the 20-bit address,Higher-order 4-bits are sent to the memory by using A19 – A16 (4 address lines).If the processor is communicating with I/O device,then just 0's are passed to the I/O-device on the Higher order 4 address lines A19 – A16, because each and every device can be identified by a 16- bit address in 8086 processor. The functionality of Status Signals (S6-S3) in the Machine Cycle other than 1st Clock Cycle as follows.

S6: - This status line can't give any information so the logic level on S6=0

S5: - This status line gives the status information of Interrupt Flag (IF)

If IF=0,then logic level on S5 = 0; If IF=1, then logic level on S5 =1.

S4-S3: - The status lines S4 and S3 give the status information of the segment which is presently communicating with the processor.

S4	S3	INDICATION
0	0	ES
0	1	SS
1	0	CS
1	1	DS

Bus High Enable/Status Signal (**BHE/S7): -** 1024KB [1MB] addressable memory of 8086 is divided into two 512KB even and odd memory banks.Even memory bank has addresses from 00000H to 0FFFFEH it contains only Even Addresses.Odd memory bank has addresses from 00001H to 0FFFFFH it contains only Odd Addresses.

BHE signal is active low signal which is used as enable signal of Odd memory bank. If BHE signal is active,the data is transmitted or received by using higher order 8 data lines (D15-D8).The BHE signal is active in the 1st clock cycle T_1 of any machine cycle.For the remaining clock cycle of any machine cycle the same signal can be used as the status signal (S7).The address line A_0 is used as Enable signal for the Even Memory Bank.The combination of BHE signal and the A_0 signal gives the information of how the data is transmitted or received to or from the memory system.

BHE	A_0	Indication
0	0	Whole word is received/transmitted[D15-D0data lines are active]
0	1	Byte from Odd memory bank[D15-D8data lines are active]
1	0	Byte from Even memory bank[D7-D0 data lines are active]
1	1	Passive

NMI (Non Maskable Interrupt) Signal: -By using this signal,the processor receives only the non maskable interrupt requests from the external devices.

INTR (Interrupt Request) Signal: -By using this signal,the processor receives the maskable interrupt requests from the external devices.

CLK (clock signal): -The processor receives the clock signals from the Clock Generator 8284.

Power supply signals(V_{cc}&V_{ss}): -V_{cc} = +5V single power supply is required for the processor operation. V_{ss}=Ground

Reset Signal: -By using this signal, the external devices reset the processor.If this signal is active, the processor terminates presently executing program and shift to execution initial address i.e. 0FFFF0H, all internal registers are loaded with their default values and Internal Buses operates at Tri-state.

Ready Signal: -It is called Synchronizing signal.This signal can be used by only slowly operated external devices.The logic level on this pin is equal to 0, and then the processor enters into WAIT state.If the logic level on this pin=1, the processor is ready to communicate with the external device.This signal used to synchronize the speed of processor with the selected I/O device.

MN/MX: -The logic level on this pin decides the processor mode of operation.The logic level on this pin=0, then processor enters into MAXIMUM mode or **Multiprocessor mode**.The logic level on this pin=1,then processor enters into MINIMUM mode or **Single Processor mode.**

TEST: -The logic level on this pin=0, then the processor operation is normal. Otherwise, the processor enters into WAIT state.

RD:-Logic level on this pin=0,then the processor performs either memory Read or I/OReadoperation. This is one of the control signal of 8086 Processor.

2. Minimum mode signals(8): - These are also called single processor mode signals.The pin MN/MX is connected to V_{cc}, and then the processor operates in this mode.

HOLD & HLDA: - HOLD and HLDA Signals are called DMA signals.The processor receives DMA request signals from the external DMA controller by using HOLD pin.The processor gives highest priority to the DMA request as compared to any other hardware Interrupt requests. Processor sends its acceptance information to DMA controller by using HLDA signal.It also gives control over the system bus to DMAC.

M/IO: - It is a status signal.The logic level on this pin=0, then the processor is communicating with the externalI/O devices.The logic level on this pin pin=1,then the processor is communicating with the memory system.

WR: - It is a control signal. If this signal is active,then the processor performs either Memory write or I/O write operation.

DEN & DT/R: - DEN and DT/R are Transceiver (Bidirectional Buffer) Signals. These are outward direction signals.

DEN (Data Enable) Signal: - It is used as Enable signal for bidirectional buffers.If DEN is active,it indicates the information on Multiplexed Address & Data lines (AD15-AD0) is valid data information.

DT/R (DataTransmit/Receive) Signal: - It is used to give the data direction to the bidirectional buffers. Logic level on DT/R=1,then the processor will be sending information to external devices through Transceivers.Logic level on DT/R=0,then the processor receives information from external devices through Transceivers.

ALE (Address Latch Enable):-This signal is used as Enable signal for Address latches. This signal de-multiplexes the multiplexed address and data lines. If this signal is active,then the information on Multiplexed Address & Data Lines (AD15-AD0) is avalid address.This signal is active only in the 1st clock cycle (T1)of any machine cycle.

INTA (Interrupt Acknowledgement Signal): - By usingthis signal, the processor sends Interrupt Acknowledgement Signal to the interrupting device.

3. Maximum Mode Signals(8): -

RQ/GT_0;RQ/GT_1 (Request/Grant Signals): -These pins are used by the other local bus master in Maximum Mode, to force the processor to release the local bus at the end of the processor current bus cycle.Each of the pin is bidirectional with RQ/GT0 having higher priority than RQ/GT1.Request/Grant sequence is as follows:

1.A pulse of one clock wide from another bus master requests the bus access to 8086.
2.During T4(current) or T1(next) clock cycle, a pulse one clock wide from 8086 to the requesting master, indicates that the 8086 has allowed the local bus to float and that it will enter the 'hold acknowledge' state at next cycle. The CPU bus interface unit is likely to be disconnected from the local bus of the system.
3.A one clock wide pulse from another master indicates to the 8086 that the hold request is about to end and the 8086 may regain control of the local bus at the next clock cycle. Thus each master to master exchange of the local bus is a sequence of 3 pulses. There must be at least one dead clock cycle after each bus exchange. The request and grant pulses are active low.For the bus request those are received while 8086 is performing memory or I/O cycle, the granting of the bus is governed by the rules as in case of HOLD and HLDA in minimum mode.

LOCK: -This output pin indicates that other system bus master will be prevented from gaining the system bus, while the LOCK signal is low. The LOCK signal is activated by the 'LOCK' prefix instruction and remains active until the completion of the next instruction. When the CPU is executing a critical instruction which requires the system bus, the LOCK prefix instruction ensures that other processors connected in the system will not gain the control of the bus.

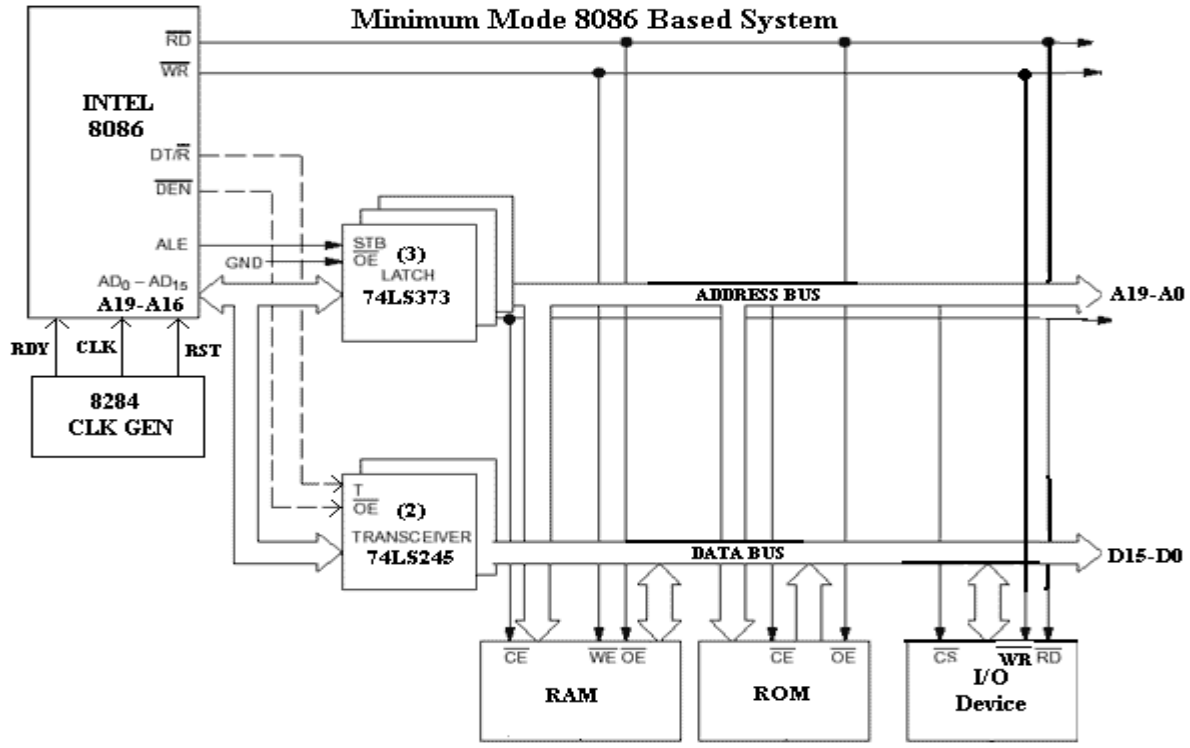
S_0,S_1,and S2 (Status Signals): - These are the status lines which reflect the type of operation, being carried out by the processor.

S_0	S_1	S_2	Indication
0	0	0	INTA
0	0	1	I/O Read
0	1	0	I/O write
0	1	1	Halt
0	0	0	OpcodeFetch
0	0	1	MemoryRead
0	1	0	MemoryWrite
0	1	1	Passive

QS_0,QS_1 (Queue Status Signals): - These lines give the status of the Instruction Queue in BIU of 8086.

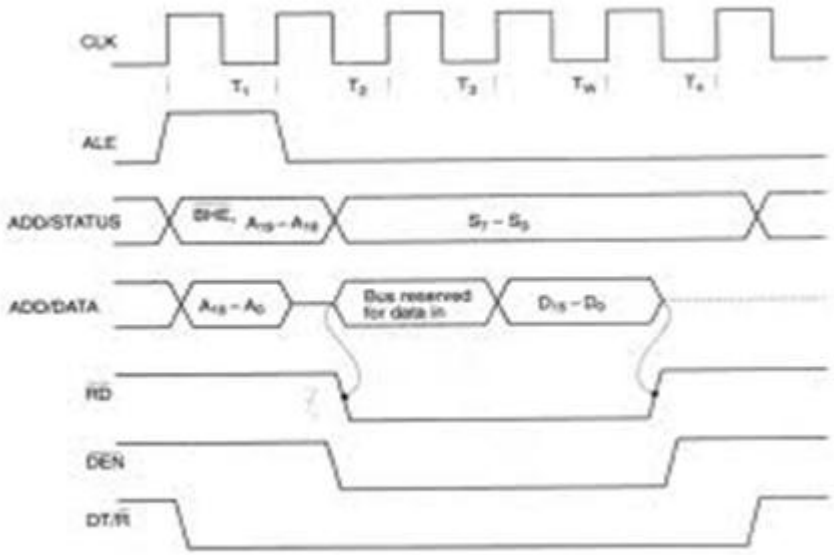
QS_0	QS_1	Indication
0	0	Inactive
0	1	First byte of opcode from Queue.
1	0	Queue is Empty
1	1	Subsequent Byte from the Queue

Minimum Mode operation of 8086 Processor: -In a minimum mode 8086 system, the microprocessor 8086 is operated in minimum mode by connecting its MN/MX pin to logic '1' it means the pin is connected to the V_{cc} . In this mode, all the control signals are given out by the microprocessor chip itself.There is a single microprocessor in the system.



1. In this mode, all the control signals are given out by the microprocessor chip itself. There is a single microprocessor in the minimum mode system.
2. The remaining components in the system are latches, transceivers, clock generator, memory and I/O devices. Some type of chip selection logic may be required for selecting memory or I/O devices, depending upon the address map of the system.
3. Latches are generally buffered output D-type flip-flops like 74LS373. They are used for separating the valid address from the multiplexed address/data signals and are controlled by the ALE signal generated by 8086.
4. Transceivers are the bidirectional buffers and sometimes they are called as data amplifiers. They are required to separate the valid data from the time multiplexed address/data signals. They are controlled by two signals namely, DEN and DT/R.
5. The DEN signal indicates the direction of data, i.e. from or to the processor. The system contains memory for the monitor and users program storage.
6. Usually, EPROMs are used for monitor storage, while RAM for user's program storage. A system may contain I/O devices.
7. The working of the minimum mode configuration system can be better described in terms of the timing diagrams rather than qualitatively describing the operations.

Read Timing Diagram for Minimum Mode Operation of 8086: -



Read Cycle Timing Diagram for Minimum Mode

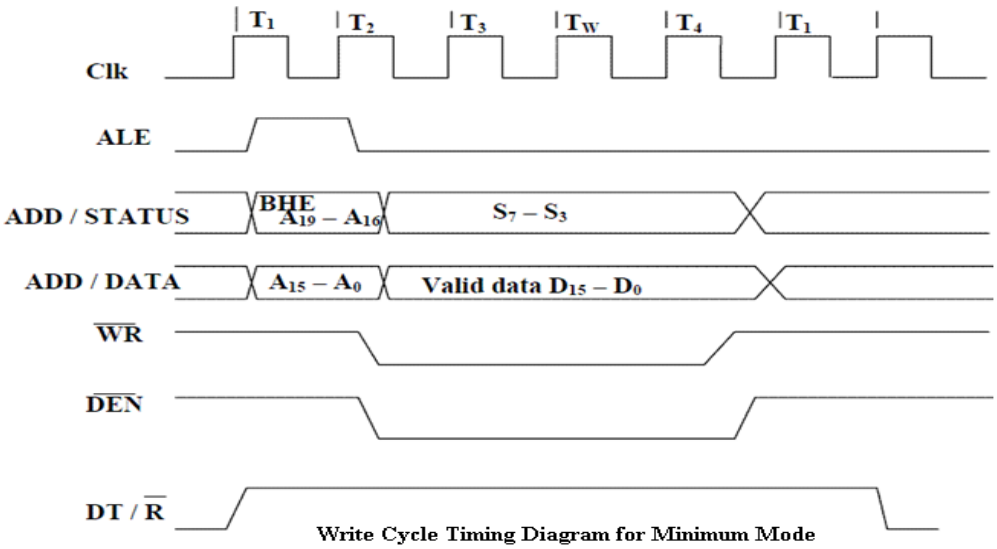
The read cycle begins in T1 with the assertion of address latch enable (ALE) signal and also M / IO signal. During the negative going edge of this signal, the valid address is latched on the local bus.

The BHE and A0 signals address low, high or both bytes. From T1 to T4, the M/IO signal indicates a memory or I/O operation.

At T2, the address is removed from the local bus and is sent to the output. The bus is then tri-stated. The read (RD) control signal is also activated in T2.

The read (RD) signal causes the address device to enable its data bus drivers. After RD goes low, the valid data is available on the data bus.

Write Timing Diagram for Minimum Mode Operation of 8086: -



Write Cycle Timing Diagram for Minimum Mode

A write cycle also begins with the assertion of ALE and the emission of the address. The M/IO signal is again asserted to indicate a memory or I/O operation. In T2, after sending the address in T1, the processor sends the data to be written to the addressed location.

The data remains on the bus until middle of T4 state. The WR becomes active at the beginning of T2 (unlike RD is somewhat delayed in T2 to provide time for floating).

The BHE and A0 signals are used to select the proper byte or bytes of memory or I/O word to be read or write.

Maximum Mode operation of 8086 Processor: - In the maximum mode, the 8086 is operated by connecting its MN/MX pin to logic '0' it means the pin is connected to the ground.

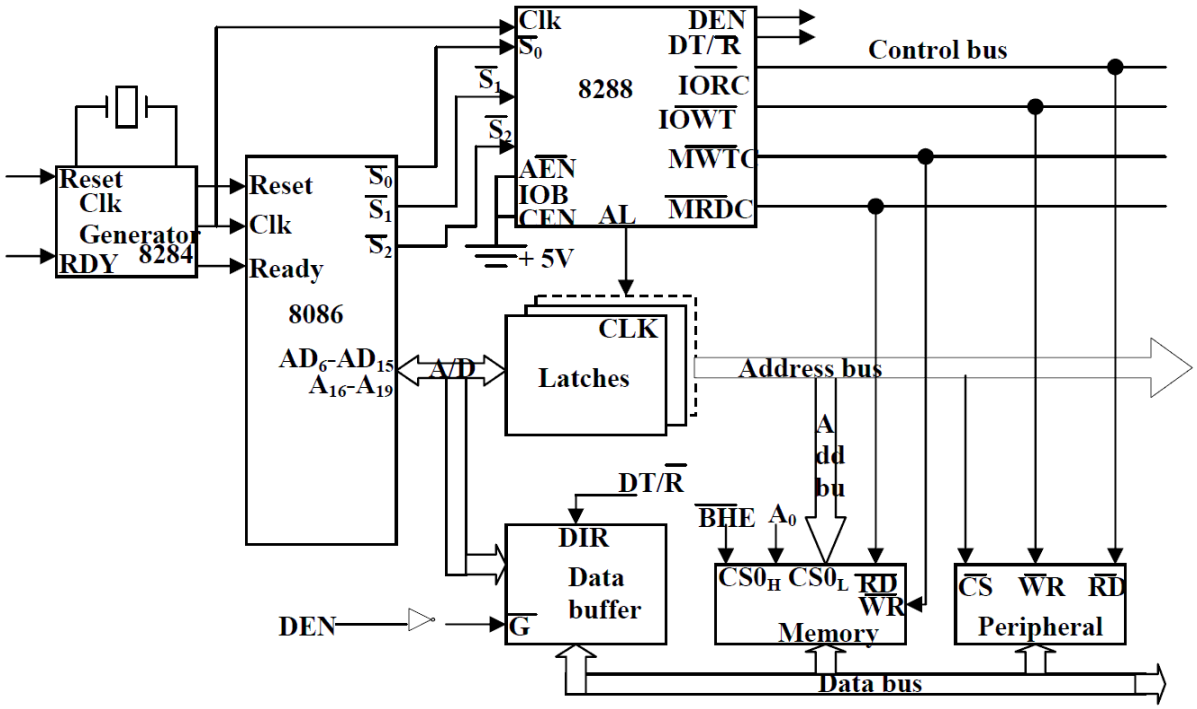
In this mode, the processor derives the status signal S2, S1, S0. Another chip called bus controller derives the control signal using this status information.

In the maximum mode, there may be more than one microprocessor in the system configuration.The components in the system are same as in the minimum mode system.

The basic function of the bus controller chip IC8288 (DEMUX) is to derive control signals like RD and WR (for memory and I/O devices), DEN, DT/R, ALE etc. using the information by the processor on the status lines.

The bus controller chip has input lines S2, S1, S0 and CLK. These inputs to 8288 are driven by CPU.

It derives the outputs ALE, DEN, DT/R, MRDC, MWTC, AMWC, IORC, IOWC and AIOWC. The AEN, IOB and CEN pins are especially useful for multiprocessor systems.



Maximum Mode 8086 System.

AEN and IOB are generally grounded. CEN pin is usually tied to +5V. The significance of the MCE/PDEN output depends upon the status of the IOB pin.

If IOB is grounded, it acts as master cascade enable to control cascade 8259A, else it acts as peripheral data enable used in the multiple bus configurations.

INTA pin used to issue two interrupt acknowledge pulses to the interrupt controller or to an interrupting device.

IORC, IOWC are I/O read command and I/O write command signals respectively.

These signals enable an IO interface to read or write the data from or to the address port.

The MRDC, MWTC are memory read command and memory write command signals respectively and may be used as memory read or write signals.

All these command signals instructs the memory to accept or send data from or to the bus.

For both of these write command signals, the advanced signals namely AIOWC and AMWTC are available.

Here the only difference between in timing diagram between minimum mode and maximum mode is the status signals used and the available control and advanced command signals.

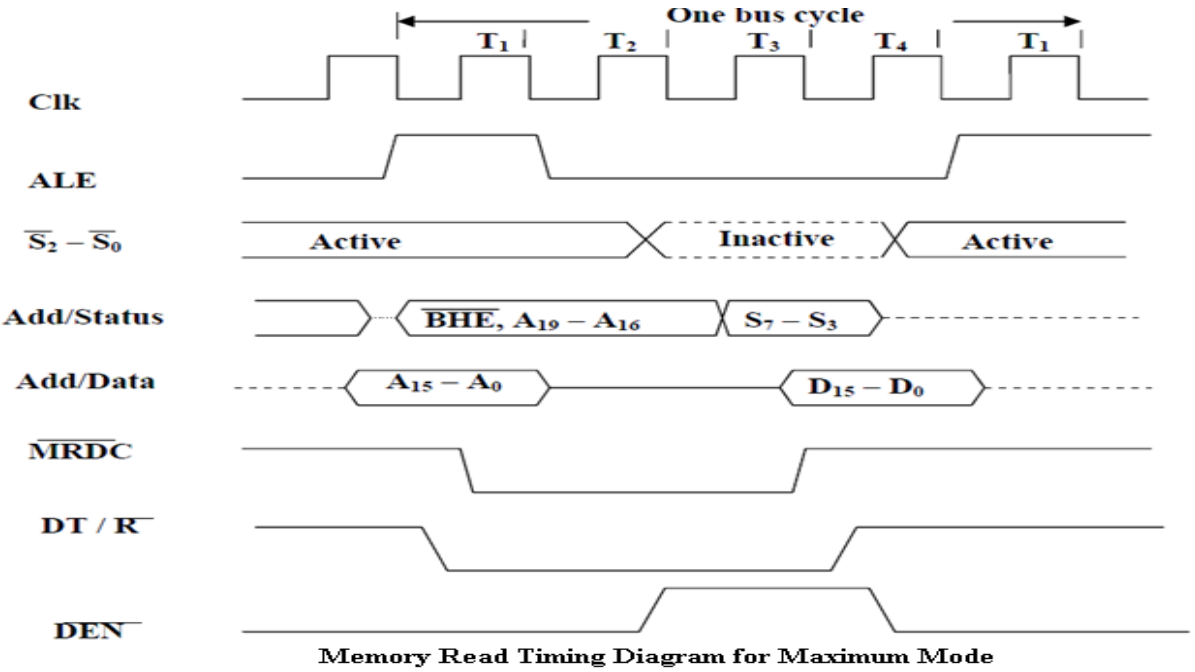
R0, S1, S2 are set at the beginning of bus cycle.8288 bus controller will output a pulse as on the ALE and apply a required signal to its DT / R pin during T1.

In T2, 8288 will set DEN=1 thus enabling transceivers, and for an input it will activate MRDC or IORC. These signals are activated until T4. For an output, the AMWC or AIOWC is activated from T2 to T4 and MWTC or IOWC is activated from T3 to T4.

The status bit S0 to S2 remains active until T3 and become passive during T3 and T4.

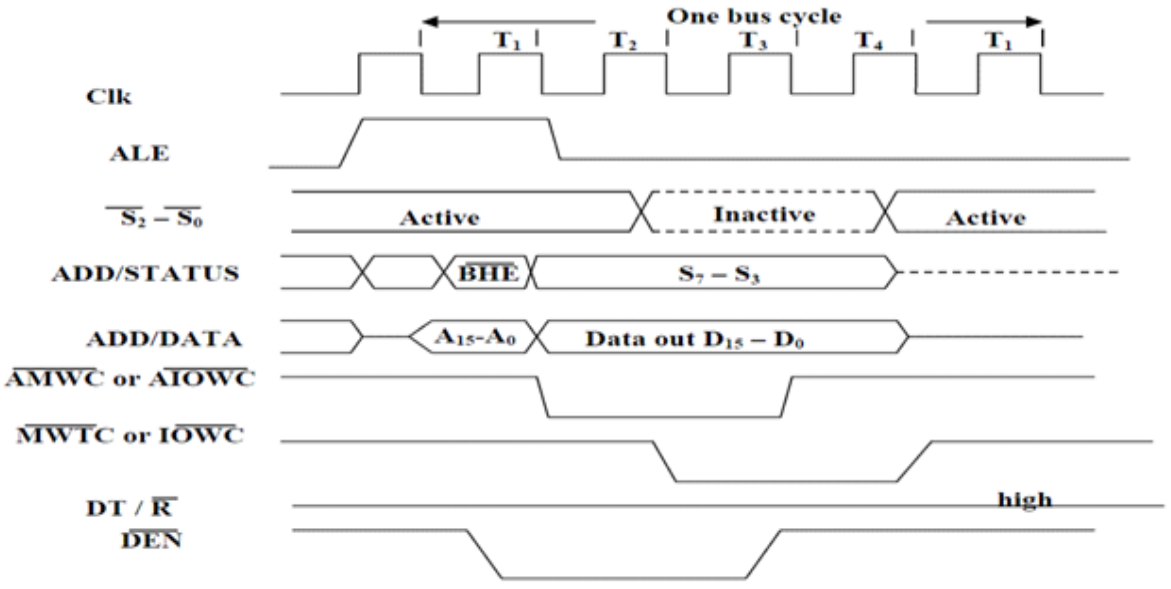
If reader input is not activated before T3, wait state will be inserted between T3 and T4.

Memory Read Timing Diagram for Maximum Mode Operation of 8086: -



Memory Read Timing Diagram for Maximum Mode

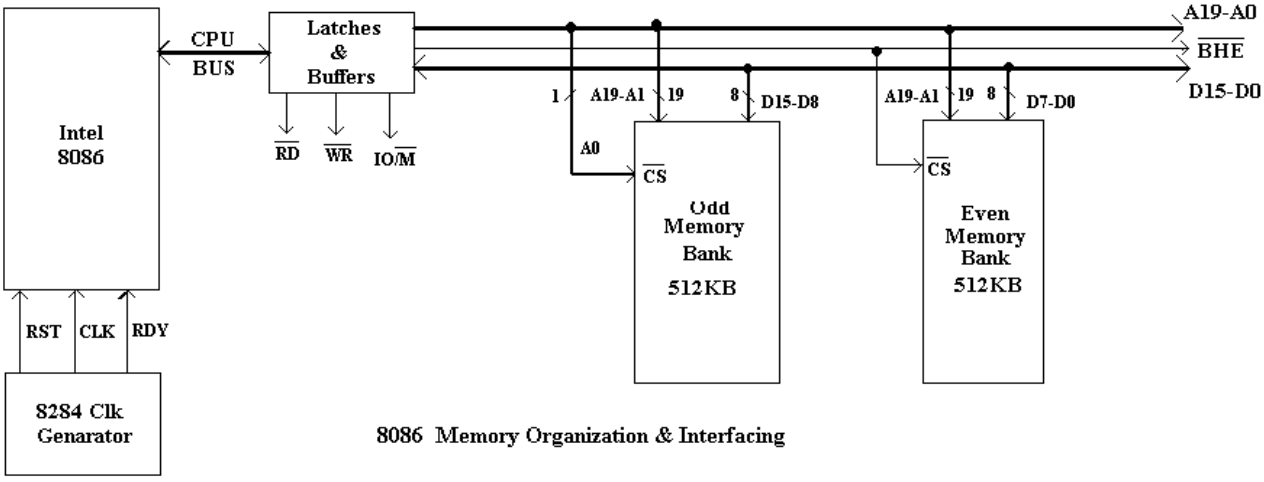
Memory Write Timing Diagram for Maximum Mode Operation of 8086: -



Maximum Mode Timing Diagram for Memory Write

Memory Organizationof 8086: -

1. 8086 Addressable 1MB of memory can be organised into two 512KB of memorybanks.
2. Those two memory banks are:
   i)Even memory bank ii)Odd memory bank.
3. Even memory bank is also called Lower order DataByteMemoryBank.
4. Oddmemorybank is also called Higherorder DataByteMemoryBank.
5. Even memory bank only contains Even Addresses. Starting address is 00000H and Last Address is 0FFFFEH.
6. Odd memory bank only contains Odd Addresses. Starting address is 00001H and Last Address is 0FFFFFH.
7. The Enable signal for Even memory bank is the address line 'A0'and the Enable signal for Odd memory bank is BHE.Both are Active low signals.
8. The reason for the memory organisation of 1MB of memory into two 512KB memory banks is to Read/Write of information size 16-bit is done in a single clock cycle.
9. For Even memory Bank to Read/Write information the lower order 8 data lines of 8086 is directly connected to the bank.
10. For Odd memory Bank to Read/Write information the higher order 8 data lines of 8086 is directly connected to the bank.



8086 Memory Organization & Interfacing

Different ways of data sending or receiving from the Memory Banks: -

CASE1: -Read/Write one data byte to/from the memory banks,the address is Even Address.For this case, the even memory bank is active because the logic level on A_0 =0,then the even memory bank is active,but odd memory bank is inactive,because logic level on BHE=1.

Ex: - MOV AL,[1024H]

CASE2: - Read/Write one data byte to/from the memory banks,the address is Odd Address.For this case,the odd memory bank is active because BHE=0,then even memory bank is inactive,because logic level on A_0 =1.

Ex: - MOV AL,[1025H]

CASE 3: - Read/Write one data word to/from the memory banks,the address is Even Address.For this case,even memory bank &odd memory banks both are active,because logic level on BHE=A_0=0.

Ex: - MOV AX,[1050H]

CASE4: - Read/Write one data word of information to/from the memory banks, if the address is odd

i)In the 1st clock cycle, logic level on A_0=1 and logic level on BHE=0 only odd memory bank is active,then the location data is transmitted/received to/from the processor by using Higher order 8-data lines.

ii) In the 2nd clock cycle,BHE=1 and A_0=0, then even memory bank is active,then thelocation data is transmitted/received to/from the processor by using lower order 8-data lines.

Ex: - MOV AX,[1055H]

Memory Interfacing: -

"Interfacing" means designing of Hardware and writing of software,for the processor is communicating with the external devices (I/O devices and memory devices). There are two types of interfacing devices:

i) Non-programmable Interfacing devices: To work these devices there is no need of software code in the Program.

Ex: - 74LS373 Octal Latches,74LS245 Bidirectional buffers, 74LS138/139 Decoders etc.

ii)Programmable Interfacing Devices: - To work these devices there is a need of software code in the Program.

Ex: - 8255 PPI (Programmable Peripheral Interface), 8251 USART (Universal Synchronous Asynchronous Receiver and Transmitter), 8259 PIC (Programmable Interrupt Controller),8237/57 DMAC(DMA Controller).

Address Decoding: - Address decoding is the process generation of Chip-select Signals for external devices by using unused address lines of the processor. There are 2 types of Address Decoding Methods.

1)Absolute Address Decoding Method: - In this address decoding method,all the unused address lines of the processor are involved in the generation of chip-select signals for the external devices.By using this method each and every I/O device or a memory location have only one address i.e. Unique Address.

2)Partial Address Decoding Method: - In this address decoding method, only some of the unused address lines of the processor are involved in the generation of chip-select signals for the external devices. By using this method each and every I/O device or a memory location have more than one address, because some address lines logic levels we don't know exactly.