MPI MID-2 QUESTION BANK

UNIT-II Hardware Features of 8086

10 mark questions

1) What is a timing diagram? Draw the timing diagrams for memory read and memory write machine cycles in minimum mode.
2) Draw the timing diagrams of 8086 I/O write and read operations in minimum mode and explain the functions of signals used.
3) Explain the different pins that are used only in maximum mode of 8086.
4) Design an interface between 8086 CPU and two chips of 16K X 8 EPROM and two chips of 32K X 8 RAM. Select the starting address of EPROM suitably. The RAM address must start at 00000H.
5) Explain the functions of minimum mode pins of 8086.
6) Draw the minimum mode configuration of 8086 and explain its read cycle operation.
7) Draw the maximum mode configuration of 8086 and explain its read cycle operation.
8) Explain the function of all the pins of 8086 Processor with a neat pin diagram.
9) Explain the physical memory organization in an 8086 system with examples.
10) Explain about multiplexed ADD/DATA and ADD/STATUS buses in 8086.

1Mark Questions

1) 8086 microprocessor IC has _____ no. of pins.
2) When status lines S_4S_3=11, indicates _____ segment register is being used for data accessing.
3) When $\overline{BHE}$ =1, A_0=0 then _____ data lines of 8086 will become active.
4) Which signal of 8086 when it is active, indicates the processor is performing memory read cycle.
5) While 8086 accessing memory what happens if the logic level on READY pin is equal to 0?
6) 8086 Interrupt Request signal is a ____ triggered input.
7) 8086 NMI signal is a ____ triggered input.
8) If the signal on $\overline{TEST}$ input is High then what happens to 8086 microprocessor operation.
9) When 8086 receives RESET signal then it restarts Execution from _____ address.
10) If the logic level on MN/$\overline{MX}$ pin is LOW, then processor enters into _____ mode.
11) If the logic level on M/$\overline{IO}$ is Low then it indicates the CPU is having _____ operation.
12) What pin(s) of 8086 indicates that the processor is performing memory write operation.
13) Which signal of 8086 indicates the availability of the valid address on the multiplexed lines?
14) What are the DMA signals available for 8086 in minimum mode?
15) The logic level on status signals $\overline{S0}$,$\overline{S1}$, $\overline{S2}$ = 001 indicates what status of 8086?
16) Which logic levels on queue status signals indicate instruction queue is empty.
17) ____ Pin of 8086 indicates that other system bus master will be prevented from gaining the system bus.

18) By using Absolute Address Decoding Method each and every I/O device or a memory location can have ____ addresses
19) When the unused memory addresses are used for addressing I/O devices, then Such I/O devices are called _____ mapped I/O devices.
20) A 4K x 8 memory contains ____ memory locations, where each location contains ___ bits of data.