16CS402 - Embedded Systems

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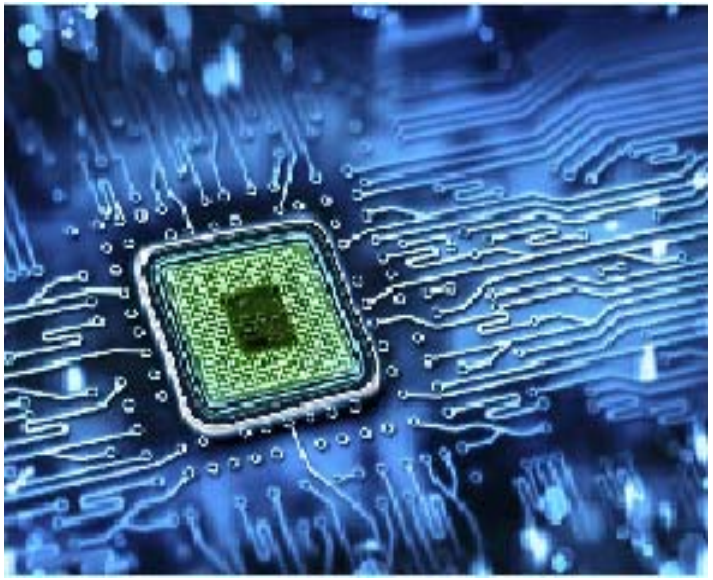
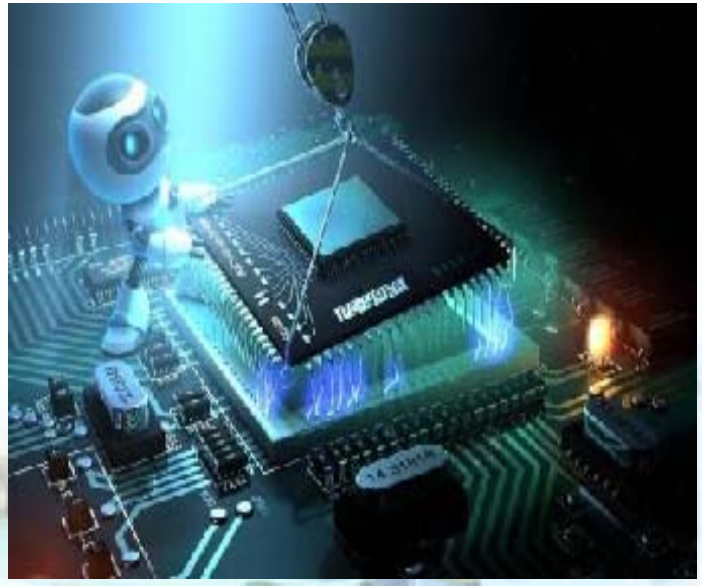


CSE

UNIT - III



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UNIT - III

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ARM Embedded Processor

- History, Architecture
- Interrupt Vector
- Programming the ARM, ARM Assembly Language
- Instruction Set, Conditional Execution
- Arithmetic and Logical Compare

ARM

- Advanced RISC Machine (ARM) is a family of RISC architectures.
- ARM is a 32-bit processor.
- When used in relation to the ARM:
  - Byte means 8 bits
  - Halfword means 16 bits (two bytes)
  - Word means 32 bits (four bytes)
- Most ARM's implement two instruction sets:
  - 32-bit ARM Instruction Set
  - 16-bit Thumb Instruction Set
- The ARM processor's **smaller size**, reduced complexity **and lower power consumption** makes them suitable for increasingly miniaturized device.
- ARM is one of the most **licensed** and widespread processor cores in the world.
- ARM processors are extensively used in consumer electronic devices (smartphones, tablets, multimedia players and wearables). Because of their reduced instruction set, they require fewer transistors, which enables a smaller die size for the IC.

Ex: ARM7, ARM9, ARM11 and Cortex-**A, -R, -M**

RISC - The Reduced Instruction Set Computers

RISC Architecture

- A **fixed (32-bit) instruction size** with few formats.
- A **load-store** architecture.
- A large register bank of thirty-two 32-bit registers.

RISC Organization

- Hard-wired instruction decode logic.
- Pipelined execution.
- **Single-cycle** execution.

RISC Advantages

- A **smaller die size**
- A **shorter development time**
- A higher performance

History of ARM

- Advanced RISC machine (ARM) is the first reduced instruction set computer (RISC) processor for commercial use, which is currently being developed by ARM Holdings.
- 1983 in England when Acorn Computers Ltd officially launched an Acorn RISC Management project after being inspired to design its own processor by Berkeley RISC, one of the high-impact projects under ARPA's (Advanced Research Projects Agency) VLSI project, dealing with RISC-based microprocessor design led by David Patterson who coined the term 'RISC.'
- ARM in the beginning was known as Acorn RISC machine. With VLSI Technology Inc. as its silicon partner, ARM came up with ARM1, the first ARM silicon on April 26, 1985, which was used as a second processor to the BBC Micro to develop the simulation software to finish work on the support chips.
- Apple Newton, a personal digital assistant, found that only Acorn RISC machine was close to the requirements needed for implementation, but since ARM had no integral memory management unit, Apple collaborated with Acorn to develop ARM.
- Both Acorn Group and Apple Computer, Inc., and VLSI Technology, Inc. as an investor, a separate company, ARM Ltd, was established in 1990. After that time, ARM became the acronym for advanced RISC machine.

ARM History

- In 1980, Patterson & Bitzel published a paper "The case for the RISC"

- In 1982, BBC Microcomputer Broadcast series of TV programs success.

- In 1983, Acorn Business Computers (ABC), Cambridge, England Developed ARM.

- Two types of ARM License :
  - Hardcore (optimized for specific process) &
  - Soft core (less optimized but used in any process)

- ARM is a 32bit RISC instruction set architecture, Suitable for low power applications.
  - Used in Mobile Phones, PDA, Music Players, Routers and Hard Drives.

✓ 1985 – ARMv1, 26bit Addressing, <25000 Transistors, by Roger Wilson & Steve Furber.
✓1987 – ARMv2, 26bit Addressing, Multiply, co-processor support, 30000 Transistors
✓1990 – ARMv3, 32bit Addressing, On-chip Cache, MMU support
✓1996 – ARMv4, 32bit Addressing, Thumb support (ARM 7TDMI Core)
✓1999 – ARMv5, Divide, Java Enhancement (Jazelle)
✓2001 – ARMv6, TEJ Enhancement , Multiprocessing, Multimedia support

ARM Basics…

ARM is a 32 bit RISC processor supports TDMI

T ⇨ Thumb

D ⇨ On-Chip Debug support

M ⇨ Enhanced Multiplier

I ⇨ Embedded ICE (In Circuit Emulator)

Applications:

- ARM7 TDMI – IPod, GPA
- ARM9 TDMI – Sony Ericsson, BenQ, NDS
- ARM11 TDMI – Apple iPhone, Nokia N93, N800

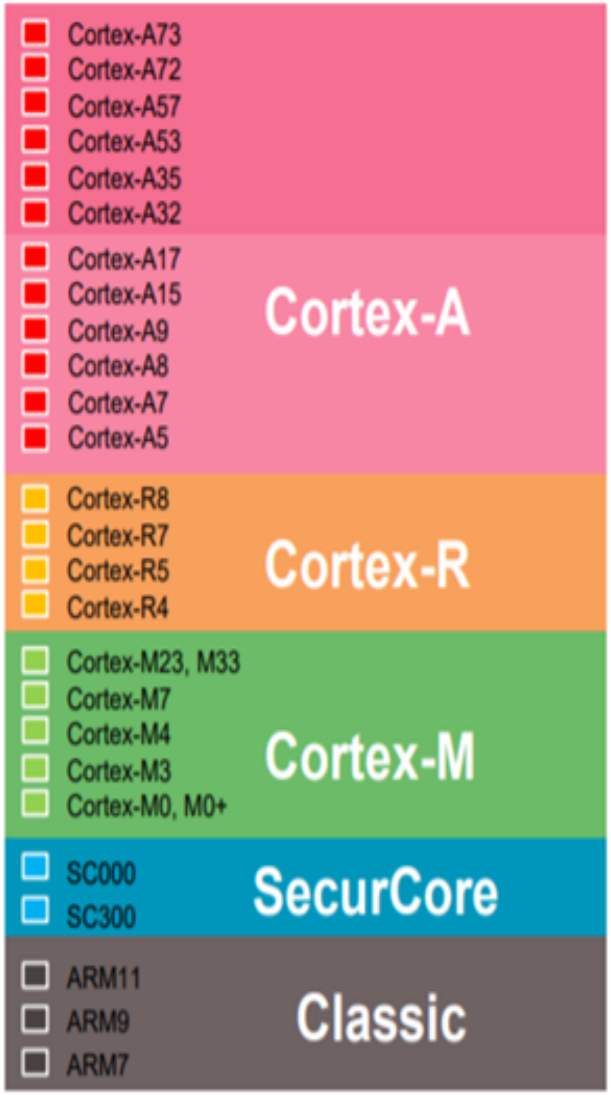
ARM Basics... Naming rule of ARM

ARM {x} {y} {z} {T} {D} {M} {I} {E} {J} {F} {-S}

- **–x: series**
- **–y: memory management / protection unit**
- **–z: cache**
- **–T: Thumb decoder**
- **–D: JTAG debugger**
- **–M: fast multiplier**
- **–I: support hardware debug**
- **–E: enhance instructions (based on TDMI)**
- **–J: Jazelle**
- **–F: vector floating point unit**
- **–S: synthesizable, suitable for EDA tools**

ARM Basics... Processor Families of ARM

- **Cortex-A series (Application)**
  - High performance processors capable of full Operating System (OS) support
  - Applications include smartphones, digital TV, smart books
- **Cortex-R series (Real-time)**
  - High performance and reliability for real-time applications;
  - Applications include automotive braking system, powertrains
- **Cortex-M series (Microcontroller)**
  - Cost-sensitive solutions for deterministic microcontroller applications
  - Applications include microcontrollers, smart sensors
- **SecurCore series**
  - High security applications
- Earlier classic processors including ARM7, ARM9, ARM11 families



ARM History – From Text book

10.1.1 | The ARM Core

What is meant by the 'core'? The core is the 'processing unit' or the 'computing engine' which has all the computing power, and this aspect is decided by the architecture, which represents the basic design of the processor.

One special and unique feature of ARM as a company is that it designs the core and licenses this IP (Intellectual Property) to others. This simply means that the company does not 'fabricate' the chip, but sells only the design. This design is taken by the licensee, who may or may not add more features (usually peripherals) to the design. Sometimes the buyer can also modify the basic design to a minor extent. The buyer company fabricates the design and sells it/uses it for its products.

There are various ways in which ARM sells its IP. It could be in the form of a soft IP. In this case, the design is sold as RTL (VHDL/Verilog code), and this allows the buyer to modify the design to a certain extent. If the design is sold as a hard IP, it means the buyer gets only the layout or the net list (connection of nets or electronic wires). Thus, the buyer can add only peripherals to the 'black box' design he has purchased.

We can thus understand that ARM the company does not 'fabricate' ARM chips. (In contrast, Intel fabricates its processors and sells them as chips.) It is because of this, that we have ARM chips and boards of various companies—Samsung, Philips, Atmel, Texas Instruments, ST Microelectronics and so on—the list is very long.

ARM History – From Text book

10.1.2 | The ARM Microcontroller

ARM has been designated as a 'microprocessor' and indeed it is a processor which has very high computing capabilities. It has a rich set of features for handling complex computations.

However, for using it as an embedded processor, it needs many more capabilities and these come in the forms of on-chip peripherals. To the ARM core, peripherals are added and thus it becomes a 'microcontroller' or an MCU (microcontroller unit), rather than an MPU (micro processor unit). Figure 10.1 shows the ARM MCU. The number and kind of peripherals added, depends on the requirements of the buyer of the IP. It is because of this that we have varying number of peripherals for ARM processors supplied by different companies. It could be obvious that to support more peripherals, the core has to be more powerful. That is why we generally find more peripherals around an ARM 9 core rather than around an ARM7 core. But as a rule, users have to spell out their requirements for the peripherals of an MCU.

When a chip has the core and the necessary peripherals to perform as a system, it is called a System on Chip (SoC)—and the term 'ARM SoC' is a very commonly used—understandably it has some version of the ARM core and a large set of peripherals.

ARM History – From Text book

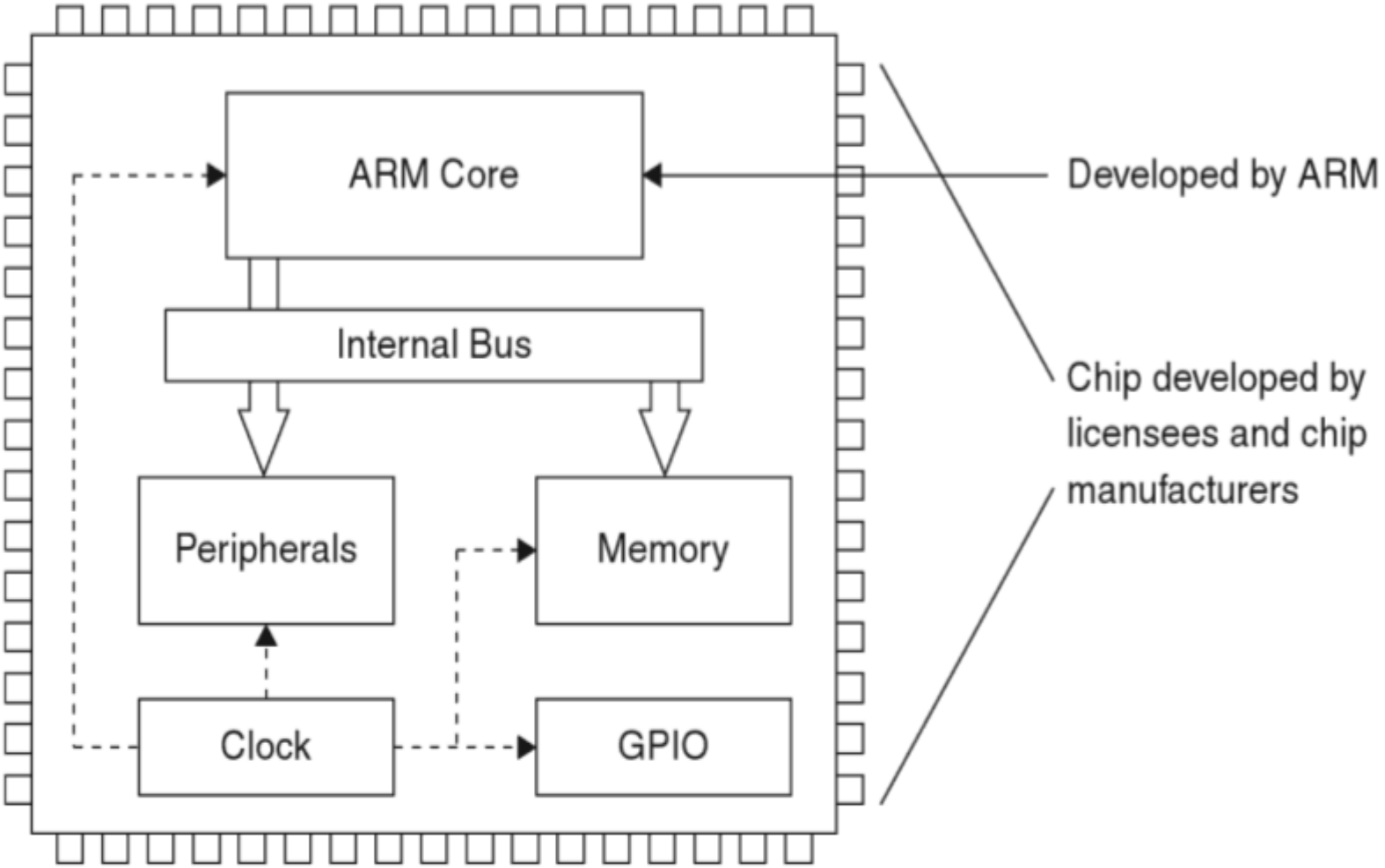


Figure 10.1 | ARM SoC—core with peripherals

ARM History – From Text book

10.1.3 | RISC vs CISC

The differences between these two schools of thought in computer architecture have been discussed in Section 0.3.

But to put the idea in a proper perspective in the context of ARM, some specific features of RISC are listed herein. These apply to most of the instructions of ARM, but not necessarily to all.

i) Instructions are of the same size, that is, 32 bits
ii) Instructions are executed in one cycle
iii) Only the load and store instructions access memory

Due to these simple guidelines in the design of the ISA (Instruction Set Architecture), the outstanding features of this RISC processor are as follows:

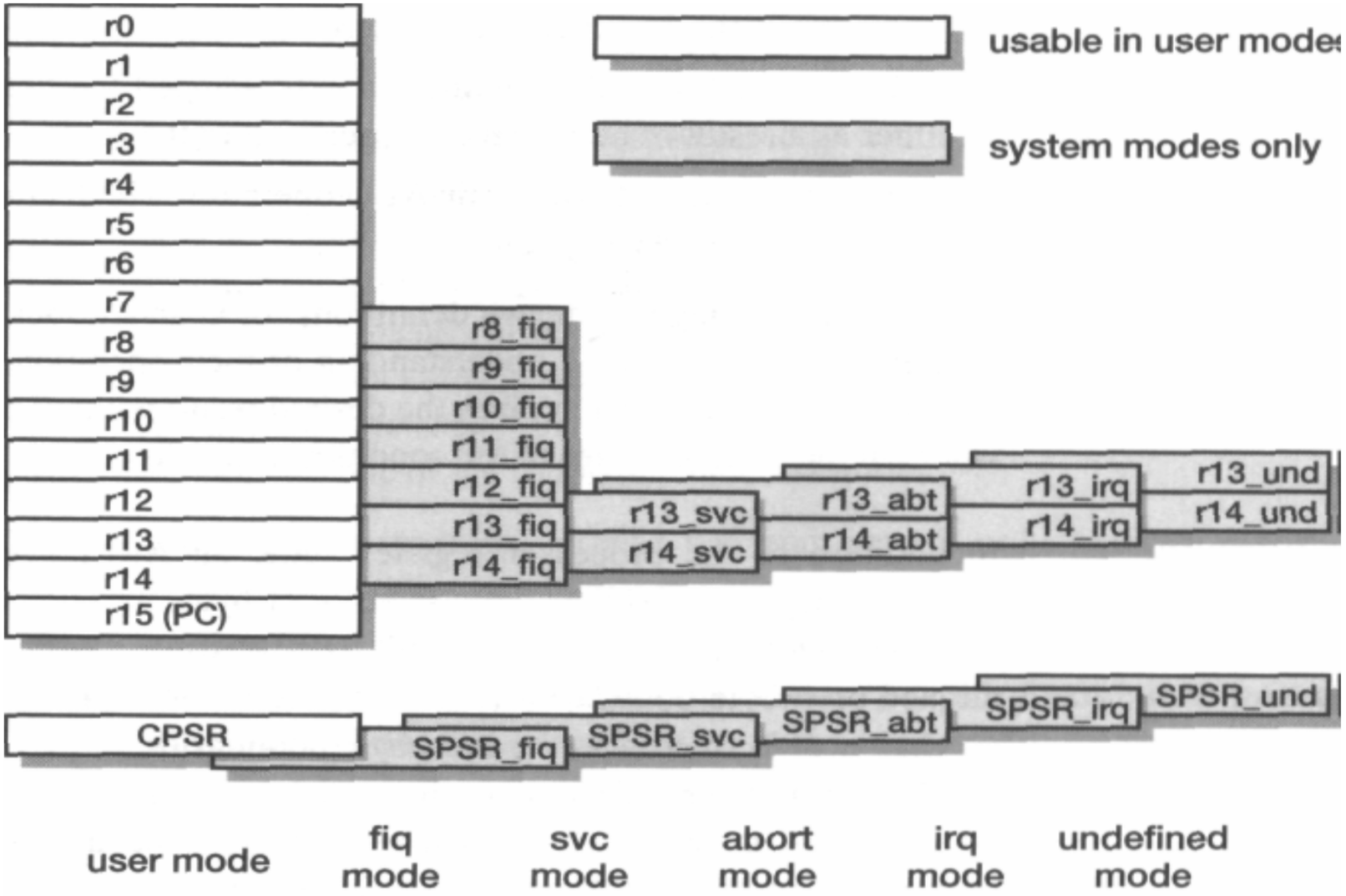
i) The number of transistors needed is much less than that of a CISC processor of comparable computational power.
ii) The die size is less because of the reduced hardware involved.
iii) Due to these aspects (and a few others, which will soon be elaborated), power dissipation is very low.

ARM History – From Text book

10.1.4 **Advanced Features:**

- Thumb (Code density)
- MMU and MPU
- Cache
- Debug Interface
- Embedded ICE
- Fast Multiplier
- Enhanced Instructions (DSP)
- Jazzele DBX (Direct Bytecode eXecution)
- Vector Floating point Unit
- Synthesizable (RTL code is available)

ARM Programmers Model



ARM - Operating Modes

The ARM7TDMI processor has seven modes of operations:

1. User mode(usr)
   - Normal program execution mode
2. Fast Interrupt mode(fiq)
   - Supports a high-speed data transfer or channel process.
3. Interrupt mode(irq)
   - Used for general-purpose interrupt handling.
4. Supervisor mode(svc)
   - Protected mode for the operating system.
5. Abort mode(abt)
   - implements virtual memory and/or memory protection
6. System mode(sys)
   - A privileged user mode for the operating system. (runs OS tasks)
7. Undefined mode(und)
   - supports a software emulation of hardware coprocessors

- Except user mode, all are known as privileged mode.

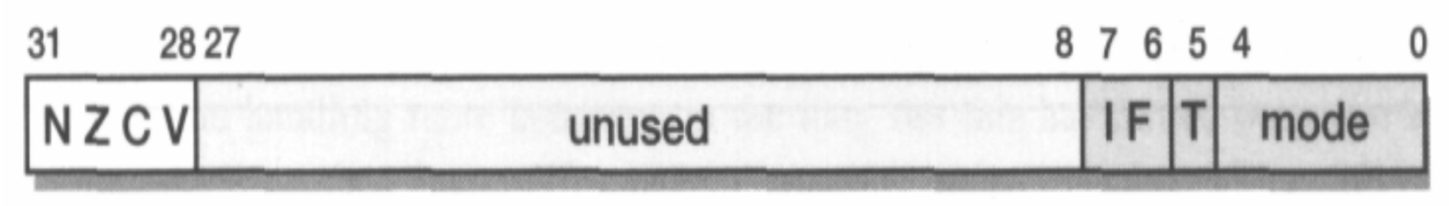
ARM - Registers

The ARM7TDMI processor has 37 registers

- 31 general 32 bit registers, including PC
  - 6 status registers
  - 15 general registers (R0 to R14), and one status registers and program counter are visible at any time –when you write user-level programs
    - R13 (SP) Stack pointer (Individual stack for each processor mode)
    - R14 (LR) Linked register
    - R15 (PC) Program Counter
- The visible registers depend on the processor mode
- The other registers (the banked registers) are switched in to support IRQ, FIQ, Supervisor, Abort and Undefined mode processing
- CPSR - Current Program Status Register contains condition code flags and the current mode bits
- 5 SPSRs (Saved Program Status Registers) which are loaded with CPSR when an exceptions occurs

ARM Programmers Model…

CPSR Format: (Current Program Status Register)



N - Negative

Z - Zero

C - Carry

V - Overflow

I – irq mode

I=1, Disable irq

F- fiq mode

F=1, Disable fiq

T-Thumb

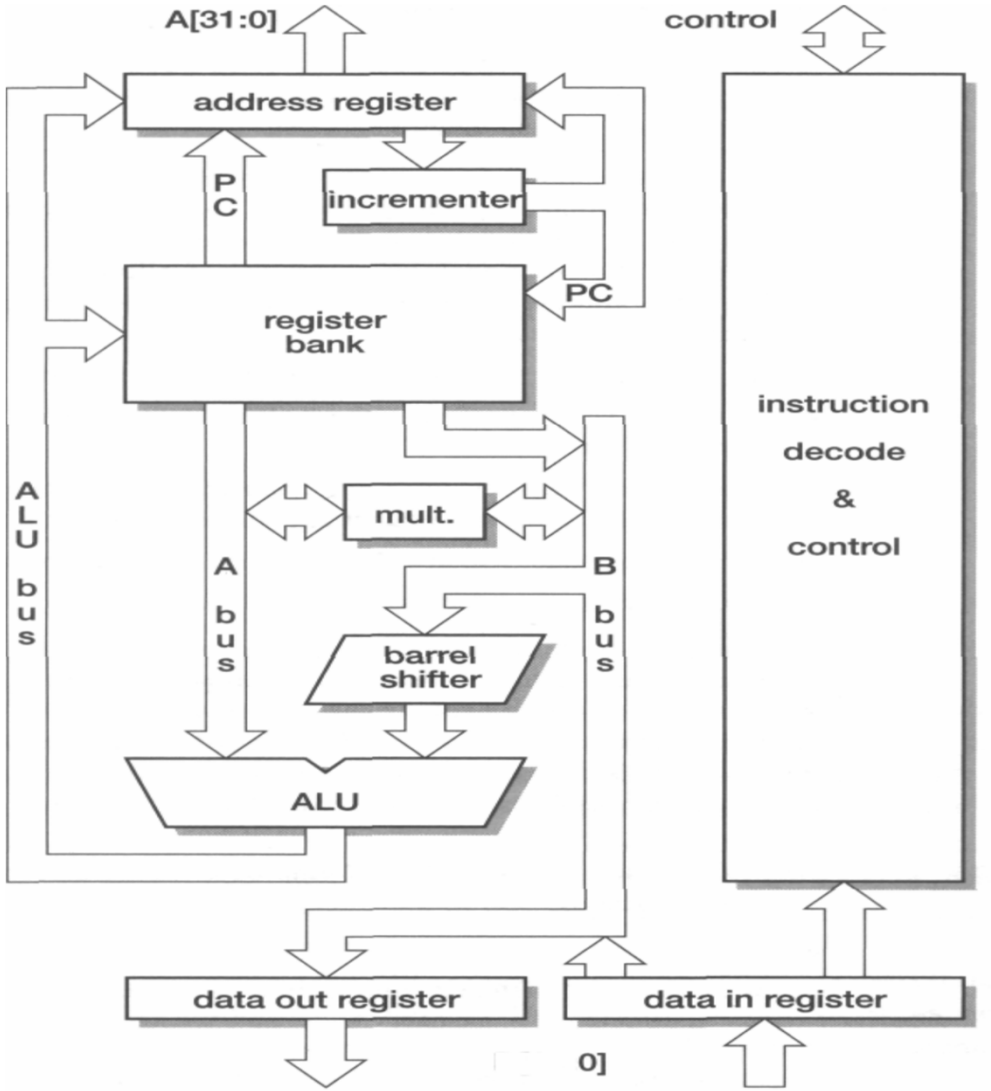
T=1, Thumb Inst. State

T=0, ARM Inst. State

Mode bits M4M3M2M1M0	Modes
10000	User Mode (usr)
10001	Fast Int Mode (fiq)
10010	Normal Int Mode (irq)
10011	Software Int Mode (svc)
10111	Abort Mode (abt)
11011	Undefined Inst Mode (und)
11111	System Mode (sys)

ARM Organization and Implementation

3-stage pipeline ARM organization:



The principal components are:

- ✓The register bank
- ✓The barrel shifter
- ✓The ALU
- ✓The address register & incrementer
- ✓The data registers
- ✓Instruction decoder & control logic.

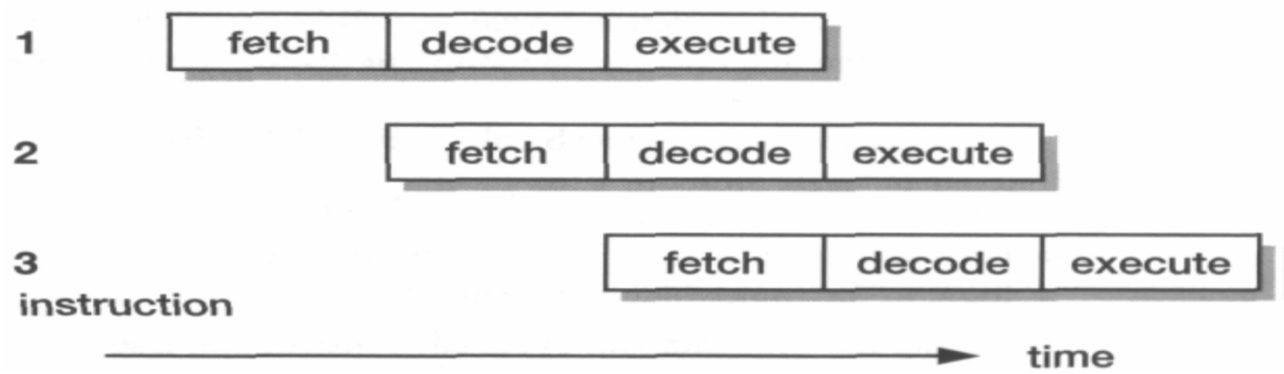
3-stage pipeline stages:

- ✓ Fetch
- ✓ Decode
- ✓ Execute

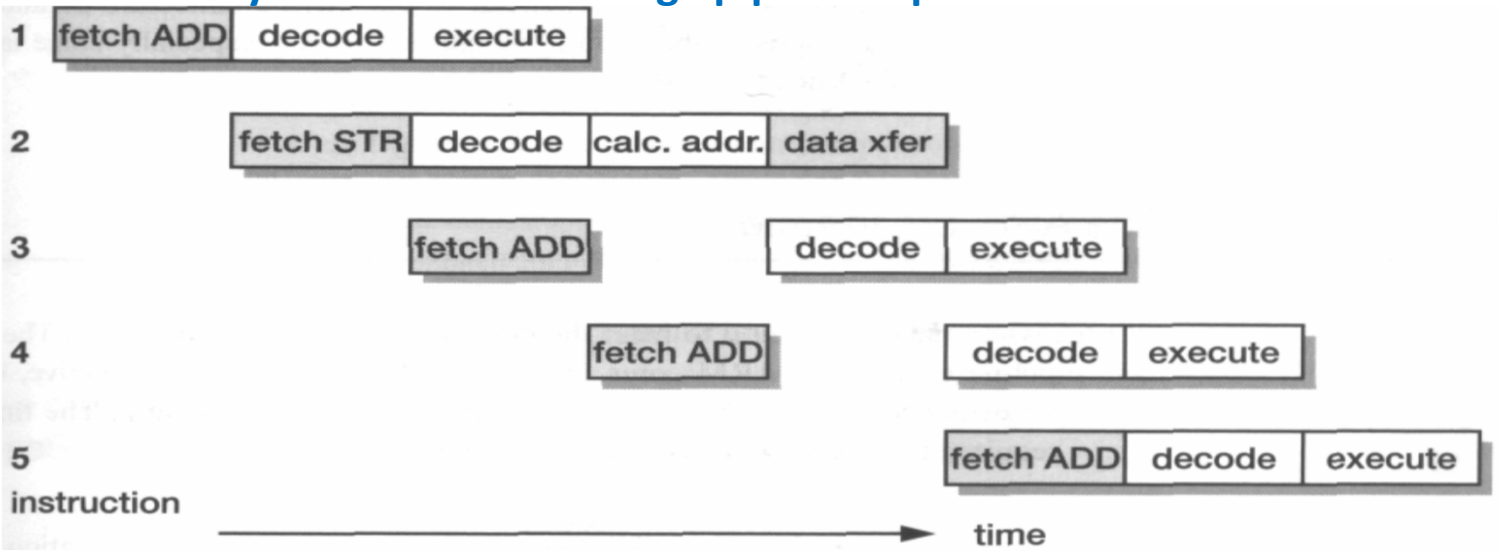
ARM Organization and Implementation…

3-stage pipeline ARM organization…

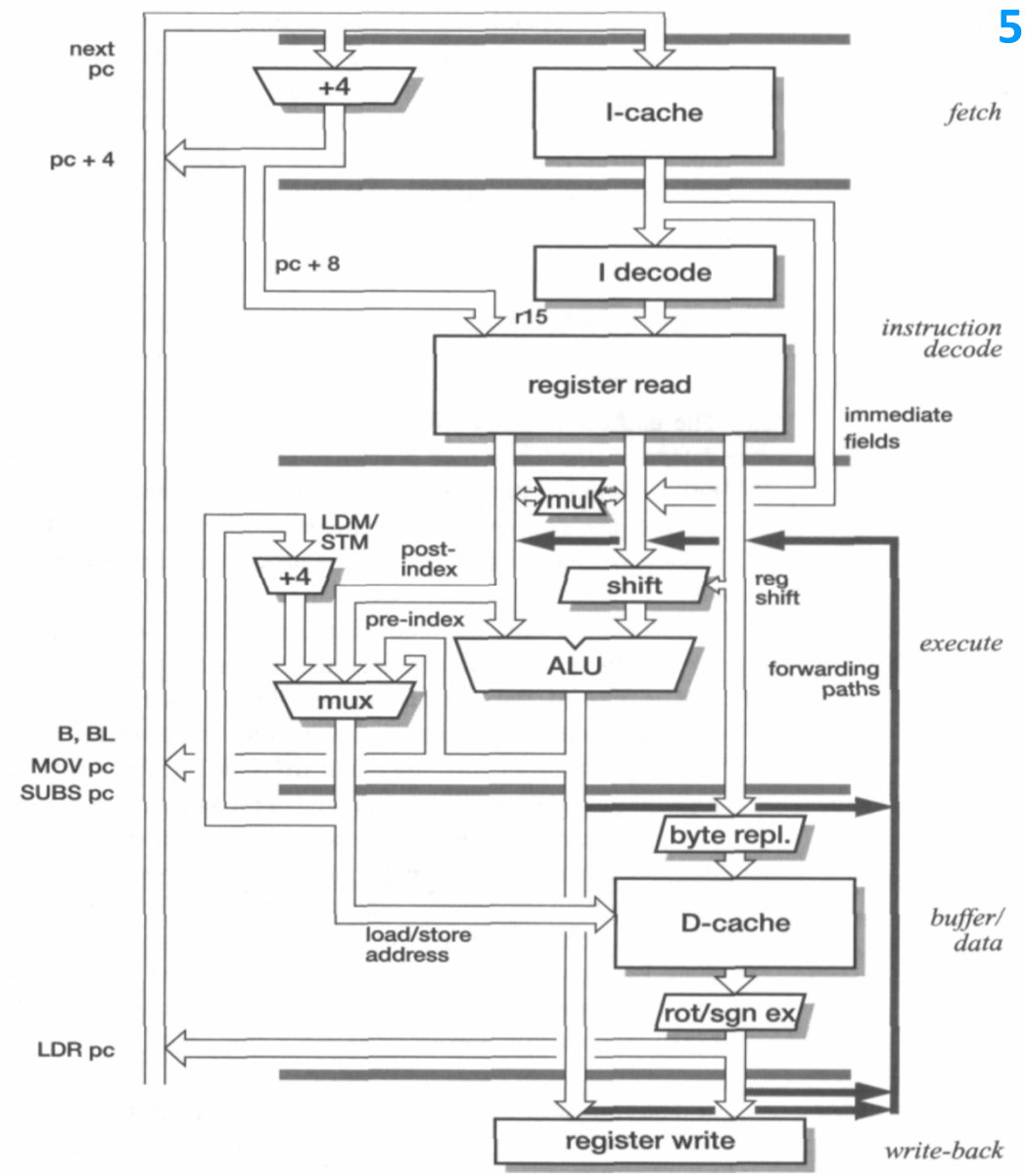
ARM single-cycle instruction 3-stage pipeline operation:



ARM multi-cycle instruction 3-stage pipeline operation:



ARM Organization and Implementation… ARM 9 TDMI



5-stage pipeline ARM organization:

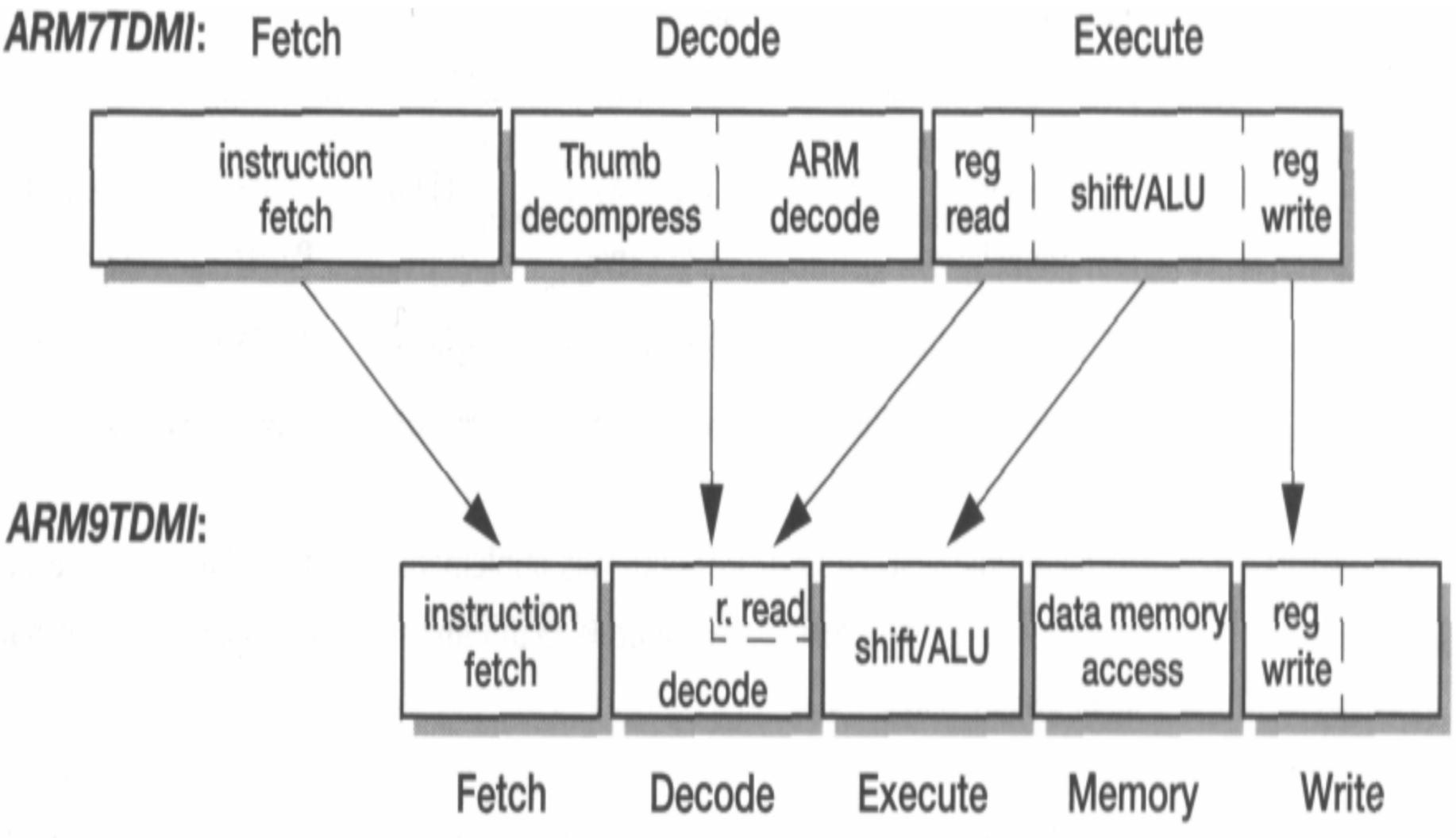
The principal components are:

- ✓The register bank
- ✓The barrel shifter
- ✓The ALU
- ✓Instruction Cache & Data Cache
- ✓Mux, Register write
- ✓Instruction decoder & control logic.

5-stage pipeline stages:

- ✓ Fetch
- ✓ Decode
- ✓ Execute
- ✓ Buffer / Data
- ✓ Write Back

ARM9TDMI…

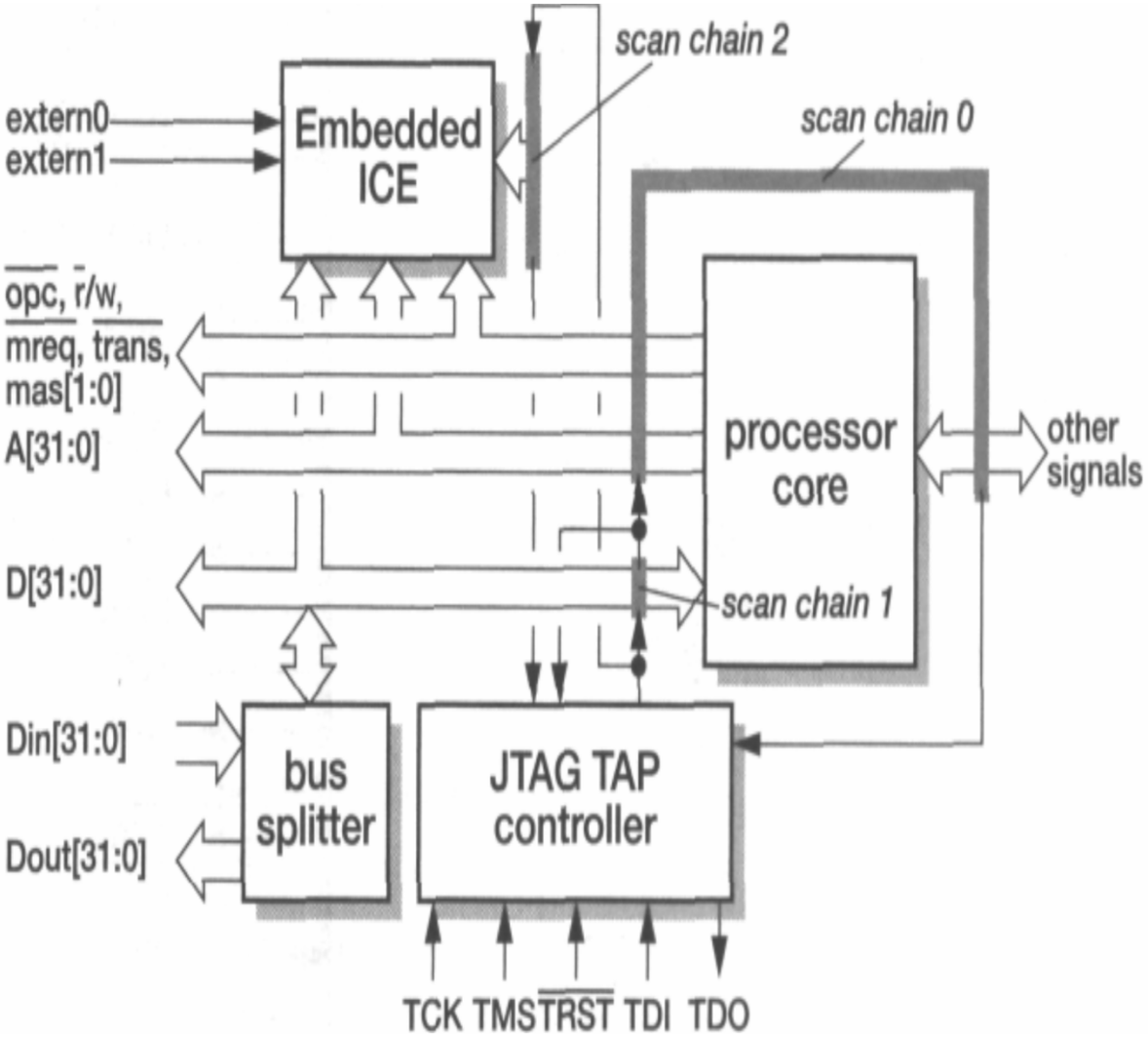


ARM7TDMI and ARM9TDMI pipeline comparison

ARM Processor Cores…

ARM7TDMI…

ARM7TDMI organization:



ARM7TDMI core is a basic ARM integer core using a 3-stage pipeline

It implements ARM architecture version 4T, with support for 64-bit result multi
plies, half-word and signed byte load/store and the Thumb instruction set.

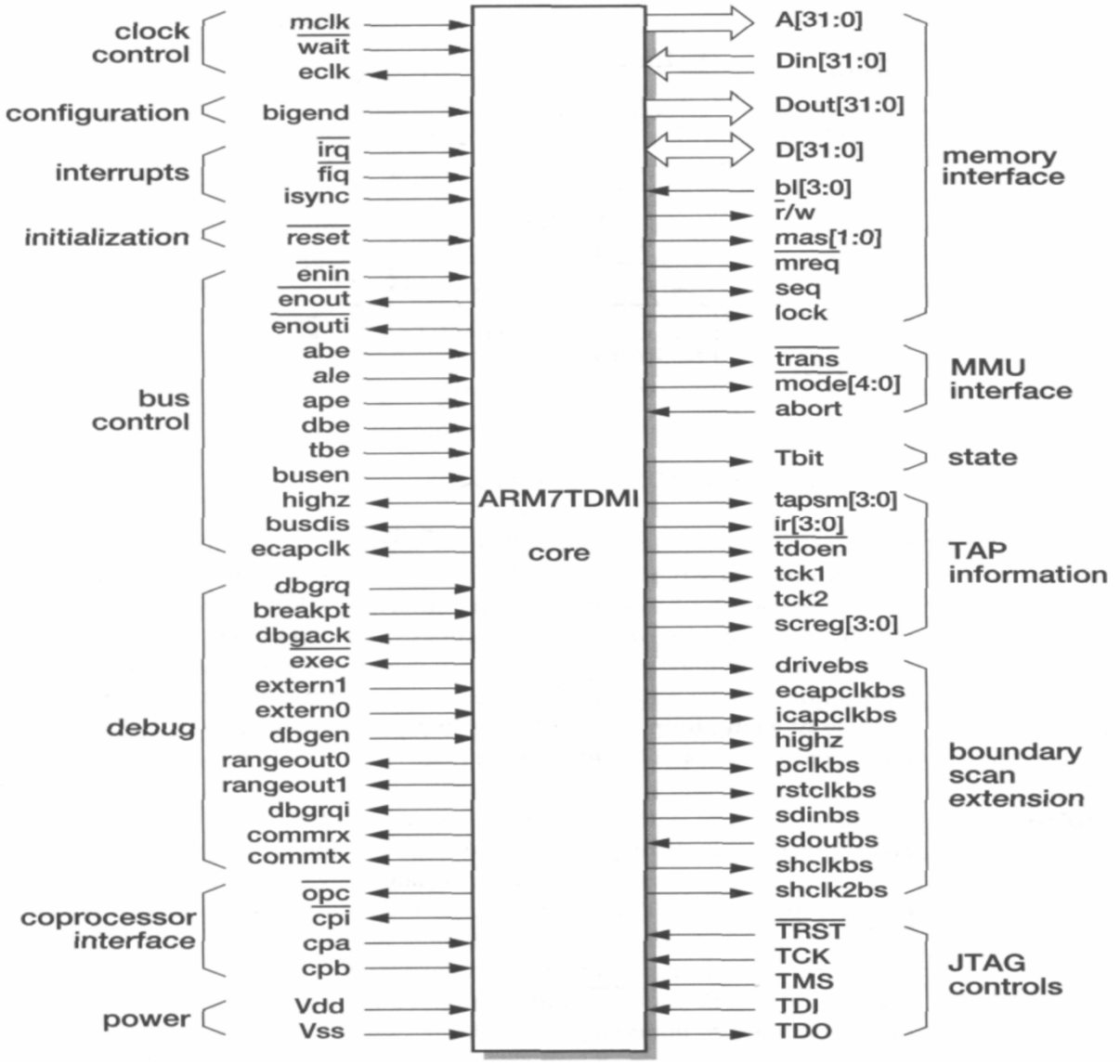
It includes the EmbeddedICE module to support embedded system debugging

ARM Processor Cores…

ARM7TDMI…

Hardware interface:

- Clock control
- Memory interface
- MMU interface
- State - T Bit
- Configuration - Endians
- Interrupts - irq, fiq
- Initialization - reset
- Bus control
- Debug support
- Coprocessor interface
- Power
- JTAG interface



The ARM7TDMI core interface signals

ARM Architecture – From Text book

10.2 | ARM Architecture

With this background, let us get started on the more intricate details of the processor.

10.2.1 | Instruction Set Architecture

It is likely that you have heard the term 'Instruction Set Architecture' (ISA) mentioned in some context or the other. The term implies the user's i.e. the programmer's view of the processor, which constitute the instruction set, addressing modes, registers, etc. ISA is the assembly programmer's or compiler designer's view of the processor. We will base most of our discussions on ARM7 which was the first and still the most popular of the ARM processors. Advanced versions may have more enhancements, but the basic architecture is more or less the same.

10.2.2 | Operating Modes

ARM has seven operating modes which are listed here. It is not important to understand the exact functions of each mode right now. But keep in mind that the user mode corresponds to the simplest mode, with least privileges, but is the mode under which most application programs run. The system mode is a highly privileged mode. This mode is used by operating systems to manipulate and control the activities of the processor. The other modes are entered on the occurrence of exceptions or rather, they are interrupt modes. See the list of the operating modes of ARM.

i) **User**: Unprivileged mode under which most tasks run
ii) **FIQ (Fast Interrupt Request)**: Entered on a high priority (fast) interrupt request
iii) **IRQ (Interrupt Request)**: Entered on a low priority interrupt request
iv) **Supervisor**: Entered on reset and when a software interrupt instruction (SWI) is executed
v) **Abort**: Used to handle memory access violations
vi) **Undef**: Used to handle undefined instructions
vii) **System**: Privileged mode using the same registers as user mode

10.2.3 | Register Set

ARM has 37 registers each of which is 32 bits long. They are listed as follows:

i) 1 dedicated program counter (PC)
ii) 1 dedicated current program status register (CPSR)
iii) 5 dedicated saved program status registers (SPSR)
iv) 30 general purpose registers

ARM Architecture – From Text book

10.2.3.1 | *General Purpose Registers*

There are 30 of them, but they are distributed among different modes.

To understand this feature, see the case of one particular mode, say the user mode. In this mode, the registers act as shown in Table 10.4.

Table 10.4 | Registers in the User Mode

Register Numbers	Designations
R0–R12	General purpose registers
R13	Stack pointer (SP)
R14	Link register (LR)
R15	Program counter (PC)

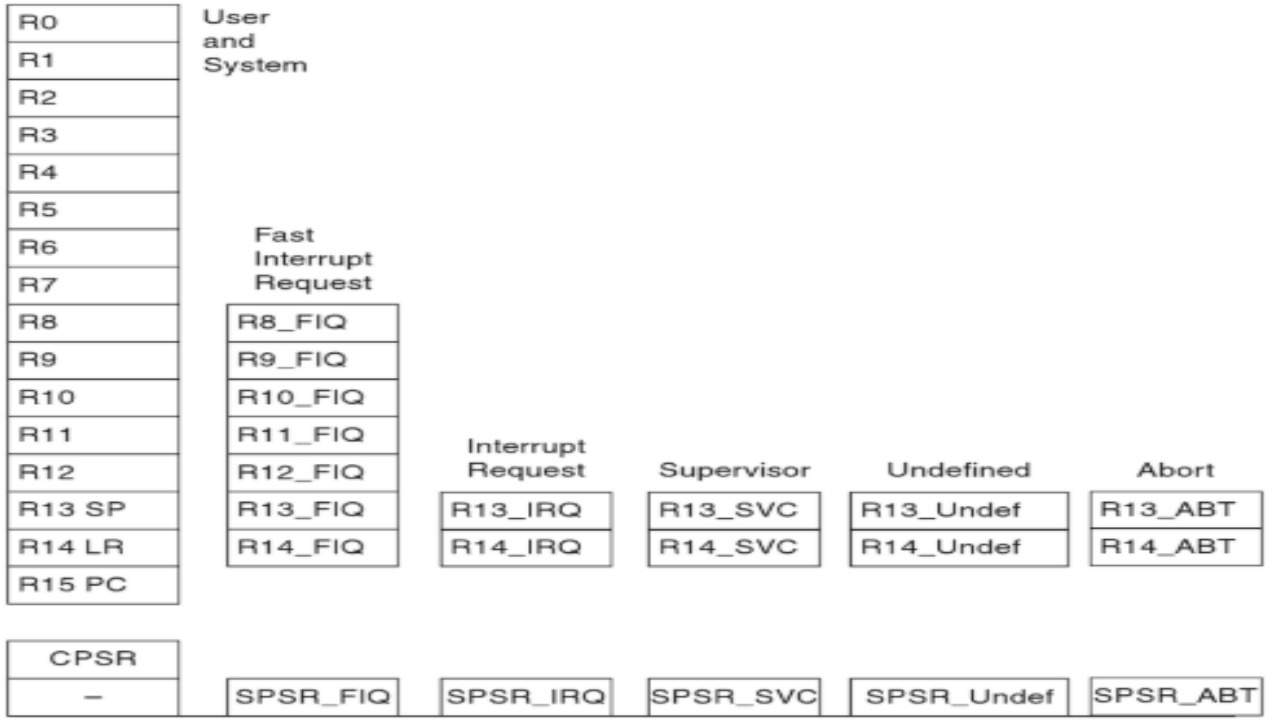


Figure 10.5 | Register set of ARM

ARM Architecture – From Text book

CPSR

The CPSR (Current Program Status Register) is a very important register, and there is only one such register for the processor. Figure 10.6 and Table 10.5 gives its details.

The CPSR contains the information about the current state of the processor. It has bits which specify the mode, control bits to enable/disable interrupts, and also specifies whether the Thumb or ARM mode is currently in use.

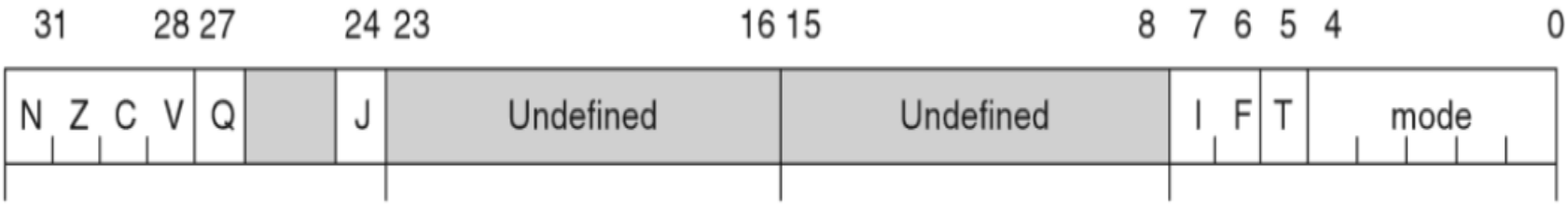


Figure 10.6 | Current Program Status Register (CPSR) bit configuration

Table 10.5 | CPSR Bits

Bit Nos.	Notation	Interpretation
0 to 4	Mode	Specifies the current mode of operation
5	T	Specifies whether in ARM(T =) or Thumb(T = 0) state
6	F	Disables (F = 1)FIQ
7	I	Disables (I = 1)IRQ
8 to 23, 25 to 26	Undefined	
24	J	In Jazelle state (J = 1)
27	Q	Sticky overflow flag
28 to 31	V, C, Z, N	Conditional flags

10.2.5 | Conditional Flags

N: Negative Flag This flag indicates the status of the MSB of the result of an operation. If we are dealing with signed number N = 1 means that the sign bit = 1, which is a negative result.

C: Carry Flag This bit is set if there is an overflow from the MSB of the data being manipulated; this can happen in additions, shifts, rotates etc. It is also set when the result of subtraction is positive. If R1–R2 gives a positive result, C = 1, indicates that R1 is greater than R2. To be precise, let's say that 'A carry occurs if the result of an add, subtract or compare is greater than or equal to 2^{32}, or as the result of an inline barrel shifter operation in a move or logical instruction'.

Z: Zero Flag If the result of an arithmetic or logical operation is zero, then Z = 1.

V: Overflow Flag This is the overflow flag, which is relevant only for signed operations. It indicates that the sign bit has possibly been corrupted because the result has gone out of the range.

Interrupt Vector: Exceptions

Exceptions are usually used to handle unexpected events which arise during the execution of a program, such as interrupts or memory faults. In the ARM architecture the term is also used to cover software interrupts and undefined instruction traps and the system reset function.

ARM exceptions may be considered in three groups:

1. Exceptions generated as the direct effect of executing an instruction

   Software interrupts, undefined instructions and prefetch abort are in this class.

2. Exceptions generated as a side-effect of an instruction

   Data aborts (a memory fault during a load/store) are in this class.

3. Exceptions generated externally, unrelated to the instruction flow

   Reset, IRQ and FIQ fall into this category.

Exceptions…

Exception Entry:

When an exception arises, ARM completes the current instruction and then to handle the exception.

The processor performs the following sequence of actions:

- It changes the operating mode to the corresponding exception.
- It saves the address of the PC (r15) into LR (r14) of the new mode.
- It saves the old value of the CPSR into the SPSR of the new mode.
- It disables IRQs by setting bit 7 of the CPSR and, if the exception is a fast interrupt, disables by setting bit 6 of the CPSR.

Exception Return:

Once the exception has been handled the user task is normally resumed.

- Any modified user registers must be restored from the handler's stack.
- The CPSR must be restored from the appropriate SPSR.
- The PC must be changed back to the relevant instruction address. (R14→ R15)

Exceptions…

Address	Exception	Mode on entry	I state on entry	F state on entry
0x00000000	Reset	Supervisor	Set	Set
0x00000004	Undefined instruction	Undefined	Set	Unchanged
0x00000008	Software interrupt	Supervisor	Set	Unchanged
0x0000000C	Prefetch Abort	Abort	Set	Unchanged
0x00000010	Data Abort	Abort	Set	Unchanged
0x00000014	Reserved	Reserved	-	-
0x00000018	IRQ	IRQ	Set	Unchanged
0x0000001C	FIQ	FIQ	Set	Set

Since multiple exceptions can arise at the same time it is necessary to define a priority order to determine the order in which the exceptions are handled.

1. **Reset (highest priority),**
2. **Data abort,**
3. **FIQ,**
4. **IRQ,**
5. **Prefetch abort,**
6. **SWI, Undefined inst. (lowest priority).**

Programming the ARM:

10.4 | Programming the ARM Processor

Now that we have had a look at the concepts regarding the instruction set architecture (ISA) of ARM, we are in a position to understand it better by programming. Writing, running and testing programs is the key to understanding any processor. By doing programming, we become capable of understanding almost everything about how registers, memory and flags act on data. In short, we get a total feel about the processing activity done inside the processor.

To get to this, we need a programming environment, that is, an Integrated Development Environment (IDE). There are many IDEs available for ARM, some of which are free of cost (and freely downloadable) and some of which are proprietary and thus have to be paid for. However for students, an evaluation version is available which is freely downloadable and available from the website www.keil.com. Here, we will use the Keil IDE also called the RVDK (Real View Development Kit), which is very popular and easy to use. This version can be used for testing programs and for simulation also. We will do all our learning using this IDE. The step-by-step procedure for using this, is detailed in Appendix A. In this part of the chapter, we will assume that you have this IDE and also that you have already browsed through Appendix A.

10.4.1 | Programming—Assembly vs C

Programming can be done in assembly as well in high level languages. In the embedded design world, high level languages are used in product design, and C is a very popular language. As such we will also do C programming (in the next chapter). But before that, let's have a stint in assembly programming. Our approach will be such that to understand the ARM core, that is, to use its registers, do memory access and so on, we will do assembly programming. This ensures that we get a good grip on the ARM core architecture. In this context, it will turn out that we focus on the computational capabilities of the core.

And when we start using ARM as a microcontroller, i.e. the core with a number of peripherals, we use C programming. This will allow us to use the processor in various practical applications involving peripherals and interaction with the external world. This part will be discussed in Chapter 11.

ARM Assembly Language

10.5 | ARM Assembly Language

As mentioned earlier, the ARM instruction set has been cleverly designed to get more than one operation to be done in a single instruction. Let's list out some features of the ARM instruction set.

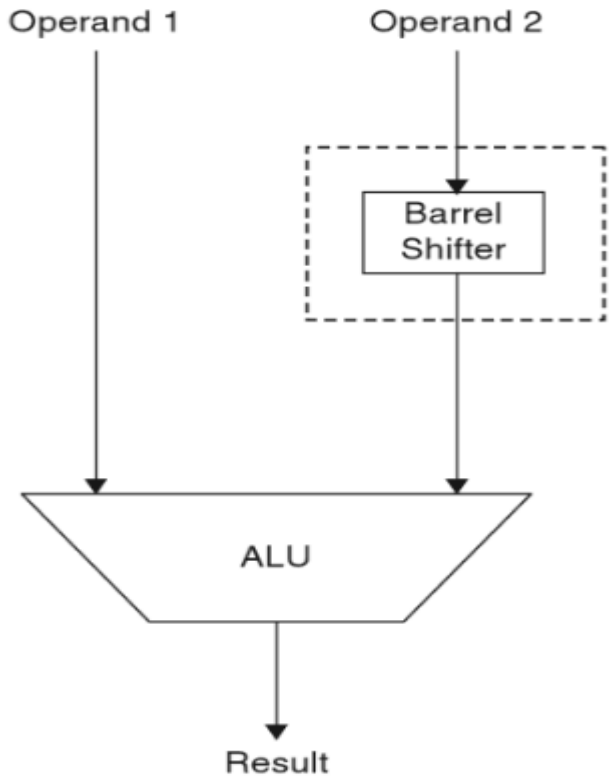


Figure 10.7 | Data processing unit

i) ARM is a RISC processor, in which every instruction has a maximum size of 32 bits. Instructions are expected to be executed in one cycle. This is true for most instructions, but not for all. Therefore it is better to say that ARM is a RISC processor with a few CISC type instructions as well.

ii) Another feature of RISC and therefore of ARM, is that it is a load–store architecture. This means that all computations are register based, that is, the operands are to be brought to registers from memory, using a load instruction. After computation, the result is to be stored in memory. For the user, this means that there is no data processing instructions in which one of the operands is in memory. All operands are to be available in registers before computation can be done.

iii) A third feature of ARM is that its ALU has a barrel shifter (Figure 10.7) associated with one of its operands. A barrel shifter is a unit that can perform more than one bit of shift/rotation, to the right or to the left on an operand. As we will soon see, the barrel shifter adds some clever processing techniques to data processing and allows shifting and an arithmetic operation to be combined in the same instruction.

iv) 'Conditions' can be appended to instructions: this implies that we can choose to 'do or not do' a particular operation based on a status of a condition flag, For most other processors, only branching operations depend on flag status. Here we will see that data movement and data processing instructions can be made 'conditional'.

ARM Assembly Language……

10.5.1 | Data Types

ARM can operate on 32-bit data, which is termed a word, 16-bit data called a half word and also on byte operands. The processing tools offer the option of storing data as 'little endian', or 'big endian'. To clarify this concept, follow the forthcoming discussion, and observe Figure 10.8

Address	Data
0x00001200	A3
0x00001201	90
0x00001202	47
0x00001203	0E

Figure 10.8a | The little endian format

Address	Data
0x00001200	0E
0x00001201	47
0x00001202	90
0x00001203	A3

Figure 10.8b | The big endian format

A 32-bit data stored in memory needs 4 bytes of space which means 4 consecutive addresses are required, as one address can store only one byte. When the lowest byte of the 32-bit word is stored in the lowest of these four addresses, it is called the 'little endian' format. Otherwise, it is the 'big endian' format. See Figure 10.8. The 32-bit data word is 0 = 0xE4790A3. The storage addresses are from 0x00001200 onwards.

In the processor industry, both formats are used. Intel prefers the little endian format, while Motorola uses the big endian format. ARM allows both formats (can be fixed up by software, in the initialization stage). In this book, we assume the little endian format.

ARM Assembly Language……

10.5.2 | Data Alignment

Storing (and loading also) of 4 bytes in memory can be done in one cycle, because the processor has a 32-bit data bus. When 32-bit data is stored in memory, four addresses are needed. But we need to specify only one address in our instruction; but there is an aspect called 'alignment'. For 32-bit data, 'alignment' implies that the last two bits of this address are zero. For example, the address 0x00001200 is an aligned address. When this address is used to store 32-bit data, this address and the next three addresses are automatically accessed. This is because of the way memory is organized, as four banks (see Figure 10.9).

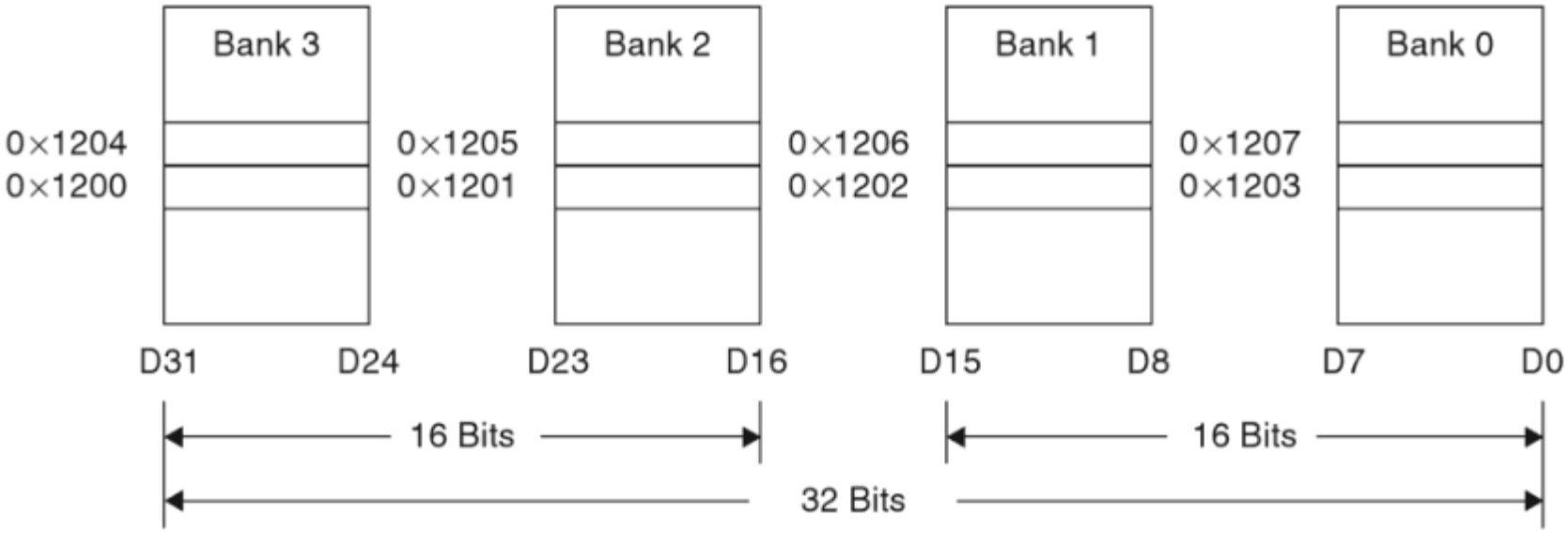


Figure 10.9 | Memory banks

ARM Assembly Language……

If the address of a 32-bit number is given as 0x1200, the accessed addresses are 0x1200, 0x1201, 0x1202 and 0x1203. The 4 bytes in these addresses are considered to be in the same row, that is, aligned. In this case, one byte each from each bank is accessed and only one memory cycle is needed to access an aligned word.

For unaligned data, one more cycle is necessary. Think of the address 0x1201. The locations to be accessed will be 0x1201, 0x1202, 0x1203 and 0x1204. Note that the first three bytes will be in the same row, while the last will be in a different row (bank), and so one more cycle of access will be required.

We summarize the conditions for 'aligned data' as follows:

- For word (32-bit) data, the specified address should have its least significant two bits as 0.
- For half word (16-bit) accesses, the specified address should have the LSB equal to 0.

Most of the tools for ARM ensure that data is stored in aligned locations, so as to avoid unnecessary extra cycles of operation.

10.5.3 | Assembly Language Rules

An assembly language line has four fields, namely, label, opcode, operand and comment. A label is positioned at the left of a line and is the symbol for the memory address which stores that line of information. There are certain rules regarding labels that are allowed under the type of assembler being used. The manual of the specific assembler should be referred, to get this clear. The second field is the opcode or instruction field. The third is the operand field, and the last is the comment field which starts with a semicolon. The use of comments is advised for making programs more readable.

A typical assembly language statement is

```
BOSE    ADD    R1, R2, R3    ; add R2 and R3 and copy the sum to R1.
```

The label is BOSE, the opcode is ADD, the operands are R1, R2 and R3 and the line after the semicolon is the comment. While writing programs, make sure you don't write instructions at the extreme left of the page—that part is the 'label' field in this book. We will use the assembler which is part of the RVDK supplied by Keil. The steps in using it have been clearly described in Appendix A. More details are available in the 'Real view assembly guide'.

ARM Instruction Set:

10.6 | ARM Instruction Set

We will now discuss the ARM instruction set, and gradually move on to writing programs.

The instruction set can be broadly classified as follows:

i) Data processing instructions
ii) Load store instructions—single register, multiple register
iii) Branch instructions
iv) Status register access instructions

The last set moves the contents of the CPSR or an SPSR to or from a general purpose register and are used only in privileged modes. We will discuss the first three sets in detail.

10.6.1 | Data Processing Instructions

ARM is a RISC processor, one of the features of which is that it processes, i.e., performs computations, on data which are in registers only. There are instructions which move data from one register to another. Such instructions have only two operands, that is, the source and the destination. Instructions which perform arithmetic/logical computations have three operands—two source operands and one destination operand.

ARM Instruction Set……

10.6.1.1 | *MOV and MVN*

The 'MOV' instruction is a 'register to register' data movement instruction with the format MOV destination, source where both the source and destination have to be registers.

The mnemonic 'MVN' stands for 'move negated' which implies moving the complemented value of the source to the destination.

Registers R1 to R12 can be used for data movement as they are general purpose registers. The registers R13, R14 and R15, which are the stack pointer, link register and the program counter respectively, can also use the MOV instructions, but this must be done carefully and only for specific purposes.

Examples

```
MOV R11, R2      ;copy the contents of R2 to R11
MOV R12, R10     ;copy the contents of R10 to R12
MVN R0, R9       ;move the complemented value of R9 to R0
                 ;if R9 = 0xFFF00000, R0 = 0x000FFFFF
```

Note Here we have discussed only the case of the MOV instruction used for moving data between registers. The MOV instruction is also used for copying immediate data into registers. That will be discussed in Section 10.17.

ARM Instruction Set……

10.6.1.2 | *The Barrel Shifter*

Now, refer to Figure 10.7. We see that there is a barrel shifter associated with data processing. The figure shows two register operands, one of which can optionally be acted upon by a barrel shifter, before being admitted to the ALU. The barrel shifter can do shifting and rotation. Let us first have a general discussion on shifts and rotations.

10.6.2 | Shift and Rotate

Two types of shifts are possible: logical and arithmetic.

10.6.2.1 | *Logical Shift Left (LSL)*

Logical Shift Left of a (say) 32-bit number causes it to shift left, (a specified number of times) and the vacant bits on the right are filled with zeros. See Figure 10.10. The last bit shifted out from the left is copied to the carry flag. Keep in mind that a left shift by one bit position corresponds to multiplication by 2. An LSL of 5 implies multiplication by 32.

10.6.2.2 | *Logical Shift Right (LSR)*

Logical Shift Right does a similar thing. The vacant bit positions on the left are filled with zeros, and the last bit shifted out is retained in the carry flag. This is shown in Figure 10.11. Shifting right by one, divides the number by 2. Two right shifts cause a division by 4.

10.6.2.3 | *Arithmetic Shift Right (ASR)*

Arithmetic Shift Right is different in the sense that the vacant bit positions on the left are filled with the MSB of the original number. See Figure 10.12. This type of shift has the function of doing 'sign extension' of data, because for positive numbers the MSB is 0, and for negative numbers, the MSB is 1. There is no instruction for arithmetic shift left, because of not having an application for it.

ARM Instruction Set……

10.6.2.4 | *Rotate Right (ROR)*

In this, the data is moved right, and the bits shifted out from the right are inserted back through the left. See Figure 10.13. The last bit rotated out is available in the carry flag. There is no 'rotate left' instruction, because left rotation by n times can be achieved by rotating to the right (32 – n) times. For example, rotating 4 times to the left is achieved by rotating 32 – 4 = 28 times to the right.

10.6.2.5 | *Rotate Right Extended (RRX)*

This corresponds to rotating right through the carry bit, meaning that the bit that drops off from the right side is moved to C and the carry bit enters through the left of the data. This should be obvious from Figure 10.14.

Figure 10.10 | Logical shift left

Figure 10.11 | Logical shift right

Figure 10.12 | Arithmetic shift right

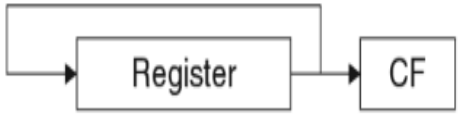


Figure 10.13 | Rotate right

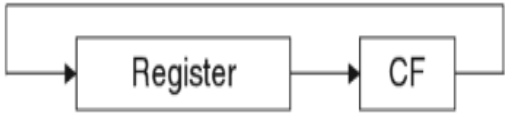


Figure 10.14 | Rotate right extended

ARM Instruction Set……

10.6.3 | Format of Shift and Rotate Instructions

The number of bit positions by which shifts and rotations are to be done may be specified by a constant or may be indicated in another register.

Examples

```
LSL R2, #4      ;shift left logically, the content of R2 by 4 bit positions
ASR R5, #8      ;shift right arithmetically, the content of R2 by 4 bit positions
ROR R1, R2      ;rotate the content of R1, by the number specified in R2
```

Example 10.1

The content of some of the registers are given as:

$$R1 = 0xEF00DE12,\ R2 = 0x0456123F,\ R5 = 4,\ R6 = 28.$$

Find the result (in the destination register), when the following instructions are executed.

i) LSL R1, #8
ii) ASR R1, R5
iii) ROR R2, R6
iv) LSR R2, #5

Solution

i) Shifting R1 left 8 times causes 8 zeros in the 8 positions on the right. R1 now contains 0x00DE1200
ii) R5 contains 4. Arithmetically right shifting R1 4 times, causes the MSB (1, for the given number) to be replicated 4 times on the left, thus causing a sign extension of the shifted number. R1 now contains 0xFEF00DE1.
iii) R6 contains 28. Rotating R2 28 times to the right is equivalent to rotating it 32–28 = 4 times, to the left. After rotation, R6 contains 0x456123F0.
iv) Here, R2 is logically shifted right 5 times, and so 5 zeros enter through the left. R2 now has the value 0x0022B091.

ARM Instruction Set……

10.6.4 | Combining the Operations of Move and Shift

Recollect the barrel shifter which is an integral part of the data processing unit of the processor. This allows shifting and data processing to be done in the same instruction cycle. We will first see how moving and shifting can be combined in one instruction itself.

```
MOV R1, R2, LSL #2
MOV R1, R2, LSR R3
```

In both the above instructions, R1 is the destination register. In the first instruction, the source operand, that is, the content of R2 is logically shifted twice and then moved to the destination register R1. In the second, the amount of 'shifting' is specified in register R3. After the shifting is done, the result is moved to R1.

Example 10.2

Find the content of the destination registers after the execution of each of the given instructions, given that the content of R5 = 0x72340200 and R2 = 4.

i) MOV R3, R5, LSL #3
ii) MOV R6, R5, ASR R2

Solution

The results here are similar to Example 10.1, except that the source and destination registers are not the same after execution of the instructions.

i) MOV R3, R5, LSL #3.
The content of R5 is shifted left 3 times, and moved to R3.
R3 now contains 0x72340200
ii) MOV R6, R5, ASR R2
R2 = 4, and so R5 is arithmetically shifted right 4 times. Since the MSB of the number in R5 is 0, when right shifting, this bit is replicated 4 times at the left of the number. After execution, R6 contains 0x07234020

Classification of Instruction Set:

The ARM and Thumb instruction sets can be broadly classified into the following functional groups.

1. **Branching and Control Instructions:** Instructions like subroutine calls, looping and changing the state between ARM and Thumb fall under this category of instructions.
2. **Register Load and Store instructions:** Loading the values of single registers to and from the memory are covered under this type of instructions. The values may be 32 bit word, a 16-bit half word or an 8 bit unsigned value.
3. **Multiple Register Load and Store Instructions:** Facilitate the to and fro movement between the contents of the multiple registers, used in block operations and stack operations.
4. **Data Processing Instructions:** Operations like addition, subtraction or bitwise logic on the contents of the registers are performed by this type of instructions.
5. **Status Register access Instructions:** These instructions primarily move the contents between the status registers and the GPRs.
6. **Coprocessor Instructions:** These provide a general framework to extend the ARM architectures.

Conditional Execution: Text Book

10.7 | Conditional Execution

ARM has another interesting feature which can be designated as 'conditional execution'. This means that instructions are executed only if a specified condition is true, and here the important thing is that it is not branch instructions alone that are meant—any data processing instruction can be used in this way.

In general, all arithmetic and logic instructions are expected to affect conditional flags. But for ARM, we must suffix the instruction by S for this to happen. Otherwise the flags are unaffected. It is the S suffix on a data processing instruction that causes the flags in the CPSR to be updated.

In Example 10.2, in the instruction MOV R3, R5, LSL #3, there is a logical operation involved, that is, the left shift operation. This should cause the carry flag and N flag to be set. But since the MOV instruction is not appended with the suffix, 'S', the flags remain unaffected, that is, reset. The MOV instruction can be made conditional by writing it as MOVS R3, R5, LSL #3. After this is executed, we find the N and C flags to be set. This flag setting can be used to make an instruction following it, to be 'conditional'. We will soon see more aspects of this.

Figure 10.15 shows the format of a typical ARM instruction. In the instruction code, four bits are allotted for the condition under which the instruction is to be executed. If no condition is indicated, these bits assume the 'always' condition.

Table 10.7 lists the conditions, condition codes and the flag statuses for these conditions. We will discuss the use of condition codes for instructions.

Note that the conditions used for signed numbers and unsigned numbers are different. For unsigned numbers, we use the mnemonic 'higher' or 'lower', while for signed numbers, the conditions are specified as 'greater than' or 'lower than'. The flag settings are also different. The logic of this is very simple, that is, we know that 6 is higher than 3, but -3 is greater than -6. Thus, it is clear that unsigned and signed numbers have to be dealt with differently.

Conditional Execution: Text Book……

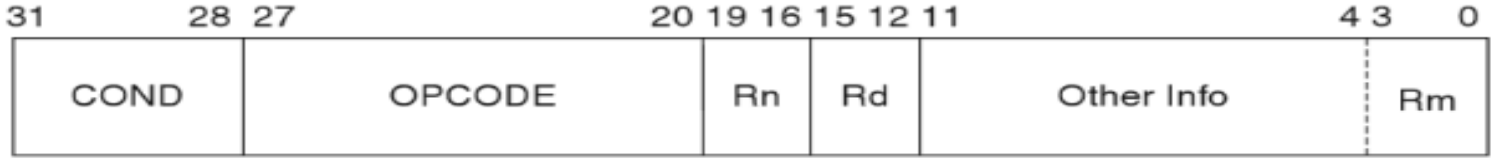


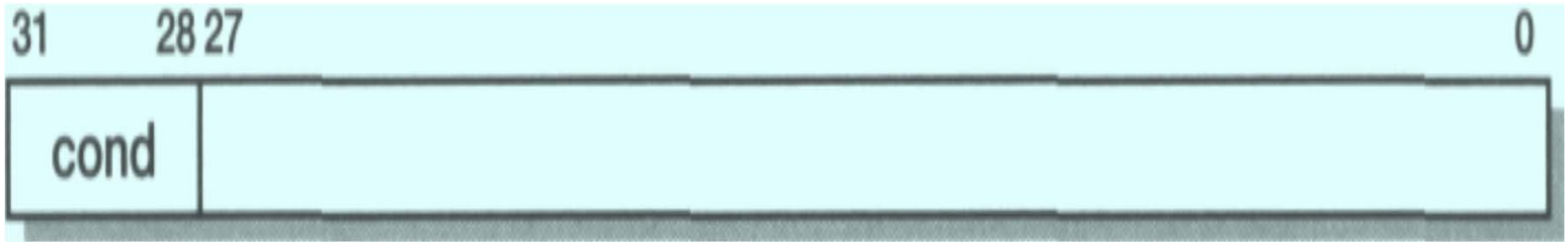
Figure 10.15 | Format of a typical instruction

Table 10.7 | List of Conditions, Codes and Corresponding Flag Status

Cond	Mnemonic	Meaning	Condition Flag State
0000	EQ	Equal	Z = 1
0001	NE	Not Equal	Z = 0
0010	CS/HS	Carry set/unsigned > =	C = 1
0011	CC/LO	Carry clear/unsigned <	C = 0
0100	MI	Minus/Negative	N = 1
0101	PL	Plus/Positive or Zero	N = 0
0110	VS	Overflow	O = 1
0111	VC	No overflow	O = 0
1000	HI	Unsigned higher	C = 1 & Z = 0
1001	LS	Unsigned lower or same	C = 0 | Z = 1
1010	GE	Signed > =	N = = V
1011	LT	Signed <	N! = V
1100	GT	Signed >	Z = = 0, N = = V
1101	LE	Signed < =	Z = = 1 or N! = V
1110	AL	Always	
1111	(NV)	Unpredictable	

Conditional Execution: Reference

All ARM7TDMI instructions can be executed conditionally, based on a 4-bit condition field in the instruction. The processor tests the state of the condition flags in the CPSR (N, Z, V, C), and if the condition flag state matches the condition, the instruction executes normally. If the condition flag state does not match the condition, the instruction is executed as a NOP (no operation).



Conditional Execution…

Condition Codes

Opcode [31:28]	Mnemonic Extension	Meaning	Condition flag state
0000	EQ	Equal	Z==1
0001	NE	Not equal	Z==0
0010	CS/HS	Carry set / unsigned higher or same	C==1
0011	CC/LO	Carry clear / unsigned lower	C==0
0100	MI	Minus / negative	N==1
0101	PL	Plus / positive or zero	N==0
0110	VS	Overflow	V==1
0111	VC	No overflow	V==0
1000	HI	Unsigned higher	(C==1) AND (Z==0)
1001	LS	Unsigned lower or same	(C==0) OR (Z==1)
1010	GE	Signed greater than or equal	N == V
1011	LT	Signed less than	N != V
1100	GT	Signed greater than	(Z==0) AND (N==V)
1101	LE	Signed less than or equal	(Z==1) OR (N!=V)
1110	AL	Always (unconditional)	Not applicable
1111	(NV)	Never	Obsolete, unpredictable in ARM7TDMI

Ex: BEQ <target Address>

It checks the zero flag if ZF==1, then it goes to the target address otherwise it executes the next instruction.

- If the condition is omitted in instructions, the AL (always) condition is used to specify that the instruction should always execute.

Arithmetic Instructions:

10.8 | Arithmetic Instructions

Now let's get a feel of the arithmetic instructions of ARM and the special ways in which they can be used.

10.8.1 | Addition and Subtraction

Addition and subtraction are three operand instructions. The destination is always a register. The source operands may both be registers or one of them may be an immediate data. There are some issues in using immediate data greater than 8 bits (Ref Section 10.17).

See Table 10.8 which gives examples of how the different addition and subtraction instructions work. Any of the general purpose registers may be used as operands, though in the table, only R3, R4 and R5 have been mentioned.

Table 10.8 | List of Arithmetic Instructions

Instruction	Operation	Calculation
ADD R3, R4, R5	Add	R3 = R4 + R5
ADC R3, R4, R5	Add with carry	R3 = R4 + R5 + C
SUB R3, R4, R5	Subtract	R3 = R4 – R5
SBC R3, R4, R5	Subtract with carry	R3 = R4 – R5 – C
RSB R3, R4, R5	Reverse subtract	R3 = R5 – R4
RSC R3, R4, R5	Reverse subtract with carry	R3 = R5 – R4 – C

Arithmetic Instructions: Text Book……

Remember the concept of suffixing data processing instructions. This can be used ingenuously for making operations conditional. For example, the add instructions (just as any other data processing instruction) does not affect the conditional flags unless it is suffixed by S. Following such an ADD instructions, we can have instructions with conditions appended to it. The set of possible conditions are listed in Table. 10.7. For any instruction, the upper 4 bits are used to specify the condition (Figure 10.15).

Consider these program lines

```
SUBS R1, R2, R3      ;the suffix 'S' has been used
MOVEQ R2, R1         ;the EQ notation tests the Z = 1 condition
```

Here the move instruction is executed only if the result of the subtraction produces a zero and sets the zero flag. The condition EQ implies the setting of the zero flag (Refer Table 10.7)). Let's use this concept in a simple example.

Arithmetic Instructions: Text Book……

Example 10.3

It is required to compare two numbers which are in registers R1 and R2. The bigger number is to be placed in R10. If the two numbers are equal, then the number is to be moved to R9.

Solution

Here we use the subtraction operation to do the comparison.

```
SUBS R3, R1, R2      ;R3 = R1 – R2
MOVEQ R9, R1         ;If R1 and R2 are equal (Z = 1) move R1 to R9
MOVHI R10, R1        ;if R1>R2, C = 1, R1 is moved to R10
MOV R10, R2          ;otherwise move R2 to R10
```

The salient points of this program are as follows:

i) First the operation, R1-R2 is performed and the result is placed in R3.
ii) Since the SUB instruction has been appended with S, the flags will be set accordingly.
iii) If the two numbers are equal, the zero flag gets set and the instruction MOVEQ will get executed. Otherwise it becomes a NOP (no operation) instruction. Here one of the numbers (R1) is to moved to R9 (as both numbers are equal).
iv) The next line checks whether the carry flag has been set. If R1>R2, the carry flag is set (C = 1) and the MOVHI (move if high) instruction gets executed. Otherwise this also becomes a NOP. The move instruction gets the bigger number into R10.
v) If the carry flag is not set, and the Z flag is also not set, it means that R2 is bigger. This is moved to R10.

Arithmetic Instructions: Text Book……

Example 10.4

Find the result of the following instructions. What do these instructions accomplish?

i) ADD R1, R2, R2, LSL #3
ii) RSB R3, R3, R3, LSL #3
iii) RSB R3, R2, R2, LSL #4
iv) SUB R0, R0, R0, LSL #2
v) RSB R2, R1, #0

Solution

i) ADD R1, R2, R2, LSL #3
One source operand is R2, LSL #3. Left shifting 3 times accomplishes multiplication by $2^3 = 8$
The result of the whole operation is R1 = R2 + 8R2 = 9R2

ii) RSB R3, R3, R3, LSL #3
R3 = 8R3 – R3 = 7 R3

iii) RSB R3, R2, R2, LSL #4
R3 = 16R2 – R2 = 15R2

iv) SUB R0, R0, R0 LSL #2
R0 = R0 – 4R0 = -3R0

v) RSB R2, R1, #0
We get R2 = 0 – R1 = -R1. i.e., we get the negative value of R1

Logical Instructions:

10.9 | Logical Instructions

Now, we will see the logical instructions of the processor. They also need to be suffixed with 'S' to have the flags updated. See Table 10.9.

Table 10.9 | List of Logical Instructions

Instruction	Operation	Logical Result
AND R3, R4, R5	Logical AND of 32 bit values	R3 = R4 AND R5
ORR R3, R4, R5	Logical OR of 32 bit values	R3 = R4 OR R5
EOR R3, R4, R5	Logical XOR of 32 bit values	R3 = R4 XOR R5
BIC R3, R4, R5	Logical bit clear	R3 = R4 (AND NOT) R5

Logical Instructions: Text Book……

Example 10.5

Given the contents of R3 and R4 as, R3 = 0x0FF00FF0, R4 = 0x0FF00FF0. and R0 = 0.
Find the values in R1, R2 and R5 at the end of the sequence of instructions shown.

i) EORS R1, R3, R4
ii) ANDS R5, R3,

Solution

The content of the destination register and the affected flag is shown alongside the executed instruction

i) EORS R1, R3, R4 ;R1 = 0x00000000, Z = 1
ii) ANDS R5, R3, R0 ;R5 = 0x00000000 Z = 1

Note One of the source operands may be 8-bit immediate data as well. Refer to Section 10.17 for details of how to handle data bigger than 8 bits.

Compare Instructions:

10.10 | Compare Instructions

This instruction compares two operands and causes the conditional flags to be affected, but neither the destination nor the source changes. Comparison is done by a subtraction operation, and the flags are set/reset according to the result of this. (ARM has four types of compare instructions as shown in Table 10.10). However, only two flags really matter and they are the zero flag and the carry flag. Refer to Table 10.11 to get an idea of the flag settings after a compare instruction.

Note Since the compare instructions explicitly affect the flags, the suffix S is not required for them.

Comparison is a very important operation, and we will use it very frequently. A number of programs using this instruction will be discussed subsequently.

Table 10.10 | List of 'Compare' Instructions

CMP R3, R4	Compare	R3 – R4, but only flags affected
CMN R3, R4	Compare negated	R3 + R4, but only flags affected
TST R3, R4	Test	R3 AND R4 but only flags affected
TEQ R3, R4	Test Equivalence	**R3 XOR R4** but only flags affected

Compare Instructions: Text Book……

Table 10.11 | Flag Settings After a Compare Instruction

If	C	Z
R3 > R4	1	0
R3 < R4	0	0
R3 = R4	1	1

What Is the use of the TST instruction?

TST is an instruction similar to compare, but it does ANDing and then sets conditional flags. If the result of ANDing is a zero, the Z flag is set. It can be used to verify if at least one of the bits of a data word is set or not. For that, 'test' the number with another one in which the required bit position has a '1'. For example, let's say we need to know if the LSB of the content of R1 is set or not. Use the instruction TST R1, #01 and verify the status of the Z flag. If Z = 1, it implies that the LSB of R1 is not set, because the AND operation for that bit, has produced a 0, not a 1.

What is the use of the TEQ instruction?

TEQ does exclusive ORing which tests for equality. If both the operands are equal, the Z flag is set. It verifies if the value in a register is equal to a specified number. The instruction TEQ R1, #45 verifies whether the content of R1 is 45.

Data Processing Instructions: Reference

The ARM data processing instructions are used to modify data values in registers. The operations that are supported include arithmetic and bit-wise logical combinations of 32-bit data types. One operand may be shifted or rotated *en route* to the ALU, for example, shift and add in a single instruction.

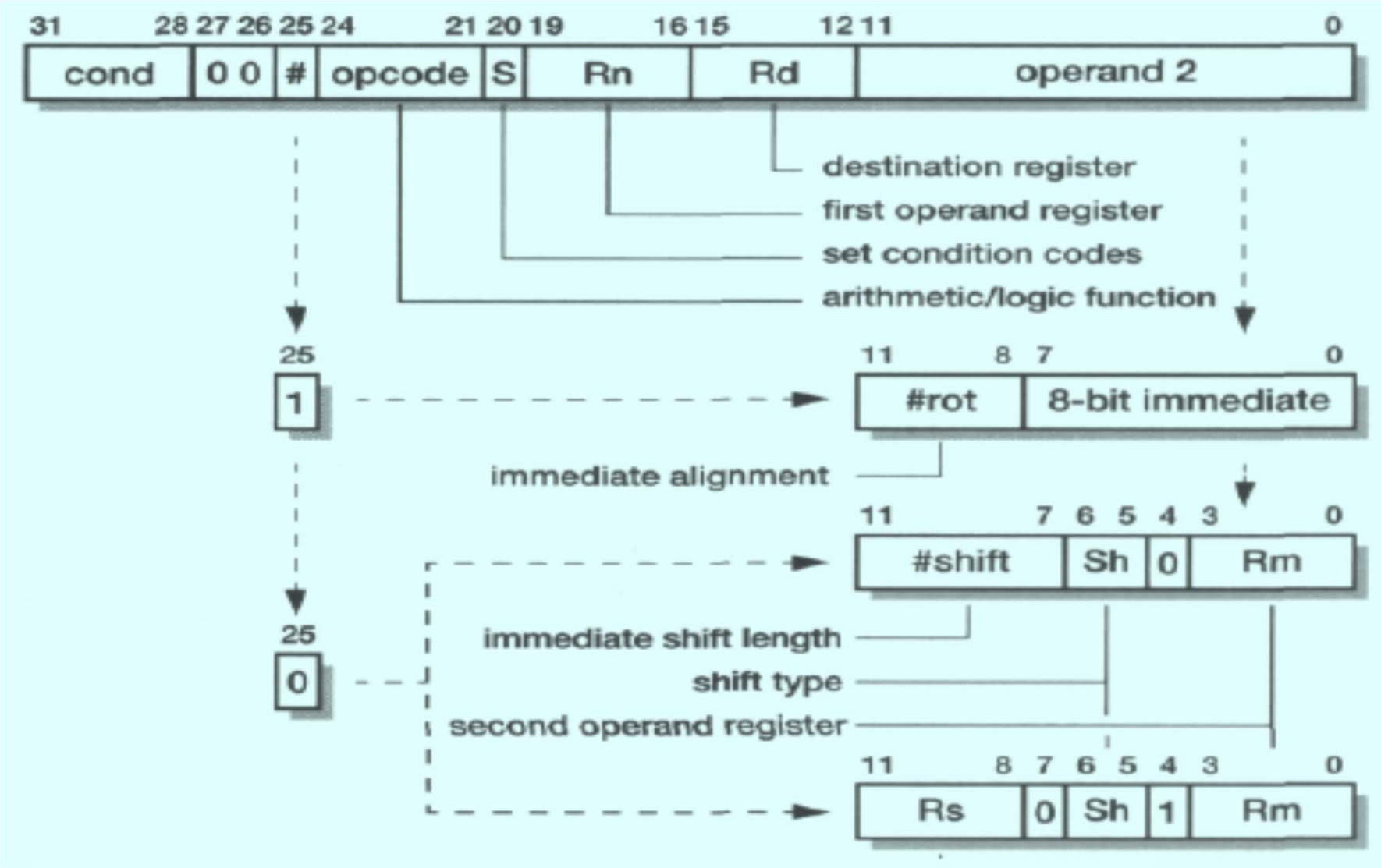
Syntax: **opcode {s} {cond} Rd, Rm, operand2**

The ARM data processing instructions employ a 3-address format, which means that the two source operands and the destination register are specified independently. One source operand is always a register; the second may be a register, a shifted register or an immediate value.

When the instruction does not require all the available operands
(for instance MOV ignores Rm and CMP ignores Rd) the unused register field should be set to zero. The assembler will do this automatically.

Data Processing Instructions…

Binary Encoding:



Data Processing Instructions…

Opcode 124:21)	Mnemonic	Meaning	Effect
0000	AND	Logical bit-wise AND	Rd:=RnANDOp2
0001	EOR	Logical bit-wise exclusive OR	Rd := Rn EOR Op2
0010	SUB	Subtract	Rd := Rn - Op2
0011	RSB	Reverse subtract	Rd := Op2 - Rn
0100	ADD	Add	Rd := Rn + Op2
0101	ADC	Add with carry	Rd := Rn + Op2 + C
0110	SBC	Subtract with carry	Rd := Rn - Op2 + C - 1
0111	RSC	Reverse subtract with carry	Rd := Op2 - Rn + C - 1
1000	TST	Test	SccnRnANDOp2
1001	TEQ	Test equivalence	Sec on Rn EOR Op2
1010	CMP	Compare	Sec on Rn - Op2
1011	CMN	Compare negated	Sec on Rn + Op2
1100	ORR	Logical bit-wise OR	Rd := Rn OR Op2
1101	MOV	Move	Rd := Op2
1110	BIC	Bit clear	Rd:=RnANDNOTOp2
1111	MVN	Move negated	Rd:=NOTOp2

Data Processing Instructions…

These instructions allow direct control of whether or not the processor's condition codes are affected by their execution through the S bit (bit 20).

- The N flag is set if the result is negative, otherwise it is cleared.
- The Z flag is set if the result is zero, otherwise it is cleared.
- The C flag is set to the carry-out from the ALU when the operation is arithmetic
- The V flag is set if there is an overflow from bit 30 to bit 31.

Ex.1:

A subroutine to multiply r0 by 10:

```
        MOV     r0, #3
        BL      TIMES10
        ..
TIMES10 MOV     r0, r0, LSL #1     ; x 2
        ADD     r0, r0, r0, LSL #2 ; x 5
        MOV     pc, r14            ; return
```

To add a 64-bit integer in r0, r1 to one in r2, r3:

```
        ADDS    r2, r2, r0         ; add lower, save carry
        ADC     r3, r3, r1         ; add higher and carry
```

Ex.2:
SUB r0,r1,r2 ; Subtract
R0 = r1 – r2
Ex.3:
RSB r0,r1,r2 ; Reverse Subtract
R0 = r2 – r1
Ex.4:
AND r0,r1,r2 ; Logical AND
Ex.5:
ORR r0,r1,r2 ; Logical OR

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THANK YOU...