Micro Processors & Interfacing

16CS307

Unit- 4

Lec-2

Mr. M Krishna Chennakesava Rao,

Asst. Professor, Dept. of ECE,

VFSTR University

1

8051-Addressing Modes

➢ An Addressing Mode indicates how the data is represented in the instruction.

➢ 8051 supports 6 types of Addressing Modes.

1. Immediate Addressing mode

2. Register Addressing Mode

3. Register Indirect Addressing Mode

4. Direct Addressing Mode

5. Indexed Addressing Mode

6. Implicit Addressing Mode

8051-Addressing Modes cont'd…

1. Immediate Addressing Mode: -

✓ The **data is directly placed** in the source operand field of the instruction,

✓ '#' symbol must prefix for the data.

Ex: -   MOV A, #38H
          ADD A, #67H

8051-Addressing Modes cont'd...

Immediate Mode – specify data by its value

```
mov A, #0          ;put 0 in the accumulator
                   ;A = 00000000

mov R4, #11h       ;put 11hex in the R4 register
                   ;R4 = 00010001

mov B, #11         ;put 11 decimal in B register
                   ;B = 00001011

mov DPTR,#7521h    ;put 7521 hex in DPTR
                   ;DPTR = 0111010100100001
```

8051-Addressing Modes cont'd...

Immediate Mode – continue

```
        MOV DPTR,#7521h
        MOV DPL,#21H
        MOV DPH, #75
```

```
        COUNT EGU 30
         ~
         ~
        mov R4, #COUNT
```

```
        MOV DPTR,#MYDATA
        ~
        ~
        0RG 200H
MYDATA:DB "IRAN"
```

8051-Addressing Modes cont'd...

2. Register Addressing Mode: -

✓ The **data is placed** in the source operand field of the instruction **through a GPR** (General Purpose Register).

✓ **Either source or destination is one of CPU register**

- EX: -   MOV A, B

         ADD   A, R0

> **CPU Registers**
>
> **A,B,SP,DPTR**

Addressing Modes

Register Addressing – either source or destination is one of CPU register

```
MOV R0,A
MOV A,R7
ADD A,R4
ADD A,R7
MOV DPTR,#25F5H
MOV R5,DPL
MOV R6,DPH
```

Note that MOV R4,R7 is incorrect

8051-Addressing Modes cont'd...

3. Register Indirect Addressing Mode: -

✓ The **address of the data is indirectly specified** in the operand field of the instruction **through a GPR** (General Purpose Register) R0 or R1.

✓ The address register for 16-bit addresses can only be a DPTR

- Ex: -   MOV A, @R0

          ADD   A, @R1

          MOV DPTR, #9000H   ; DPTR ← 9000h

          MOVX A, @DPTR   ; A ← M[9000]

8051-Addressing Modes cont'd...

<u>Register Indirect</u> – the address of the source or destination is specified in registers

Uses registers R0 or R1 for 8-bit address:
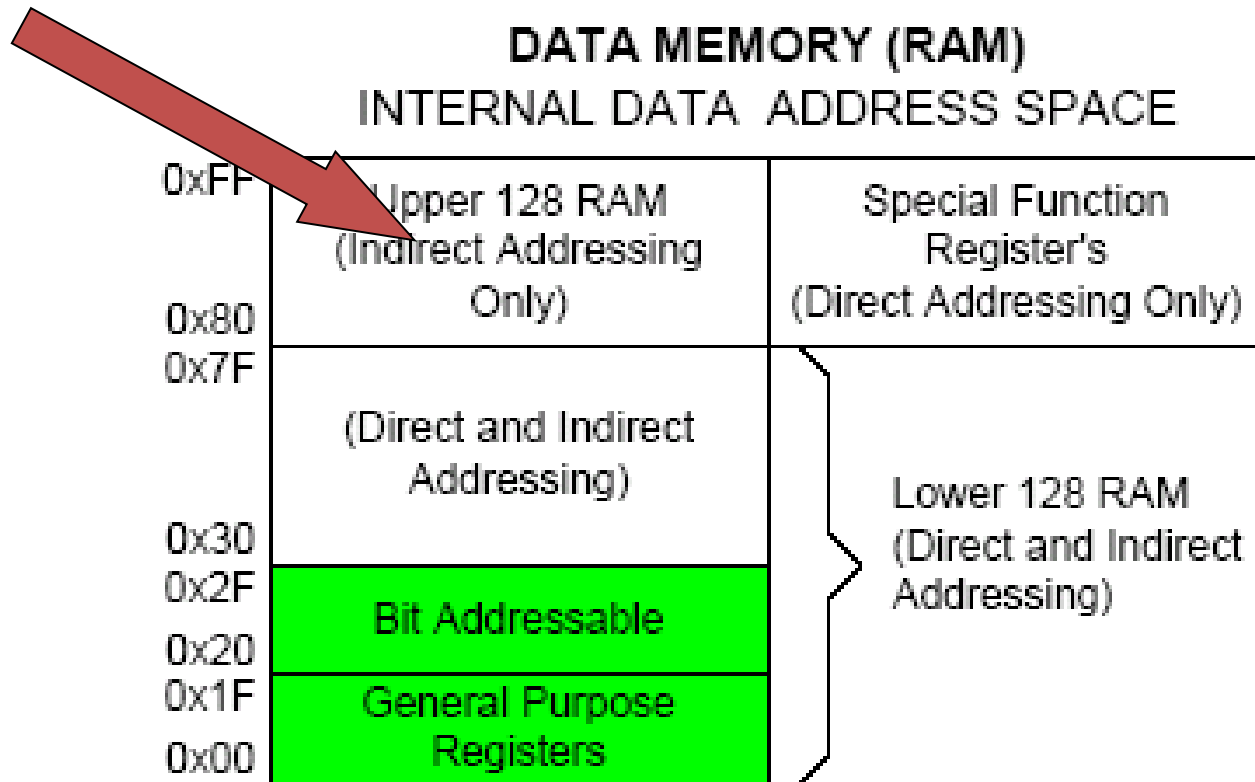
```
mov psw, #0          ; use register bank 0
mov r0, #0x3C
mov @r0, #3          ; memory at 3C gets #3
                     ; M[3C] ← 3
```

Uses DPTR register for 16-bit addresses:

```
mov dptr, #0x9000    ; dptr ← 9000h
movx a, @dptr        ; a ← M[9000]
```

Note that 9000 is an address in external memory

Use Register Indirect to access upper RAM block (+8052)

DATA MEMORY (RAM)
INTERNAL DATA ADDRESS SPACE

0xFF Upper 128 RAM (Indirect Addressing Only) 0x80	Special Function Register's (Direct Addressing Only)
0x7F (Direct and Indirect Addressing) 0x30	Lower 128 RAM (Direct and Indirect Addressing)
0x2F Bit Addressable 0x20	
0x1F General Purpose Registers 0x00	

8051-Addressing Modes cont'd...

4. Direct Addressing Mode: -

✓ The **address of the data is directly placed** in the operand field of the instruction.

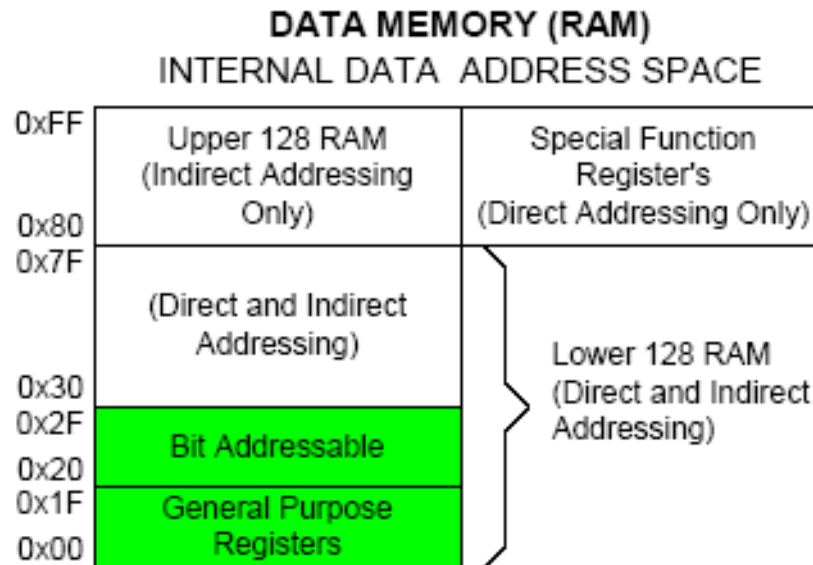✓ The address is the internal RAM or internal SFR (Special Function Register).

- Ex: -   MOV   A, 20H

            MOV R1, 70H

8051-Addressing Modes cont'd...

Direct Mode – specify data by its 8-bit address

Usually for 30h-7Fh of RAM

```
Mov a, 70h          ; copy contents of RAM at 70h to a
Mov R0,40h          ; copy contents of RAM at 40h to a
Mov 56h,a           ; put contents of a at 56h
Mov 0D0h,a          ; put contents of a into PSW
```

DATA MEMORY (RAM)

INTERNAL DATA ADDRESS SPACE

0xFF	Upper 128 RAM (Indirect Addressing Only)	Special Function Register's (Direct Addressing Only)
0x80		
0x7F	(Direct and Indirect Addressing)	
0x30		Lower 128 RAM (Direct and Indirect Addressing)
0x2F	Bit Addressable	
0x20		
0x1F	General Purpose Registers	
0x00		

8051-Addressing Modes cont'd...

Direct Mode – play with R0-R7 by direct address

```
MOV A,4   ≡   MOV A,R4


MOV A,7   ≡   MOV A,R7


MOV 7,2   ≡   MOV R7,R6    ✗

MOV R2,#5   ;Put 5 in R2
MOV R2,5    ;Put content of RAM at 5 in R2
```

8051-Addressing Modes cont'd...

5. Indexed Addressing Mode: -

✓ The **address of the data** is indirectly placed in the operand field of the instruction through combination 'A' register PC or DPTR.

✓ Only Program memory can be accessed using this AM.

✓ This 8051-AM is used for look table manipulations.

- Ex: - MOVC A, @A+DPTR

  MOVC A, @A+PC

8051-Addressing Modes cont'd...

Register Indexed Mode – source or destination address is the sum of the base address and the accumulator(Index)

- Base address can be DPTR or PC

```
mov dptr, #4000h
mov a, #5
movc a, @a + dptr   ;a ← M[4005]
```

8051-Addressing Modes cont'd...

6. Implied Addressing Mode: -

✓ The operand is implicitly represented in the operation code of the instruction.

• Ex: - NOP,   RET,   RETI