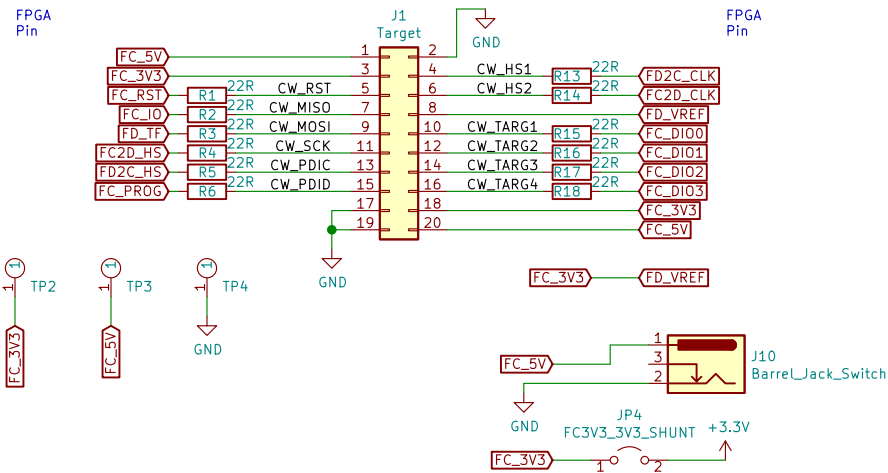
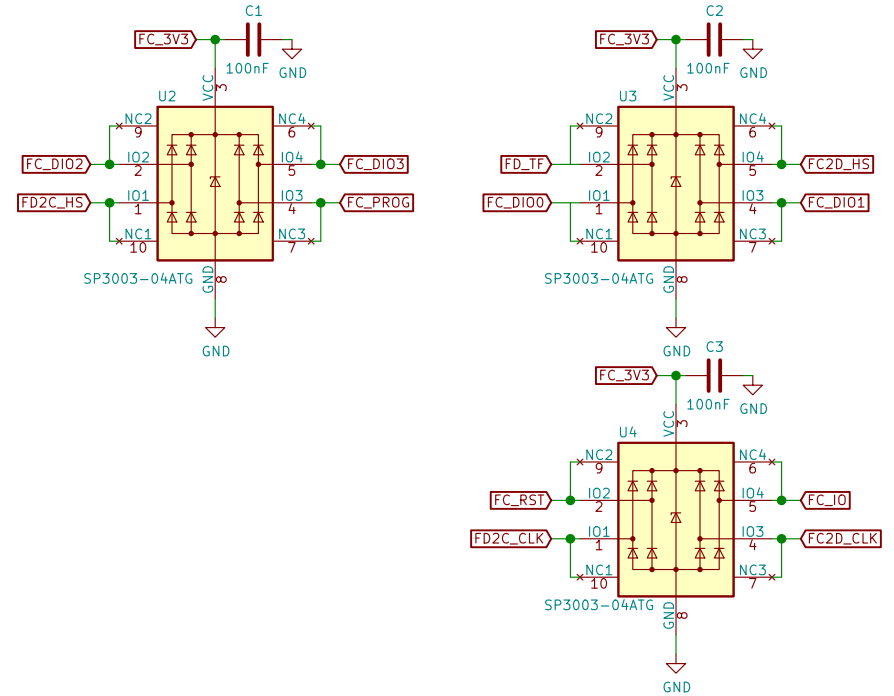


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A	<div>Sheet: Connectors_ IO</div> <div>File: target.sch</div>		<div>Sheet: Power</div> <div>File: power.sch</div>			
B	<div>Sheet: FPGA Power and Programming</div> <div>File: fpgaprogram.sch</div>		<div>Sheet: FPGA 1</div> <div>File: fpga 1.sch</div>			
C	<div>Sheet: User Button and IO</div> <div>File: User Button and IO.sch</div>		<div>Sheet: FPGA 2</div> <div>File: FPGA 2.sch</div>			
D	<div> <div>H1</div> <div>H2</div> <div>H3</div> <div>H4</div> <div>MountingHoleMountingHoleMountingHoleMountingHole</div> </div>			<div> <div>cerg:cerg</div> <div>CERG-Logo</div> <div></div> </div>		<div> <div>Project: FOBOS Artix-7 a12t DUT</div> <div>Author: Jens-Peter Kaps</div> <div>Copyright © Cryptographic Engineering Research Group</div> <div>License: Apache License Version 2.0</div> <div>Cryptographic Engineering Research Group</div> <div>Sheet: /</div> <div>File: dut-artix7-a12t.sch</div> <div> <div>Title: FOBOS Artix-7 a12t DUT</div> <div> <div>Size: USLetter</div> <div>Date: 2020-07-28</div> </div> <div> <div>KiCad E.D.A. kicad (5.1.7)-1</div> <div> <div>Rev: 1.0</div> <div>Id: 1/7</div> </div> </div> </div> </div>
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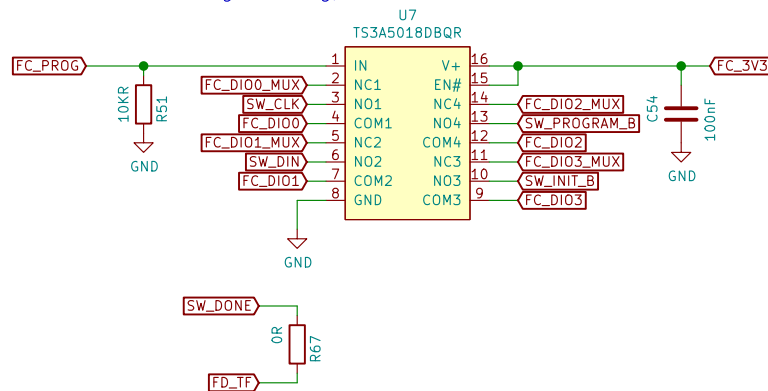
FOBOS Target Connector



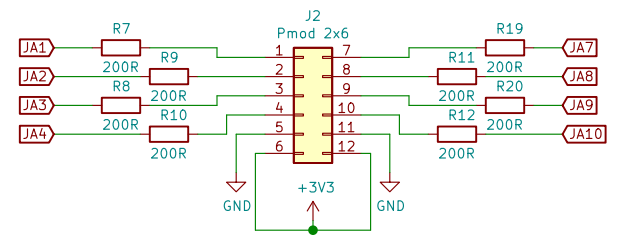
ESD Protection



Programming/DUT Communication Switches



PMOD Connector



Make footprint compatible with Digilent inc PMOD standard

cerg:cerg_logo
CERG-Logo

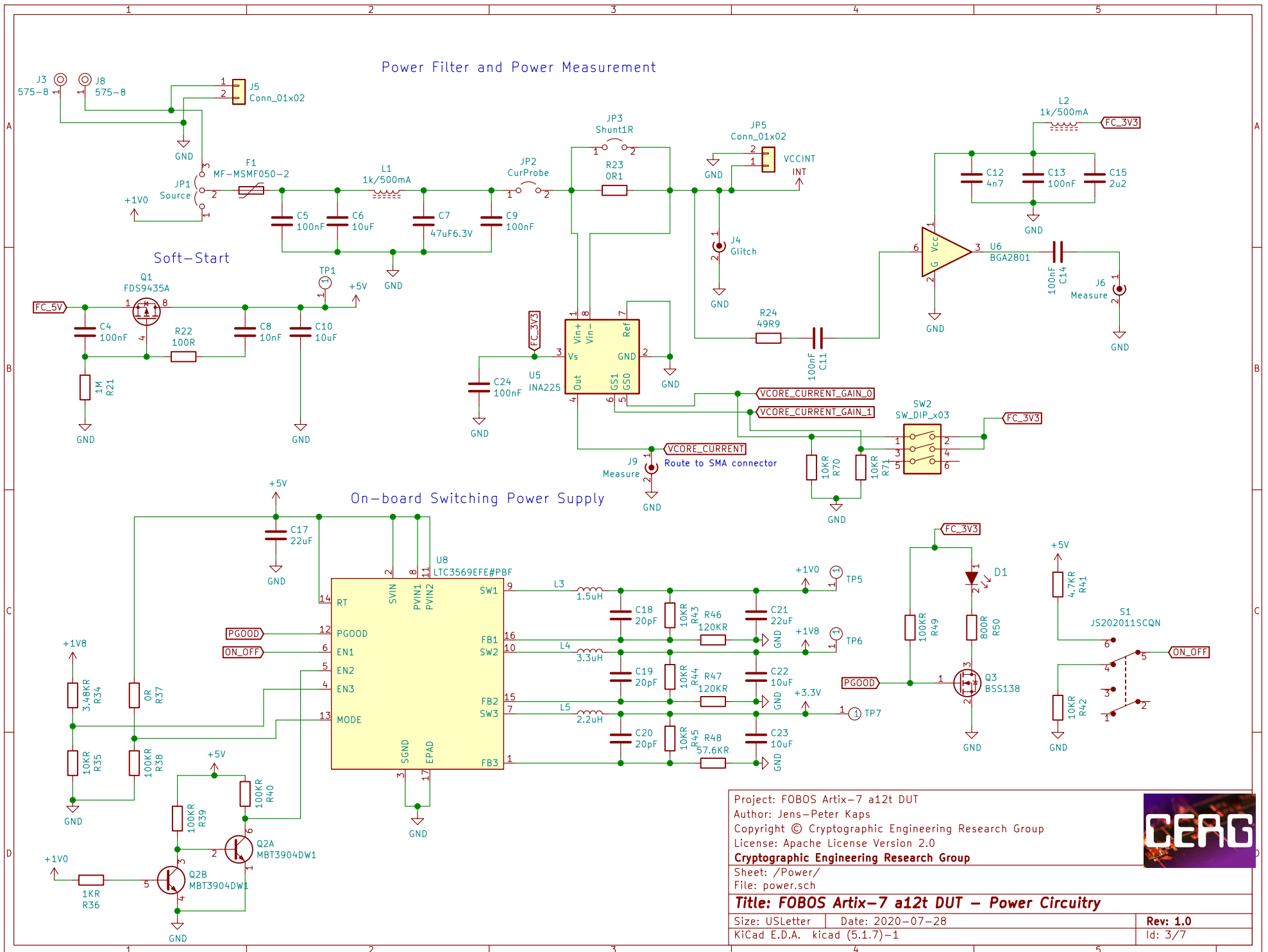
Project: FOBOS Artix-7 a12t DUT
Author: Jens-Peter Kaps
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Sheet: /Connectors, IO/
File: target.sch



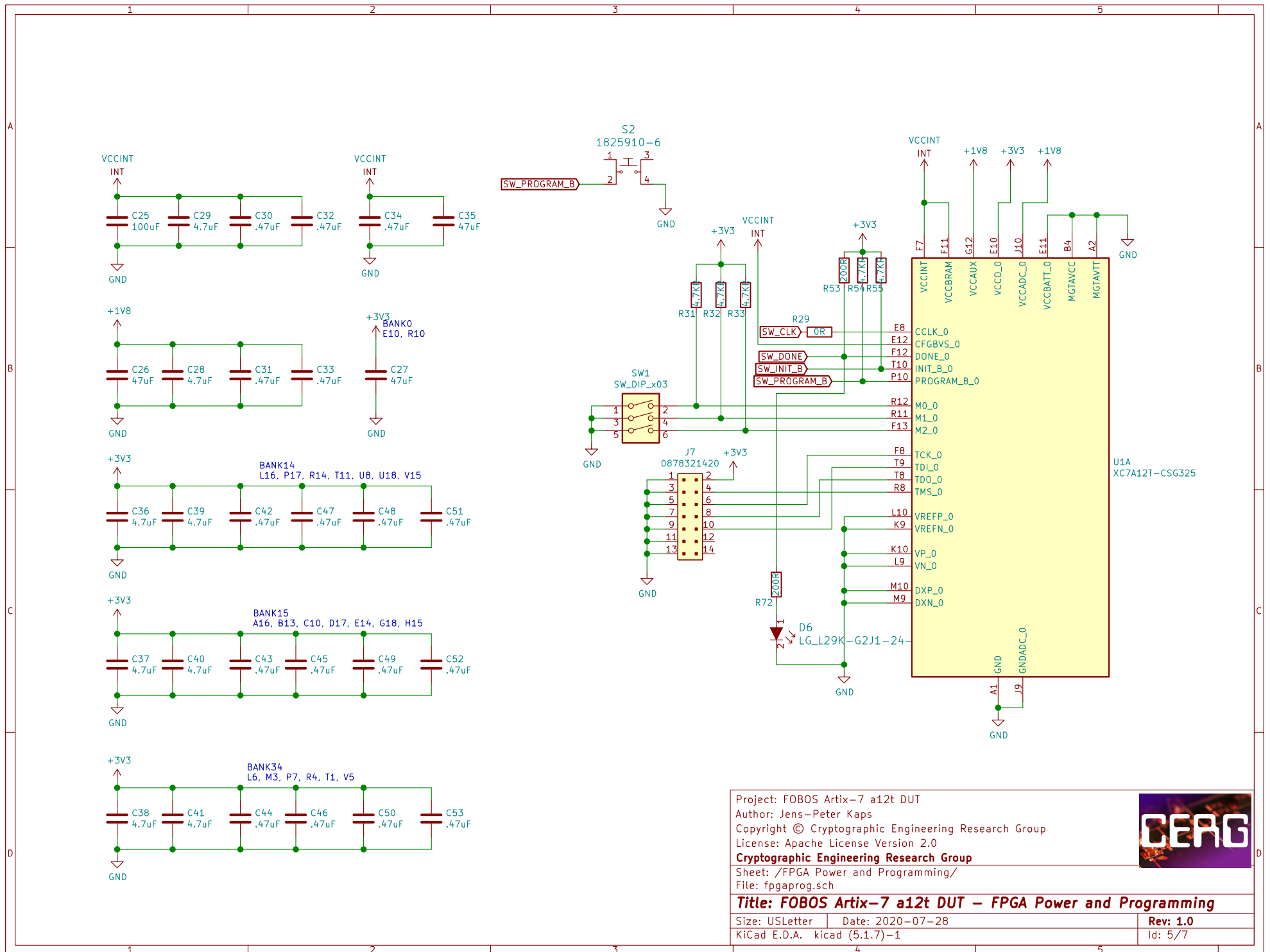
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Size: USLetter Date: 2020-07-28
KiCad E.D.A. kicad (5.1.7)-1

Rev: 1.0
Id: 2/7



Rev: 1.0
Id: 3/7



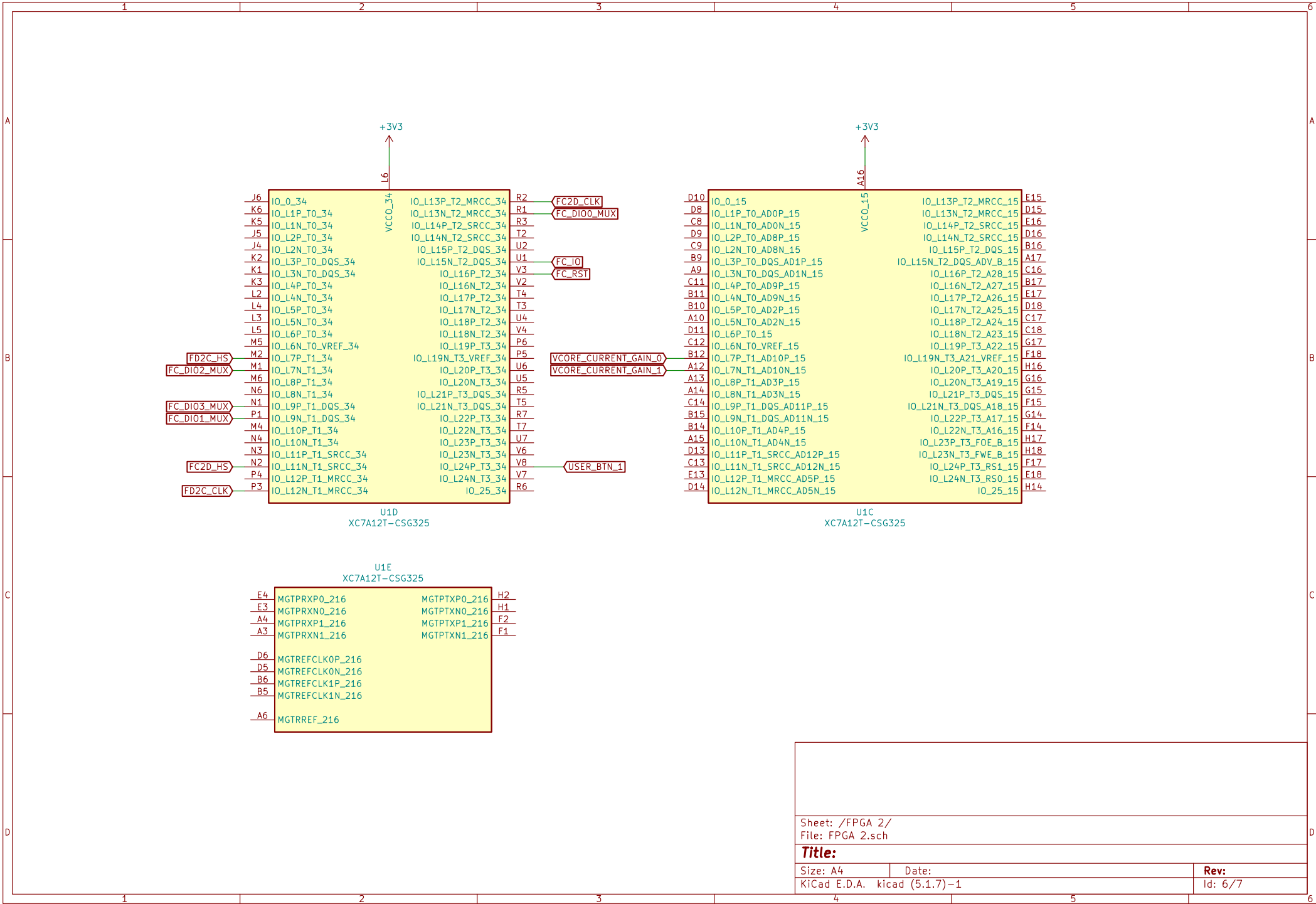
Project: FOBOS Artix-7 a12t DUT
 Author: Jens-Peter Kaps
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 File: fpgaprogramming.sch

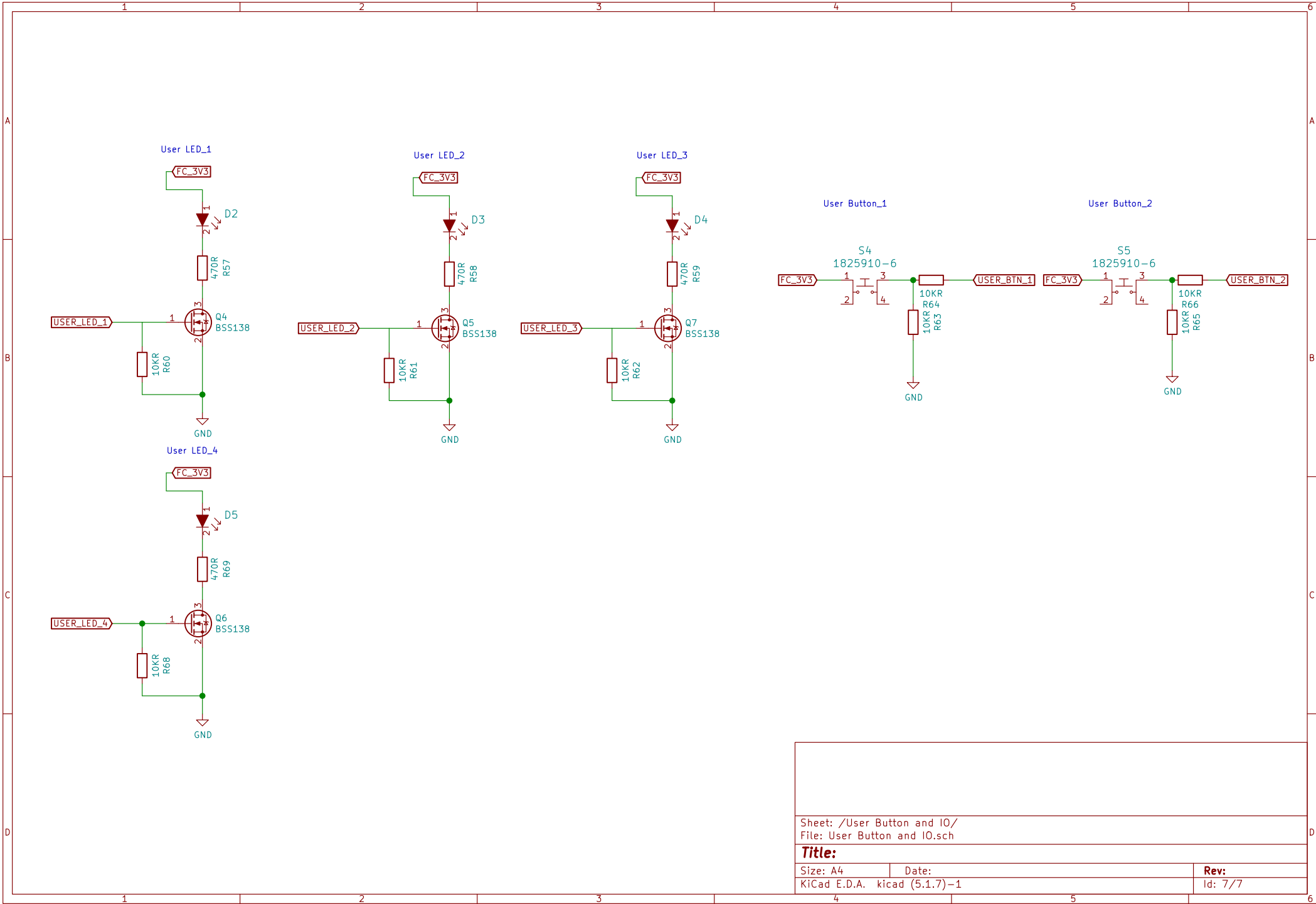


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Size: USLetter | Date: 2020-07-28
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Rev: 1.0
 Id: 5/7





Sheet: /User Button and IO/
File: User Button and IO.sch

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