Intel® Cyclone® 10 LP Device Datasheet

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Intel® Cyclone® 10 LP Device Datasheet

This document describes the electrical and switching characteristics for Intel® Cyclone® 10 LP devices as well as I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

Operating Conditions

When Intel Cyclone 10 LP devices are implemented in a system, they are rated according to a set of defined parameters.

To maintain the highest possible performance and reliability of Intel Cyclone 10 LP devices, you must consider the operating requirements described in this document. Intel Cyclone 10 LP devices are offered in commercial, industrial, extended industrial and, automotive grades as follows:

- –6 (fastest) and –8 speed grades for commercial devices
- –7 and –8 speed grades for industrial devices
- –7 speed grade for automotive devices

Intel Cyclone 10 LP devices are offered in the following core voltages:

- Lower core voltage option (1.0 V)—"Z": For –I8 speed grade
- Standard core voltage option (1.2 V)—"Y": For –C6, –C8, –I7, and –A7 speed grades

A prefix associated with the operating temperature range is attached to the speed grades:

- Commercial with a "C" prefix: –C6, –C8
- Industrial with an "I" prefix: –I7, –I8
- Automotive with an "A" prefix: –A7

Related Information

Intel Cyclone 10 LP Available Options, Intel Cyclone 10 LP Device Overview
Provides more information about the supported speed grades for Intel Cyclone 10 LP devices.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Intel Cyclone 10 LP devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions.

Caution: Conditions beyond those listed in the following table cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time have adverse effects on the device.

Table 1. Absolute Maximum Ratings for Intel Cyclone 10 LP Devices

Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.

Symbol	Parameter	Min	Max	Unit
V_{CCINT}	Core voltage	–0.5	1.8	V
V_{CCA}	Phase-locked loop (PLL) analog power supply	–0.5	3.75	V
V_{CCD_PLL}	PLL digital power supply	–0.5	1.8	V
V_{CCIO}	I/O banks power supply	–0.5	3.75	V
V_I	DC input voltage	–0.5	4.2	V
I_{OUT}	DC output current, per pin	–25	40	mA
T_{STG}	Storage temperature	–65	150	°C
T_J	Operating junction temperature	–40	125	°C

Maximum Allowed Overshoot or Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in the following table and undershoot to –2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. The following table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device.

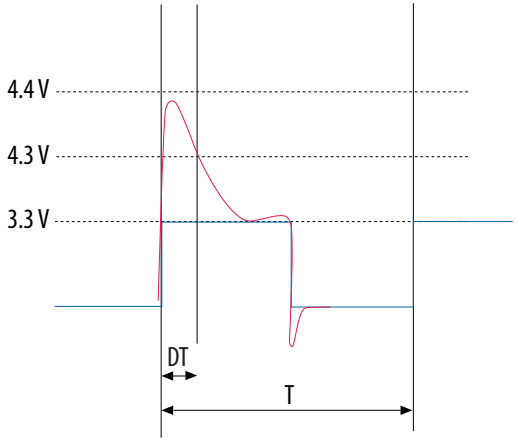
Note: A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

Table 2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Intel Cyclone 10 LP Devices

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit
V_i	AC Input Voltage	V_I = 4.20	100	%
		V_I = 4.25	98	%
		V_I = 4.30	65	%
		V_I = 4.35	43	%
		V_I = 4.40	29	%
		V_I = 4.45	20	%
		V_I = 4.50	13	%
		V_I = 4.55	9	%
		V_I = 4.60	6	%

In the following figure, the overshoot voltage is shown in red and is present on the input pin of the Intel Cyclone 10 LP device at over 4.3 V but below 4.4 V. For example, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

Figure 1. Intel Cyclone 10 LP Devices Overshoot Duration



Recommended Operating Conditions

This section describes the functional operation limits for AC and DC parameters for Intel Cyclone 10 LP devices.

Table 3. Recommended Operating Conditions for Intel Cyclone 10 LP Devices

This table lists the steady-state voltage and current values expected from Intel Cyclone 10 LP devices. All supplies must be strictly monotonic without plateaus.

V_{CCIO} for all I/O banks must be powered up during device operation. All VCCA pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CCINT} (1)	Supply voltage for internal logic	1.2-V operation	1.15	1.2	1.25	V
		1.0-V operation	0.97	1.0	1.03	V
V_{CCIO} (1)(2)	Supply voltage for output buffers	3.3-V operation	3.135	3.3	3.465	V

continued...

(1) V_{CC} must rise monotonically.

(2) V_{CCIO} powers all input buffers.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		3.0-V operation	2.85	3	3.15	V
		2.5-V operation	2.375	2.5	2.625	V
		1.8-V operation	1.71	1.8	1.89	V
		1.5-V operation	1.425	1.5	1.575	V
		1.2-V operation	1.14	1.2	1.26	V
V_{CCA} (1)	Supply (analog) voltage for PLL regulator	—	2.375	2.5	2.625	V
V_{CCD_PLL} (1)	Supply (digital) voltage for PLL	1.2-V operation	1.15	1.2	1.25	V
		1.0-V operation	0.97	1.0	1.03	V
V_I	Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
		For extended temperature	–40	—	125	°C
		For automotive use	–40	—	125	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) (3)	50 µs	—	50 ms	—
		Fast POR (4)	50 µs	—	3 ms	—
I_{Diode}	Magnitude of DC current across PCI*-clamp diode when enable	—	—	—	10	mA

ESD Performance

The electrostatic discharge (ESD) voltages use the human body model (HBM) and charged device model (CDM) for Intel Cyclone 10 LP devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os.

(3) The POR time for Standard POR ranges between 50 and 200 ms. Each individual power supply must reach the recommended operating range within 50 ms.

(4) The POR time for fast POR ranges between 3 and 9 ms. Each individual power supply must reach the recommended operating range within 3 ms.

Table 4. ESD for Intel Cyclone 10 LP Devices GPIOs and HSSI I/Os

Symbol	Parameter	Passing Voltage	Unit
V_{ESDHBM}	ESD voltage using the HBM (GPIOs)	± 2000	V
V_{ESDCDM}	ESD using the CDM (GPIOs)	± 500	V

DC Characteristics

Supply Current

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used.

Table 5. I/O Pin Leakage Current for Intel Cyclone 10 LP Devices

This value is specified for normal device operation. The value varies during device power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

The 10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

Symbol	Parameter	Condition	Min	Max	Unit
I_I	Input pin leakage current	V_I = 0 V to $V_{CCIOMAX}$	–10	10	µA
I_{OZ}	Tristated I/O pin leakage current	V_O = 0 V to $V_{CCIOMAX}$	–10	10	µA

Bus Hold

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 6. Bus Hold Parameter for Intel Cyclone 10 LP Devices

Bus hold trip points are based on the calculated input voltages from the JEDEC standard.

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus hold low, sustaining current	$V_{IN} > V_{IL}$ (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus hold high, sustaining current	$V_{IN} < V_{IL}$ (minimum)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

OCT Specifications

Table 7. Series OCT Without Calibration across Process, Temperature, and Voltage (PVT) Specifications for Intel Cyclone 10 LP Devices

Description	V_{CCIO} (V)	Resistance Tolerance		Unit
		Commercial Maximum	Industrial, Extended industrial, and Automotive Maximum	
Series OCT without calibration	3.0	±30	±40	%
	2.5	±30	±40	%
	1.8	±40	±50	%
	1.5	±50	±50	%
	1.2	±50	±50	%

Table 8. Series OCT with Calibration at Device Power-Up Specifications for Intel Cyclone 10 LP Devices

OCT calibration is automatically performed at device power-up for OCT-enabled I/Os.

Description	V_{CCIO} (V)	Calibration Accuracy		Unit
		Commercial Maximum	Industrial, Extended industrial, and Automotive Maximum	
Series OCT with calibration at device power-up	3.0	±10	±10	%
	2.5	±10	±10	%
	1.8	±10	±10	%
	1.5	±10	±10	%
	1.2	±10	±10	%

Table 9. OCT Variation with Voltage and Temperature after Calibration at Device Power-Up for Intel Cyclone 10 LP Devices

Use this table to determine the final OCT resistance considering the variations after calibration at device power-up.

Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
3.0	0.262	–0.026
2.5	0.234	–0.039
1.8	0.219	–0.086
1.5	0.199	–0.136
1.2	0.161	–0.288

Final OCT Resistance Equation

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$$ (5) (6) (7) (8)

(5) ΔR_V is a variation of resistance with voltage.

(6) V_2 is final voltage.

(7) V_1 is the initial voltage.

$\Delta R_T = (T_2 - T_1) \times dR/dT$ (9) (10) (11) (12)

For $\Delta R_x < 0$; $MF_x = 1/ (|\Delta R_x|/100 + 1)$ (13) (14)

For $\Delta R_x > 0$; $MF_x = \Delta R_x/100 + 1$ (13) (14)

$MF = MF_V \times MF_T$ (14)

$R_{final} = R_{initial} \times MF$ (14) (15) (16)

Impedance Change Example

Calculate the change of 50-Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V as follows:

$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$

$\Delta R_T = (85 - 25) \times 0.262 = 15.72$

Because ΔR_V is negative,

$MF_V = 1 / (3.83/100 + 1) = 0.963$

Because ΔR_T is positive,

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(8) dR/dV is the change percentage of resistance with voltage after calibration at device power-up.

(9) ΔR_T is a variation of resistance with temperature.

(10) T_2 is the final temperature.

(11) T_1 is the initial temperature.

(12) dR/dT is the change percentage of resistance with temperature after calibration at device power-up.

(13) Subscript $_x$ refers to both $_V$ and $_T$.

(14) MF is multiplication factor.

(15) R_{final} is final resistance.

(16) $R_{initial}$ is initial resistance.

$MF_T = 15.72/100 + 1 = 1.157$

$MF = 0.963 \times 1.157 = 1.114$

$R_{final} = 50 \times 1.114 = 55.71\ \Omega$

Pin Capacitance

Table 10. Pin Capacitance for Intel Cyclone 10 LP Devices

Symbol	Parameter	Typical – Quad Flat Pack (QFP)	Typical – Ball-Grid Array (BGA) (17)	Unit
C_{IOTB}	Input capacitance on top and bottom I/O pins	7	6	pF
C_{IOLR}	Input capacitance on right I/O pins	7	5	pF
C_{LVDSLR}	Input capacitance on right I/O pins with dedicated LVDS output	8	7	pF
C_{VREFLR} (18)	Input capacitance on right dual-purpose VREF pin when used as V_{REF} or user I/O pin	21	21	pF
C_{VREFTB} (18)	Input capacitance on top and bottom dual-purpose VREF pin when used as V_{REF} or user I/O pin	23 (19)	23	pF
C_{CLKTB}	Input capacitance on top and bottom dedicated clock input pins	7	6	pF
C_{CLKLR}	Input capacitance on right dedicated clock input pins	6	5	pF

(17) The pin capacitance applies to FBGA, UBGA, and MBGA packages.

(18) When you use the VREF pin as a regular input or output, you can expect a reduced performance of toggle rate and t_{CO} because of higher pin capacitance.

(19) C_{VREFTB} for the 10CL025 device is 30 pF.

Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 11. Internal Weak Pull-Up and Weak Pull-Down Resistor Values for Cyclone 10 Devices

All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK pin.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$R_{\_PU}$	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option	V_{CCIO} = 3.3 V ± 5% (20) (21)	7	25	41	kΩ
		V_{CCIO} = 3.0 V ± 5% (20) (21)	7	28	47	kΩ
		V_{CCIO} = 2.5 V ± 5% (20) (21)	8	35	61	kΩ
		V_{CCIO} = 1.8 V ± 5% (20) (21)	10	57	108	kΩ
		V_{CCIO} = 1.5 V ± 5% (20) (21)	13	82	163	kΩ
		V_{CCIO} = 1.2 V ± 5% (20) (21)	19	143	351	kΩ
$R_{\_PD}$	Value of the I/O pin pull-down resistor before and during configuration	V_{CCIO} = 3.3 V ± 5% (22)	6	19	30	kΩ
		V_{CCIO} = 3.0 V ± 5% (22)	6	22	36	kΩ
		V_{CCIO} = 2.5 V ± 5% (22)	6	25	43	kΩ
		V_{CCIO} = 1.8 V ± 5% (22)	7	35	71	kΩ
		V_{CCIO} = 1.5 V ± 5% (22)	8	50	112	kΩ

(20) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(21) $R_{\_PU} = (V_{CCIO} - V_I)/I_{R\_PU}$
Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5% , $V_I = V_{CC}$ + 5% – 50 mV;
Typical condition: 25°C; $V_{CCIO} = V_{CC}$, V_I = 0 V;
Maximum condition: 100°C; $V_{CCIO} = V_{CC}$ – 5% , V_I = 0 V; in which V_I refers to the input voltage at the I/O pin.

(22) $R_{\_PD} = V_I/I_{R\_PD}$
Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5% , V_I = 50 mV;
Typical condition: 25°C; $V_{CCIO} = V_{CC}$, $V_I = V_{CC}$ – 5% ;
Maximum condition: 100°C; $V_{CCIO} = V_{CC}$ – 5% , $V_I = V_{CC}$ – 5% ; in which V_I refers to the input voltage at the I/O pin.

Hot-Socketing

Table 12. Hot-Socketing Specifications for Intel Cyclone 10 LP Devices

During hot-socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

Symbol	Parameter	Maximum
$I_{IOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA (23)
$I_{XCVRTX(DC)}$	DC current per transceiver TX pin	100 mA
$I_{XCVRRX(DC)}$	DC current per transceiver RX pin	50 mA

Schmitt Trigger Input

Intel Cyclone 10 LP devices support Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rate.

Table 13. Hysteresis Specifications for Schmitt Trigger Input for Supported V_{CCIO} Range in Intel Cyclone 10 LP Devices

Symbol	Parameter	Condition (V)	Minimum	Unit
$V_{SCHMITT}$	Hysteresis for Schmitt trigger input	V_{CCIO} = 3.3	200	mV
		V_{CCIO} = 2.5	200	mV
		V_{CCIO} = 1.8	140	mV
		V_{CCIO} = 1.5	110	mV

I/O Standard Specifications

Tables in this section list the input voltage sensitivities (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Intel Cyclone 10 LP devices.

(23) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Single-Ended I/O Standard Specifications

Table 14. Single-Ended I/O Standard Specifications for Intel Cyclone 10 LP Devices

AC load, C_L = 10 pF

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA) (24)	I_{OH} (mA) (24)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL	3.135	3.3	3.465	—	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS	3.135	3.3	3.465	—	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0-V LVTTL	2.85	3.0	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.45	2.4	4	–4
3.0-V LVCMOS	2.85	3.0	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	V_{CCIO} + 0.3	0.4	2.0	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	2.25	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2
3.0-V PCI	2.85	3.0	3.15	—	0.3 × V_{CCIO}	0.5 × V_{CCIO}	V_{CCIO} + 0.3	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	–0.5
3.0-V PCI-X	2.85	3.0	3.15	—	0.35 × V_{CCIO}	0.5 × V_{CCIO}	V_{CCIO} + 0.3	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	–0.5

Related Information

AN 447: Interfacing Intel Devices with 3.3/3.0/2.5 V LVTTL/LVCMOS I/O Systems
Provides more information about interfacing Intel Cyclone 10 LP devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards.

(24) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the **3.3-V LVTTL** specification (4 mA), set the current strength settings to 4 mA or higher. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the handbook.

Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

Table 15. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Intel Cyclone 10 LP Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V) (25)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V_{CCIO} (26)	0.5 × V_{CCIO} (26)	0.52 × V_{CCIO} (26)	—	0.5 × V_{CCIO}	—
				0.47 × V_{CCIO} (27)	0.5 × V_{CCIO} (27)	0.53 × V_{CCIO} (27)			

Single-Ended SSTL and HSTL I/O Standards Signal Specifications

Table 16. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Intel Cyclone 10 LP Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.57	V_{TT} + 0.57	8.1	–8.1
SSTL-2 Class II	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.76	V_{TT} + 0.76	16.4	–16.4
SSTL-18 Class I	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	V_{TT} – 0.475	V_{TT} + 0.475	6.7	–6.7
SSTL-18 Class II	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	0.28	V_{CCIO} – 0.28	13.4	–13.4

continued...

(25) V_{TT} of the transmitting device must track V_{REF} of the receiving device.

(26) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.

(27) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	14	–14

Related Information

I/O and High Speed I/O in Intel Cyclone 10 LP Devices chapter, Intel Cyclone 10 LP Core Fabric and General Purpose I/Os Handbook

Provides more information about receiver input and transmitter output waveforms, and other differential I/O standards.

Differential SSTL I/O Standard Specifications

Table 17. Differential SSTL I/O Standard Specifications for Intel Cyclone 10 LP Devices

Differential SSTL requires a V_{REF} input.

I/O Standard	V_{CCIO} (V)			$V_{Swing(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{Swing(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	$V_{CCIO}/2$ – 0.2	—	$V_{CCIO}/2$ + 0.2	0.7	V_{CCIO}	$V_{CCIO}/2$ – 0.125	—	$V_{CCIO}/2$ + 0.125
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	V_{CCIO}	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175	0.5	V_{CCIO}	$V_{CCIO}/2$ – 0.125	—	$V_{CCIO}/2$ + 0.125

Differential HSTL I/O Standard Specifications

Table 18. Differential HSTL I/O Standard Specifications for Intel Cyclone 10 LP Devices

Differential HSTL requires a V_{REF} input.

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	0.48 × V_{CCIO}	—	0.52 × V_{CCIO}	0.48 × V_{CCIO}	—	0.52 × V_{CCIO}	0.3	0.48 × V_{CCIO}

Differential I/O Standard Specifications

Table 19. Differential I/O Standard Specifications for Intel Cyclone 10 LP Devices

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (28)			V_{OD} (mV) (29)			V_{OS} (V) (29)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (Row I/Os) (30)	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.80	—	—	—	—	—	—
						0.55	≤ 500 Mbps D_{MAX} ≤ 700 Mbps	1.80						
						1.05	D_{MAX} > 700 Mbps	1.55						
LVPECL (Column I/Os) (30)	2.375	2.5	2.625	100	—	0.05	D_{MAX}≤ 500 Mbps	1.80	—	—	—	—	—	—
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.80						

continued...

(28) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

(29) R_L range: 90 ≤ R_L ≤ 110 Ω.

(30) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported for output pins.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (28)			V_{OD} (mV) (29)			V_{OS} (V) (29)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
						1.05	D_{MAX} > 700 Mbps	1.55						
LVDS (Row I/Os)	2.375	2.5	2.625	100	—	0.05	D_{MAX}≤ 500 Mbps	1.80	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.80						
						1.05	D_{MAX} > 700 Mbps	1.55						
LVDS (Column I/Os)	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.80	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.80						
						1.05	D_{MAX} > 700 Mbps	1.55						
BLVDS (Row I/Os) (31)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
BLVDS (Column I/Os) (31)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
mini-LVDS (Row I/Os) (32)	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1.0	1.2	1.4
mini-LVDS (Column I/Os) (32)	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1.0	1.2	1.4
RSDS (Row I/Os) (32)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5

continued...

(28) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.
(29) R_L range: 90 ≤ R_L ≤ 110 Ω.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (28)			V_{OD} (mV) (29)			V_{OS} (V) (29)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
RSDS (Column I/Os) (32)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS (Row I/Os) (32)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4
PPDS (Column I/Os) (32)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4

Power Consumption

Use the following methods to estimate power for a design:

- the Excel-based EPE
- the Intel Quartus® Prime power analyzer feature

The interactive Excel-based EPE is used prior to designing the device to get a magnitude estimate of the device power. The Intel Quartus Prime power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The power analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, combined with detailed circuit models, can yield very accurate power estimates.

Related Information

- Early Power Estimator User Guide
  Provides more information about the power estimation tools.
- Power Analysis chapter, Intel Quartus Prime Standard Edition Handbook Volume 3: Verification
  Provides more information about the power estimation tools.

(28) V_{IN} range: 0 V ≤ V_{IN} ≤ 1.85 V.

(29) R_L range: 90 ≤ R_L ≤ 110 Ω.

(31) There are no fixed V_{IN}, V_{OD}, and V_{OS} specifications for BLVDS. They depend on the system topology.

(32) The Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins.

Switching Characteristics

This section provides performance characteristics of Intel Cyclone 10 LP core and periphery blocks for commercial grade devices.

Core Performance Specifications

Clock Tree Specifications

Table 20. Clock Tree Performance for Intel Cyclone 10 LP Devices

Device	Performance					Unit
	C6	C8	I7	I8	A7	
10CL006	500	402	437.5	362	402	MHz
10CL010	500	402	437.5	362	402	MHz
10CL016	500	402	437.5	362	402	MHz
10CL025	500	402	437.5	362	402	MHz
10CL040	500	402	437.5	362	402	MHz
10CL055	500	402	437.5	362	—	MHz
10CL080	500	402	437.5	362	—	MHz
10CL120	—	402	437.5	362	—	MHz

PLL Specifications

PLL specifications are for Intel Cyclone 10 LP devices operating in the commercial junction temperature range (0°C to 85°C), the industrial junction temperature range (–40°C to 100°C), the extended industrial junction temperature range (–40°C to 125°C), and the automotive junction temperature range (–40°C to 125°C).

Table 21. PLL Specifications for Intel Cyclone 10 LP Devices

This table is applicable for general purpose PLLs and multipurpose PLLs.

You must connect V_{CCD_PLL} to V_{CCINT} through the decoupling capacitor and ferrite bead.

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN} (33)	Input clock frequency (–C6, –C8, –I7, and –A7 speed grades)	5	—	472.5	MHz
	Input clock frequency (–I8 speed grade)	5	—	362	MHz
f_{INPFD}	PFD input frequency	5	—	325	MHz
f_{VCO} (34)	PLL internal VCO operating range	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER\_CCJ}$ (35)	Input clock cycle-to-cycle jitter $F_{REF} \geq 100$ MHz	—	—	0.15	UI
	$F_{REF} < 100$ MHz	—	—	±750	ps
f_{OUT_EXT} (external clock output) (33)	PLL output frequency	—	—	472.5	MHz
f_{OUT} (to global clock)	PLL output frequency (–C6 speed grade)	—	—	472.5	MHz
	PLL output frequency (–I7, –A7 speed grades)	—	—	450	MHz
	PLL output frequency (–C8 speed grade)	—	—	402.5	MHz
	PLL output frequency (–I8 speed grade)	—	—	362	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	1	ms

continued...

(33) This parameter is limited in the Intel Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(34) The V_{CO} frequency reported by the Intel Quartus Prime software in the PLL Summary section of the compilation report takes into consideration the V_{CO} post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(35) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.

Symbol	Parameter	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or areset is deasserted)	—	—	1	ms
$t_{OUTJITTER\_PERIOD\_DEDCLK}$ (36)	Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER\_CCJ\_DEDCLK}$ (36)	Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER\_PERIOD\_IO}$ (36)	Regular I/O period jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER\_CCJ\_IO}$ (36)	Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 (37)	—	SCANCLK cycles

continued...

(36) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.

(37) With 100-MHz scanclk frequency.

Symbol	Parameter	Min	Typ	Max	Unit
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
$t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}$ (38) (39)	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	425	ps
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	42.5	mUI

Embedded Multiplier Specifications

Table 22. Embedded Multiplier Specifications for Intel Cyclone 10 LP Devices

Mode	Resources Used	Performance				Unit
	Number of Multipliers	C6	I7, A7	C8	I8	
9 × 9-bit multiplier	1	340	300	260	240	MHz
18 × 18-bit multiplier	1	287	250	200	185	MHz

Memory Block Specifications

Table 23. M9K Memory Block Performance Specifications for Intel Cyclone 10 LP Devices

Memory	Mode	Resources Used		Performance				Unit
		LEs	M9K Memory	C6	I7, A7	C8	I8	
M9K Block	FIFO 256 × 36	47	1	315	274	238	200	MHz
	Single-port 256 × 36	0	1	315	274	238	200	MHz
	Simple dual-port 256 × 36 CLK	0	1	315	274	238	200	MHz
	True dual port 512 × 18 single CLK	0	1	315	274	238	200	MHz

(38) The cascaded PLLs specification is applicable only with the following conditions:
- Upstream PLL—0.59 MHz ≥ Upstream PLL bandwidth < 1 MHz
- Downstream PLL—Downstream PLL bandwidth > 2 MHz

(39) PLL cascading is not supported for transceiver applications.

Periphery Performance

I/O performance supports several system interfaces, such as the high-speed I/O interface and the PCI/PCI-X bus interface. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-LVTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.

Note: Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

RSDS Transmitter Timing Specifications

Table 24. RSDS Transmitter Timing Specifications for Intel Cyclone 10 LP Devices

Applicable for true RSDS and emulated RSDS_E_3R transmitter.

True RSDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated RSDS transmitter is supported at the output pin of all I/O Banks.

Symbol	Mode	C6			I7			C8, A7			I8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	MHz
	×8	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	MHz
	×7	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	MHz
	×4	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	MHz
	×2	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	MHz
	×1	5	—	360	5	—	311	5	—	311	5	—	311	MHz
Device operation in Mbps	×10	100	—	360	100	—	311	100	—	311	100	—	311	Mbps
	×8	80	—	360	80	—	311	80	—	311	80	—	311	Mbps
	×7	70	—	360	70	—	311	70	—	311	70	—	311	Mbps
	×4	40	—	360	40	—	311	40	—	311	40	—	311	Mbps
	×2	20	—	360	20	—	311	20	—	311	20	—	311	Mbps

continued...

Symbol	Mode	C6			I7			C8, A7			I8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	×1	10	—	360	10	—	311	10	—	311	10	—	311	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	%
Transmitter channel-to-channel skew (TCCS)	—	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{LOCK} (40)	—	—	—	1	—	—	1	—	—	1	—	—	1	ms

Emulated RSDS_E_1R Transmitter Timing Specifications

Table 25. Emulated RSDS_E_1R Transmitter Timing Specifications for Intel Cyclone 10 LP Devices

Emulated RSDS_E_1R transmitter is supported at the output pin of all I/O Banks.

Symbol	Modes	C6			I7			C8, A7			I8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	85	5	—	85	5	—	85	5	—	85	MHz
	×8	5	—	85	5	—	85	5	—	85	5	—	85	MHz
	×7	5	—	85	5	—	85	5	—	85	5	—	85	MHz
	×4	5	—	85	5	—	85	5	—	85	5	—	85	MHz
	×2	5	—	85	5	—	85	5	—	85	5	—	85	MHz
	×1	5	—	170	5	—	170	5	—	170	5	—	170	MHz

continued...

(40) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

Symbol	Modes	C6			I7			C8, A7			I8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Device operation in Mbps	×10	100	—	170	100	—	170	100	—	170	100	—	170	Mbps
	×8	80	—	170	80	—	170	80	—	170	80	—	170	Mbps
	×7	70	—	170	70	—	170	70	—	170	70	—	170	Mbps
	×4	40	—	170	40	—	170	40	—	170	40	—	170	Mbps
	×2	20	—	170	20	—	170	20	—	170	20	—	170	Mbps
	×1	10	—	170	10	—	170	10	—	170	10	—	170	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{LOCK} (41)	—	—	—	1	—	—	1	—	—	1	—	—	1	ms

(41) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

Mini-LVDS Transmitter Timing Specifications

Table 26. Mini-LVDS Transmitter Timing Specifications for Intel Cyclone 10 LP Devices

Applicable for true and emulated mini-LVDS transmitter.

True mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated mini-LVDS transmitter is supported at the output pin of all I/O banks.

Symbol	Modes	C6			I7			C8, A7			I8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	MHz
	×8	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	MHz
	×7	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	MHz
	×4	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	MHz
	×2	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	MHz
	×1	5	—	400	5	—	311	5	—	311	5	—	311	MHz
Device operation in Mbps	×10	100	—	400	100	—	311	100	—	311	100	—	311	Mbps
	×8	80	—	400	80	—	311	80	—	311	80	—	311	Mbps
	×7	70	—	400	70	—	311	70	—	311	70	—	311	Mbps
	×4	40	—	400	40	—	311	40	—	311	40	—	311	Mbps
	×2	20	—	400	20	—	311	20	—	311	20	—	311	Mbps
	×1	10	—	400	10	—	311	10	—	311	10	—	311	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	ps

continued...

Symbol	Modes	C6			I7			C8, A7			I8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{LOCK} (42)	—	—	—	1	—	—	1	—	—	1	—	—	1	ms

True LVDS Transmitter Timing Specifications

Table 27. True LVDS Transmitter Timing Specifications for Intel Cyclone 10 LP Devices

True LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6.

Symbol	Modes	C6		I7		C8, A7		I8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{HSCLK} (input clock frequency)	×10	5	420	5	370	5	320	5	320	MHz
	×8	5	420	5	370	5	320	5	320	MHz
	×7	5	420	5	370	5	320	5	320	MHz
	×4	5	420	5	370	5	320	5	320	MHz
	×2	5	420	5	370	5	320	5	320	MHz
	×1	5	420	5	402.5	5	402.5	5	362	MHz
HSIODR	×10	100	840	100	740	100	640	100	640	Mbps
	×8	80	840	80	740	80	640	80	640	Mbps
	×7	70	840	70	740	70	640	70	640	Mbps
	×4	40	840	40	740	40	640	40	640	Mbps
	×2	20	840	20	740	20	640	20	640	Mbps
	×1	10	420	10	402.5	10	402.5	10	362	Mbps

continued...

(42) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

Symbol	Modes	C6		I7		C8, A7		I8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{DUTY}	—	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	ps
t_{LOCK} (43)	—	—	1	—	1	—	1	—	1	ms

Emulated LVDS Transmitter Timing Specifications

Table 28. Emulated LVDS Transmitter Timing Specifications for Intel Cyclone 10 LP Devices

Emulated LVDS transmitter is supported at the output pin of all I/O Banks.

Symbol	Modes	C6		I7		C8, A7		I8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{HSCLK} (input clock frequency)	×10	5	320	5	320	5	275	5	275	MHz
	×8	5	320	5	320	5	275	5	275	MHz
	×7	5	320	5	320	5	275	5	275	MHz
	×4	5	320	5	320	5	275	5	275	MHz
	×2	5	320	5	320	5	275	5	275	MHz
	×1	5	402.5	5	402.5	5	402.5	5	362	MHz
HSIODR	×10	100	640	100	640	100	550	100	550	Mbps
	×8	80	640	80	640	80	550	80	550	Mbps
	×7	70	640	70	640	70	550	70	550	Mbps
	×4	40	640	40	640	40	550	40	550	Mbps
	×2	20	640	20	640	20	550	20	550	Mbps

continued...

(43) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

Symbol	Modes	C6		I7		C8, A7		I8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
	×1	10	402.5	10	402.5	10	402.5	10	362	Mbps
t_{DUTY}	—	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	ps
t_{LOCK} (44)	—	—	1	—	1	—	1	—	1	ms

LVDS Receiver Timing Specifications

Table 29. LVDS Receiver Timing Specifications for Intel Cyclone 10 LP Devices

LVDS receiver is supported at all I/O Banks.

Symbol	Modes	C6		I7		C8, A7		I8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{HSCLK} (input clock frequency)	×10	10	437.5	10	370	10	320	10	320	MHz
	×8	10	437.5	10	370	10	320	10	320	MHz
	×7	10	437.5	10	370	10	320	10	320	MHz
	×4	10	437.5	10	370	10	320	10	320	MHz
	×2	10	437.5	10	370	10	320	10	320	MHz
	×1	10	437.5	10	402.5	10	402.5	10	362	MHz
HSIODR	×10	100	875	100	740	100	640	100	640	Mbps
	×8	80	875	80	740	80	640	80	640	Mbps
	×7	70	875	70	740	70	640	70	640	Mbps
	×4	40	875	40	740	40	640	40	640	Mbps

continued...

(44) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

Symbol	Modes	C6		I7		C8, A7		I8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
	×2	20	875	20	740	20	640	20	640	Mbps
	×1	10	437.5	10	402.5	10	402.5	10	362	Mbps
SW	—	—	400	—	400	—	400	—	550	ps
Input jitter tolerance	—	—	500	—	500	—	550	—	600	ps
t_{LOCK} (45)	—	—	1	—	1	—	1	—	1	ms

Duty Cycle Distortion Specifications

Table 30. Worst-Case Duty Cycle Distortion on Intel Cyclone 10 LP Devices I/O Pins

The duty cycle distortion specification applies to clock outputs from the PLLs, global clock tree, and IOE driving the dedicated and general purpose I/O pins.

Intel Cyclone 10 LP devices meet the specified duty cycle distortion at the maximum output toggle rate for each combination of I/O standard and current strength.

Symbol	C6		I7		C8, I8, A7		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

OCT Calibration Timing Specification

Table 31. Timing Specification for Series OCT with Calibration at Device Power-Up for Intel Cyclone 10 LP Devices

OCT calibration takes place after device configuration and before entering user mode.

Symbol	Description	Maximum	Unit
t_{OCTCAL}	Duration of series OCT with calibration at device power-up	20	µs

(45) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

IOE Programmable Delay

The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Intel Quartus Prime software. The values in the table show the delay of programmable IOE delay chain with maximum offset settings after excluding the intrinsic delay (delay at minimum offset settings).

The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Intel Quartus Prime software.

Table 32. IOE Programmable Delay on Column Pins for Intel Cyclone 10 LP 1.0 V Core Voltage Devices

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset		Unit
				Fast Corner	Slow Corner	
				I8	I8	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.924	3.411	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.875	3.367	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.631	1.124	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.931	1.684	ns

Table 33. IOE Programmable Delay on Row Pins for Intel Cyclone 10 LP 1.0 V Core Voltage Devices

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset		Unit
				Fast Corner	Slow Corner	
				I8	I8	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.921	3.412	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.919	3.441	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.623	1.168	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.919	1.656	ns

Table 34. IOE Programmable Delay on Column Pins for Intel Cyclone 10 LP 1.2 V Core Voltage Devices

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset							Unit
				Fast Corner			Slow Corner				
				C6	I7	A7	C6	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.211	1.211	2.177	2.433	2.388	2.508	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.307	1.203	1.203	2.19	2.540	2.430	2.545	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.437	0.402	0.402	0.747	0.880	0.834	0.873	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.693	0.665	0.665	1.200	1.532	1.393	1.441	ns

Table 35. IOE Programmable Delay on Row Pins for Intel Cyclone 10 LP 1.2 V Core Voltage Devices

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset							Unit
				Fast Corner			Slow Corner				
				C6	I7	A7	C6	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.209	1.209	2.201	2.510	2.429	2.548	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.207	1.207	2.202	2.558	2.447	2.557	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.458	0.419	0.419	0.783	0.924	0.875	0.915	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.686	0.657	0.657	1.185	1.506	1.376	1.422	ns

Configuration Specifications

This section provides configuration specifications and timing for the Intel Cyclone 10 LP devices.

JTAG Timing Parameters

Table 36. JTAG Timing Parameters for Intel Cyclone 10 LP Devices

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	19	—	ns
t_{JCL}	TCK clock low time	19	—	ns
t_{JPSU_TDI}	JTAG port setup time for TDI	1	—	ns
t_{JPSU_TMS}	JTAG port setup time for TMS	3	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output (46)	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output (46)	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance (46)	—	15	ns
t_{JSSU}	Capture register setup time	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Active Configuration Mode Specifications

Table 37. Active Configuration Mode Specifications for Intel Cyclone 10 LP Devices

Programming Mode	DCLK Range	Typical DCLK	Unit
Active Serial (AS)	20 to 40	33	MHz

(46) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.

AS Configuration Timing

Table 38. AS Configuration Timing for Intel Cyclone 10 LP Devices

Symbol	Parameter	Configuration Time	Unit
t_{SU}	Setup time	10	ns
t_{DH}	Hold time	0	ns
t_{CO}	Clock-to-output time	4	ns

Related Information

AS Configuration Timing
Provides the AS configuration timing waveform.

Passive Configuration Mode Specifications

Table 39. Passive Configuration Mode Specifications for Intel Cyclone 10 LP Devices

Programming Mode	V_{CCINT} Voltage Level (V)	DCLK f_{MAX}	Unit
Passive Serial (PS)	1.0 (47)	66	MHz
	1.2	133	MHz
Fast Passive Parallel (FPP) (48)	1.0 (47)	66	MHz
	1.2 (49)	100	MHz

(47) V_{CCINT} = 1.0 V is only supported for Intel Cyclone 10 LP 1.0 V core voltage devices.

(48) FPP configuration mode supports all Intel Cyclone 10 LP devices (except for E144 package devices).

(49) Intel Cyclone 10 LP 1.2 V core voltage devices support 133 MHz DCLK f_{MAX} for 10CL006, 10CL010, 10CL016, 10CL025, and 10CL040 only.

PS Configuration Timing

Table 40. PS Configuration Timing Parameters for Intel Cyclone 10 LP Devices

Symbol	Parameter	Minimum		Maximum		Unit
		1.2 V Core Voltage	1.0 V Core Voltage	1.2 V Core Voltage	1.0 V Core Voltage	
t_{CF2CD}	nCONFIG low to CONF_DONE low	—		500		ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—		500		ns
t_{CFG}	nCONFIG low pulse width	500		—		ns
t_{STATUS}	nSTATUS low pulse width	45		230 (50)		µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—		230 (51)		µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	230 (50)		—		µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2		—		µs
t_{DH}	Data hold time after rising edge on DCLK	0		—		ns
t_{CD2UM}	CONF_DONE high to user mode (52)	300		650		µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period		—		—
t_{CD2UMC}	CONF_DONE high to user mode with **CLKUSR** option on	t_{CD2CU} + (3,192 × CLKUSR period)		—		—
t_{DSU}	Data setup time before rising edge on DCLK	5	8	—		
t_{CH}	DCLK high time	3.2	6.4	—	—	ns

continued...

(50) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(51) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(52) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for starting the device.

Symbol	Parameter	Minimum		Maximum		Unit
		1.2 V Core Voltage	1.0 V Core Voltage	1.2 V Core Voltage	1.0 V Core Voltage	
t_{CL}	DCLK low time	3.2	6.4	—	—	ns
t_{CLK}	DCLK period	7.5	15	—	—	ns
f_{MAX}	DCLK frequency	—	—	133	66	MHz

Related Information

PS Configuration Timing
Provides the PS configuration timing waveform.

FPP Configuration Timing

Table 41. FPP Timing Parameters for Intel Cyclone 10 LP Devices

Symbol	Parameter	Minimum		Maximum		Unit
		1.2 V Core Voltage	1.0 V Core Voltage	1.2 V Core Voltage	1.0 V Core Voltage	
t_{CF2CD}	nCONFIG low to CONF_DONE low	—		500		ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—		500		ns
t_{CFG}	nCONFIG low pulse width	500		—		ns
t_{STATUS}	nSTATUS low pulse width	45		230 (53)		µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—		230 (54)		µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	230 (53)		—		µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2		—		µs
t_{DH}	Data hold time after rising edge on DCLK	0		—		ns
t_{CD2UM}	CONF_DONE high to user mode (55)	300		650		µs

continued...

(53) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(54) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

Symbol	Parameter	Minimum		Maximum		Unit
		1.2 V Core Voltage	1.0 V Core Voltage	1.2 V Core Voltage	1.0 V Core Voltage	
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period		—		—
t_{CD2UMC}	CONF_DONE high to user mode with **CLKUSR** option on	t_{CD2CU} + (3,192 × CLKUSR period)		—		—
t_{DSU}	Data setup time before rising edge on DCLK	5	8	—	—	ns
t_{CH}	DCLK high time	3.2	6.4	—	—	ns
t_{CL}	DCLK low time	3.2	6.4	—	—	ns
t_{CLK}	DCLK period	7.5	15	—	—	ns
f_{MAX}	DCLK frequency	—	—	133	66	MHz

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveform.

I/O Timing

I/O timing data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the timing analysis. You may generate the I/O timing report manually using the Timing Analyzer or using the automated script.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

AN 775: I/O Timing Information Generation Guidelines
Provides the techniques to generate I/O timing information using the Intel Quartus Prime software.

(55) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for starting the device.

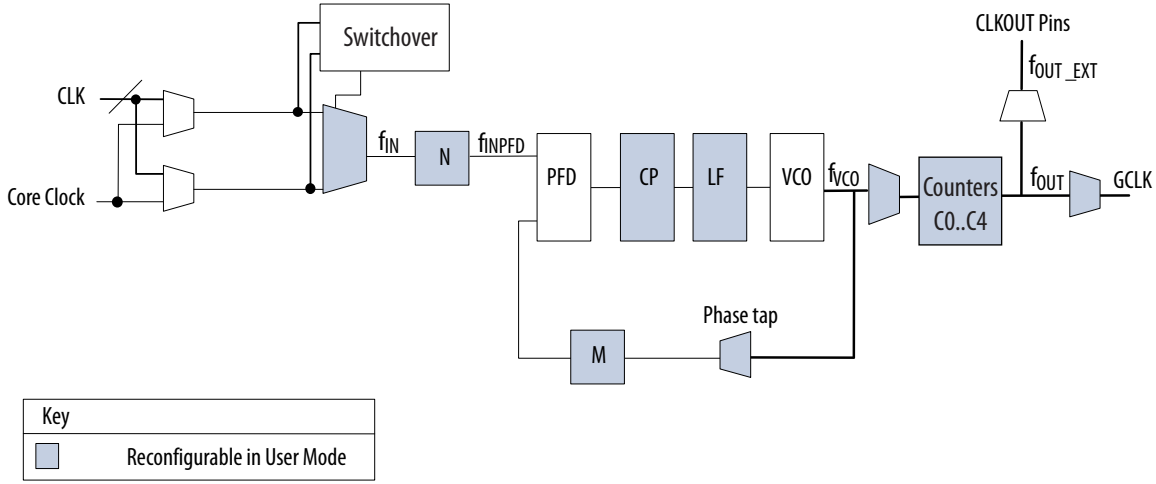
Glossary

Terms

- Receiver input skew margin (RSKM)—High-speed I/O block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2.
- SW (Sampling Window)—High-speed I/O block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window.

Clock Pins and Blocks

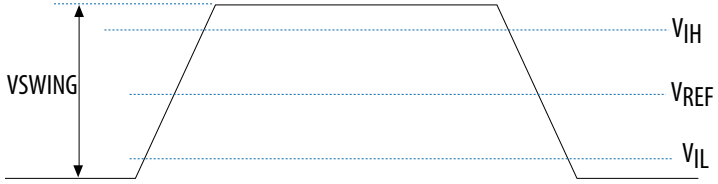
- f_{HSCLK}—High-speed I/O block: High-speed receiver/transmitter input and output clock frequency.
- GCLK—Input pin directly to Global Clock network.
- GCLK PLL—Input pin to Global Clock network through the PLL.
- HSIODR—High-speed I/O block: Maximum/minimum LVDS data transfer rate (HSIODR = 1/TUI).
- PLL Block—The following figure highlights the PLL specification parameters



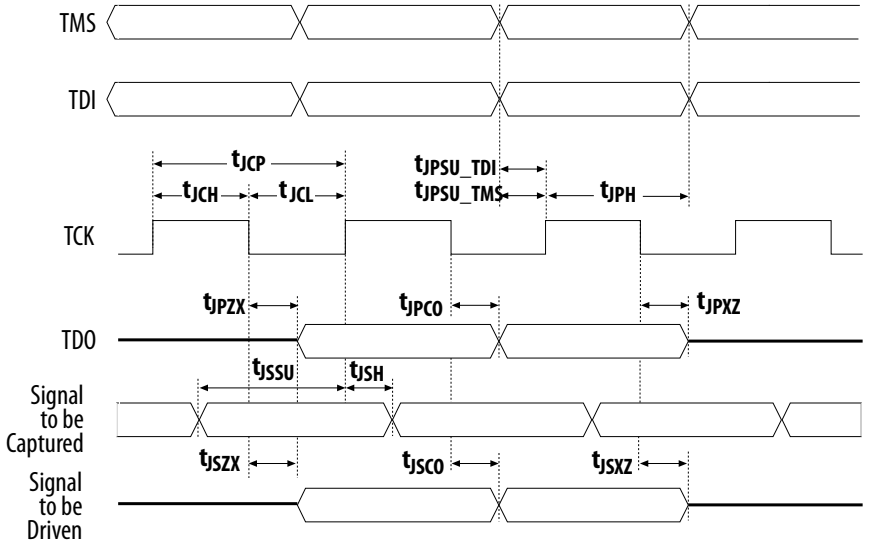
- R_L—Receiver differential input discrete resistor (external to Intel Cyclone 10 LP devices).

Example Waveforms

Input Waveforms for the SSTL Differential I/O Standard

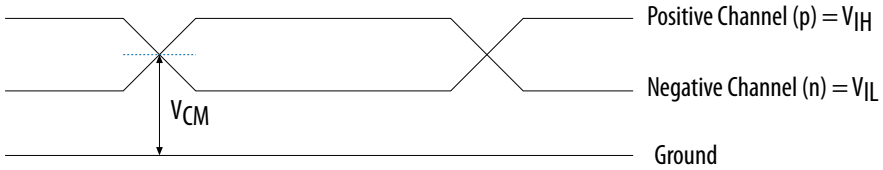


JTAG Waveform



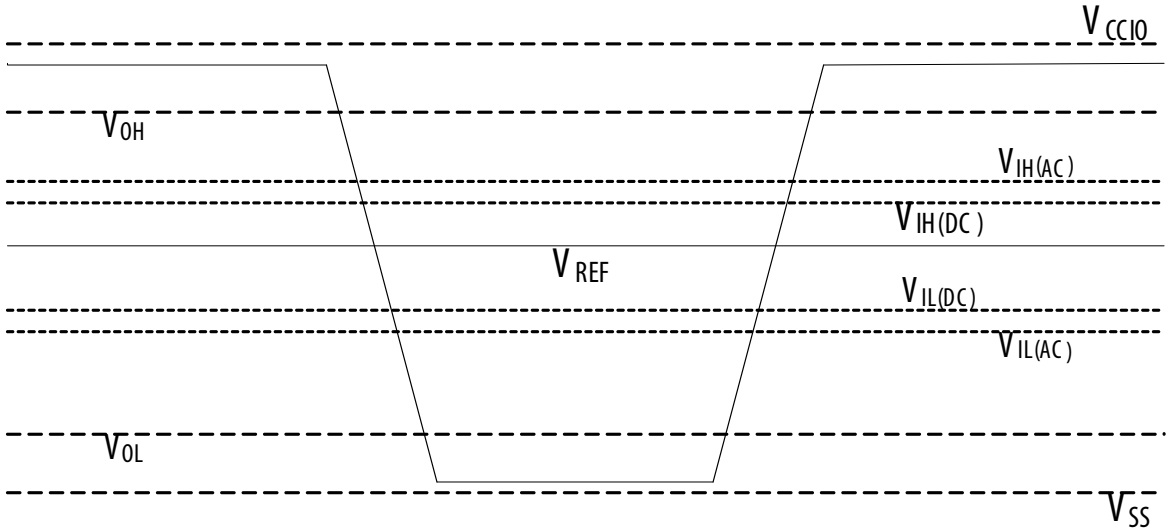
Receiver Waveform for LVDS and LVPECL Differential Standards

Single-Ended Waveform



Differential Input Waveform

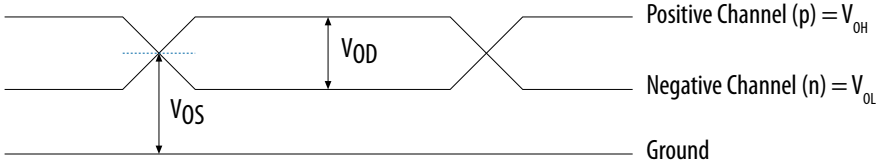
Single-Ended Voltage-Referenced I/O Standard



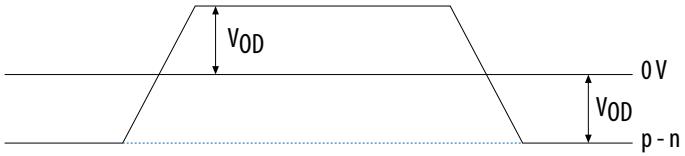
The JEDEC standard for SSTl and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.

Transmitter Output Waveform for the LVDS, Mini-LVDS, PPDS and RSDS Differential I/O Standards:

Single-Ended Waveform



Differential Waveform (Mathematical Function of Positive and Negative Channel)



Delay Definitions

- t_C—High-speed receiver and transmitter input and output clock period.
- Channel-to-channel-skew (TCCS)—High-speed I/O block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
- t_{cin}—Delay from the clock pad to the I/O input register.
- t_{CO}—Delay from the clock pad to the I/O output.
- t_{cout}—Delay from the clock pad to the I/O output register.
- t_{DUTY}—High-speed I/O block: Duty cycle on high-speed transmitter output clock.
- t_{FALL}—Signal high-to-low transition time (80–20%).
- t_H—Input register hold time.

- Timing Unit Interval (TUI)—High-speed I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
- $t_{INJITTER}$—Period jitter on the PLL clock input.
- $t_{OUTJITTER\_DEDCLK}$—Period jitter on the dedicated clock output driven by a PLL.
- $t_{OUTJITTER\_IO}$—Period jitter on the general purpose I/O driven by a PLL.
- t_{pllcin}—Delay from the PLL inclk pad to the I/O input register.
- $t_{pllcout}$—Delay from the PLL inclk pad to the I/O output register.
- t_{RISE}—Signal low-to-high transition time (20–80%).
- t_{SU}—Input register setup time.

Voltage Definitions

- $V_{CM(DC)}$—DC common mode input voltage.
- $V_{DIF(AC)}$—AC differential input voltage: The minimum AC input differential voltage required for switching.
- $V_{DIF(DC)}$—DC differential input voltage: The minimum DC input differential voltage required for switching.
- V_{ICM}—Input common mode voltage: The common mode of the differential signal at the receiver.
- V_{ID}—Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
- V_{IH}—Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high.
- $V_{IH(AC)}$—High-level AC input voltage.
- $V_{IH(DC)}$—High-level DC input voltage.
- V_{IL}—Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low.
- $V_{IL\ (AC)}$—Low-level AC input voltage.
- $V_{IL\ (DC)}$—Low-level DC input voltage.
- V_{IN}—DC input voltage.
- V_{OCM}—Output common mode voltage: The common mode of the differential signal at the transmitter.
- V_{OD}—Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} - V_{OL}$.
- V_{OH}—Voltage output high: The maximum positive voltage from an output that the device considers is accepted as the minimum positive high level.

- V_{OL}—Voltage output low: The maximum positive voltage from an output that the device considers is accepted as the maximum positive low level.
- V_{OS}—Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
- $V_{OX\ (AC)}$—AC differential output cross point voltage: the voltage at which the differential output signals must cross.
- V_{REF}—Reference voltage for the SSTL and HSTL I/O standards.
- $V_{REF\ (AC)}$—AC input reference voltage for the SSTL and HSTL I/O standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on V_{REF} must not exceed 2% of $V_{REF(DC)}$.
- $V_{REF\ (DC)}$—DC input reference voltage for the SSTL and HSTL I/O standards.
- $V_{SWING\ (AC)}$—AC differential input voltage: AC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
- $V_{SWING\ (DC)}$—DC differential input voltage: DC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
- V_{TT}—Termination voltage for the SSTL and HSTL I/O standards.
- $V_{X\ (AC)}$—AC differential input cross point voltage: The voltage at which the differential input signals must cross.

Document Revision History for Intel Cyclone 10 LP Device Datasheet

Document Version	Changes
2018.05.07	• Removed the specifcations for the quad flat no leads (QFN) package in the *Pin Capacitance for Intel Cyclone 10 LP Devices* table. • Added the following configuration specifications: — AS Configuration Timing — PS Configuration Timing — FPP Configuration Timing • Updated the description in the *IOE Programmable Delay* section. • Updated the I/O Timing section on the I/O timing information generation guidelines.
2017.05.08	Initial release.