Sheet: Connectors, IO

File: target.sch

Sheet: Power

File: power.sch

Sheet: FPGA Programming

File: fpgaprog.sch

Sheet: FPGA 1

File: fpga 1.sch

Sheet: User Button and IO

File: User Button and IO.sch

Sheet: FPGA 2

File: FPGA 2.sch

Sheet: FPGA Power

File: fpgapower.sch

H1 MountingHole

H2 MountingHole

H3 MountingHole

H4 MountingHole

cerg:cerg

CERG-Logo

Project: FOBOS Artix-7 a12t DUT

Author: Jens-Peter Kaps, Eddie Ferrufino

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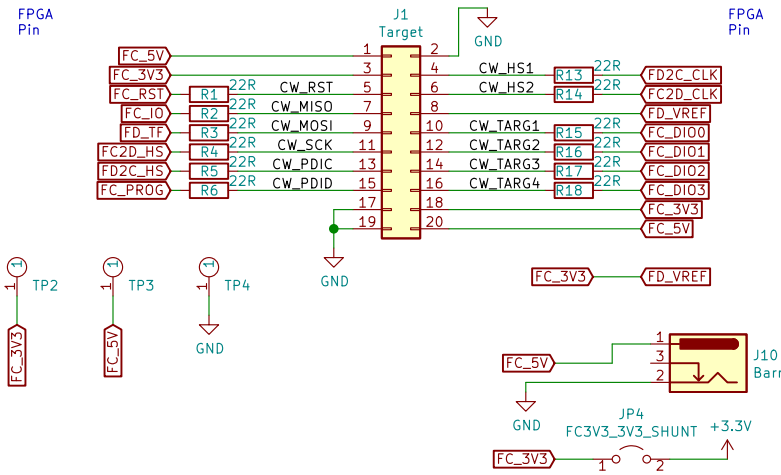
Sheet: /

File: dut-artix7-a12t.sch

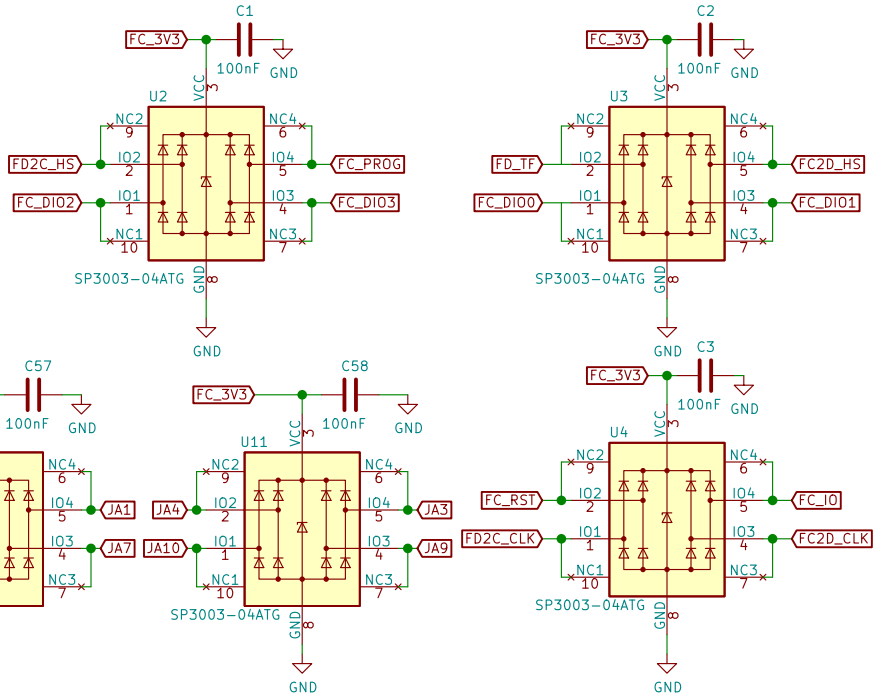
Title: FOBOS Artix-7 a12t DUT

Size: USLetter	Date: 2020-07-28	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.7)-1		Id: 1/8

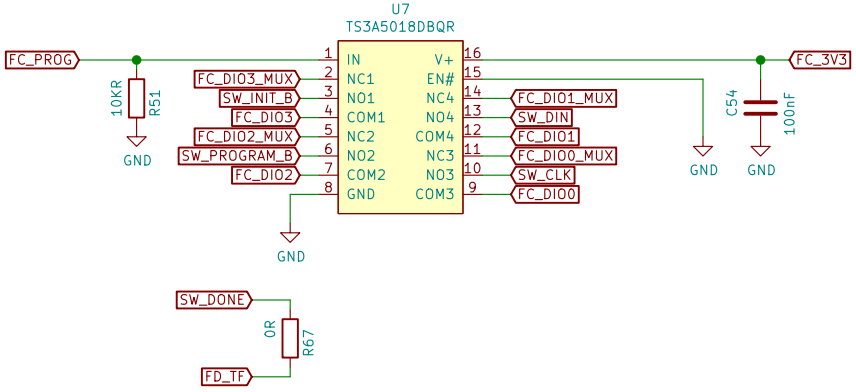
FOBOS Target Connector



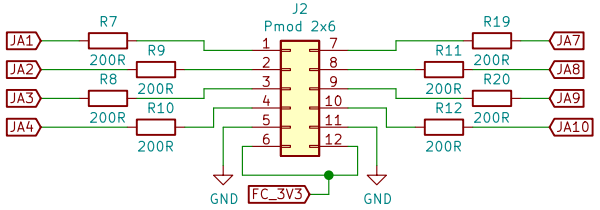
ESD Protection



Programming/DUT Communication Switches



PMOD Connector



cerg:cerg_logo
CERG-Logo

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Sheet: /Connectors, IO/
File: target.sch

Title: FOBOS Artix-7 a12t DUT - Connectors, IO

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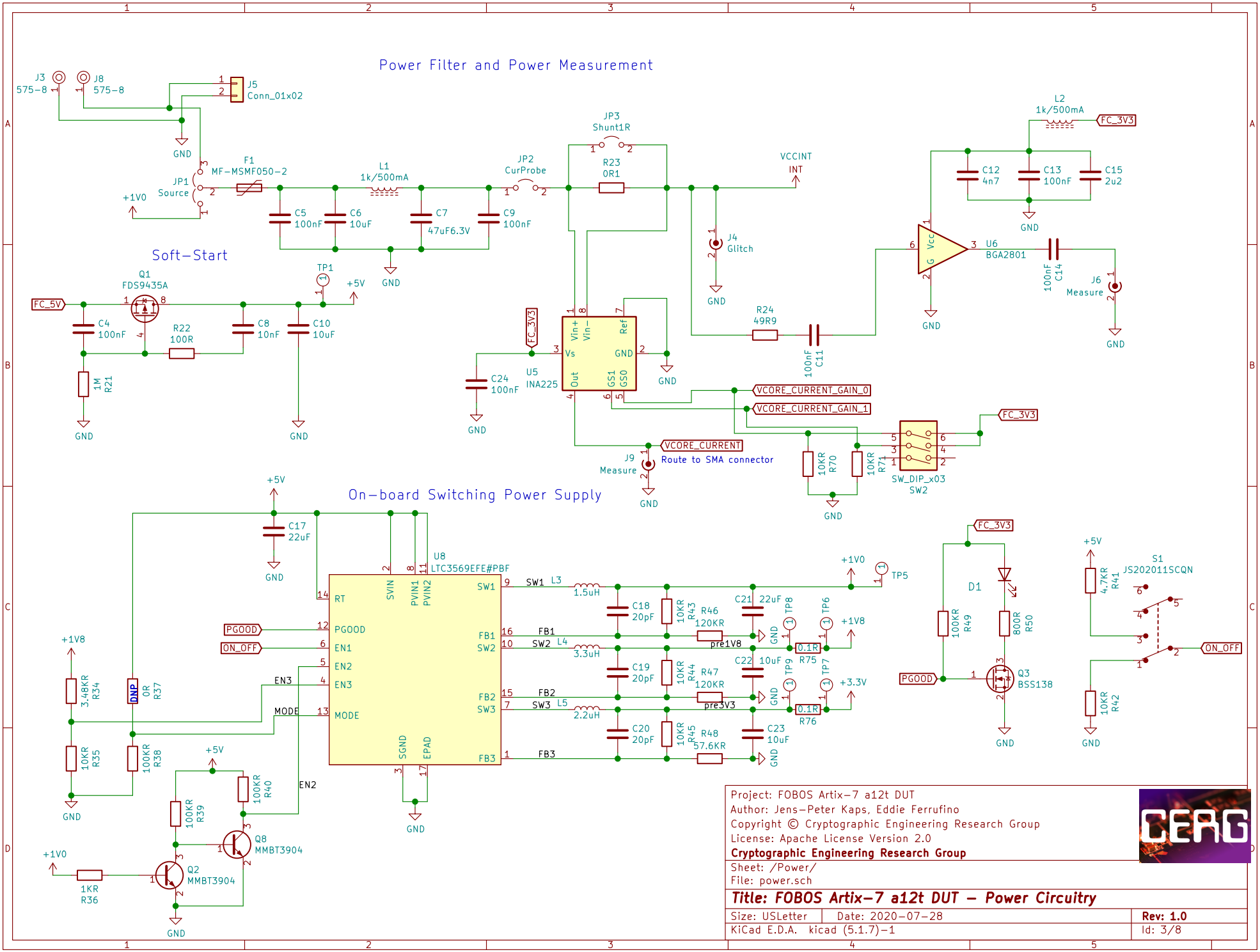

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Sheet: /Power/
File: power.sch

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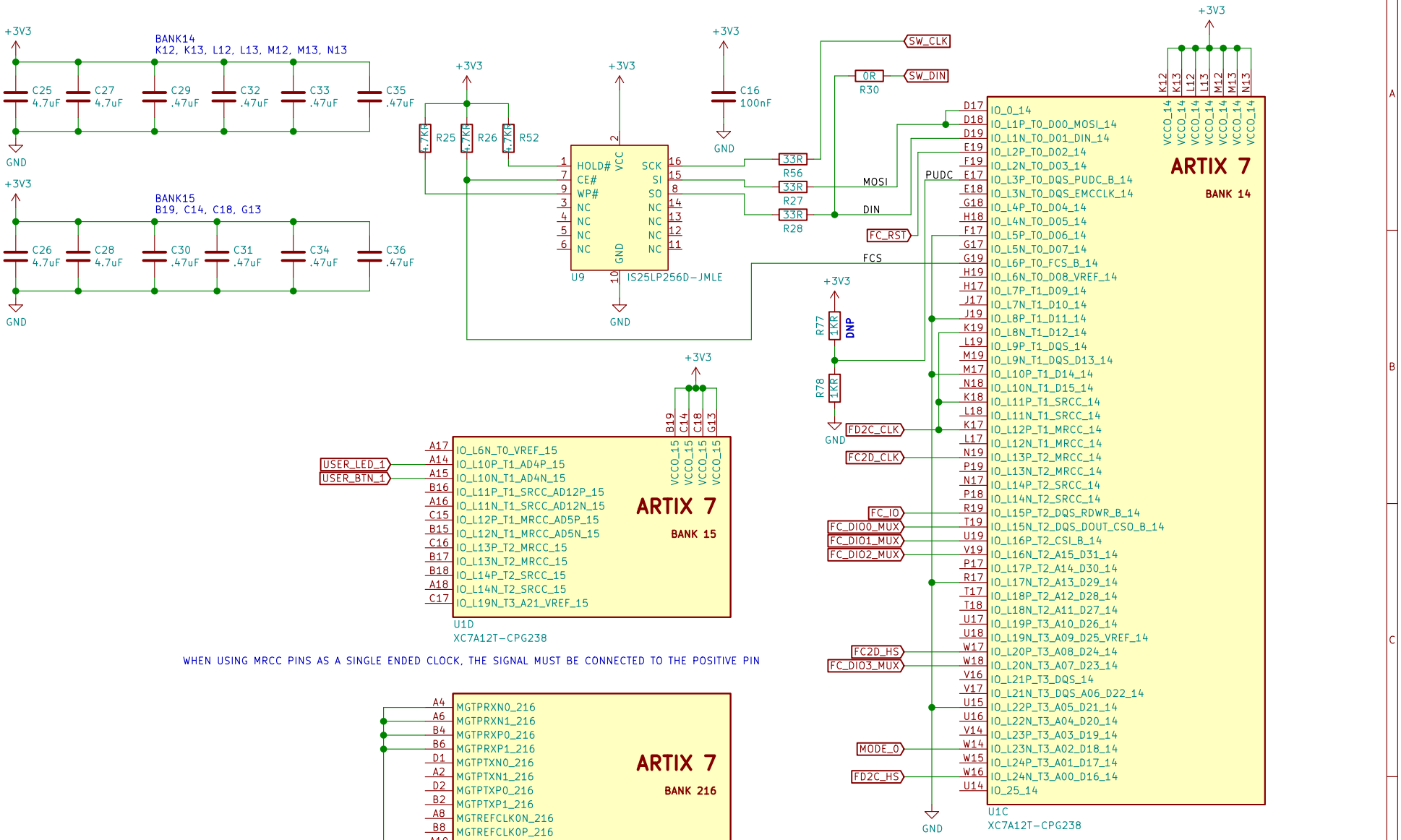
Size: USLetter	Date: 2020-07-28	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.7)-1		Id: 3/8



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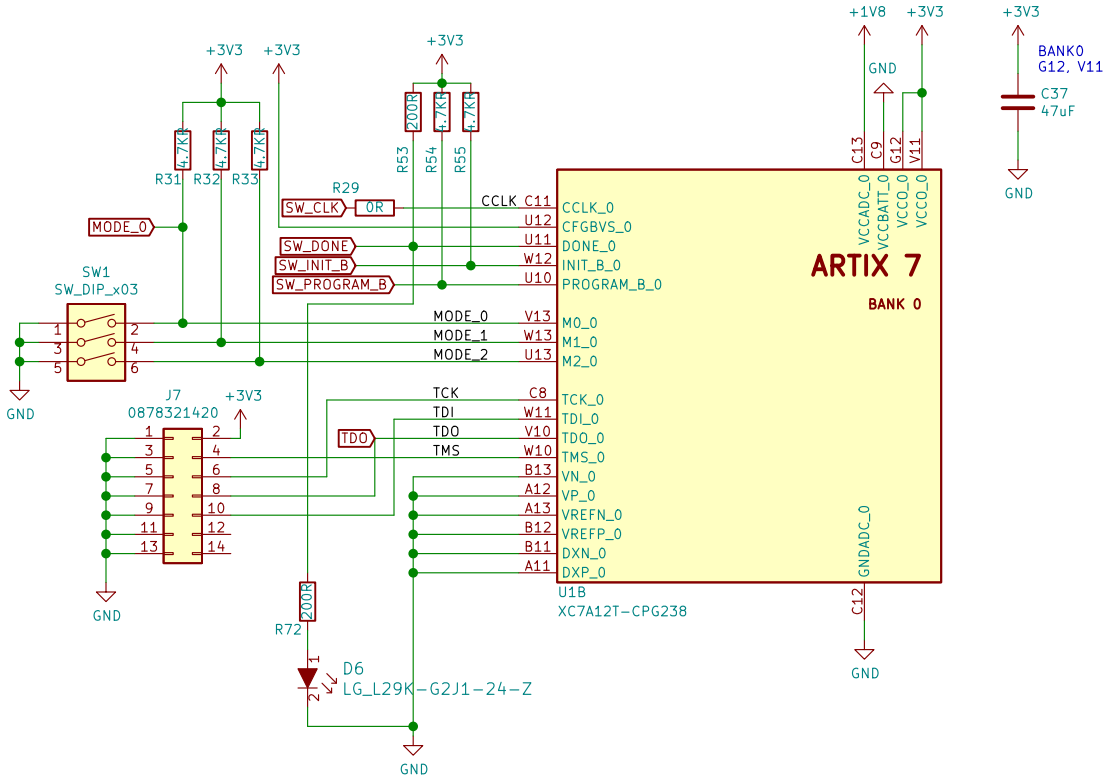
Sheet: /FPGA 1/
File: fpga 1.sch

Title: FOBOS Artix-7 a12t DUT - FPGA

Size: USLetter	Date: 2020-07-28	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.7)-1		Id: 4/8



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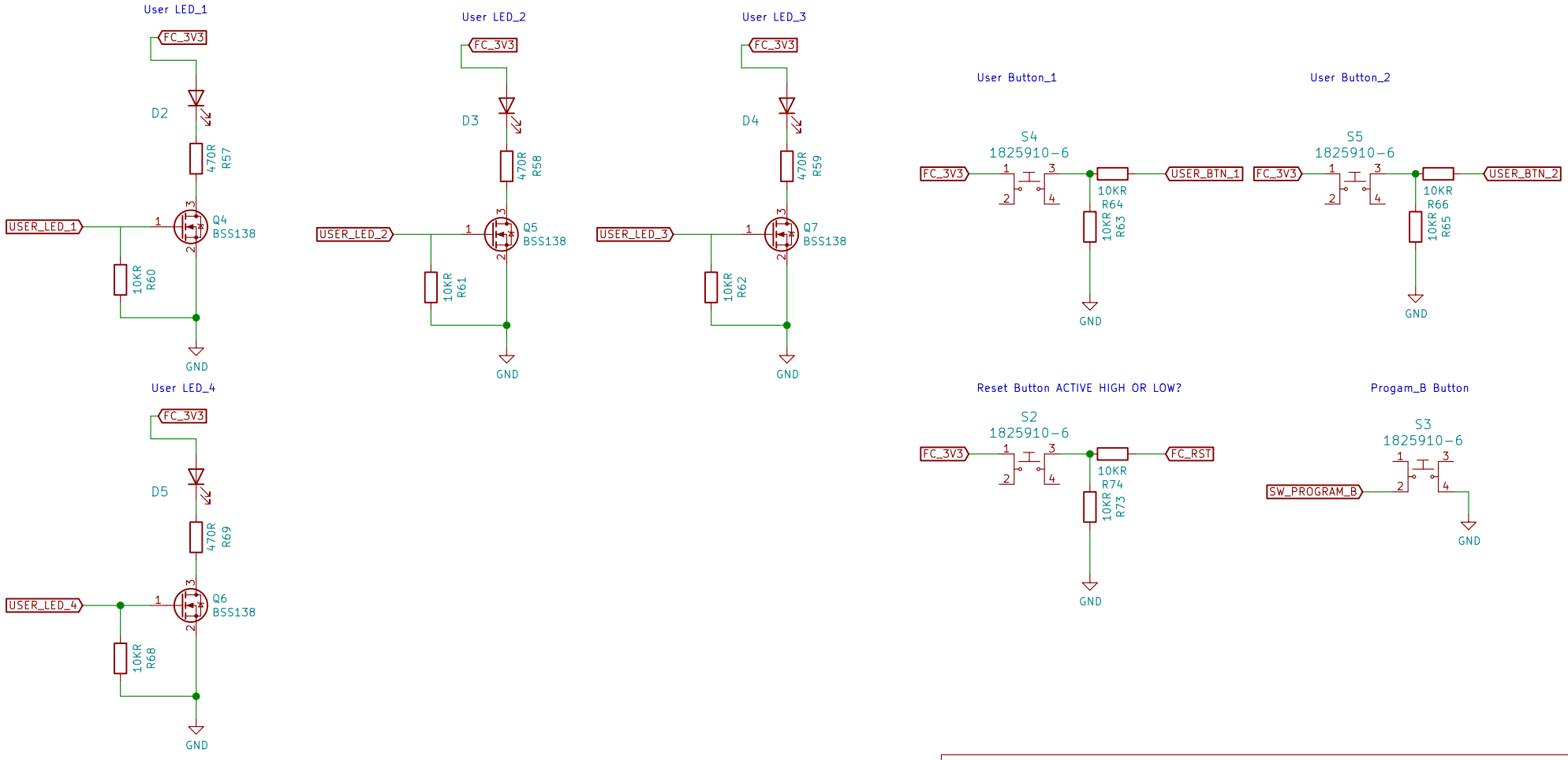
Sheet: /FPGA Programming/		
File: fpgaprog.sch		
Title: FOBOS ARTIX7-A12T-CPG238 DUT - FPGA Programming		
Size: USLetter	Date: 2020-07-28	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.7)-1		Id: 5/8



Project: FOBOS Artix-7 a12t DUT
Author: Jens-Peter Kaps, Eddie Ferrufino

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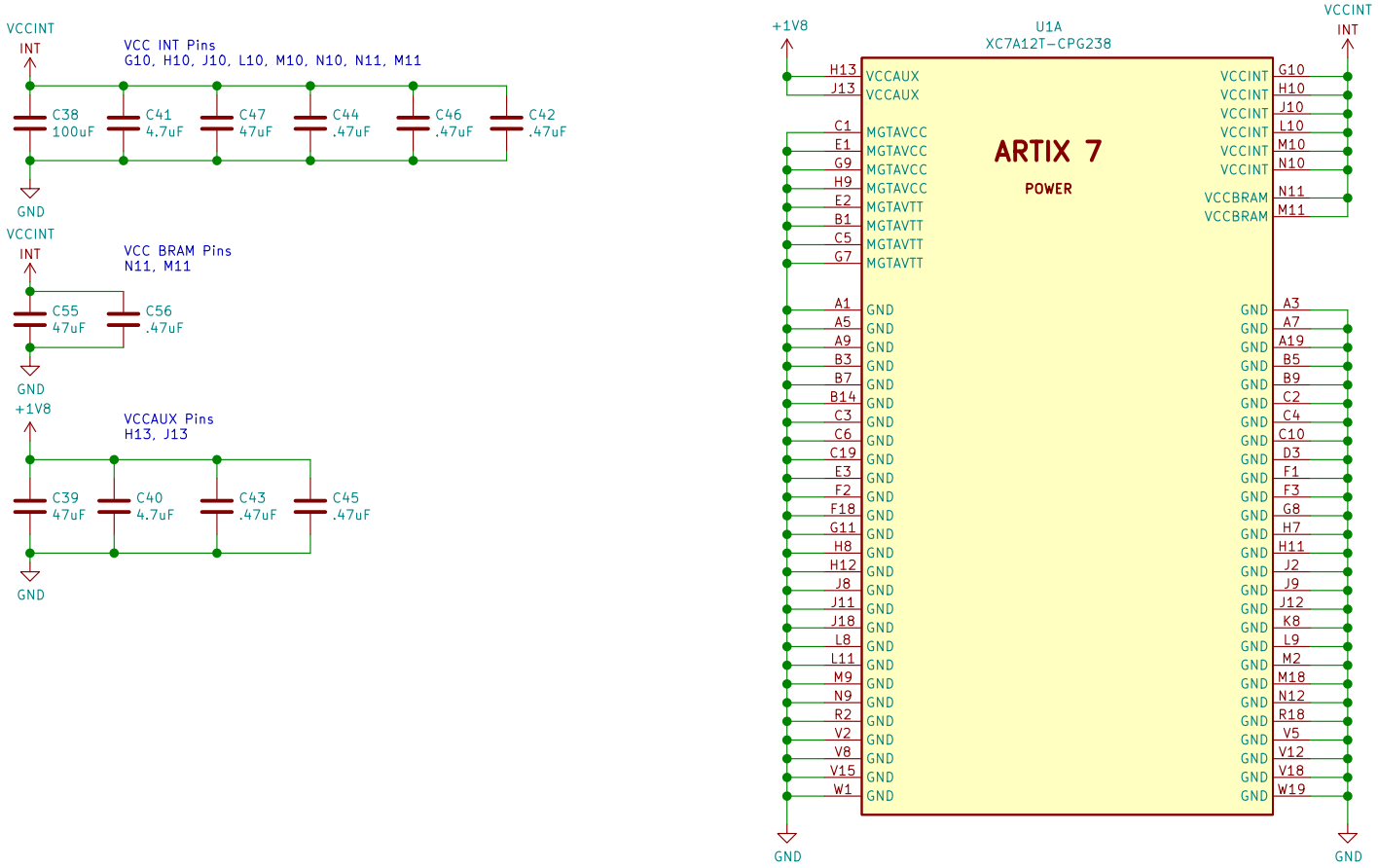
Sheet: /User Button and IO/
File: User Button and IO.sch

Title: FOBOS Artix-7 a12t DUT - User Buttons and I/O

Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.7)-1		Id: 6/8



Project: FOBOS Artix-7 a12t DUT
Author: Jens-Peter Kaps, Eddie Ferrufino

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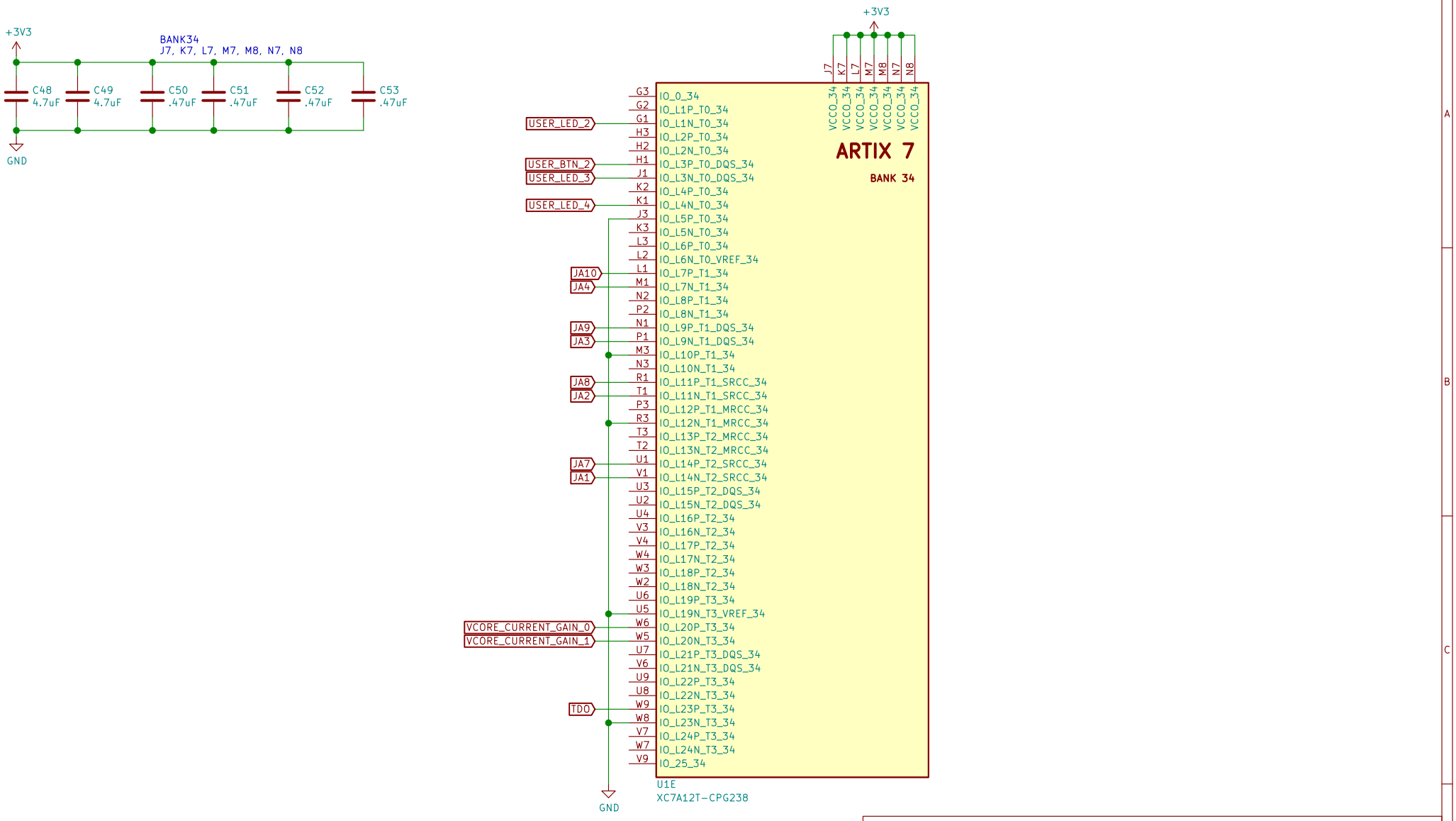
Sheet: /FPGA Power/
File: fpgapower.sch

Title: FOBOS Artix-7 a12t DUT - FPGA Power

Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.7)-1		Id: 7/8



WHEN USING MRCC PINS AS A SINGLE ENDED CLOCK, THE SIGNAL MUST BE CONNECTED TO THE POSITIVE PIN

Project: FOBOS Artix-7 a12t DUT
Author: Jens-Peter Kaps, Eddie Ferrufino

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Sheet: /FPGA 2/
File: FPGA 2.sch

Title: FOBOS Artix-7 a12t DUT - FPGA Part 2

Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.7)-1		Id: 8/8