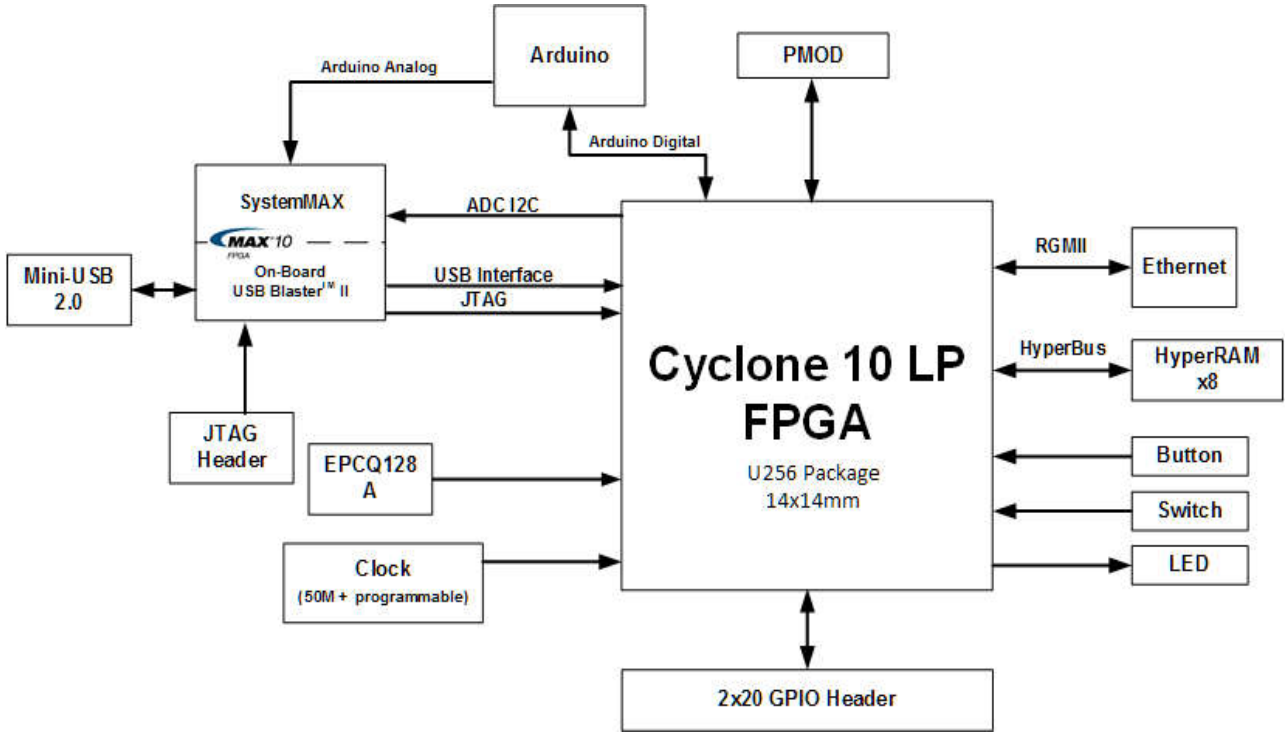
NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0321321-A1
Gerber Files	110-0321321-A1
PCB Design Files	120-0321321-A1
Assembly Drawing	130-0321321-A1
Fab Drawing	140-0321321-A1
Schematic Drawing	150-0321321-A1
PCB Film	160-0321321-A1
Bill of Materials	170-0321321-A1
Schematic Design Files	180-0321321-A1
Functional Specification	210-0321321-A1
PCB Layout Guidelines	220-0321321-A1
Assembly Rework	320-0321321-A1

REV	DATE	PAGES	DESCRIPTION
A1	08/16/17	All	Initial Release
A1.1	10/12/17	Pg.4, 6	Delete comment which may confuse users
A2	11/27/17	Pg.4	1. Change U2 from EPCQ64 to EPCQ128A 2. Add compatible HyperRAM note



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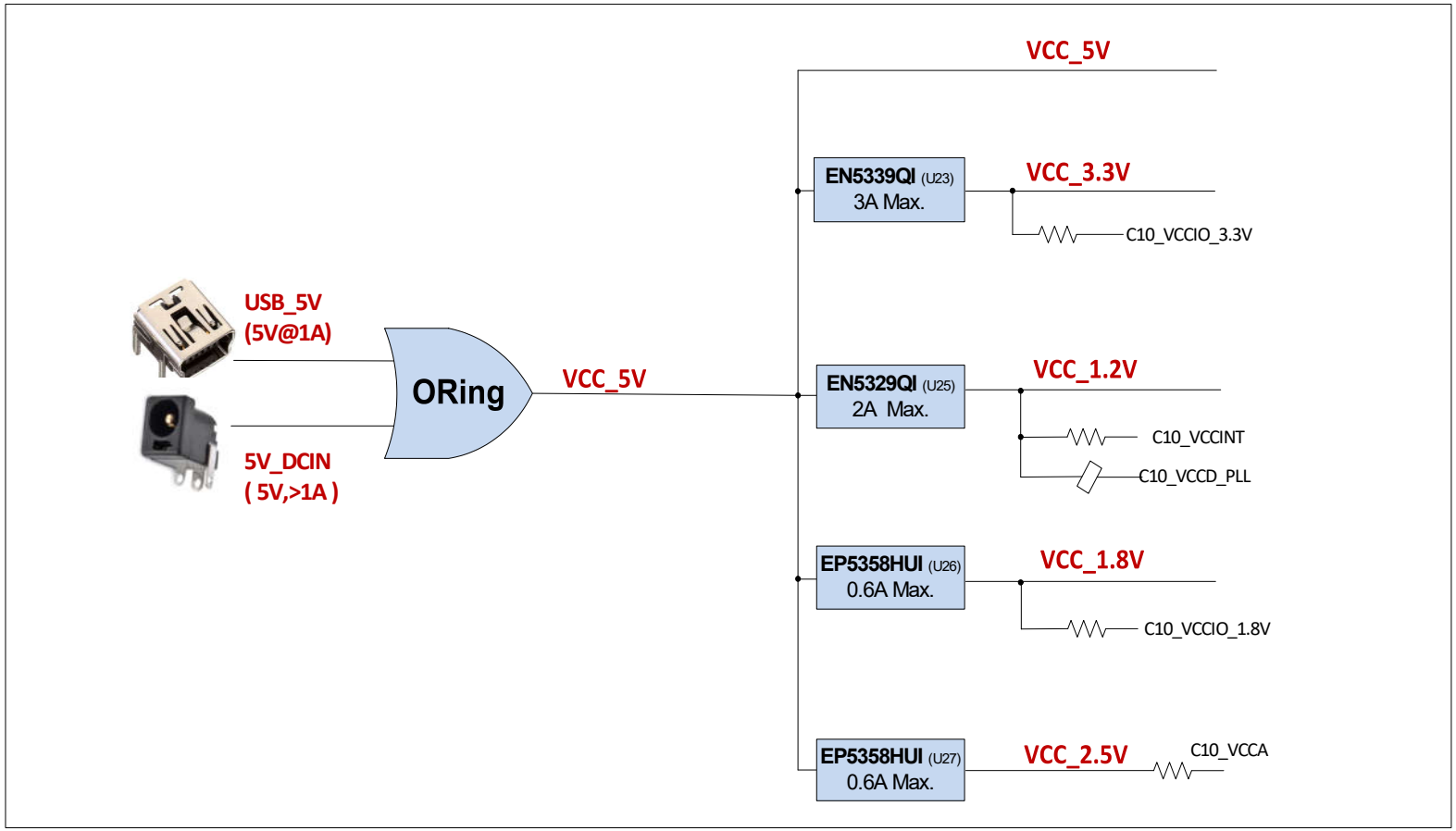
Title: **Cyclone 10 LP FPGA Evaluation Kit Board**

Size	Document Number	Rev
B	150-0321321-A1 (6XX-44504R)	A2

Date: Monday, November 27, 2017 Sheet 1 of 17



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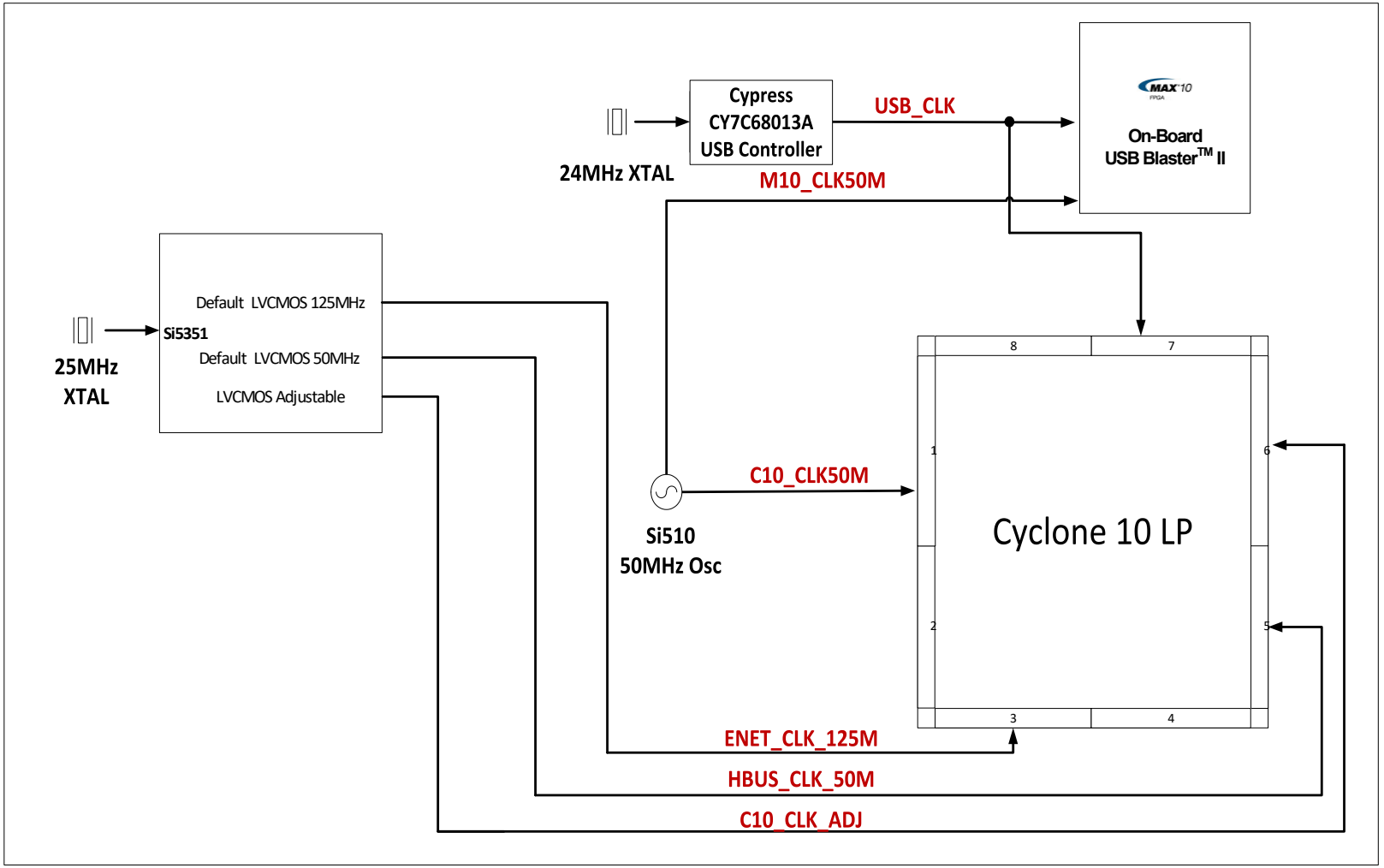
Title: Cyclone 10 LP FPGA Evaluation Kit Board

Size	Document Number	Rev
B	150-0321321-A1 (6XX-44504R)	A2

Date: Monday, November 27, 2017 Sheet 2 of 17



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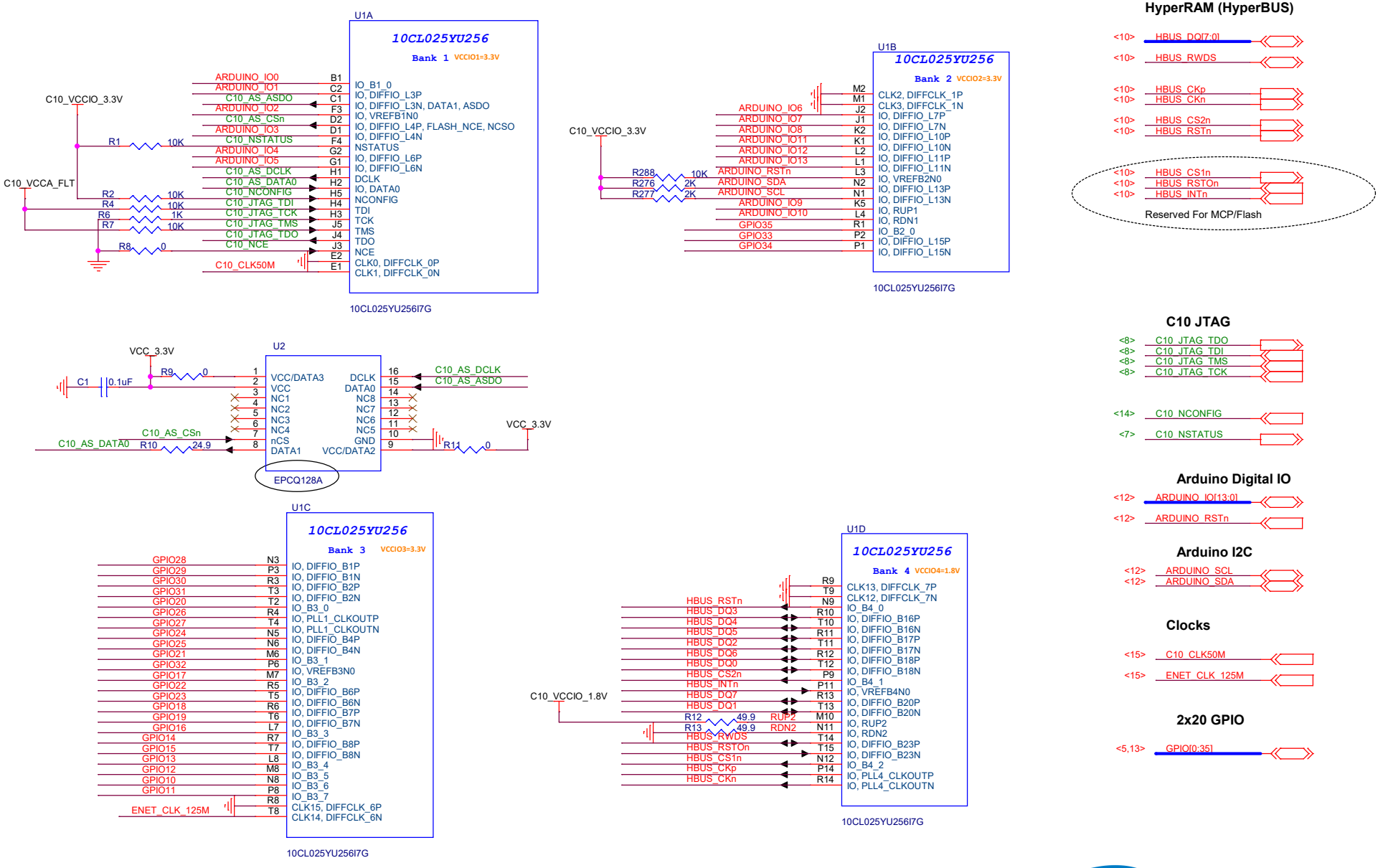
Title: Cyclone 10 LP FPGA Evaluation Kit Board

Size	Document Number	Rev
B	150-0321321-A1 (6XX-44504R)	A2

Date: Monday, November 27, 2017 Sheet 3 of 17



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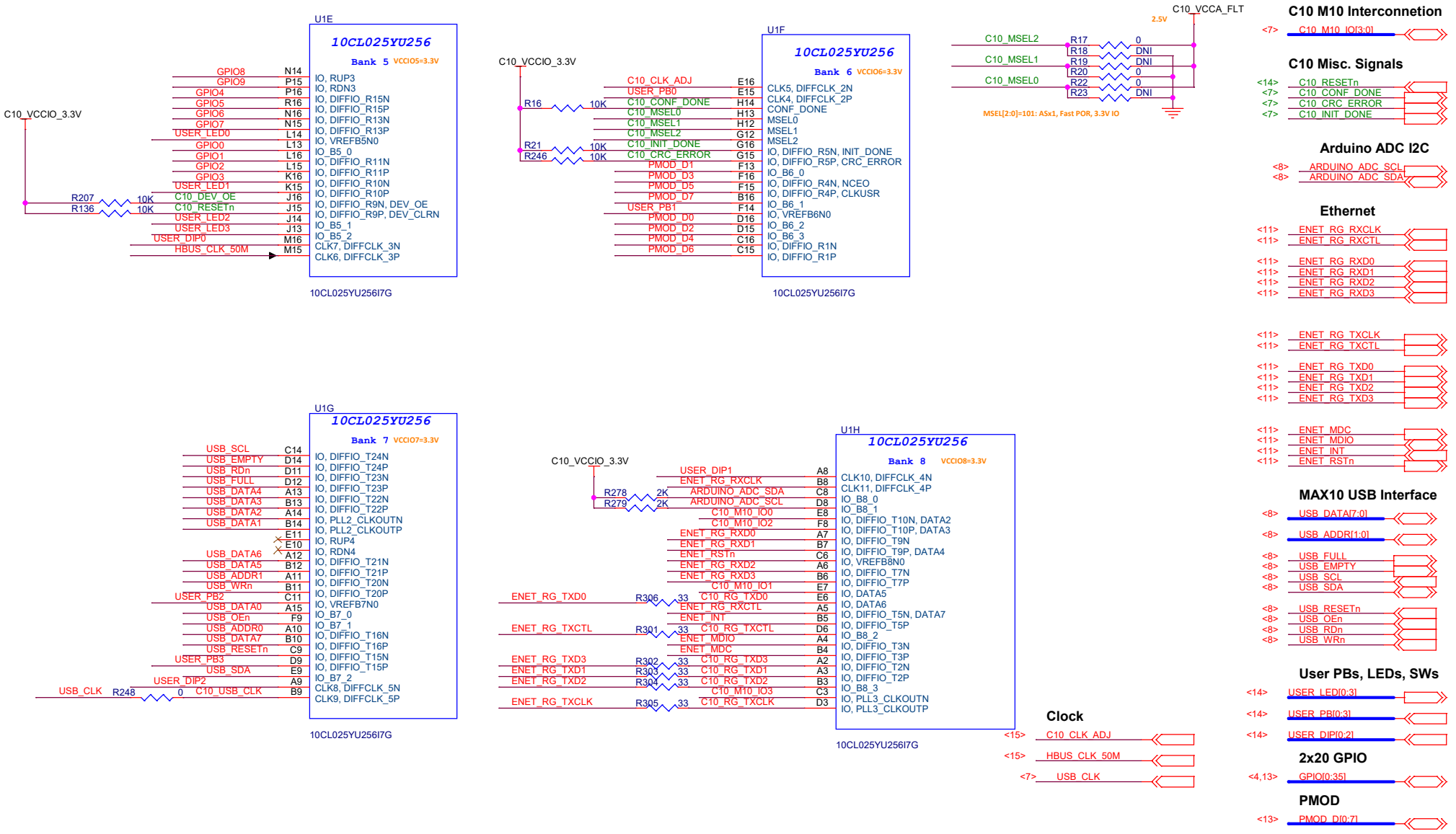
Title: **Cyclone 10 LP FPGA Evaluation Kit Board**

Size	Document Number	Rev
B	150-0321321-A1 (6XX-44504R)	A2

Date: Monday, November 27, 2017 Sheet 4 of 17


U1E
10CL025YU256
Bank 5 VCCIO5=3.3V
10CL025YU256I7G
U1F
10CL025YU256
Bank 6 VCCIO6=3.3V
10CL025YU256I7G
U1G
10CL025YU256
Bank 7 VCCIO7=3.3V
10CL025YU256I7G
U1H
10CL025YU256
Bank 8 VCCIO8=3.3V
10CL025YU256I7G
C10_VCCIO_3.3V
C10_VCCA_FLT
2.5V
MSEL[2:0]=101: ASx1, Fast POR, 3.3V IO
C10 M10 Interconnetion
C10 Misc. Signals
Arduino ADC I2C
Ethernet
MAX10 USB Interface
User PBs, LEDs, SWs
2x20 GPIO
PMOD
Clock
Intel Corporation, 301, Bibo Rd #888, Shanghai, China, 201203
Cyclone 10 LP FPGA Evaluation Kit Board
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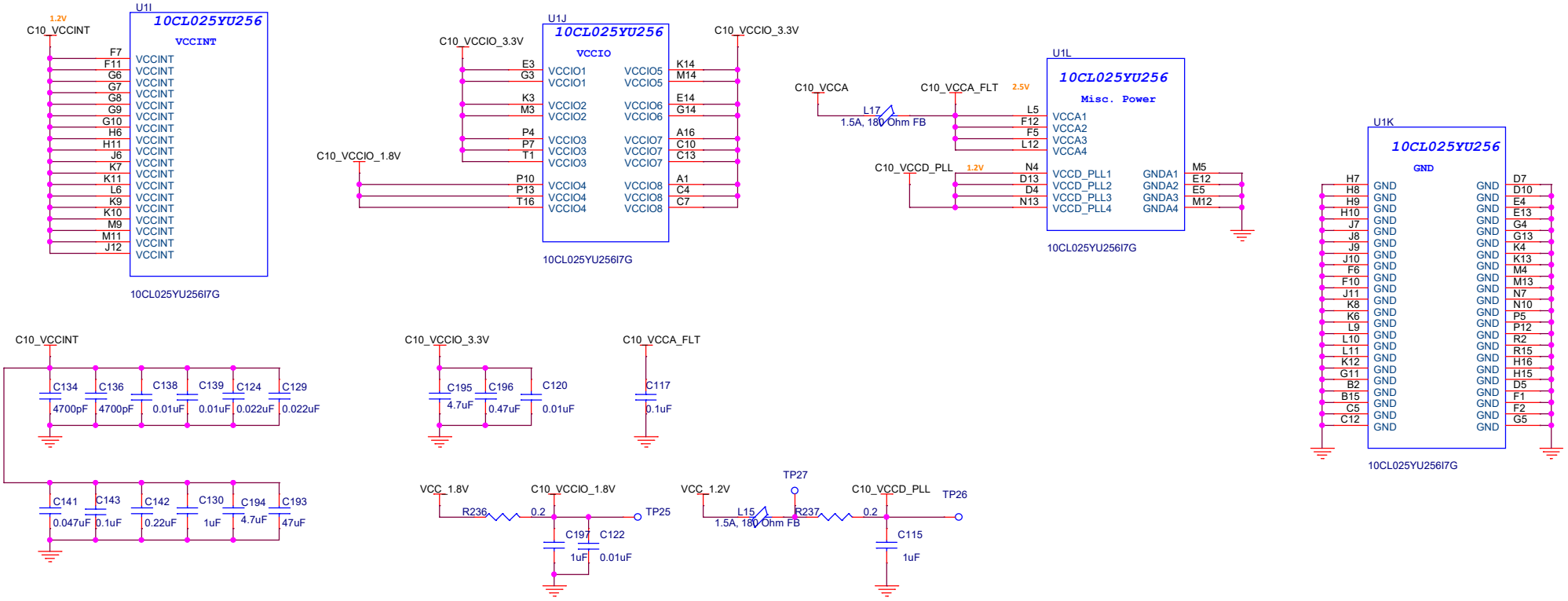
Size B
Document Number 150-0321321-A1 (6XX-44504R)
Rev A2
Date: Monday, November 27, 2017
Sheet 5 of 17



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Title: **Cyclone 10 LP FPGA Evaluation Kit Board**

Size	Document Number	Rev
B	150-0321321-A1 (6XX-44504R)	A2

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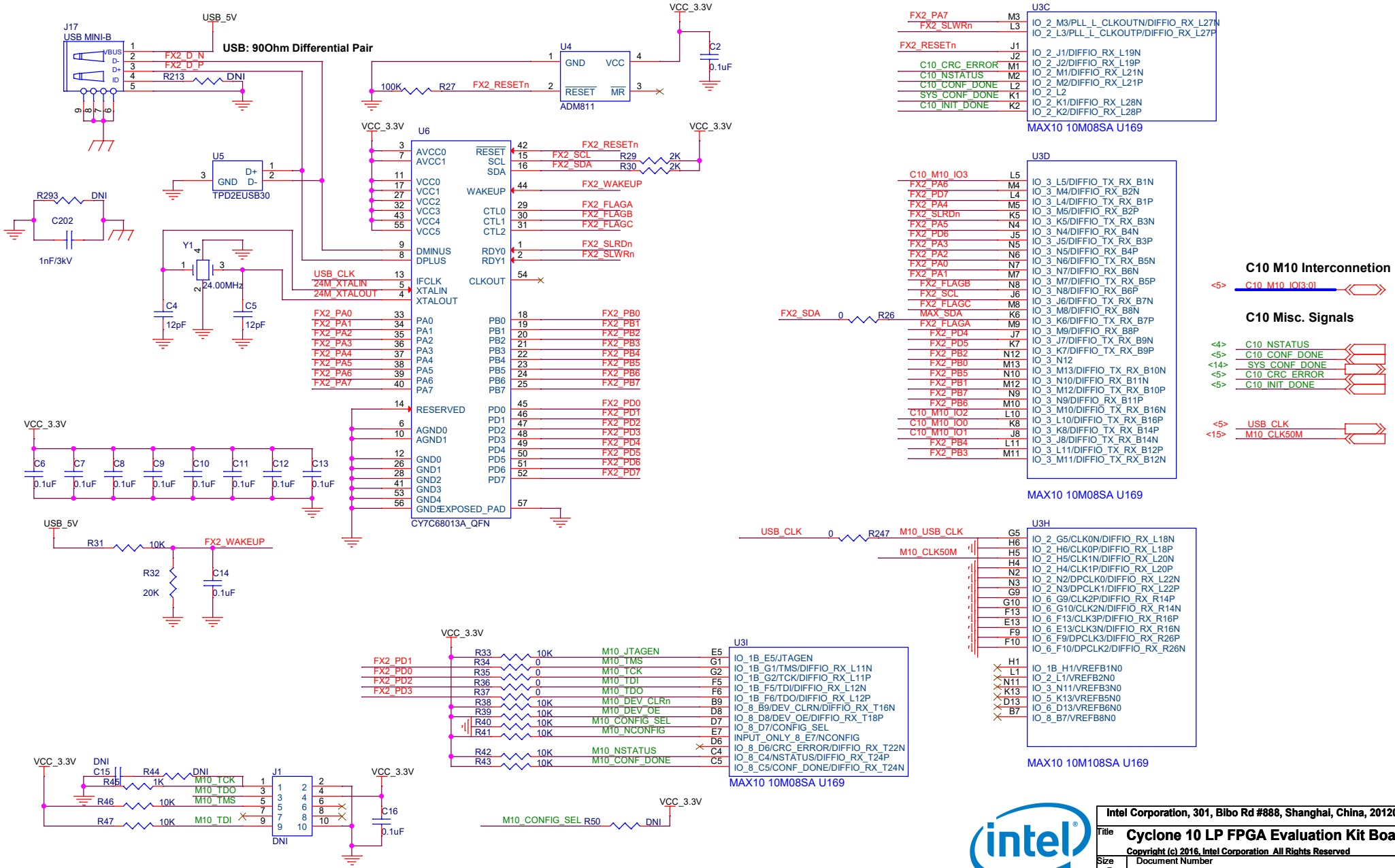
USB: 90Ohm Differential Pair
J17
USB MINI-B
USB_5V
FX2_D_N
FX2_D_P
R213
DNI
U4
GND
VCC
RESET
MR
ADM811
100K
R27
FX2_RESETn
C2
0.1uF
VCC_3.3V
U5
TPD2EUSB30
R293
C202
1nF/3kV
Y1
24.00MHz
C4
12pF
C5
12pF
U6
AVCC0
AVCC1
VCC0
VCC1
VCC2
VCC3
VCC4
VCC5
DMINUS
DPLUS
IFCLK
XTALIN
XTALOUT
RESET
SCL
SDA
WAKEUP
CTL0
CTL1
CTL2
RDY0
RDY1
CLKOUT
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
RESERVED
AGND0
AGND1
GND0
GND1
GND2
GND3
GND4
GND5
EXPOSED_PAD
CY7C68013A_QFN
FX2_RESETn
FX2_SCL
FX2_SDA
R29
R30
2K
FX2_WAKEUP
FX2_FLAGA
FX2_FLAGB
FX2_FLAGC
FX2_SLRDn
FX2_SLWRn
USB_CLK
24M_XTALIN
24M_XTALOUT
C6
C7
C8
C9
C10
C11
C12
C13
0.1uF
R31
10K
FX2_WAKEUP
R32
20K
C14
0.1uF
U3C
IO_2_M3/PLL_L_CLKOUTN/DIFFIO_RX_L27N
IO_2_L3/PLL_L_CLKOUTP/DIFFIO_RX_L27P
IO_2_J1/DIFFIO_RX_L19N
IO_2_J2/DIFFIO_RX_L19P
IO_2_M1/DIFFIO_RX_L21N
IO_2_M2/DIFFIO_RX_L21P
IO_2_L2
IO_2_K1/DIFFIO_RX_L28N
IO_2_K2/DIFFIO_RX_L28P
C10_CRC_ERROR
C10_NSTATUS
C10_CONF_DONE
SYS_CONF_DONE
C10_INIT_DONE
MAX10 10M08SA U169
U3D
IO_3_L5/DIFFIO_TX_RX_B1N
IO_3_M4/DIFFIO_RX_B2N
IO_3_L4/DIFFIO_TX_RX_B1P
IO_3_M5/DIFFIO_RX_B2P
IO_3_K5/DIFFIO_TX_RX_B3N
IO_3_N4/DIFFIO_RX_B4N
IO_3_J5/DIFFIO_TX_RX_B3P
IO_3_N5/DIFFIO_RX_B4P
IO_3_N6/DIFFIO_TX_RX_B5N
IO_3_N7/DIFFIO_RX_B6N
IO_3_M7/DIFFIO_TX_RX_B5P
IO_3_N8/DIFFIO_RX_B6P
IO_3_J6/DIFFIO_TX_RX_B7N
IO_3_M8/DIFFIO_RX_B8N
IO_3_K6/DIFFIO_TX_RX_B7P
IO_3_M9/DIFFIO_RX_B8P
IO_3_J7/DIFFIO_TX_RX_B9N
IO_3_K7/DIFFIO_TX_RX_B9P
IO_3_N12
IO_3_M13/DIFFIO_TX_RX_B10N
IO_3_N10/DIFFIO_RX_B11N
IO_3_M12/DIFFIO_TX_RX_B10P
IO_3_N9/DIFFIO_RX_B11P
IO_3_M10/DIFFIO_TX_RX_B16N
IO_3_L10/DIFFIO_TX_RX_B16P
IO_3_K8/DIFFIO_TX_RX_B14P
IO_3_J8/DIFFIO_RX_B14N
IO_3_L11/DIFFIO_TX_RX_B12P
IO_3_M11/DIFFIO_TX_RX_B12N
C10_M10_IO3
C10_M10_IO2
C10_M10_IO0
C10_M10_IO1
FX2_SDA
R26
MAX10 10M08SA U169
C10 M10 Interconnetion
C10_M10_IO[3:0]
C10 Misc. Signals
C10_NSTATUS
C10_CONF_DONE
SYS_CONF_DONE
C10_CRC_ERROR
C10_INIT_DONE
USB_CLK
M10_CLK50M
U3H
IO_2_G5/CLK0N/DIFFIO_RX_L18N
IO_2_H6/CLK0P/DIFFIO_RX_L18P
IO_2_H5/CLK1N/DIFFIO_RX_L20N
IO_2_H4/CLK1P/DIFFIO_RX_L20P
IO_2_N2/DPCLK0/DIFFIO_RX_L22N
IO_2_N3/DPCLK1/DIFFIO_RX_L22P
IO_6_G9/CLK2P/DIFFIO_RX_R14P
IO_6_G10/CLK2N/DIFFIO_RX_R14N
IO_6_F13/CLK3P/DIFFIO_RX_R16P
IO_6_E13/CLK3N/DIFFIO_RX_R16N
IO_6_F9/DPCLK3/DIFFIO_RX_R26P
IO_6_F10/DPCLK2/DIFFIO_RX_R26N
IO_1B_H1/VREFB1N0
IO_2_L1/VREFB2N0
IO_3_N11/VREFB3N0
IO_5_K13/VREFB5N0
IO_6_D13/VREFB6N0
IO_8_B7/VREFB8N0
USB_CLK
M10_USB_CLK
R247
M10_CLK50M
MAX10 10M108SA U169
U3I
IO_1B_E5/JTAGEN
IO_1B_G1/TMS/DIFFIO_RX_L11N
IO_1B_G2/TCK/DIFFIO_RX_L11P
IO_1B_F5/TDI/DIFFIO_RX_L12N
IO_1B_F6/TDO/DIFFIO_RX_L12P
IO_8_B9/DEV_CLRN/DIFFIO_RX_T16N
IO_8_D8/DEV_OE/DIFFIO_RX_T18P
IO_8_D7/CONFIG_SEL
INPUT_ONLY_8_E7/NCONFIG
IO_8_D6/CRC_ERROR/DIFFIO_RX_T22N
IO_8_C4/NSTATUS/DIFFIO_RX_T24P
IO_8_C5/CONF_DONE/DIFFIO_RX_T24N
MAX10 10M08SA U169
FX2_PD1
FX2_PD0
FX2_PD2
FX2_PD3
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
10K
0
M10_JTAGEN
M10_TMS
M10_TCK
M10_TDI
M10_TDO
M10_DEV_CLRn
M10_DEV_OE
M10_CONFIG_SEL
M10_NCONFIG
M10_NSTATUS
M10_CONF_DONE
J1
M10_TCK
M10_TDO
M10_TMS
M10_TDI
R45
R46
R47
R44
C15
1K
C16
0.1uF
M10_CONFIG_SEL
R50
Intel Corporation, 301, Bibo Rd #888, Shanghai, China, 201203
Title
Cyclone 10 LP FPGA Evaluation Kit Board
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Size
B
Document Number
150-0321321-A1
(6XX-44504R)
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A2
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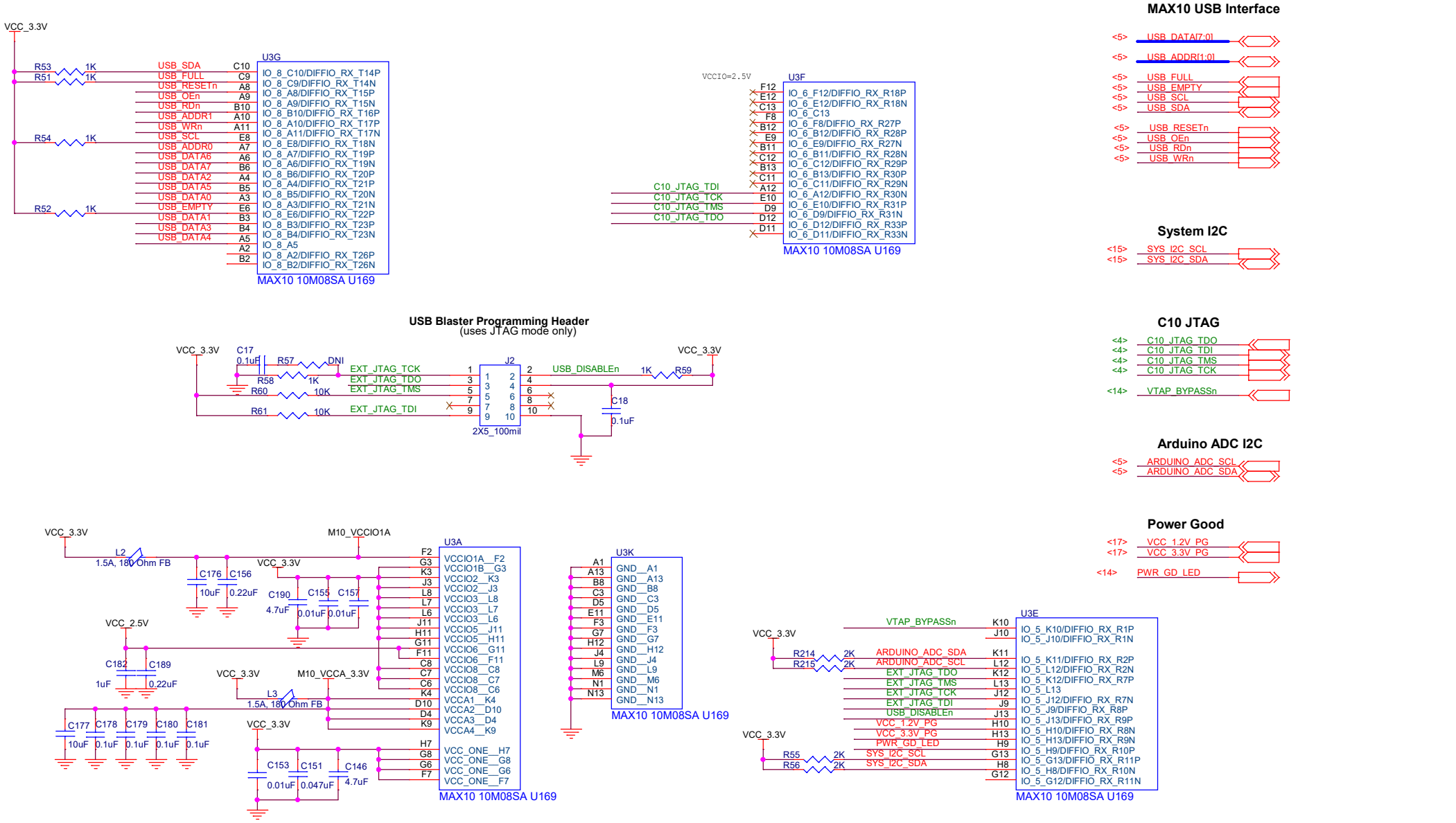
7
of
17



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Title: Cyclone 10 LP FPGA Evaluation Kit Board			
Size: B	Document Number: 150-0321321-A1 (6XX-44504R)		Rev: A2
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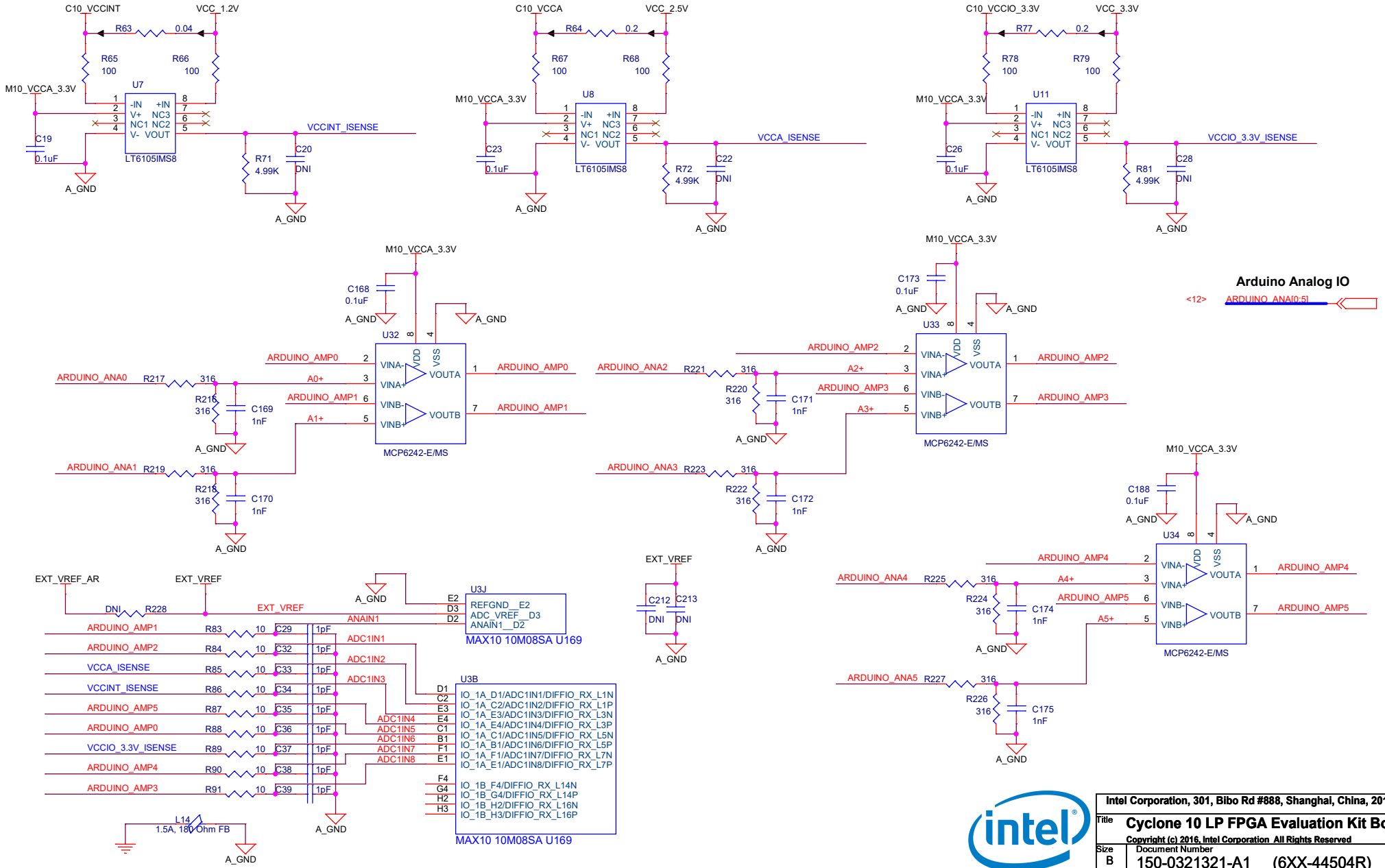

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Title: Cyclone 10 LP FPGA Evaluation Kit Board

Size	Document Number	Rev
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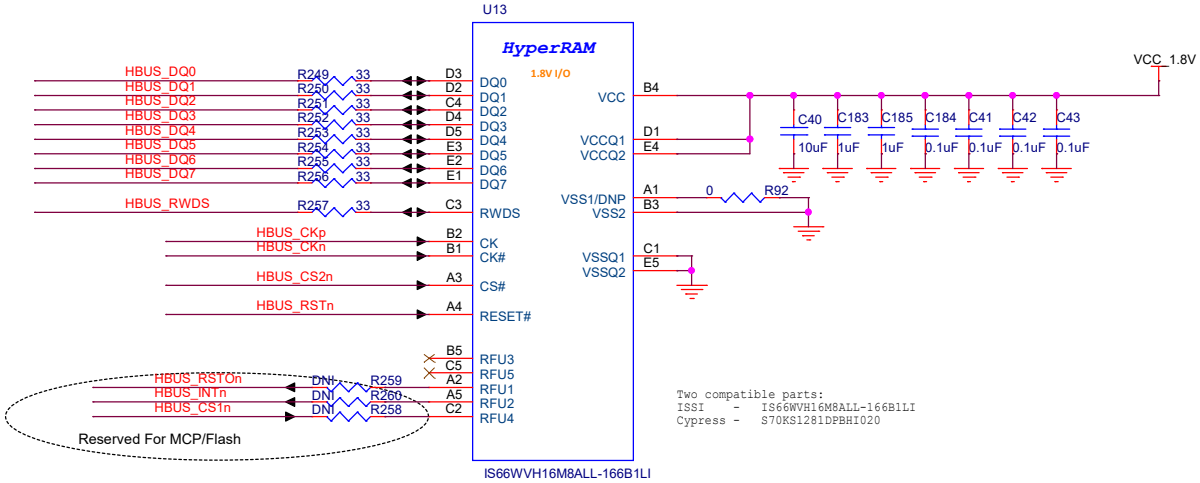
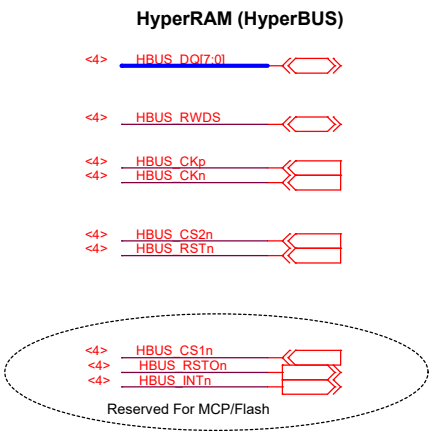
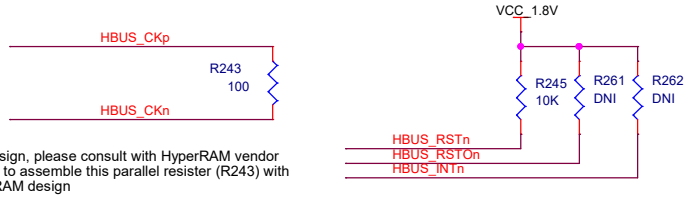


Two compatible parts:
ISSI - IS66WVH16M8ALL-166B1LI
Cypress - S70KS1281DPBHI020

HBUS_CS1n: For Flash (Reserved)
HBUS_CS2n: For RAM





In customer's design, please consult with HyperRAM vendor to decide if need to assemble this parallel resister (R243) with specified HyperRAM design

Title: Cyclone 10 LP FPGA Evaluation Kit Board

Size	Document Number	Rev
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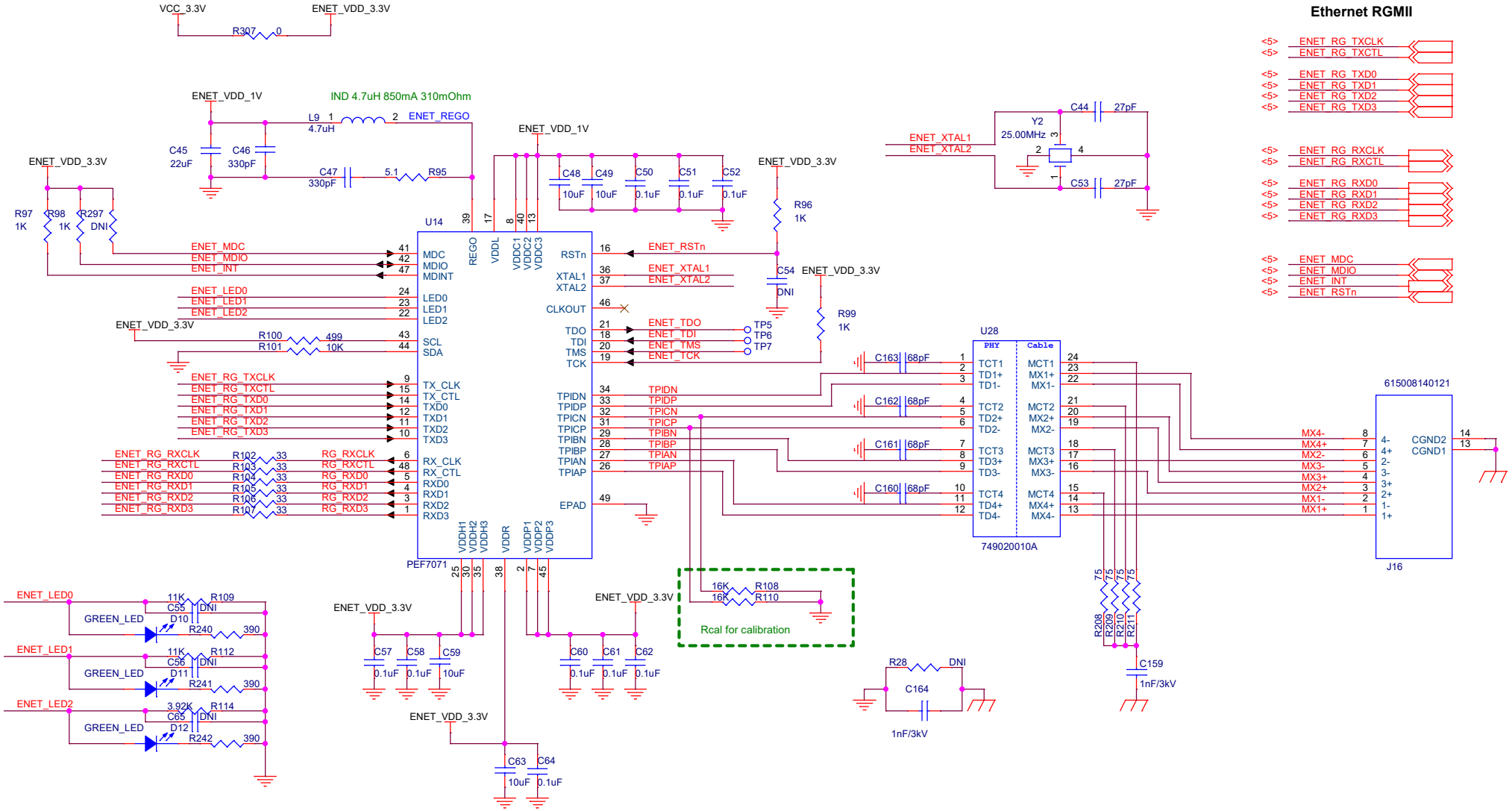

	CBV[3]		CBV[2]		CBV[1]		CBV[0]		Rcfg + Ccfg
LED0	ADR[3]	0	ADR[2]	0	ADR[1]	0	ADR[0]	0	11K+DNI
LED1	ADR[4]	0	MODE[1]	0	MODE[0]	0	FLOW	0	11K+DNI
LED2	CONF[1]	0	CONF[0]	1	ANEG[1]	0	ANEG[0]	0	3.92K+DNI

NET	ON	OFF	Blink
NET_LED0	Link-up	Link-down	Traffc
NET_LED1	100Mbps	Other Status	N/A
NET_LED2	1000Mbps	Other Status	N/A

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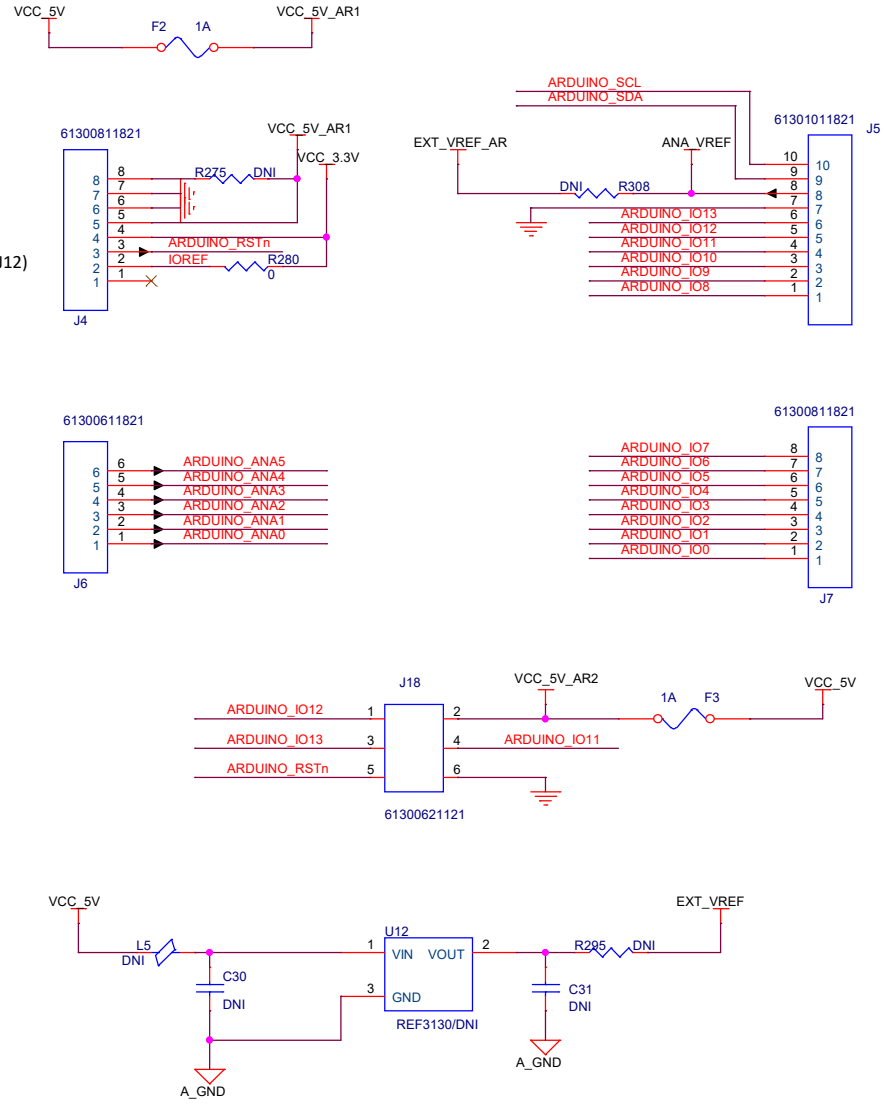
Arduino Power Output Capability
3.3V: J4.2, J4.4 100mA Max. total
5V: J4.5, J18.2 500mA Max. total
Using external adaptor power input (J12)



Arduino Digital IO

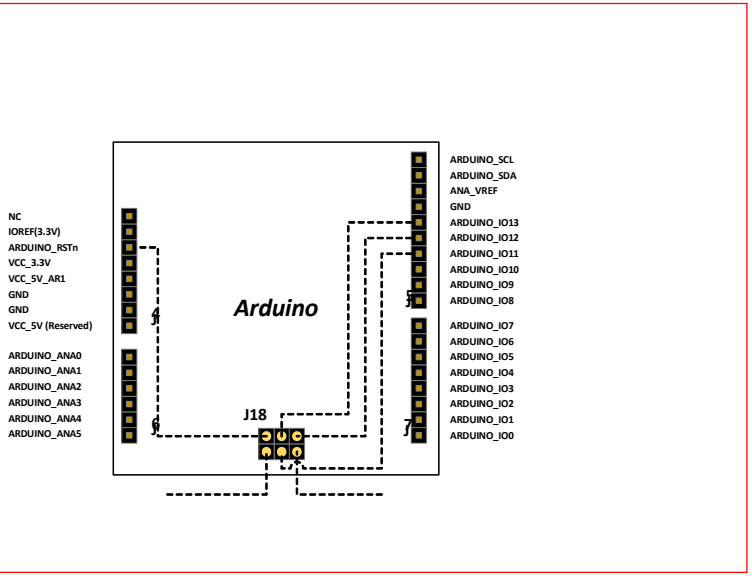
<4> ARDUINO_IO[13:0]
<4> ARDUINO_RSTn

Arduino Analog IO

<9> ARDUINO_ANA[0:5]

Arduino I2C

<4> ARDUINO_SCL
<4> ARDUINO_SDA



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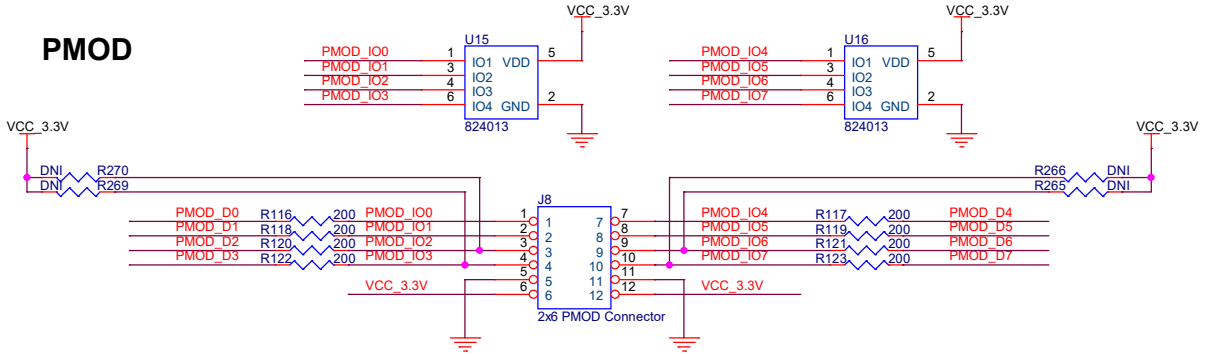
PMOD



PMOD Specification not specified module power consumption but assumed no more than approximately 100mA.

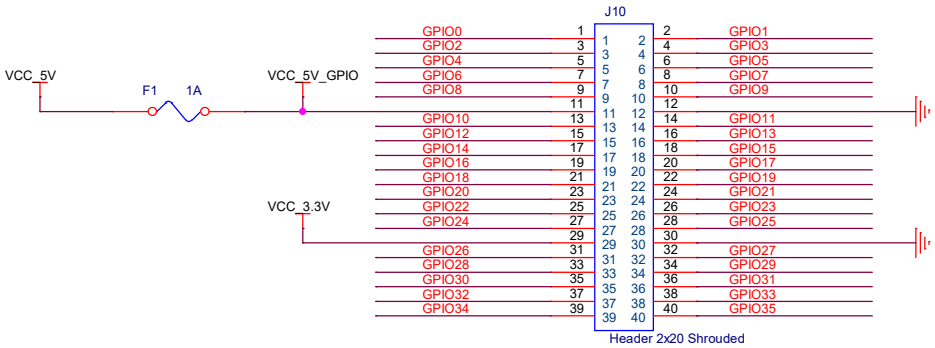
PMOD

<5> PMOD_D[0:7]

2x20 GPIO

<4,5> GPIO[0:35]

2x20pin GPIO Header



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Title: **Cyclone 10 LP FPGA Evaluation Kit Board**

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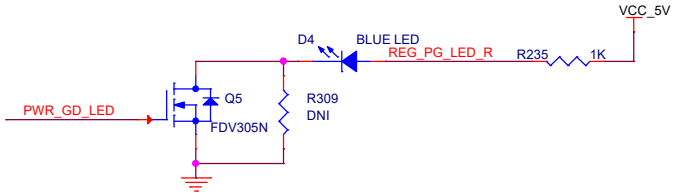
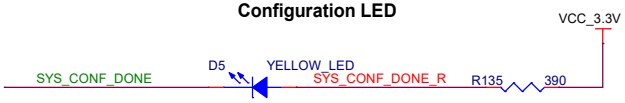
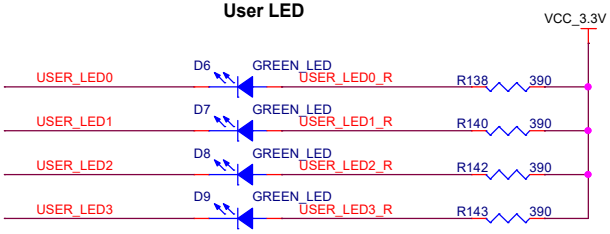
POWER LED



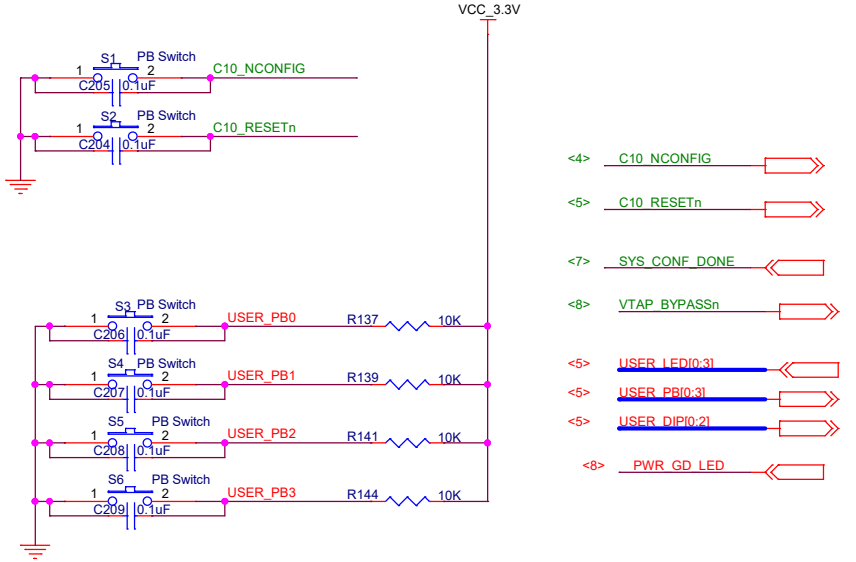
Configuration LED



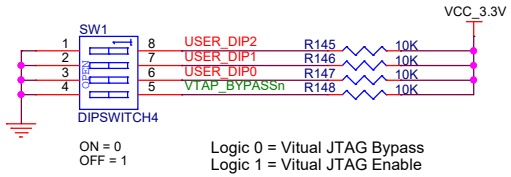
User LED



Push Buttons



DIP Switches



ON = 0
OFF = 1

Logic 0 = Vitual JTAG Bypass
Logic 1 = Vitual JTAG Enable

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Title: **Cyclone 10 LP FPGA Evaluation Kit Board**

Size	Document Number	Rev
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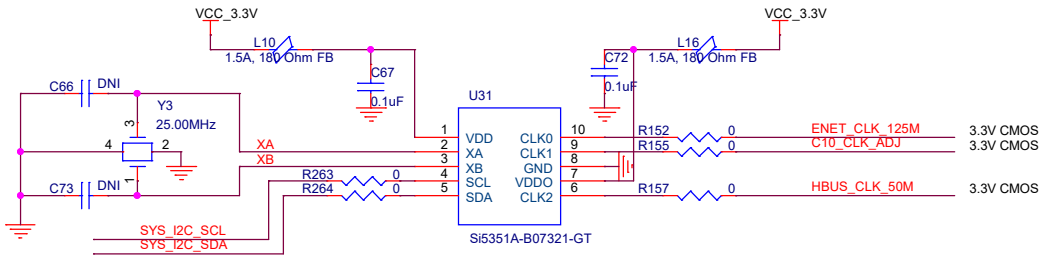
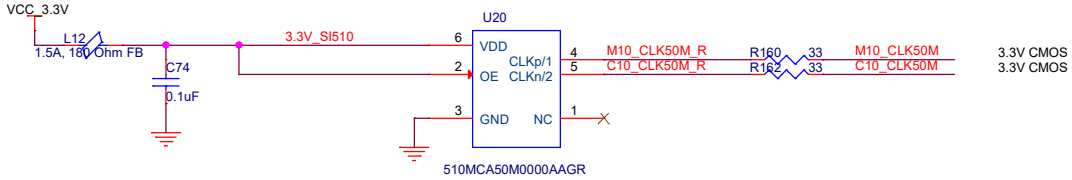
Si5351A

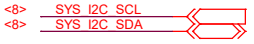


Use Clock GUI to Program Si5351A
Default Prequency:
CLK0: 125MHz
CLK1: 100MHz
CLK2: 50MHz
I2C Address: 0x60

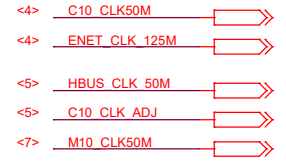
50MHz Oscillator



System I2C



Clocks



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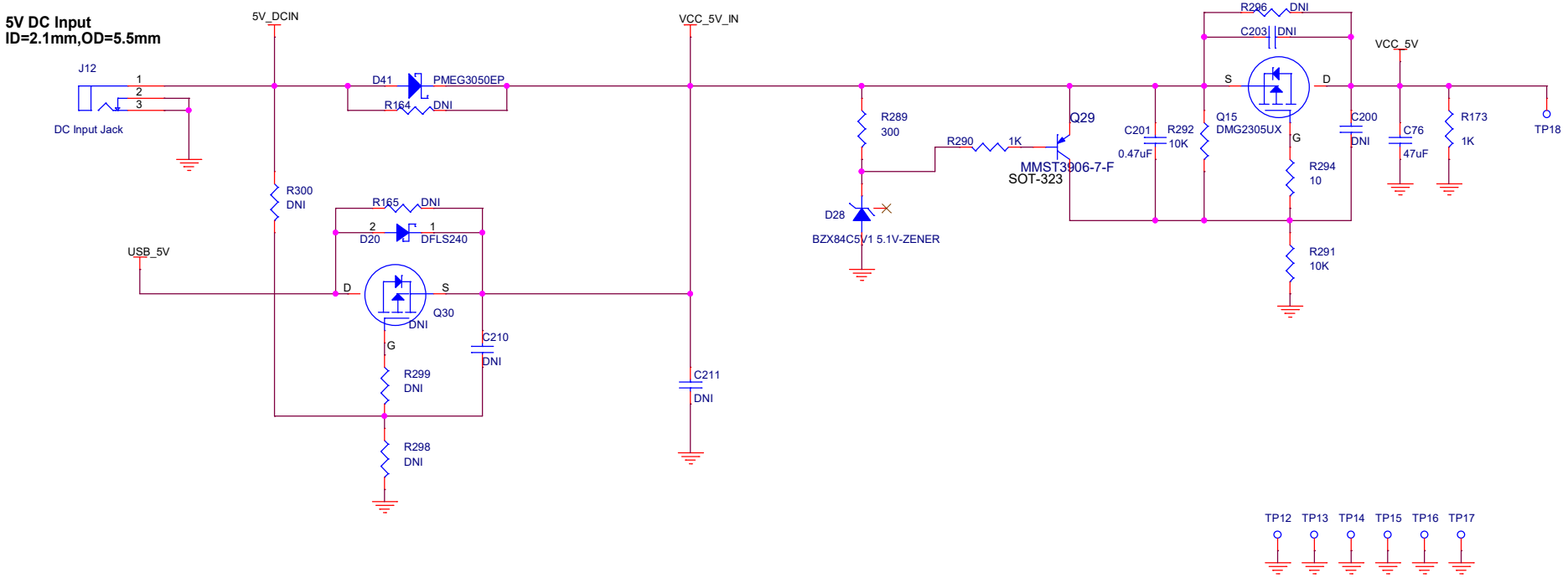
5V Input Selection, Protection and Control



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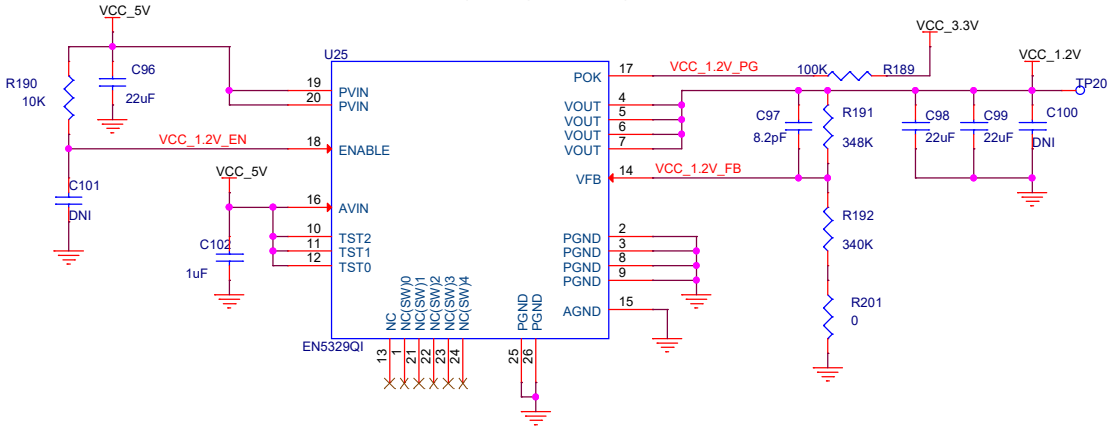
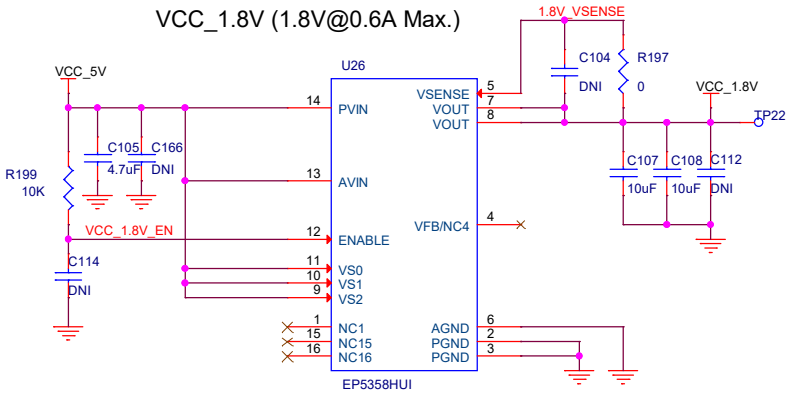
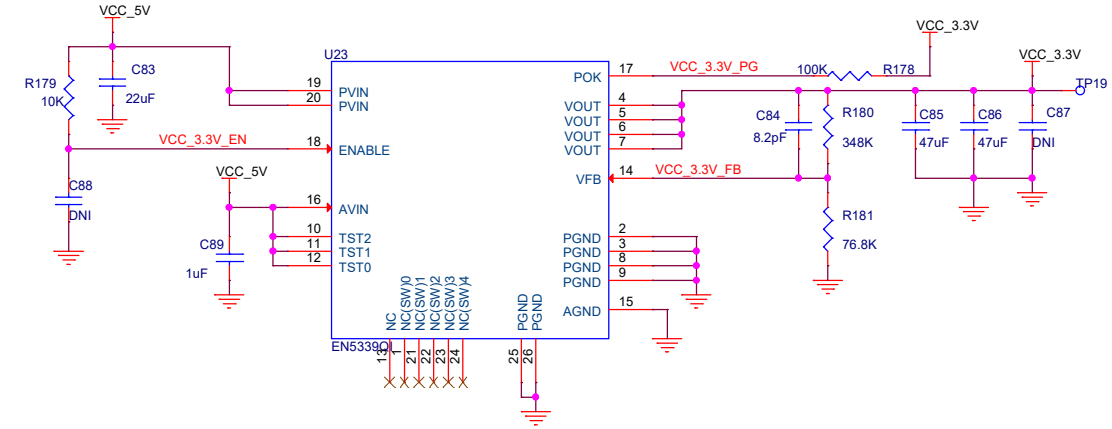
VCC_1.2V (1.2V@2A Max.)



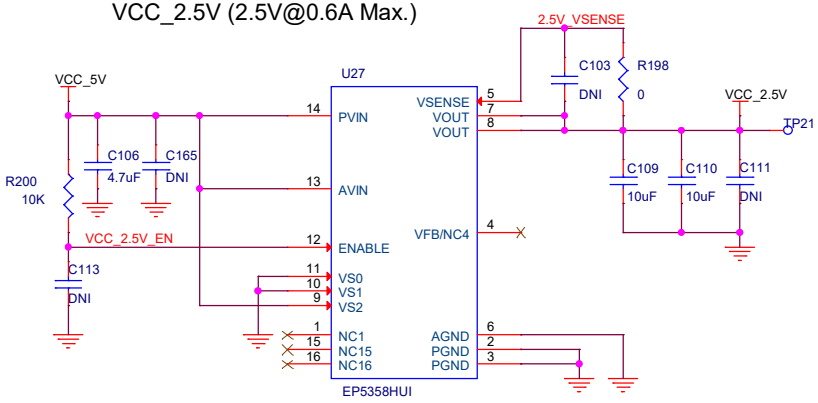
VCC_1.8V (1.8V@0.6A Max.)



VCC_3.3V (3.3V@3A Max.)



VCC_2.5V (2.5V@0.6A Max.)



<8> VCC_3.3V_PG

<8> VCC_1.2V_PG

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