# PCB Stackup Design Considerations for Intel® FPGAs

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intel.

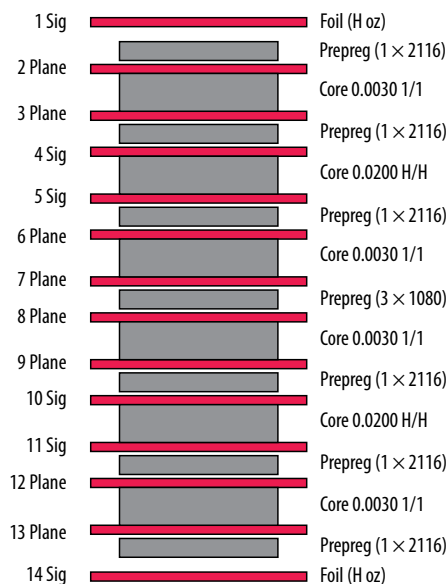# 1. PCB Stackup Design Considerations for Intel® FPGAs

This application note presents an overview of the PCB stackup construction and material selection criteria. It discusses the important material parameters that influence the electrical performance and manufacturability of the design, as well as layer usage and the importance of layer organization within the stackup for arriving at a well-designed PCB. Cost consideration is also discussed where applicable. Finally, specific recommendations and requirements for Intel® FPGAs, including the Stratix®, Arria®, MAX®, and Cyclone® device families, are listed at the end of this app note.

The PCB stackup design plays a central part in the overall system performance, especially with high-performance FPGAs that incorporate transceiver technology. The PCB stackup is the substrate upon which all design components are assembled. A poorly designed PCB stackup with inappropriately selected materials can degrade the electrical performance of signal transmission, power delivery, manufacturability, and long term reliability of the finished product. To successfully design PCB stackups for FPGA designs, you must have a good understanding of both PCB construction and the factors that influence material selection and cost.

## 1.1. PCB Stackup Construction

A typical PCB stackup is constructed from multiple alternating layers of core, prepreg, and copper foil materials heat-pressed and glued together.

**Figure 1. Cross-section of a 14-Layer PCB Stackup**

| Layer | Material |
|---|---|
| 1 Sig | Foil (H oz) |
| | Prepreg (1 × 2116) |
| 2 Plane | |
| | Core 0.0030 1/1 |
| 3 Plane | |
| | Prepreg (1 × 2116) |
| 4 Sig | |
| | Core 0.0200 H/H |
| 5 Sig | |
| | Prepreg (1 × 2116) |
| 6 Plane | |
| | Core 0.0030 1/1 |
| 7 Plane | |
| | Prepreg (3 × 1080) |
| 8 Plane | |
| | Core 0.0030 1/1 |
| 9 Plane | |
| | Prepreg (1 × 2116) |
| 10 Sig | |
| | Core 0.0200 H/H |
| 11 Sig | |
| | Prepreg (1 × 2116) |
| 12 Plane | |
| | Core 0.0030 1/1 |
| 13 Plane | |
| | Prepreg (1 × 2116) |
| 14 Sig | Foil (H oz) |

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The PCB manufacturer purchases the core material as a thin dielectric with copper clad foils bonded to both sides. The core's dielectric is a cured (hardened) fiberglass-weave material with epoxy resin that acts as an insulation layer between the copper foils. For core materials, the foils form the internal copper layers (signal or plane) in the PCB. Prepreg is an uncured fiberglass-epoxy resin weave that acts as the insulation between core layers and is the gluing agent for the cores. During the PCB manufacturing process, multiple core and prepreg layers are combined with a top and bottom copper foil sheet. The combined layers are heat-pressed together to build the complete PCB stackup. The heat-press treatment cures the prepreg and binds all the different layers together to form the PCB.

## 1.2. Material Selection

The complex FPGA boards that incorporate the Stratix 10 device families of transceiver technologies require higher layer counts as well as lower loss materials to run at up to 56 Gbps. High layer count facilitates the high density signal break-out, routing, and power distribution, while the high-performance low-loss material is required to successfully transmit and receive 10 Gbps+ transceiver data rates over extended backplane channel lengths. High layer count PCBs often suffer from lamination and drilling challenges in the PCB manufacturing process. Together with low-loss materials, they put added cost pressure on the system designer. To meet these challenges, designers must understand the material properties that influence signal loss and PCB manufacturability in order to properly select the best performance material at the lowest cost for a successful and robust design.

## 1.2.1. Material Loss Considerations

At low data rates, signal loss is caused mainly by impedance mismatches and less so by dielectric absorption and conductor losses from the material. Impedance mismatch is well understood by design engineers who regularly specify controlled impedance traces by tightly managing trace geometries, separation, and routes during the layout design. However, at data rates of 10 Gbps and above, material loss becomes very important and controlled dielectric construction must be considered during the design process. To mitigate loss caused by the material, the following material parameters must be considered during the material selection process:

- Relative Dielectric Constant
- Loss Tangent
- Fiberglass Weave Composition
- Skin Effect

These material parameters have significant impact on the electrical properties. Therefore, you should consider them as critical parameters during the stackup design.

### Related Information

- Relative Dielectric Constant on page 5
- Loss Tangent on page 5
- Fiberglass Weave Composition on page 7
- Skin Effect on page 8

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### 1.2.1.1. Relative Dielectric Constant

The relative dielectric constant ($\varepsilon_r$) is a measure of a material's ability to be polarized by an electric field and store electrostatic energy, as well as its ability to facilitate signal propagation. The relative dielectric constant varies with frequency. Material datasheets often refer to this parameter as Dk. Low $\varepsilon_r$ or Dk materials make excellent insulators and are good for isolating signals on adjacent layers.

From a board designer's perspective, the benefits of a lower dielectric constant include the following:

- Better insulation
- Faster signal propagation through the material
- Higher trace impedance for a given trace geometry
- Smaller stray trace capacitance

PCB manufacturers typically characterize $\varepsilon_r$ at 1 MHz. However, the dielectric constant of a material is generally a function of its frequency. As frequency increases, $\varepsilon_r$ is reduced. Because of this non-uniformity, a transmission line's impedance can vary from its calculated value at 1 MHz, causing it to differ from what a propagating signal actually sees on the channel. As board designer, you should get the Dk value at high frequency range for using the high data rates signal on the board.

Because digital signals are comprised of many frequencies (harmonics), the resulting difference in impedance that is presented to the different harmonics can cause signal loss from both reflections and phase distortion (phase jitter) arising from the different harmonics arriving at the destination at different times.

Always choose lower $\varepsilon_r$ material with a flat frequency response whenever possible for best signal performance and to minimize signal distortion and phase jitter.

### 1.2.1.2. Loss Tangent

Loss tangent ($\tan(\delta)$) is a measure of signal loss as the signal propagates down the transmission line. Material datasheets and PCB manufacturers commonly refer to this signal loss as the dissipation factor (Df). $\tan(\delta)$ or Df is the result of electromagnetic wave absorption by the dielectric material and depends on the material's structure and glass-resin composition. A lower loss tangent results in more of the original transmitted signal getting through to its destination. This is important for transceiver-based designs where multi-gigabit signals must be transmitted across long backplane channels. A large loss tangent means more dielectric absorption and less of the transmitted signal is getting through to its destination. Below equation shows the signal attenuation due to the loss tangent, measured in decibels per inch (dB/in).

$$\text{Attenuation} = 2.3 * f * \tan(\delta) * \sqrt{\varepsilon_r}$$

Where:

- $f$ is the frequency in GHz
- $\tan(\delta)$ is the dimensionless loss tangent
- $\varepsilon_r$ is the relative dielectric constant of the material

Ideally, selecting the lowest loss material is the best choice. However, lower loss comes at an increased cost tradeoff. A better approach is to plot attenuation equation against frequency for the various material choices under consideration and compare

the signal attenuation for the target data rate and reach required. For example, below figure shows this attenuation for some common PCB materials by plotting attenuation equation against frequency up to 20 GHz.

**Figure 2.      Comparison of Loss Tangent Attenuation**
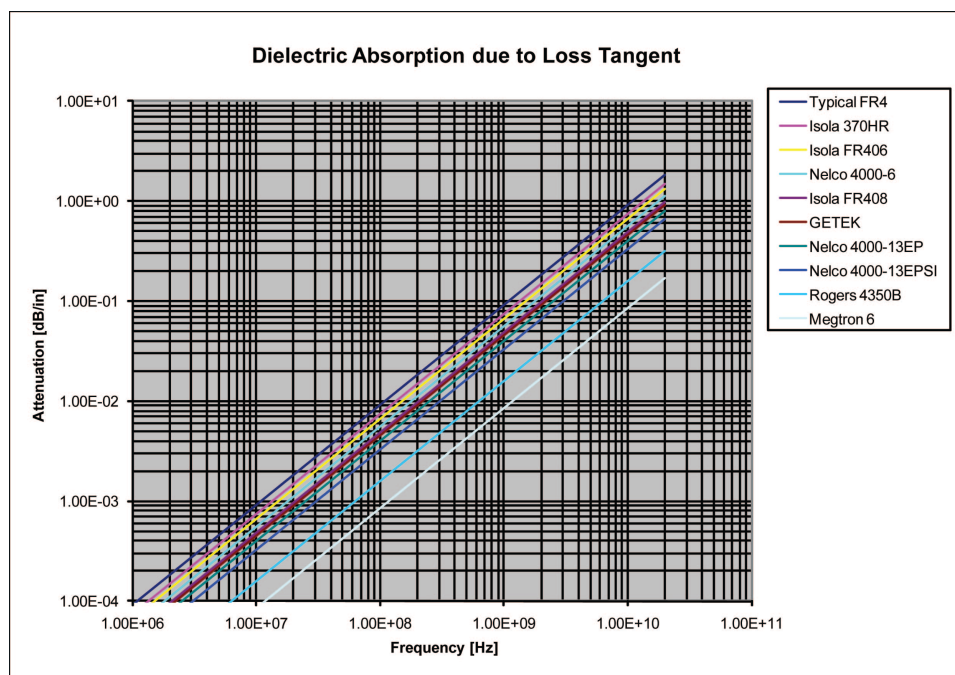


**Table 1.      Material Dielectric Constant and Loss Tangent**

Below table lists the $\varepsilon_r$ and tan($\delta$) of each material plotted in above figure.

| Material | $\varepsilon_r$ | tan($\delta$) |
|---|---|---|
| Typical FR4 | 4 | 0.02 |
| GETEK | 3.9 | 0.01 |
| Isola 370HR | 4.17 | 0.016 |
| Isola FR406 | 4.29 | 0.014 |
| Isola FR408 | 3.70 | 0.011 |
| Panasonic Megtron 6 | 3.4 | 0.002 |
| Nelco 4000-6 | 4.12 | 0.012 |
| Nelco 4000-13 EP | 3.7 | 0.009 |
| Nelco 4000-13 EP SI | 3.2 | 0.008 |
| Rogers 4350B | 3.48 | 0.0037 |

For example, suppose a design running at 10 Gbps requiring a maximum reach of 40 inches is targeted for the Nelco 4000-13 EP material. Because the Nyquist frequency is 5 GHz for a 10 Gbps data rate, the resulting loss that is due solely to the dielectric absorption of Nelco 4000-13EP material is 0.2 dB per inch multiplied by 40 inches of trace length, resulting in 8 dB of signal attenuation just from the material dielectric

absorption. Next, suppose a maximum total loss budget of 10 dB is required for a signal to be properly recovered at the receiver. In this case, most of the signal loss is already consumed by the material dielectric, so a lower loss material or shorter reach must be considered, because additional conductor losses are expected from trace discontinuities, skin effect, vias, and connector assemblies that may be present in the transmission path.

Furthermore, as an example of material cost considerations, below table lists an approximate normalized cost factor relationship for some common PCB materials relative to FR4. Because material costs can vary depending on the PCB vendor, consult the PCB vendor for their latest pricing and relative cost factor data when deciding on material performance versus cost tradeoffs.
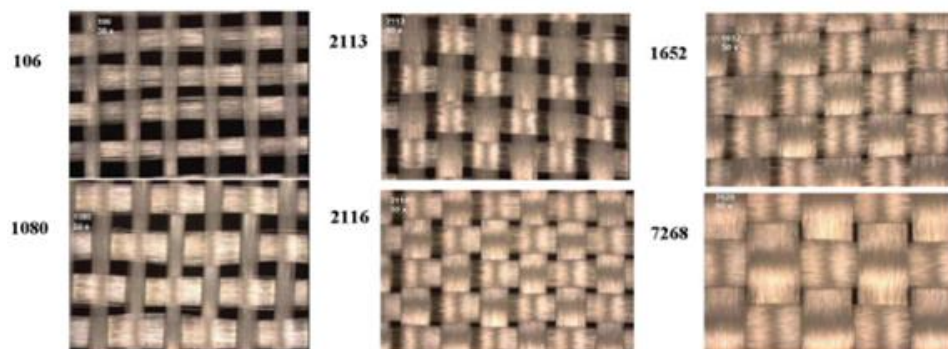
**Table 2.    Normalized Material Cost Comparison**

| Material Group | Vendor Specific | FR4 Relative Cost Factor |
|---|---|---|
| 170 Tg FR4 (Baseline) | Nelco 4000-6 | 1 |
| High Tg / Reliability-Filled | Isola 370HR | 1.1 |
| High Speed / Low Loss | Isola FR408 | 1.8 |
| High Speed / Low Loss | Nelco 4000-13 EP | 2.1 |
| High Speed / Very Low Loss | Nelco 4000-13 EP SI | 3.2 |
| High Frequency | Arlon 85N | 4 |
| High Frequency | IS680-3.45 | 4.2 |
| High Speed / Very Low Loss | Panasonic Megtron 6 | 5 |
| High Frequency | Rogers 4350B | 5.6 |

## 1.2.1.3. Fiberglass Weave Composition

The fiberglass within the core and prepreg is constructed by weaving fibers of glass yarn together to form fabric-like fiberglass sheets. These sheets are then impregnated with an epoxy resin to form the core (cured resin) and prepreg (uncured resin) materials. Because the glass yarn comes in different densities and thicknesses, the resulting sheets can range from loosely-weaved to tightly-weaved fiberglass-epoxy fill.

**Figure 3.    Different Styles of Fibreglss Weaves**



The fiberglass weaves are typically classified into different glass styles, based on the yarn count and the type of fiberglass yarn used, as listed in below table.

**Table 3.    Common Fibreglass Weave Styles**

| Glass Style | Count Warp | Count per Inch | Warp Yarn | Yarn Fill | Glass Thickness |
|---|---|---|---|---|---|
| 106 | 56 | 56 | ECD-900 1/0 | ECD-900 1/0 | 0.0015 |
| 1080 | 60 | 47 | ECD-450 1/0 | ECD-450 1/0 | 0.0025 |
| 1280 | 60 | 60 | ECD-450 1/0 | ECD-450 1/0 | 0.0022 |
| 2113 | 60 | 56 | ECE-225 1/0 | ECD-450 1/0 | 0.0029 |
| 2116 | 60 | 58 | ECE-225 1/0 | ECE-225 1/0 | 0.0038 |
| 3070 | 70 | 70 | ECDE-300 1/0 | ECDE-300 1/0 | 0.0034 |
| 1652 | 52 | 52 | ECG-150 1/0 | ECG-150 1/0 | 0.0045 |
| 7628 | 44 | 31 | ECG-75 1/0 | ECG-75 1/0 | 0.0068 |

The tighter the weave netting, the more uniform the dielectric constant. Loose weaves resulting in less uniform dielectric constants in the PCB laminate can cause trace impedance variations and propagation skews in tightly matched signals, such as differential pairs that directly reference the weave. For example, on a sparse weaving such as glass style 106, one leg of the differential pair may be routed directly over a fiber weave while the other leg is routed between the fiber weaves. This results in a different $\varepsilon_r$ for each leg of the differential channel.

In general, to counteract this skew, route traces at a small angle in a zig-zag fashion relative to the fiberglass strands to average out the number of on-weave and off-weave traces. This technique requires more board routing room and may not be achievable in a space-constrained board. In this situation, select a more tightly woven glass style for the dielectric surrounding the high speed trace layers. Because more tightly woven glass styles add cost to the PCB, a good compromise is to select a medium woven glass style such as 2116 for the high-speed trace layers and a lower-cost 106 or 1080 glass style for other lower-speed signal layers.

For board design with ultra-high speed transceiver signals, Intel recommends to choose spread glass materials to mitigate this effect.

**Related Information**

AN 528: PCB Dielectric Material Selection and Fiber Weave Effect on High-Speed Channel

## 1.2.1.4. Skin Effect

In addition to dielectric absorption, signal attenuation can also occur because of resistive losses from the channel. Channel resistance is a function of frequency. For low frequencies, you can calculate the DC channel resistance from below equation.

**DC Channel Resistance**

$$R_{DC} = \rho \frac{L}{A}$$

Where:

- $R_{DC}$ is the DC channel resistance in ohms (Ω)

- $\rho$ is the resistivity of copper 6.787x10$^{-7}$ ohm-in)

- $L$ is the trace length in inches

- $A$ is the cross-sectional area of the trace in square inches

However, as the frequency increases, the resistive channel loss increases because current flows toward the surface of the copper trace. The surface penetration of this current flow is referred to as the skin depth (δ). This skin effect reduces the cross-sectional area of the channel, increasing the channel resistance. Countering this effect typically requires widening the trace width to increase the effective surface area. Increasing the copper weight of the traces does little, because most of the current is limited by the skin depth. The extent of trace width required usually entails calculating the skin depth.

**Skin Depth**

$$\delta = 2.598 * 10^{-3} \cdot \frac{1}{f}$$

Where:

- $\delta$ is skin depth in inches

- $f$ is frequency in MHz

**Channel Resistance for a Copper Trace**

$$R_{AC} = \rho \frac{L}{W * \delta}$$

Where:

- $R_{AC}$ is the frequency dependent channel resistance for a copper trace

- $\rho$ is the resistivity of copper (6.787x10$^{-7}$ ohm-in)

- $L$ is the trace length in inches

- $\delta$ is skin depth in inches

- $W$ is the trace width in inches

Based on the results of the skin depth and channel resistance, signal traces must be sized appropriately to reduce resistive losses because of the skin effect.

## 1.3. Glass Transition Temperature

In addition to material loss contributions, the manufacturability of the PCB must also be considered. One parameter that can impact PCB manufacturability is the glass transition temperature (Tg).

All materials are subject to expansion and contraction as a result of temperature changes. The rate of expansion and contraction is determined by the material's coefficient of thermal expansion (CTE). The glass transition temperature (Tg) is the knee point temperature at which the resin in the material begins to expand much faster than the expansion of the surrounding glass weave and copper. Ideally, the resin, glass, and copper in the PCB all have similar temperature coefficients so all three materials expand and contract together at a similar rate. However, at temperatures beyond Tg, the faster expansion of the resin increases the mechanical stress on the PCB structure. Because the copper and glass-weave are laminated

together, they reinforce the PCB in the lateral X and Y direction. The resulting expansion is forced to take place mostly in the vertical Z direction. This rapid vertical expansion can over-stress via structures resulting in via fractures and even PCB delamination in severe cases if the expansion is excessive.

When choosing a material, ensure the Tg is high enough to withstand the expected manufacturing temperature cycles for both assembly and rework to ensure PCB manufacturing reliability. For restriction of hazardous substance (RoHS) compliant processes, reflow temperatures can sustain 240° C and even peak at 260° C. Work with the PCB manufacturer to ensure the selected material is appropriate for the targeted manufacturing process.

## 1.4. PCB Stackup Design

The goal of any PCB stackup design is to select the material and specify the layer ordering such that it adequately delivers the required signal performance and power integrity at the lowest PCB cost. After the appropriate PCB material is selected, consider the following issues to design the layer stackup.

### 1.4.1. Layer Count

The total number of layers required for a given design is dependent on the complexity of the board. These factors include the number of signal nets that must break out from the ball-grid array (BGA) device, the number of power planes or pours, and the component density and type of packages for those components. Typically, large BGA device breakouts and individual power or ground plane requirements determine the final board layer count. For complex FPGA boards, the FPGA device in many cases is usually the largest BGA device on the board and thus determines the board's minimum layer count.

### 1.4.2. Signal Layers

In high-density FPGAs, many signal layers are required to achieve full breakout of all available I/Os.

A good estimate for the minimum number of signal layers required is to count the depth of the row or column I/O signal balls of the FPGA device, divide that number by two, and round up to the nearest even whole number.

For example, on a Stratix IV GX device in an F1517 BGA package, the I/O row and column span 13 deep as shown in below figure. Therefore, a minimum of seven signal layers are required for a complete I/O signal breakout for that device. However, for a balanced PCB stackup, eight signals layers must be used.

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**Figure 4.    BGA I/O Signal Depth**
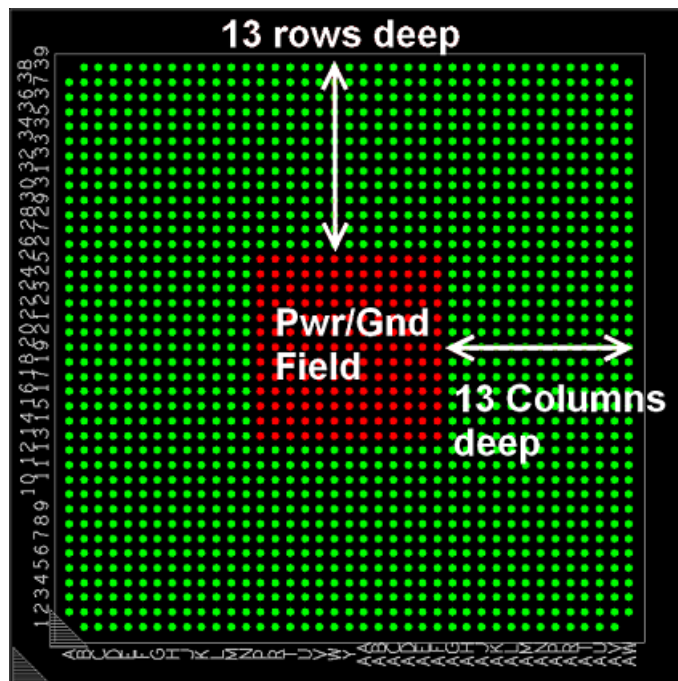


After the dedicated signal layers are determined, they must be arranged within the stackup. To maintain impedance control and provide a current return path, signal layers require an accompanying reference plane layer. Depending on whether microstrip or stripline topologies are used, several stackup construction choices are available.

Below figure (left) shows a microstrip construction. The Signal-Plane topology (S-P) places the signal layer on the surface of the PCB (either top or bottom) with a reference plane layer directly adjacent to the signal layer. With this topology, the difference between εr of air on one side and εr of the dielectric material on the other side causes odd and even mode trace velocity differences that result in far-end crosstalk in differential pair routing. One way to mitigate this situation when using microstrip routing is to use an embedded microstrip, where a thin layer of epoxy or soldermask is added over the surface traces to make εr more uniform, as shown in below figure (right).

**Figure 5.    Microstrip Signal Topologies**



Microstrip                          Embedded Microstrip

In a stripline construction, the single stripline topology uses Plane-Signal-Plane (P-S-P) to provide the best signal isolation but requires more layers for complete signal isolation. As a result, a more commonly used stripline construction is the dual stripline. This Plane-Signal-Signal-Plane (P-S-S-P) topology results in more efficient layer usage, but care must be observed to manage adjacent layer coupling. This coupling is usually reduced in the stackup design by increasing the adjacent signal-to-

signal separation compared to the signal-to-plane separation. Doing this forces the majority of the return current along the reference plane layer directly above or below the signal instead of onto the adjacent signal layer. However, having large separations adds to the overall thickness of the board. This can impact standard board manufacturing if the aspect ratio of the via drill to board thickness is larger than 10:1. In addition to layer separation, signal-to-signal coupling can also be minimized by routing adjacent layers orthogonally to each other to minimize the overlapping coupling region. An added benefit of stripline routing is zero far-end crosstalk because of a uniform εr surrounding the signal traces.

**Figure 6.      Stripline Signal Topologies**



Single Stripline          Dual Stripline
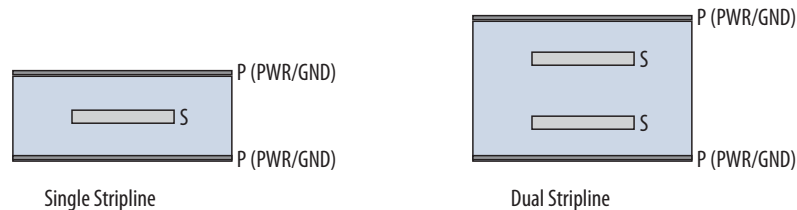
## 1.4.3. High Speed Signal Layer Planning

When routing high-speed traces such as FPGA transceiver signal pairs, plan the routing layer during the stackup design. For devices with a limited number of transceiver channels, it may be easier to strategically assign just a few signal layers for all the channel routes, so the stubs of the through-vias are minimized and the added cost of backdrilling is eliminated.

**Figure 7.      Through-Via with Minimal Short Stub**
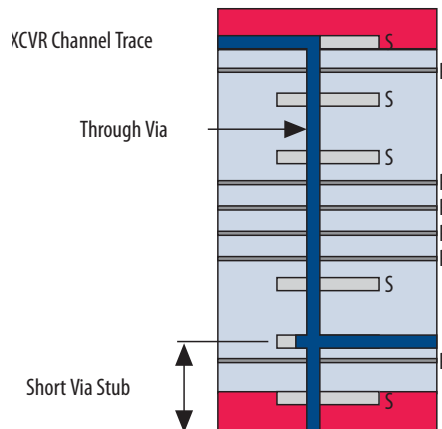


However, for high channel count FPGAs such as the Stratix V device family, the increased channel density requires more than a few layers to accommodate all the channel routing. This means that not all channel via stubs can be optimized out by layer assignment. For these cases, backdrilled or blind vias must be used for the best signal integrity performance of the channel.

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**Figure 8.    Backdrilled (left) and Blind Via (right)**
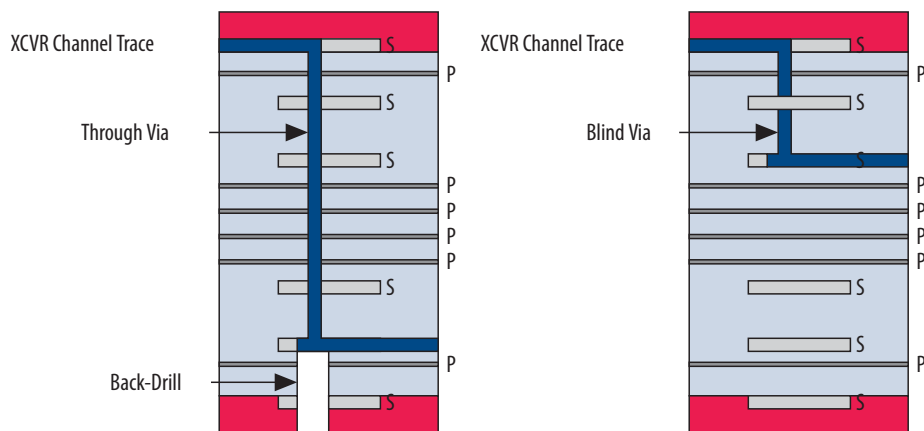


Another consideration for transceiver signal layer assignment results from the physical nature of press-fit connectors, as most of the backplane connectors consider the penetration depth of the signal pins. This depth limits the extent of backdrilling because the penetration of the connector pins determines the maximum backdrilled depth. Therefore, for signals that route to press-fit backplane connectors, assign the signal layer equal to or below the penetration depth of the connector pins to allow backdrilling to be fully effective. For example, routing transceiver channels on layers above the penetration depth of the backplane connector results in the connector pins acting as a stub, even when backdrilling is applied.

**Figure 9.    Maximum Backdrilled Depth of the Connector Pins**
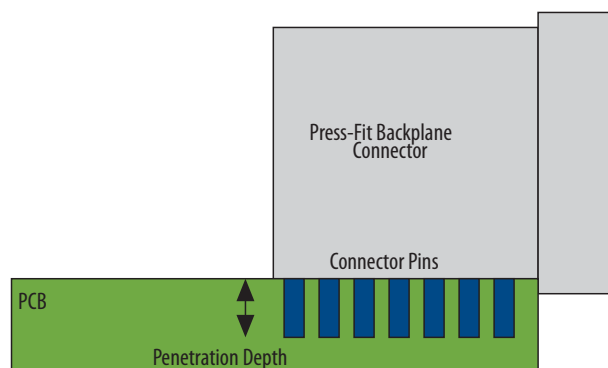


## 1.4.4. Power and Ground Layers

Power and ground layers are determined by the number of different power rails that require a separate layer on the board, the reference and return path requirements, and any isolation requirements. Power is typically shared as much as possible on any designated power layer to reduce the total layer count. As a result, power layers tend to be segmented and ground layers are solid planes that fill the entire layer. Also, power is typically placed next to a ground layer to create planar capacitance, which aids high-frequency decoupling, reduces electromagnetic interference (EMI) radiation, and enhances electromagnetic compliance (EMC) robustness.

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You can generally use both power and ground layers for impedance reference and current return paths for signal layers. However, given a choice between using a power or ground plane as the signal reference or return path, always choose the ground plane. In addition to the likelihood of the power plane for FPGA designs being segmented, using the power plane as the return path for high-speed routing layers allows switching noise to couple to the power plane. Avoid this situation especially for sensitive power rails, such as transceiver analog and PLL power where any additional noise on those rails can directly impact device performance. One way to avoid this situation is to design the stackup topology so that the split power planes are completely isolated from the signal layers by sandwiching the segmented power layers between solid ground layers. Below figure (left) shows an example of two segmented power planes (PWR1 and PWR2) that are completely isolated between two solid ground planes. Although this topology requires more ground layers, it is preferred over the power-ground-power construction shown in below figure (right) because it removes the concern of having to manage signals crossing split power planes during layout.

**Figure 10.   Split Power Plane Topologies**



## 1.4.5. Power Plane and Capacitor Placement Strategy

This section provides specific recommendations for setting the power plane priorities within the PCB stackup and the placement of decoupling capacitors relative to those power planes in Intel devices. The method used to determine the power plane and capacitor placement priority is mainly determined by the Frequency Domain Target Impedance Method (FDTIM).

In general, the rules for capacitor and power plane placement depend on the resulting target impedance of the power rail and the goal of minimizing the various inductances to best meet those target impedances. Placement of power planes and their associated decoupling capacitors in non-optimal locations within the PCB stackup can limit their effectiveness in delivering power, resulting in higher than desired jitter.

### Related Information

- Target Impedance Decoupling Method
- AN 574: Printed Circuit Board (PCB) Power Delivery Network (PDN) Design

### 1.4.5.1. General Rules for Capacitor and Power Plane Placement

Follow these rules for placing the capacitor and power plane in an Intel device:

- Place each decoupling capacitor in close proximity to the corresponding power plane it decouples, so the capacitor mounting inductance loop is minimized .
- If possible, place the power and ground planes in close proximity to the FPGA device so they minimize the BGA via inductance loop.

**Figure 11.    Capacitor and Power Plane Placement to Minimize Mounting Iductance**
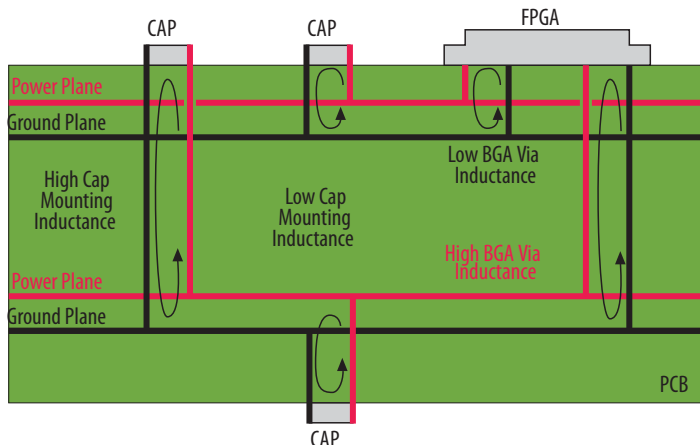


## 1.4.5.2. Rules for Transceiver Power Plane Placement

Follow these rules for placing the transceiver power plane in an Intel device:

- The sensitive transceiver power rails are most susceptible to noise and can directly impact channel jitter performance. As a result, the transceiver power rails usually have the highest priority in the power plane stackup placement over other power rails unless either of the following conditions apply:

  — The transceiver rails have internal regulation that helps isolate them from on-board noise. Internally regulated power rails can be placed further away from the FPGA device.

  — The current demand of the transceiver power rail is low enough to yield a high impedance target that is easily decoupled even when their power planes are placed further away from the FPGA device.

- Place critical transceiver power rails closest to the FPGA device to minimize the BGA via inductance. For example, critical power rails in a Stratix V transceiver device include the VCCR (transceiver receive path power) and VCCT (transceiver transmit path power) power rails.

**Figure 12.     Transceiver Power Plane Placement Close to an FPGA Device**
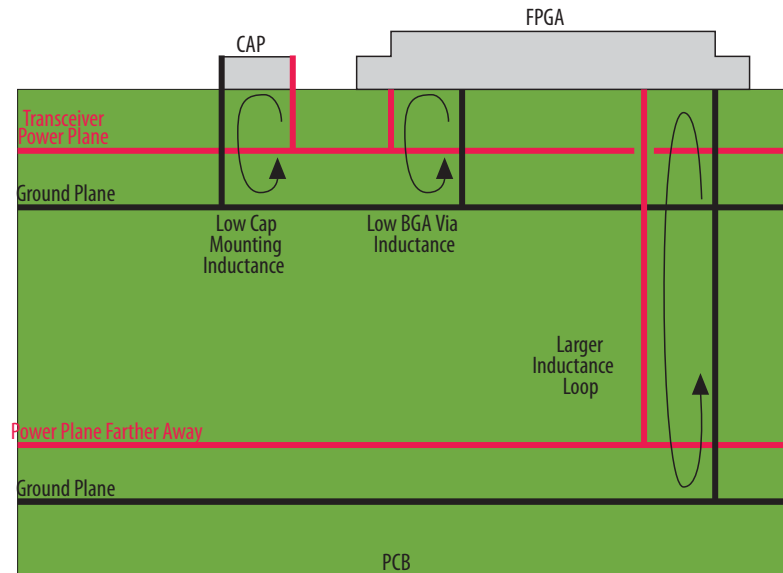


## 1.4.5.3. Rules for High-Current Power Rails

Follow these rules for placing the high-current power rails in an Intel device:

- High-current power rails result in lower target impedance and present a greater challenge for decoupling. As a general rule, high-current power rails should typically be placed close to the FPGA device to minimize the BGA via inductance. However, depending on whether non-transceiver or transceiver-based devices are used, the priority can be adjusted to optimize the high-current power rail placement:

  — For non-transceiver devices (such as Stratix V E devices), high-current rails such as core power (VCC) should be placed closest to the FPGA device because there are no sensitive transceiver power rails requiring a higher priority.

**Figure 13.    Placement of Core Power in Non-Transceiver Devices**
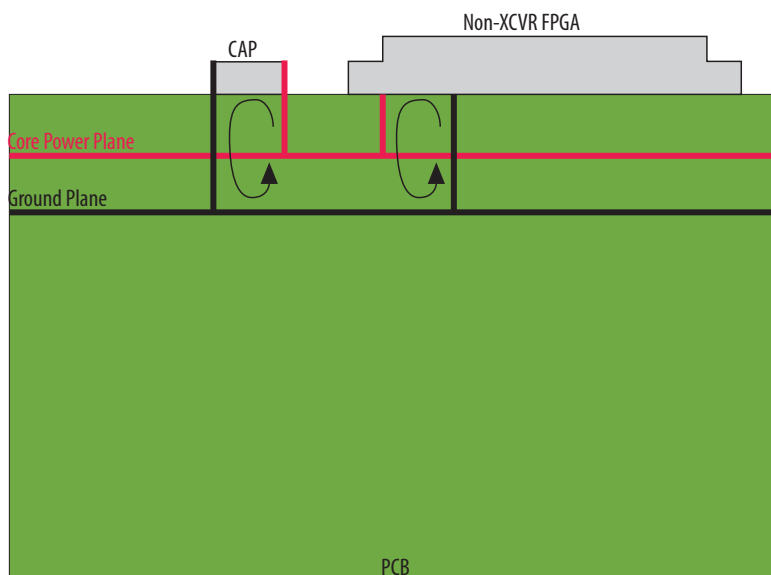


  — For transceiver-based devices (such as Stratix V GX, GT, or GS devices), high-current rails should receive second priority behind the critical transceiver powers. As second priority, these rails are usually placed on the next available power layer after the critical transceiver power. However, for high-current core power, place the rails furthest from the FPGA device to minimize the capacitor mounting inductance while benefiting from the reduced effective BGA via inductance that result from having an increased number of parallel core power and ground via pairs. Do not share power or ground vias in the BGA breakout, because this negates the benefits of having parallel power and ground vias to reduce the effective BGA via inductance. Furthermore, because some device packages incorporate On-Package-Decoupling (OPD) for core power, placing core power furthest from the FPGA device provides greater flexibility for placement of other high-current rails within the stackup.

**Figure 14.    Placement of High-Current Rails for Transceiver-Based Devices**
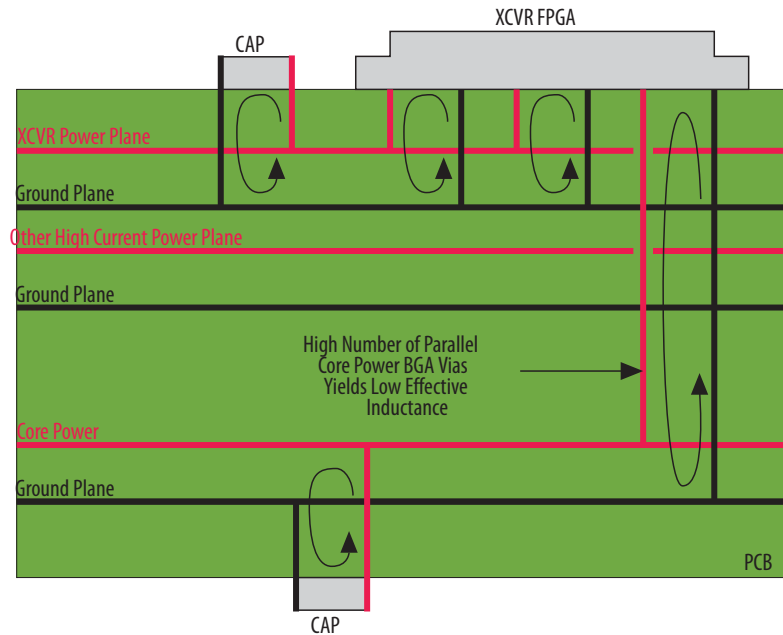


## 1.4.5.4. Rules for PLL and Other Power Rails

Follow these rules for placing the PLL and other power rails in an Intel device:

- PLL power rails should receive third priority in the power plane stackup. Typically, PLL power planes are located in the middle of the layer stack. As a result, the decoupling capacitors for these supplies can reside on either side of the PCB.

- Place any remaining power rails where convenient in the layer stack and ensure sufficient decoupling capacitors are provided to adequately decouple the rail to meet its target impedance as determined by the Intel PDN tool.

**Related Information**

Intel Device Pin Connection Guidelines

## 1.4.6. Planar Capacitance and Spreading Inductance

Power planes adjacent to ground planes benefit from embedded planar (or buried) capacitance, which aids high frequency decoupling. Because planar capacitance is inversely proportional to the dielectric thickness between the power and ground planes, choose thin dielectrics between power and ground planes to increase planar capacitance while reducing planar spreading inductance and overall board thickness. The reduction of planar spreading inductance results in a lower impedance path and increases the effectiveness of discrete capacitances (such as 0402 or 0603 capacitances) that are frequently used for decoupling on the board.

When designing power plane capacitance into the stackup, use below equation to model the resulting planar capacitance.

**Planar Capacitance**

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$$C = \varepsilon o * \varepsilon_r * \frac{A}{h}$$

Where:

- $C$ is the capacitance

- $\varepsilon o$ is the permittivity of free space (8.85x10$^{-12}$ F/m)

- $\varepsilon r$ is the relative permittivity of the dielectric

- $A$ is the area of overlap between the power and ground plane

- $h$ is the dielectric separation between the planes

Use below equation to determine the planar spreading inductance of the power-ground plane sandwich.

$$Ls = \mu_o * h * \frac{l}{w}$$

Where:

- $Ls$ is the planar spreading inductance

- $\mu_o$ is the permeability of free space (32 pH/mil)

- $h, l$, and $w$ are the respective separation between the power-ground sandwich, length and width of the plane in mils

## 1.4.7. Plane Layer Separation

To benefit from the inherent planar capacitance associated with the different potential planes, make the power-to-ground layer separation as small as possible. Because the dielectric breakdown voltage (DBV) in all common PCB materials is generally 1000 V/mil or higher, dielectric failure between power and ground planes is not a concern for typical electronic applications where the voltage requirement is usually 12 V and lower. As a result, when designing planar capacitance, use the thinnest core dielectric available for the power-ground sandwich for the highest capacitance per planar area.

The thinnest standard core dielectric commonly used for the power-ground planar capacitance without incurring a cost premium is typically 3 mils. For thinner cores, several manufacturers offer 2 mil core, 1 mil core, and even sub-1 mil core thicknesses at an additional cost. Consider the ZBC cores from vendors like Sanmina, FaradFlex cores from Oak Mitsui Technologies, or ECM (Embedded Capacitance Material) cores from 3M Corporation for constructing even larger buried capacitances per area within the PCB stackup.

## 1.4.8. Copper Weight

A copper foil is specified in terms of its weight in ounces per square foot (oz/ft$^2$), although it is more commonly referred to in ounces (oz). Typical PCB copper weights are 0.5 oz, 1 oz, and 2 oz. Below table lists the corresponding copper thicknesses for various copper weights.

**Table 4.    Copper Weight and Thickness**

| Copper Weight (oz) | Thickness (µm) | Thickness (mil) |
|---|---|---|
| 0.5 | 17.5 | 0.7 |
| 1 | 35 | 1.4 |
| 2 | 70 | 2.8 |

Half-ounce copper is typically used for signal traces and one-ounce copper is used for plane layers. Denser copper weights can be used for power delivery if higher DC current is expected. However, thicker copper layers increase the overall board thickness and raise manufacturability concerns related to lamination and drilling. For high frequency signals, increasing the copper weight does not significantly improve the signal loss from trace resistance because of the skin effect. Instead, use wider traces on either half- or one-ounce copper. The current carrying capacity in copper is determined by the allowable temperature rise above ambient resulting from the current flowing through it. Below table list the current rating for different copper weights extrapolated from graphs published in the military standard specification, MIL-STD-275E. You can use these tables to appropriately size your power delivery structures. For example, to pass 10 A of current on 1 oz surface copper layers, you must use at least 200 mil wide copper trace to maintain at most a 20° C rise in temperature above ambient for the conductor.

**Table 5.    MIL-STD 275E External Layer Current Capacity Rating**

| Trace Width (mil) | Temperature Rise Above Ambient | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 10° C | | | 20° C | | | 30° C | | |
| | Copper Weight (oz/ft$^2$) | | | | | | | | |
| | 0.5 | 1 | 2 | 0.5 | 1 | 2 | 0.5 | 1 | 2 |
| | Maximum Current (A) | | | | | | | | |
| 10 | 0.5 | 1.0 | 1.4 | 0.6 | 1.2 | 1.6 | 0.7 | 1.5 | 2.2 |
| 15 | 0.7 | 1.2 | 1.6 | 0.8 | 1.3 | 2.4 | 1.0 | 1.6 | 3.0 |
| 20 | 0.7 | 1.3 | 2.1 | 1.0 | 1.7 | 3.0 | 1.2 | 2.4 | 3.6 |
| 25 | 0.9 | 1.7 | 2.5 | 1.2 | 2.2 | 3.3 | 1.5 | 2.8 | 4.0 |
| 30 | 1.1 | 1.9 | 3.0 | 1.4 | 2.5 | 4.0 | 1.7 | 3.2 | 5.0 |
| 50 | 1.5 | 2.6 | 4.0 | 2.0 | 3.6 | 6.0 | 2.6 | 4.4 | 7.3 |
| 75 | 2.0 | 3.5 | 5.7 | 2.8 | 4.5 | 7.8 | 3.5 | 6.0 | 10.0 |
| 100 | 2.6 | 4.2 | 6.9 | 3.5 | 6.0 | 9.9 | 4.3 | 7.5 | 12.5 |
| 200 | 4.2 | 7.0 | 11.5 | 6.0 | 10.0 | 11.0 | 7.5 | 13.0 | 20.5 |
| 250 | 5.0 | 8.3 | 12.3 | 7.2 | 12.3 | 20.0 | 9.0 | 15.0 | 24.0 |
| 300 | 5.8 | 9.8 | - | 8.2 | 13.8 | - | 10.1 | 17.0 | - |
| 350 | 6.4 | 11.1 | - | 9.3 | 15.2 | - | 11.3 | 19.6 | - |
| 400 | 7.0 | 12.0 | - | 10.0 | 16.7 | - | 12.6 | 21.2 | - |

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**Table 6.** **MIL-STD 275E Internal Layer Current Capacity Rating**

| Trace Width (mil) | Temperature Rise Above Ambient | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 10° C | | | 20° C | | | 30° C | | |
| | Copper Weight (oz/ft²) | | | | | | | | |
| | 0.5 | 1 | 2 | 0.5 | 1 | 2 | 0.5 | 1 | 2 |
| | Maximum Current (A) | | | | | | | | |
| 10 | 0.25 | 0.4 | 0.63 | 0.35 | 0.54 | 0.85 | 0.42 | 0.64 | 1.1 |
| 15 | 0.36 | 0.55 | 0.88 | 0.44 | 0.7 | 1.2 | 0.57 | 0.9 | 1.6 |
| 20 | 0.41 | 0.67 | 1.15 | 0.55 | 0.86 | 1.5 | 0.65 | 1.18 | 1.7 |
| 25 | 0.49 | 0.75 | 1.3 | 0.63 | 1.1 | 1.75 | 0.76 | 1.38 | 2.15 |
| 30 | 0.58 | 0.78 | 1.5 | 0.72 | 1.25 | 2.0 | 0.88 | 1.62 | 2.5 |
| 50 | 0.80 | 1.4 | 2.1 | 1.18 | 1.80 | 3.00 | 1.25 | 2.20 | 3.75 |
| 75 | 1.08 | 1.9 | 2.83 | 1.45 | 2.75 | 4.0 | 1.75 | 3.5 | 5.0 |
| 100 | 1.32 | 2.2 | 3.5 | 1.75 | 3.1 | 5.0 | 2.2 | 3.9 | 7.2 |
| 200 | 2.2 | 3.60 | 5.8 | 3.0 | 5.15 | 8.0 | 3.8 | 6.50 | 10.5 |
| 250 | 2.5 | 4.20 | 6.8 | 3.6 | 6.30 | 10.0 | 4.3 | 7.50 | 12.4 |
| 300 | 2.9 | 4.80 | - | 4.1 | 6.90 | - | 5.2 | 8.50 | - |
| 350 | 3.3 | 5.60 | - | 4.6 | 7.70 | - | 5.8 | 9.80 | - |
| 400 | 3.6 | 6.00 | - | 5.2 | 8.70 | - | 6.4 | 10.6 | - |

## 1.4.9. Hybrid Construction

One technique to control cost in high speed designs is to use hybrid construction PCBs. In hybrid construction, only the layers where the high performance signals are required use a higher cost but lower loss copper clad laminate core. All other layers can use a lower cost FR4 derivative core material. A common requirement for hybrid construction is to maintain a homogeneous prepreg (usually FR4) throughout the PCB to bond the core layers together. Mixing prepreg in the PCB can result in lamination issues because different temperatures may be required for the different prepregs to bond properly. For example, consider a design where very high speed transceiver channels are to be routed only on the top and bottom layers using embedded microstrip topology to avoid any via stubs without backdrilling. In this case, the top and bottom layers can use a low-loss core such as Rogers 4350B while the rest of the internal layers can use typical FR4 cores.

**Figure 15.  Hybrid PCB Stackup**
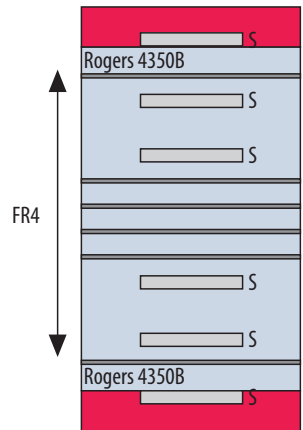


## 1.5. PCB Panelization

Always consider board panelization during the initial PCB sizing to maximize the number of board yield per PCB panel and reduce the cost per board. Although common PCB panel dimensions are 12 × 18 in and 18 × 24 in, the actual usable area left to the designer is typically one inch less on all sides of the panel. Therefore, the usable dimensions are 10 × 16 in and 16 × 22 in, respectively. Also, when panelizing multiple boards up on a PCB panel, the minimum spacing requirement between boards must be 100 mils to allow the individual boards to be routed out after fabrication. Below figure shows an example of maximum panel utilization on an 18 × 24 in panel. In this example, six Stratix IV GX SI development kit boards have been panelized as 6-up on a standard 18 × 24 in panel with 100 mil separation between adjacent boards to accommodate final routing of the board.

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**Figure 16.    PCB Panelization**
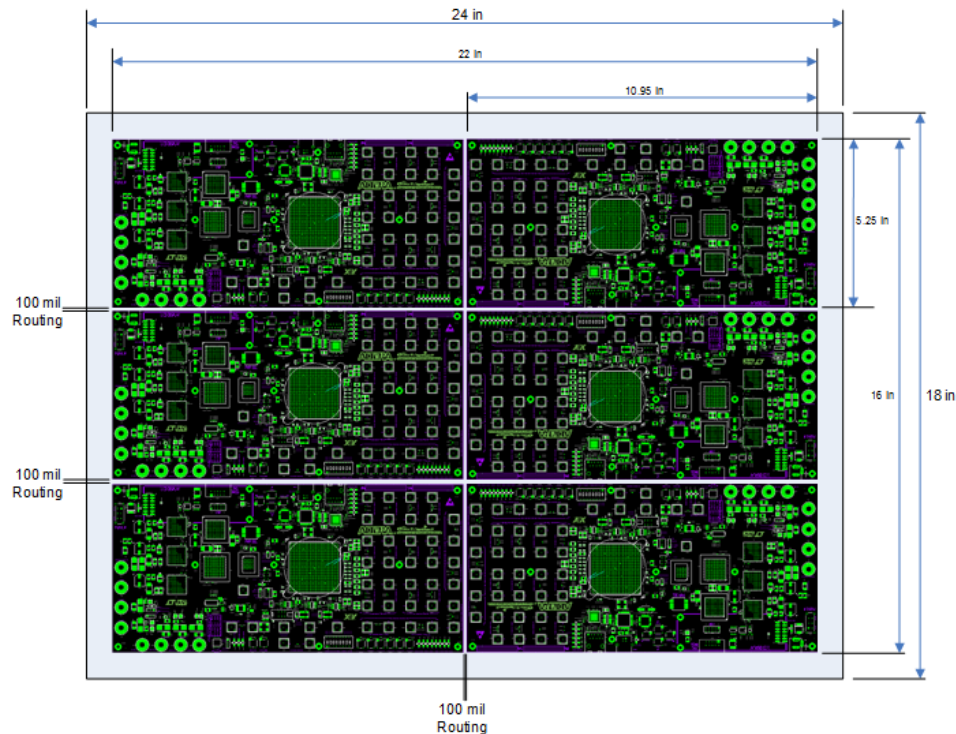


## 1.6. Conclusion

High-speed FPGA designs at data rates of 10 Gbps and higher require careful attention to material selection and layer stack planning to ensure a robust PCB design. This application note provides a detailed understanding of the PCB stackup construction with considerations for material selection and PCB manufacturability, as well as best practice guidelines for designing the layer stackup arrangement. Specific stackup design guidelines for Intel FPGA device families are provided at the end of this application note.

## 1.7. Specific Recommendations for Intel FPGA Devices

The following sections provide device family specific recommendations. For power plane placement recommendations, the FPGA device is assumed to be on the top of the PCB.

No specific recommendations for MAX 10 or MAX V devices.

### 1.7.1. Stratix 10 Device Recommendations

#### 1.7.1.1. Stratix 10 Device Family Power Plane Placement Example

**Top of PCB**

- **Sensitive Transceiver Power—**VCCT_GXB, VCCR_GXB
- **Analog and Digital PLL Power—**VCCA_PLL, VCCPLLDIG_SDM, VCCPLLDIG_HPS, VCCPLL_SDM, VCCPLL_HPS
- **Other Transceiver Power—**VCCH_GXB
- **I/O and Other Power—**VCCIO, VCCIO3V, VCCIO_SDM, VCCIO_HPS
- **Core Power—**VCC, VCCP, VCCL_HPS

**Bottom of PCB**

## 1.7.2. Stratix V Device Recommendations

### 1.7.2.1. Stratix V GX, GT, and GS Family Power Plane Placement Example

**Top of PCB**

- **Sensitive Transceiver Power—**VCCT_GXB, VCCR_GXB
- **Analog and Digital PLL Power—**VCCA_FPLL, VCCD_FPLL
- **Other Transceiver Power—**VCCA_GXB, VCCH_GXB
- **I/O and Other Power—**VCCPT, VCCAUX, VCCIO, VCCPD, VCCPGM
- **Core Power—**VCC, VCCHIP, VCCHSSI

**Bottom of PCB**

### 1.7.2.2. Stratix V E Family Power Plane Placement Example
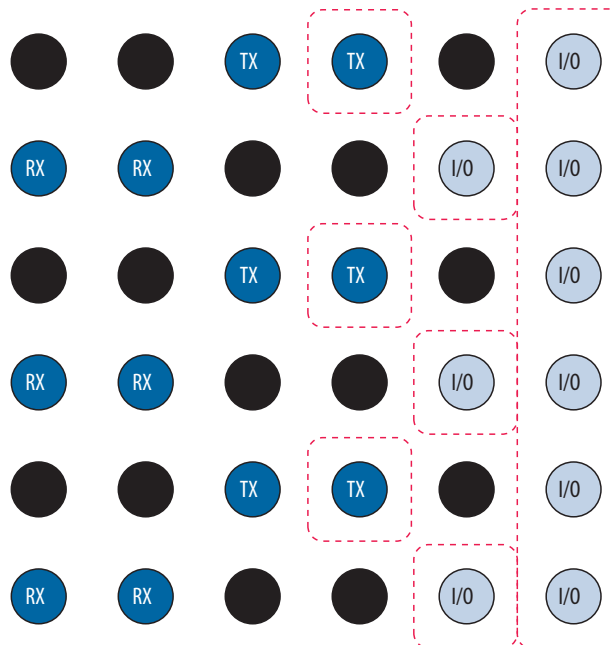
**Top of PCB**

- **Core Power—**VCC
- **Analog and Digital PLL Power—**VCCA_FPLL, VCCD_FPLL
- **I/O and Other Power—**VCCPT, VCCAUX, VCCIO, VCCPD, VCCPGM

**Bottom of PCB**

### 1.7.2.3. Stratix V Transceiver Channel Breakout Recommendations

For Stratix V GX, GT, and GS devices, some transceiver TX channel pins are located near regular I/O pins

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**Figure 17.** **Stratix V I/O Adjacent to TX Pins**



For these pins, crosstalk coupling from the I/O pins to the TX pins can degrade the TX channel performance. To minimize the coupling, do the following:

- If possible, avoid using those I/O pins and assign them as outputs driving ground in the Stratix V software.

- If it is necessary to use those I/Os pins near the TX pins, assign lower voltage swing I/Os to those pins and avoid using 3.0 V or 2.5 V I/O standards. The following I/O standards are preferred for use on those I/O pins:

  — LVDS

  — SSTL or HSTL (1.2 V, 1.5 V, or 1.8 V)

  — 1.2 V non-voltage referenced I/O standard

  — 1.5 V non-voltage referenced I/O standard

  — 1.8 V non-voltage referenced I/O standard

- Choose lower current drive strength whenever possible.

- Assign low voltage I/O functions that switch less frequently.

- Apply internal terminations where possible to reduce overshoot and ringing.

- Limit the inductive coupling region between the I/O and TX pins. You can do this by limiting the depth of the I/O signal breakout to specific routing layers. IntelFPGA recommends limiting those I/O breakouts to a depth of 40 mils or less to reduce the mutual inductive coupling region of the I/O and TX breakout via.

**Figure 18.    Limiting Mutual Inductive Coupling**
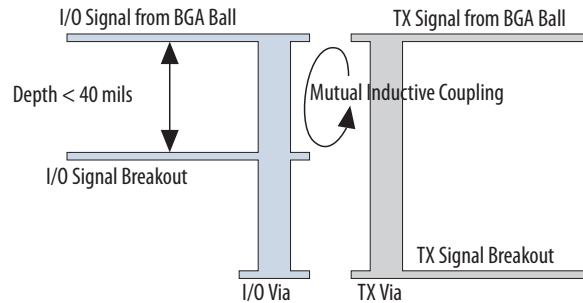


## 1.7.3. Stratix IV Device Recommendations

### 1.7.3.1. Stratix IV GX and GT Family Power Plane Placement Example

**Top of PCB**

- **Sensitive Transceiver Power—**VCCL_GXB, VCCT, VCCR
- **Analog and Digital PLL Power—**VCCA_DPLL, VCCD_PLL
- **Other Transceiver Power—**VCCA, VCCH_GXB
- **I/O and Other Power—**VCCPT, VCCAUX, VCCIO, VCCPD, VCCPGM, VCC_CLKIN
- **Core Power—**VCC, VCCHIP

**Bottom of PCB**

### 1.7.3.2. Stratix IV E Family Power Plane Placement Example

**Top of PCB**

- **Core Power—**VCC, VCCHIP
- **Analog and Digital PLL Power—**VCCA_PLL, VCCD_PLL
- **I/O and Other Power—**VCCPT, VCCAUX, VCCIO, VCCPD, VCCPGM, VCC_CLKIN

**Bottom of PCB**

## 1.7.4. Arria 10 Device Recommendations

### 1.7.4.1. Arria 10 Device Family Power Plane Placement Example

**Top of PCB**

- **Sensitive Transceiver Power—**VCCT_GXB, VCCR_GXB
- **Analog and Digital PLL Power—**VCCA_PLL, VCCPLL_HPS
- **Other Transceiver Power—**VCCH_GXB
- **I/O and Other Power—**VCCIO, VCCIO_SDM, VCCIO_HPS
- **Core Power—**VCC, VCCP, VCCL_HPS, VCCERAM

**Bottom of PCB**

## 1.7.5. Arria V Device Recommendations

### 1.7.5.1. Arria V Device Family Power Plane Placement Example

**Top of PCB**

- **Sensitive Transceiver Power—**VCCT_GXB, VCCR_GXB, VCCL_GXB
- **Analog and Digital PLL Power—**VCCA_FPLL, VCCD_FPLL, VCCPLL_HPS
- **Other Transceiver Power—**VCCA_GXB, VCCH_GXB
- **I/O and Other Power—**VCCIO, VCCIO_HPS, VCCPD, VCCPD_HPS
- **Core Power—**VCC, VCCP, VCC_HPS

**Bottom of PCB**

## 1.7.6. Arria II Device Recommendations

### 1.7.6.1. Arria II GX Family Power Plane Placement Example

**Top of PCB**

- **Sensitive Transceiver Power—**VCCL_GXB
- **Analog and Digital PLL Power—**VCCA_PLL, VCCD_PLL
- **Other Transceiver Powerr—**VCCA, VCCH_GXB
- **I/O and Other Power—**VCCIO, VCCPD, VCCCB
- **Core Power—**VCC

**Bottom of PCB**

## 1.7.7. Cyclone 10 Device Recommendations

### 1.7.7.1. Cyclone 10 LP Device Family Power Plane Placement Example

**Top of PCB**

- **Analog and Digital PLL Power—**VCCA, VCCD_PLL
- **I/O and Other Power—**VCCIO
- **Core Power—**VCCINT

**Bottom of PCB**

## 1.7.8. Cyclone V Device Recommendations

### 1.7.8.1. Cyclone V Device Family Power Plane Placement Example

**Top of PCB**

- **Sensitive Transceiver Power—**VCCE_GXB, VCCL_GXB
- **Analog and Digital PLL Power—**VCCA_FPLL, VCCPLL_HPS
- **Other Transceiver Power—**VCCH_GXB
- **I/O and Other Power—**VCCIO, VCCPD, VCCPGM, VCCIO_HPS, VCCPD_HPS
- **Core Power—**VCC, VCC_HPS

**Bottom of PCB**

## 1.7.9. Cyclone IV Device Recommendations

### 1.7.9.1. Cyclone IV GX Family Power Plane Placement Example

**Top of PCB**

- **Sensitive Transceiver Power—**VCCL_GXB
- **Analog and Digital PLL Power—**VCCA, VCCD_PLL
- **Other Transceiver Power—**VCCA_GXB, VCCH_GXB
- **I/O and Other Power—**VCCIO, VCC_CLKIN
- **Core Power—**VCCINT

**Bottom of PCB**

### 1.7.9.2. Cyclone IV E Family Power Plane Placement Example

**Top of PCB**

- **Core Power—** VCCINT
- **Analog and Digital PLL Power—**VCCA, VCCD_PLL
- **I/O and Other Power—**VCCIO, VCC_CLKIN

**Bottom of PCB**

## 1.7.10. Cyclone III Device Recommendations

### 1.7.10.1. Cyclone III Family Power Plane Placement Example

**Top of PCB**

- **Core Power—**VCCINT
- **PLL Power—**VCCA, VCCD_PLL
- **I/O Power—**VCCIO

**Bottom of PCB**

## 1.8. References

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## 1.9. Document Revision History

**Table 7.       Document Revision History**

| Date | Version | Changes |
|---|---|---|
| June 2017 | 2.0 | Added recommendations for Stratix 10, Arria 10, Cyclone 10, Arria V, and Cyclone V devices. |
| October 2010 | 1.0 | Initial release |