**THIẾT KẾ HỆ THỐNG SỐ VỚI HDL**

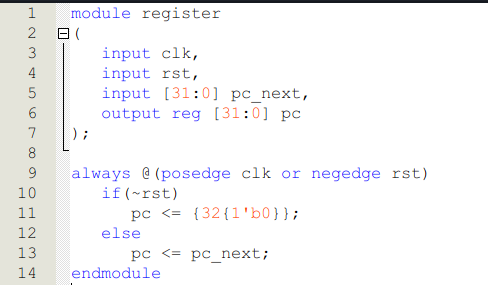
**BÀI THỰC HÀNH 5 ,6, 7**

**GVHD:** Tạ Trí Đức

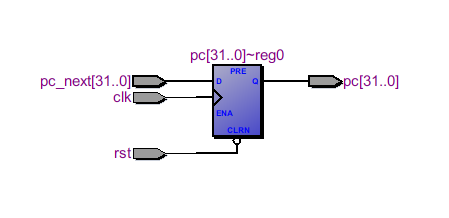
**Sinh viên thực hiện:** Phạm Quốc Tiến – 22521472

1. **Thiết kế khối MIPS**
   1. **Khối PC**

Code:

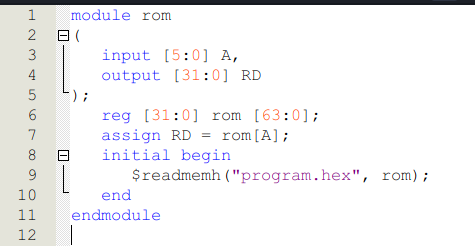


RTL:

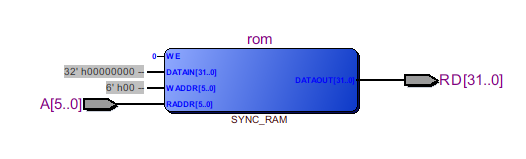


* 1. **Khối I-MEM**

Code:



RTL:

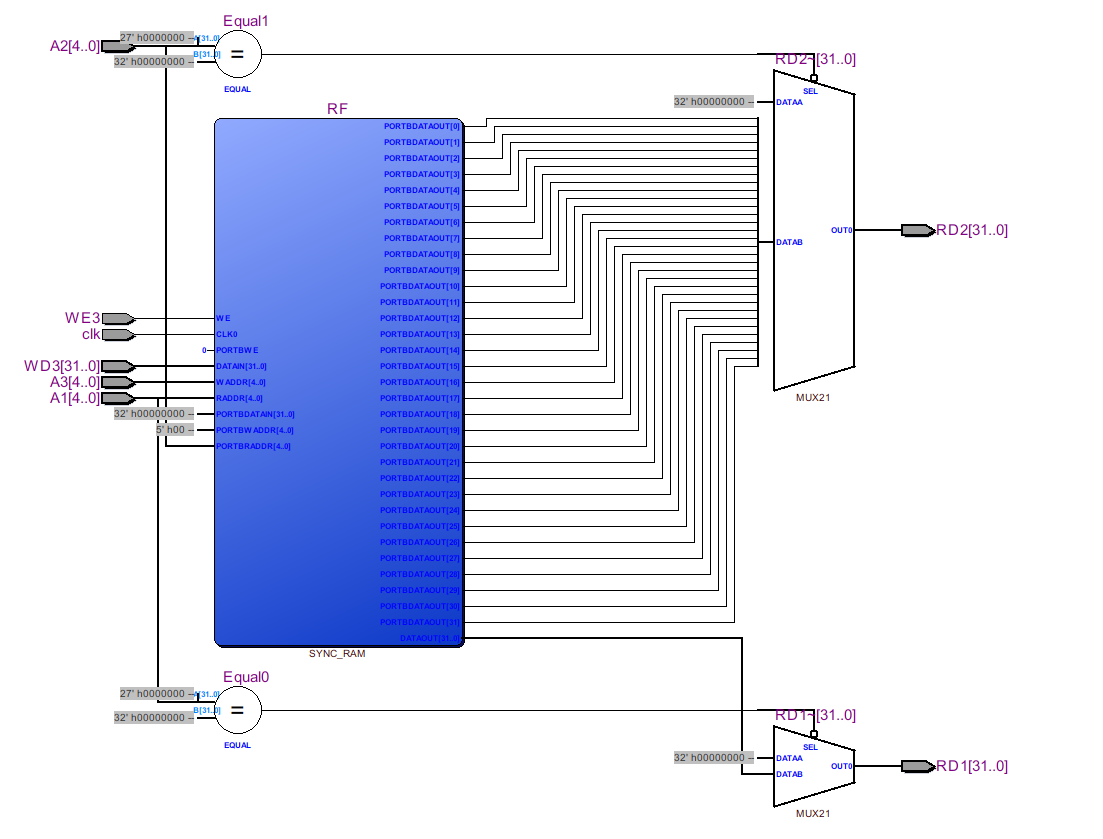


* 1. **Khối Register File**

Code:

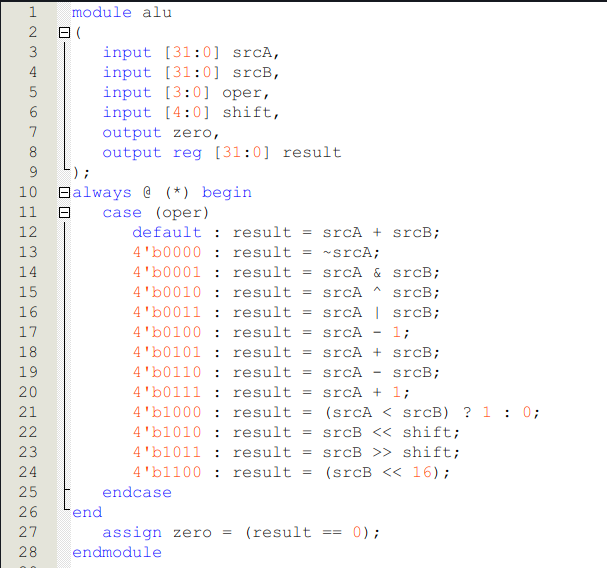


RTL:



* 1. **Khối ALU**

Code:



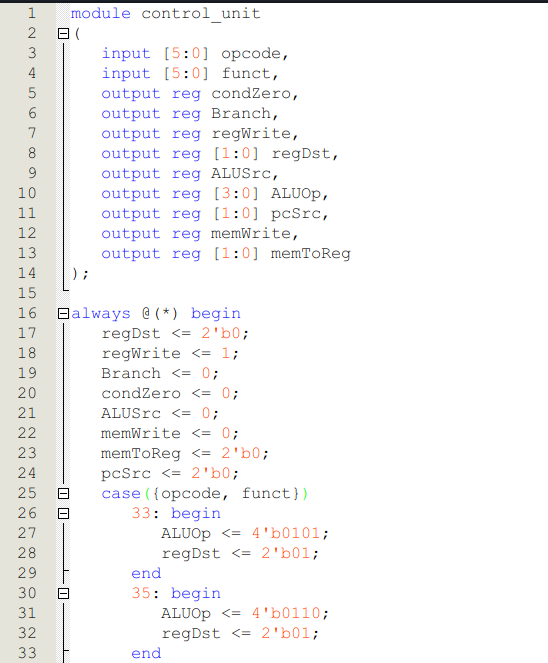
RTL:

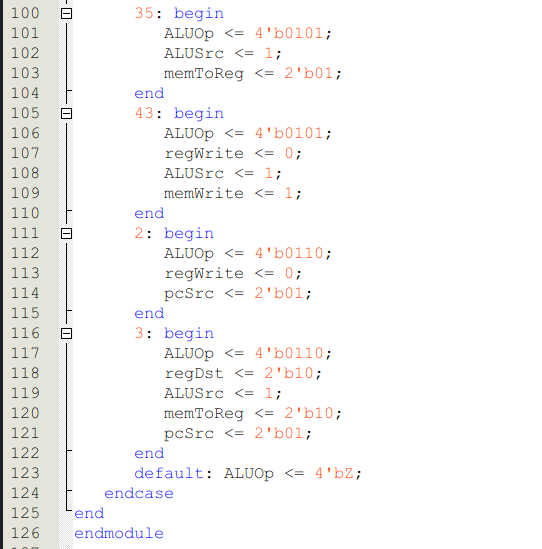
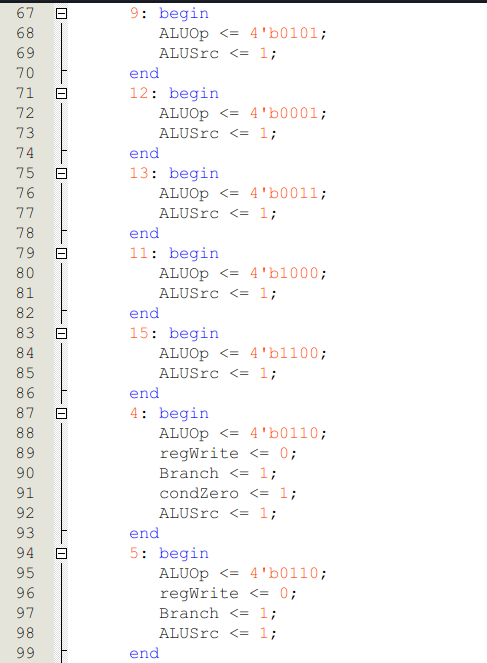
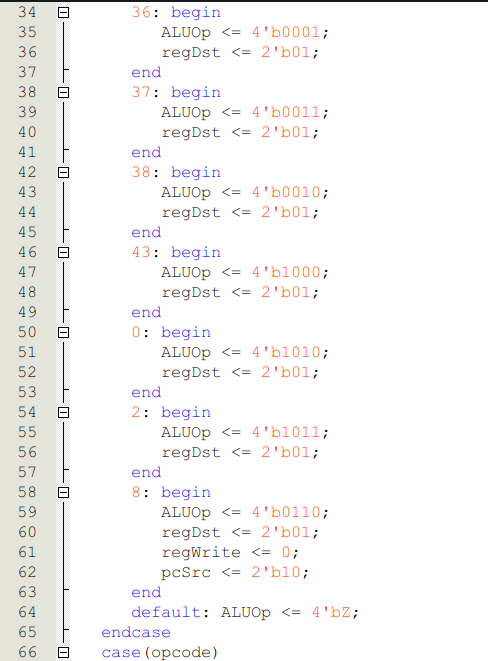
A black and white image of lines and numbers

AI-generated content may be incorrect.

* 1. **Khối Control**

Code:





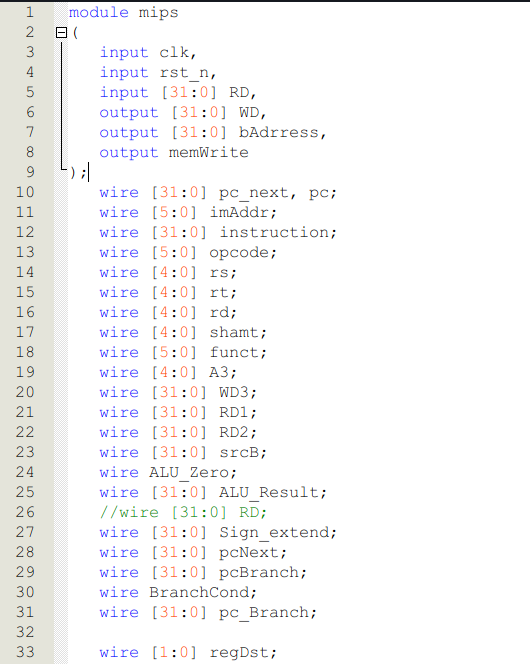
RTL:

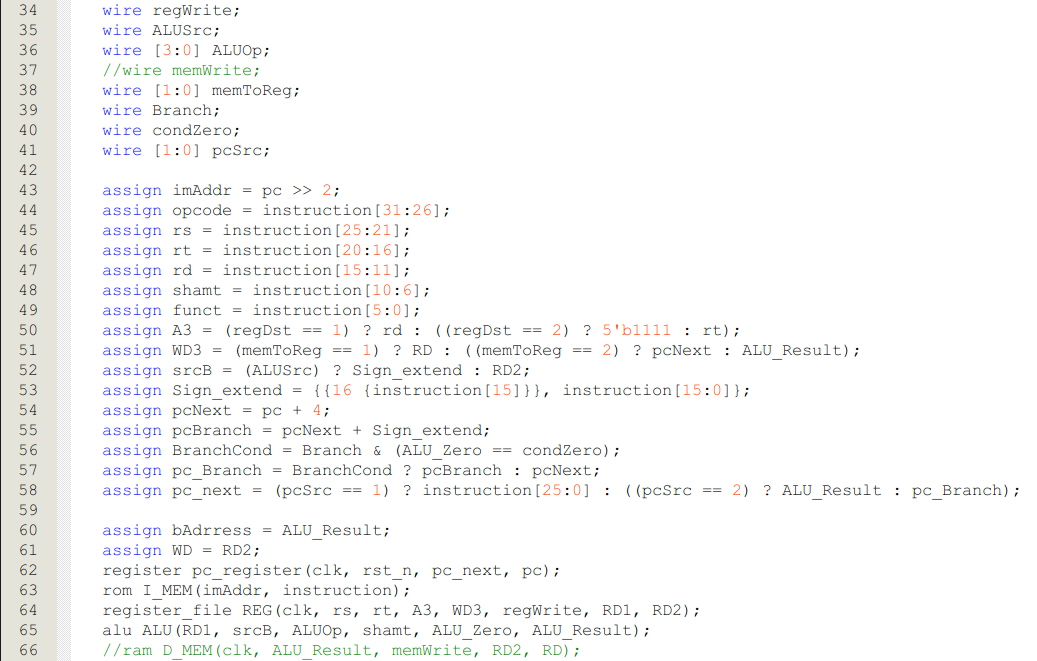
A diagram of a diagram

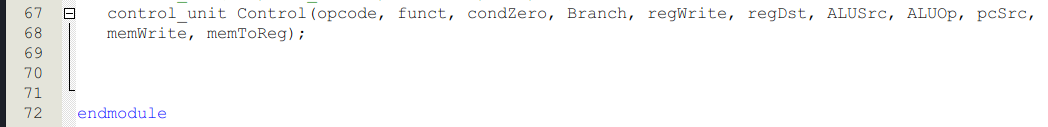
AI-generated content may be incorrect.

* 1. **Khối MIPS**

Code:







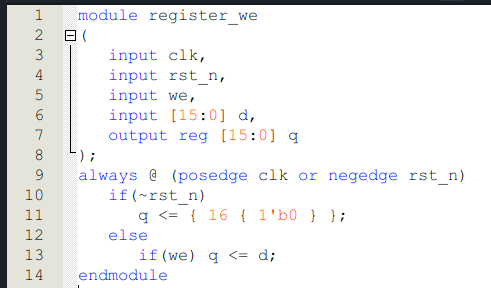
RTL:

A white board with green squares

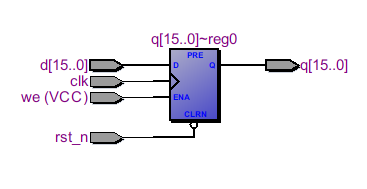
AI-generated content may be incorrect.

1. **Thiết kế khối GPIO**
   1. **Khối Register**

Code:



RTL:

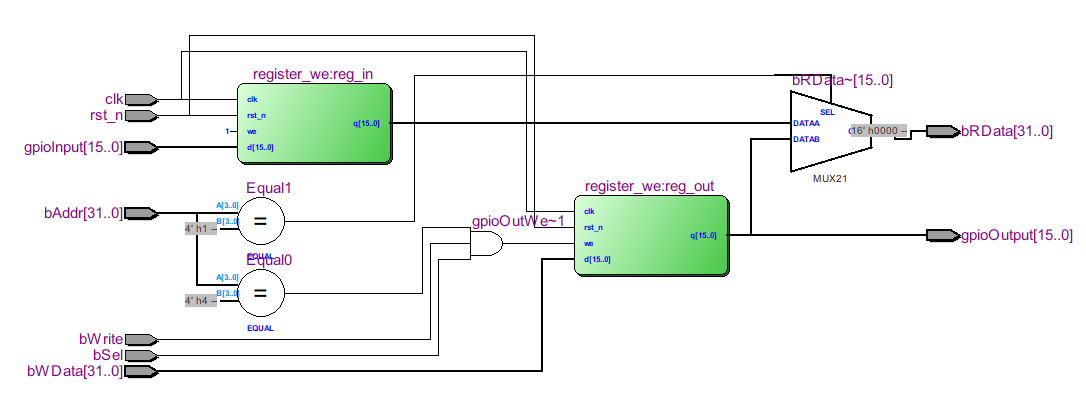


* 1. **Khối GPIO**

Code:

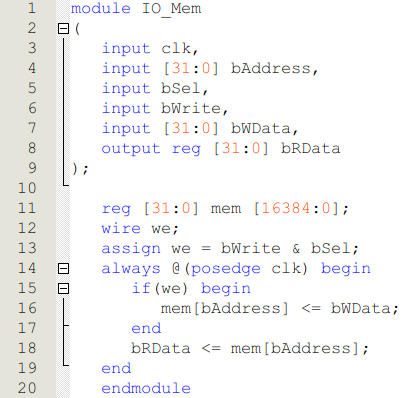


RTL:

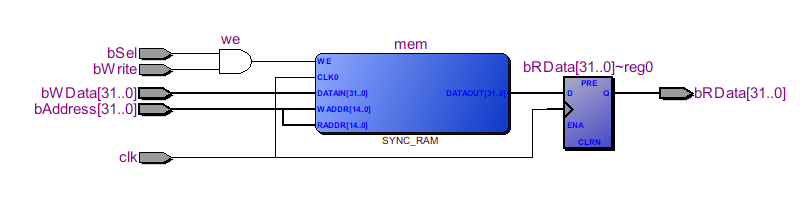


1. **Thiết kế khối Memory IO**

Code:

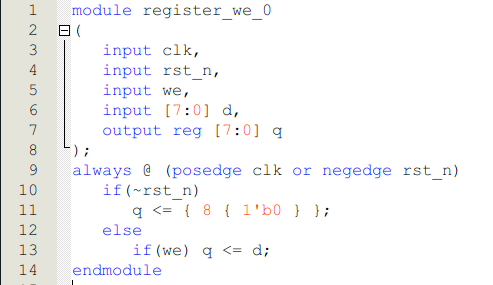


RTL:

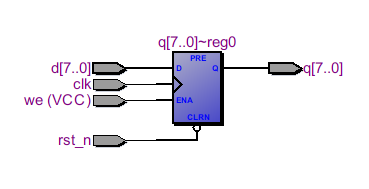


1. **Thiết kế khối PWM**
   1. **Khối Register**

Code:

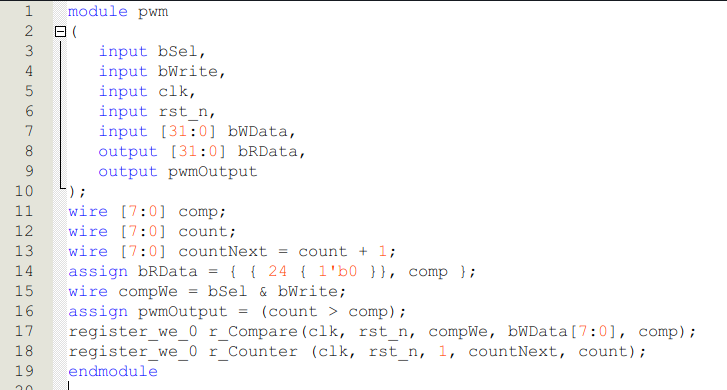


RTL:

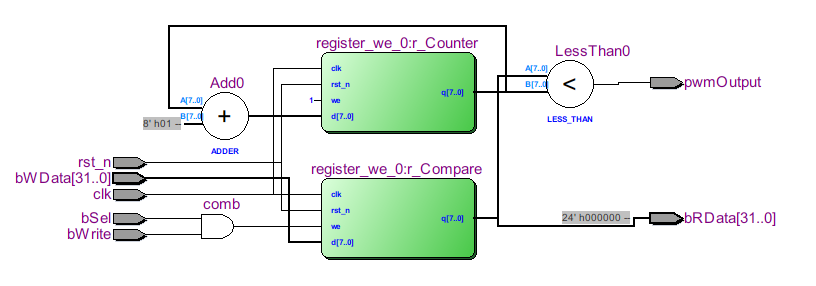


* 1. **Khối PWM**

Code:

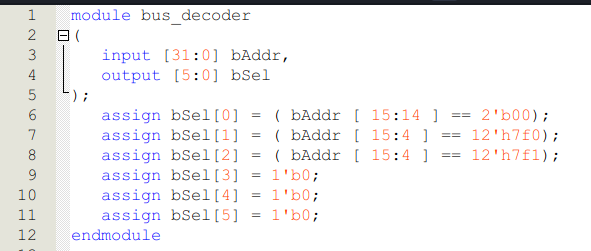


RTL:

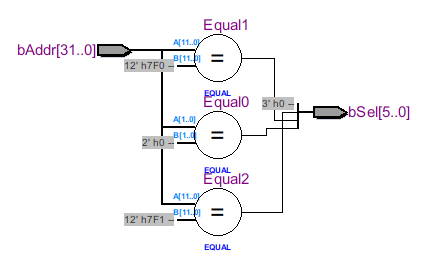


1. **Thiết kế BUS**
   1. **Khối Decoder**

Code:

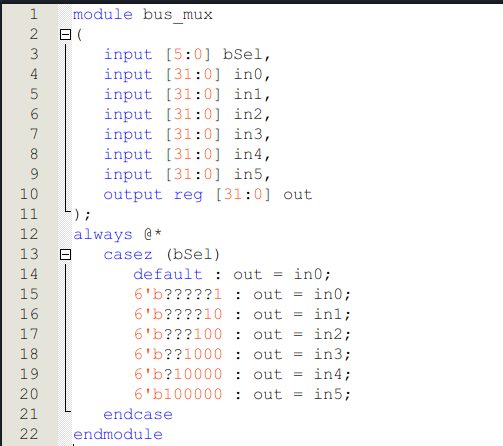


RTL:



* 1. **Khối Mux**

Code:



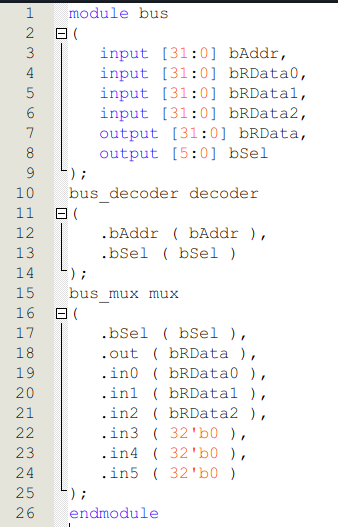
RTL:

A diagram of a diagram

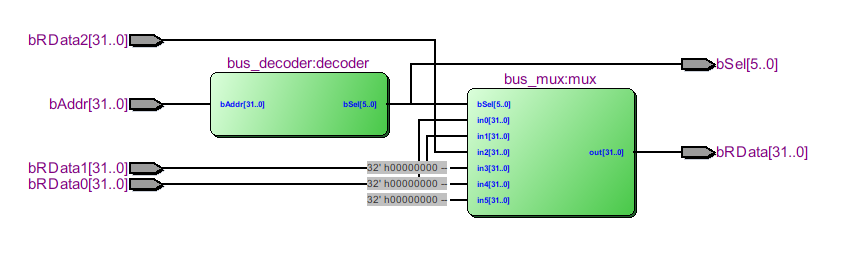
AI-generated content may be incorrect.

* 1. **BUS**

Code:

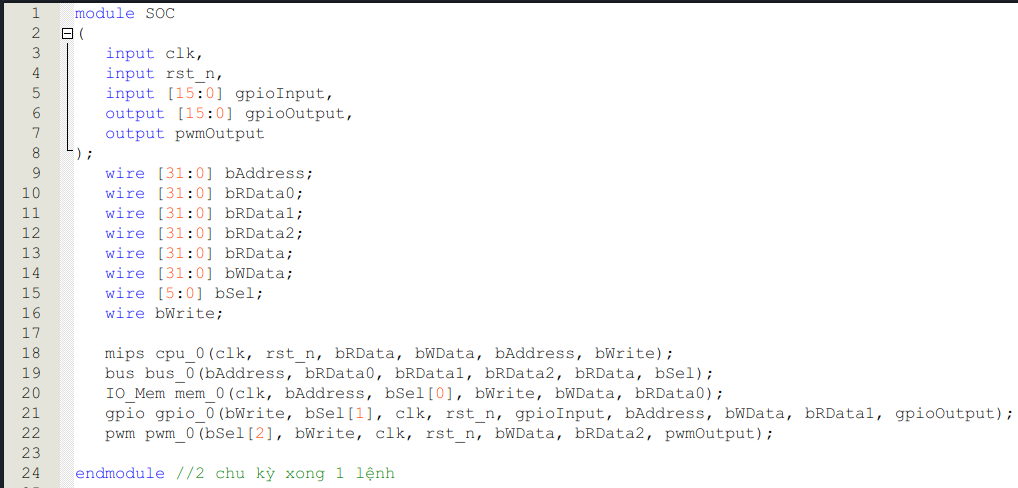


RTL:

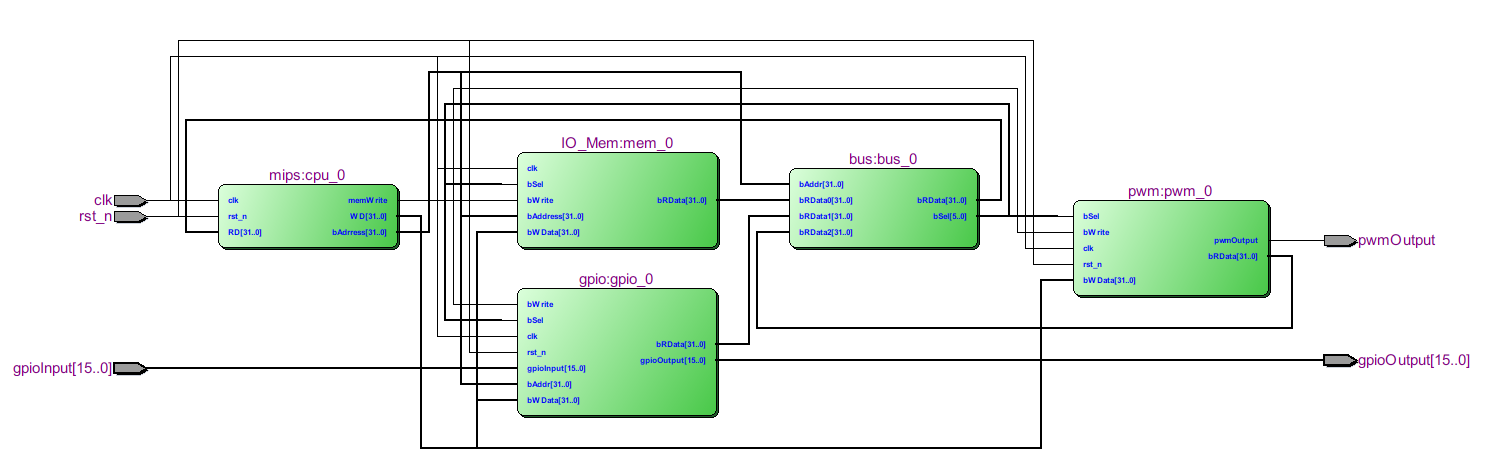


1. **Thiết kế SOC**

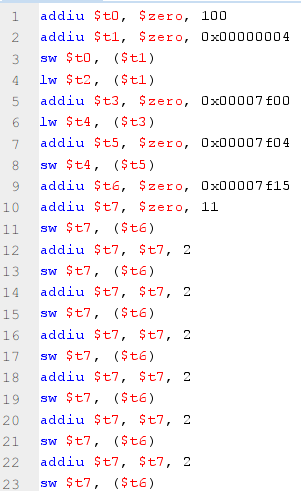
Code:



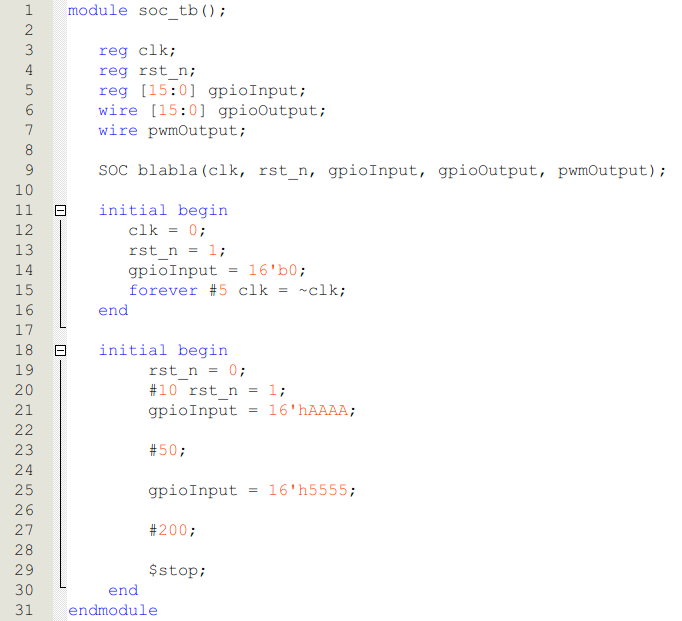
RTL:



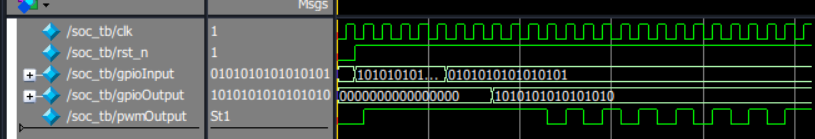
Code Assembly:



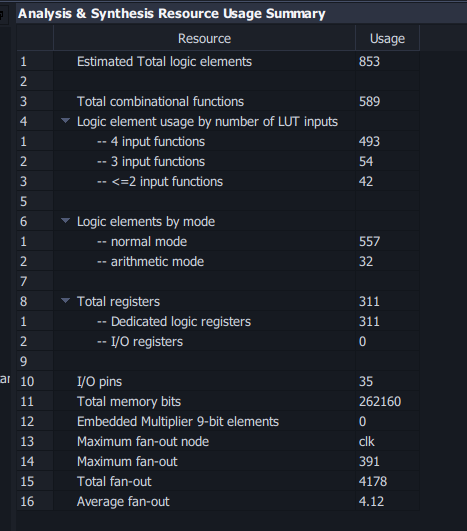
Testbench:



Sóng mô phỏng:

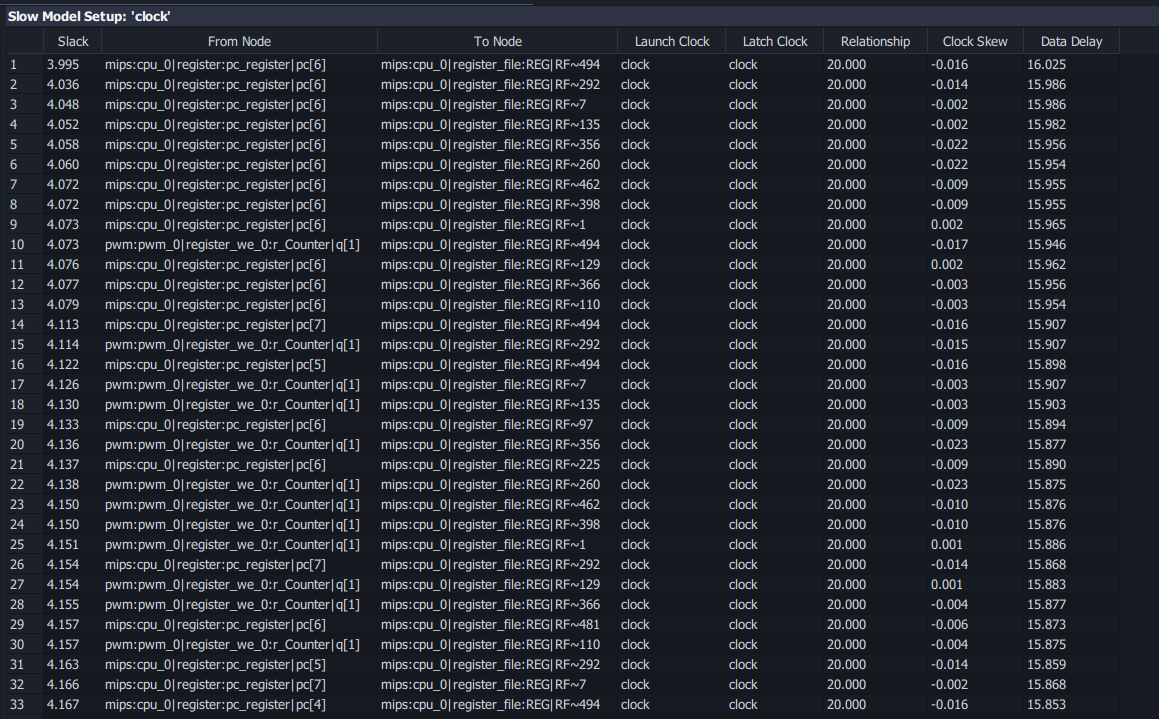


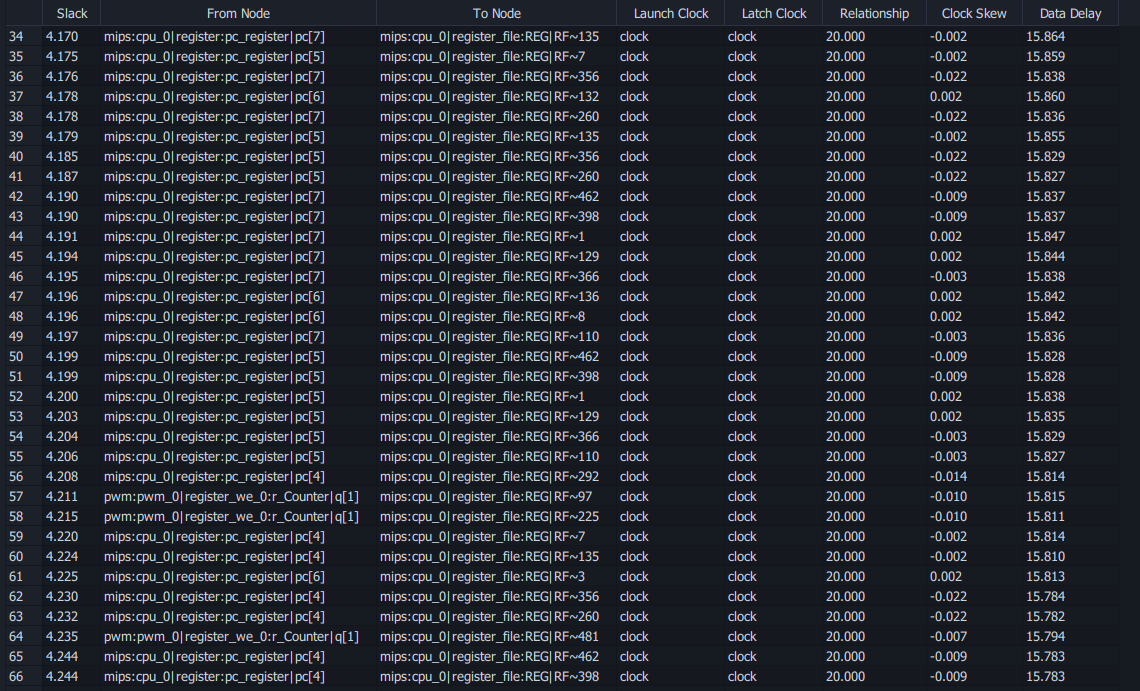
1. **Report**
   1. **Resource**

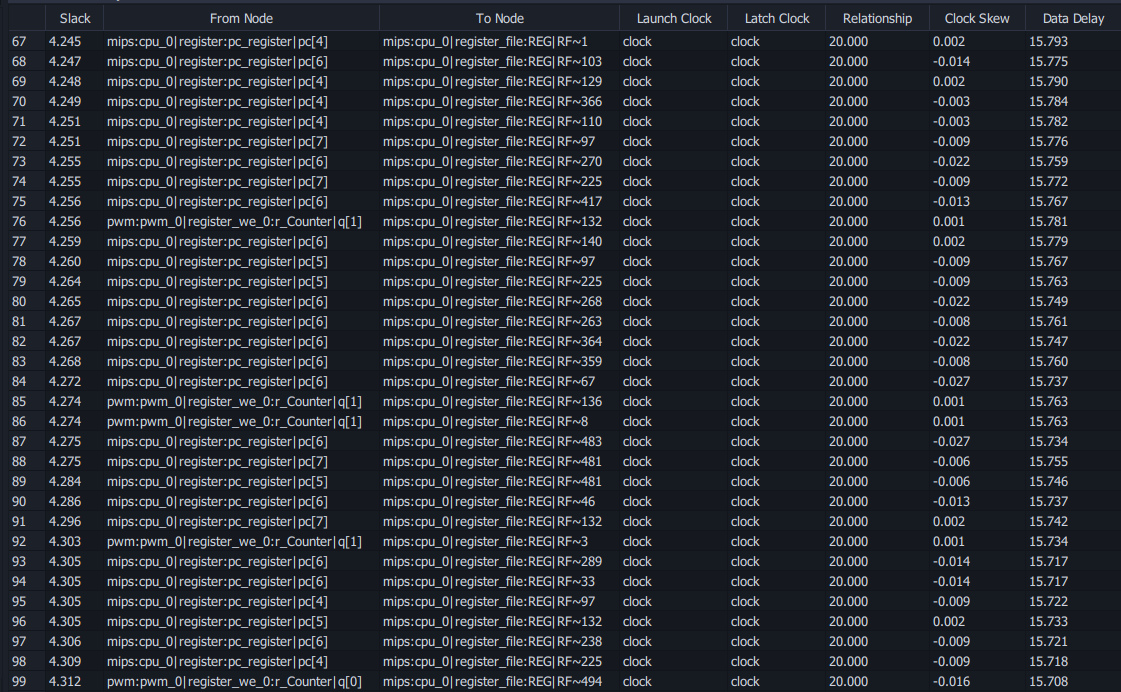


* 1. **Timing**











* 1. **Power**

