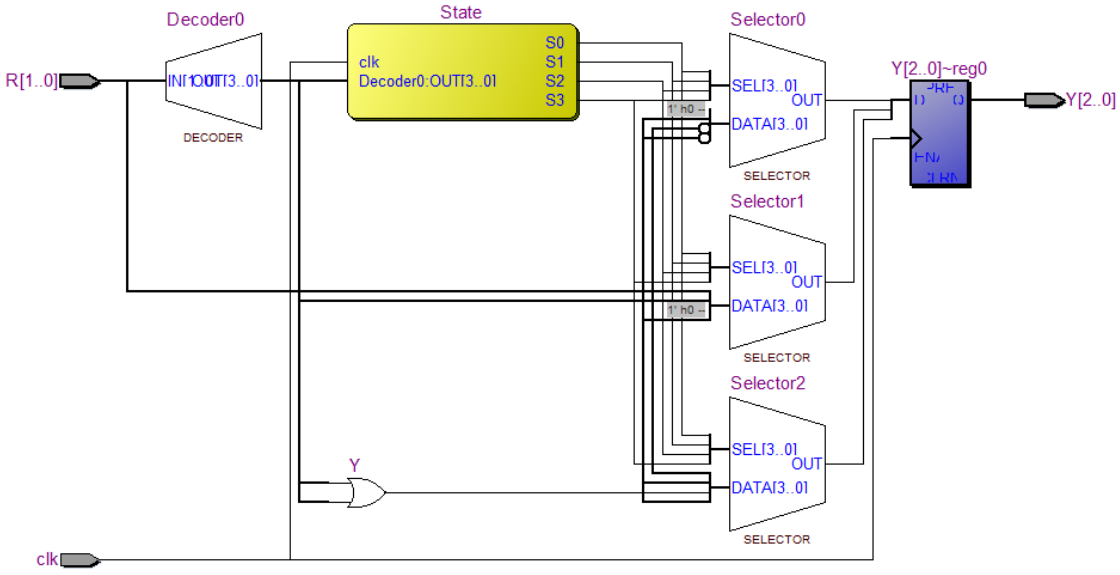
Code

```
module BT6(R, Y, clk);
input [1:0] R;
reg [1:0] State;
output reg [2:0] Y;
input clk;

parameter S0 = 2'b00;
parameter S1 = 2'b01;
parameter S2 = 2'b10;
parameter S3 = 2'b11;

parameter U1 = 3'b001;
parameter U2 = 3'b010;
parameter U3 = 3'b011;
parameter D1 = 3'b100;
parameter D2 = 3'b101;
parameter D3 = 3'b110;
parameter K = 3'b000;

initial
   State <= S0;

always @(posedge clk)
case(State)
   0 : begin
         case(R)
            0 : begin
                State <= S0;
                Y <= K;
                end
            1 : begin
                State <= S1;
                Y <= U1;
                end
```

```
35              2 : begin
36                  State <= S2;
37                  Y <= U2;
38                  end
39              3 : begin
40                  State <= S3;
41                  Y <= U3;
42                  end
43          endcase
44      end
45  1 : begin
46          case(R)
47              0 : begin
48                  State <= S0;
49                  Y <= D1;
50                  end
51              1 : begin
52                  State <= S1;
53                  Y <= K;
54                  end
55              2 : begin
56                  State <= S2;
57                  Y <= U1;
58                  end
59              3 : begin
60                  State <= S3;
61                  Y <= U2;
62                  end
63          endcase
64      end
65  2 : begin
66          case(R)
67              0 : begin
68                  State <= S0;
```

```
                Y <= D2;
                end
            1 : begin
                State <= S1;
                Y <= D1;
                end
            2 : begin
                State <= S2;
                Y <= K;
                end
            3 : begin
                State <= S3;
                Y <= U1;
                end
        endcase
      end
   3 : begin
        case(R)
            0 : begin
                State <= S0;
                Y <= D3;
                end
            1 : begin
                State <= S1;
                Y <= D2;
                end
            2 : begin
                State <= S2;
                Y <= D1;
                end
            3 : begin
                State <= S3;
                Y <= K;
                end
        endcase
      end
endcase
endmodule
```

RTL


Decoder0
State
Selector0
Y[2..0]~reg0
R[1..0]
clk
Decoder0:OUTI3..0]
S0
S1
S2
S3
SELI3..0]
DATAI3..0]
OUT
DECODER
SELECTOR
Selector1
Selector2
Y
Y[2..0]
clk

Testbench

```
1  `timescale 1ns/100ps
2
3  module BT6_tb;
4
5      reg [1:0] R;
6      reg clk;
7
8      wire [2:0] Y;
9
10     BT6 uut (
11         .R(R),
12         .Y(Y),
13         .clk(clk)
14     );
15
16     initial begin
17         clk = 0;
18         forever #10 clk = ~clk;
19     end
20
21     initial begin
22         R = 0;
23
24         #20;
25
26         $display("Input R1 3 lan");
27         R = 1;
28         #20;
29         #20;
30         #20;
31
32         $display("\nLen tang 3 roi xuong tang G");
33         R = 3;
34         #20;
```

```
35          R = 0;
36          #20;
37          #20;
38
39          $display("\nLen xuong random");
40          R = 2;
41          #20;
42          R = 1;
43          #20;
44          R = 3;
45          #20;
46          R = 2;
47          #20;
48          R = 0;
49          #20;
50
51          $display("\nTest FSM flow");
52          R = 0;
53          #20;
54          R = 1;
55          #20;
56          R = 1;
57          #20;
58          R = 2;
59          #20;
60          R = 2;
61          #20;
62          R = 3;
63          #20;
64          R = 3;
65          #20;
66
67          #40;
68          $finish;
69      end
70
71      initial begin
72          $monitor("Time = %0t, State = %b, R = %b, Y = %b",
73                   $time, uut.State, R, Y);
74      end
75
76  endmodule
```

Biểu đồ sóng


Msgs
/BT6_tb/R
11
/BT6_tb/clk
1
/BT6_tb/Y
000
00 01 11 00 10 01 11 10 00 01 10 11
000 001 000 010 110 000 010 100 010 100 101 000 001 000 001 000 001 000