THIẾT KẾ HỆ THỐNG SỐ VỚI HDL
BÀI THỰC HÀNH 2

GVHD: Tạ Trí Đức

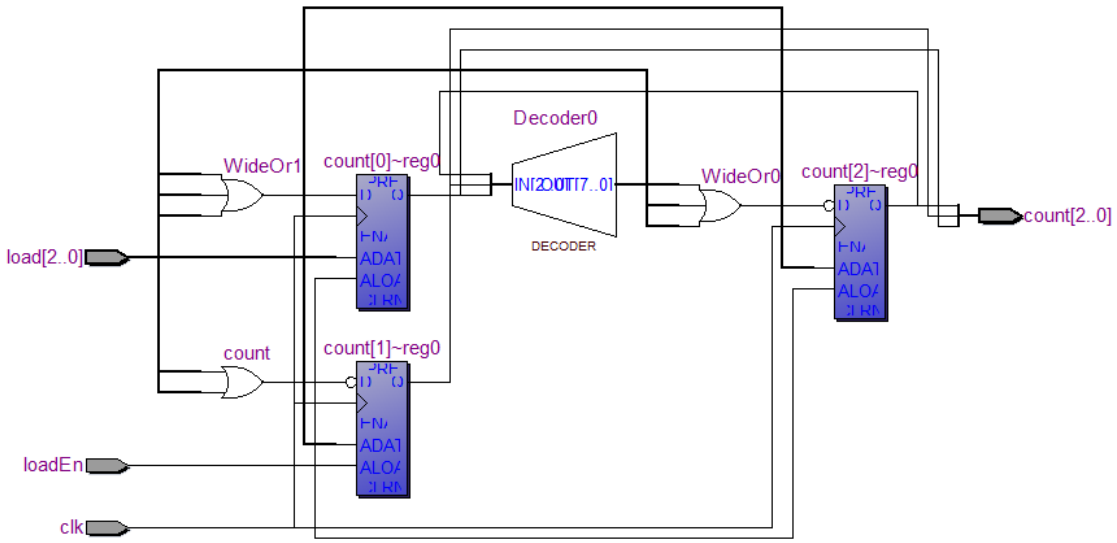
Sinh viên thực hiện: Phạm Quốc Tiến – 22521472

1) Thiết kế bộ đếm

Code:

```
1  module lab_2_1 (loadEn, clk, load, count);
2  input loadEn, clk;
3  input [2:0] load;
4  output reg [2:0] count;
5  always @ (posedge clk, posedge loadEn)
6     begin
7     if (loadEn)
8        count <= load;
9     else
10       case(count)
11          3'b000 : count <= 3'b110;
12          3'b110 : count <= 3'b100;
13          3'b100 : count <= 3'b111;
14          3'b111 : count <= 3'b011;
15          3'b011 : count <= 3'b000;
16          3'b101 : count <= 3'b010;
17          3'b010 : count <= 3'b111;
18          3'b001 : count <= 3'b110;
19       endcase
20    end
21 endmodule
22
```

RTL:



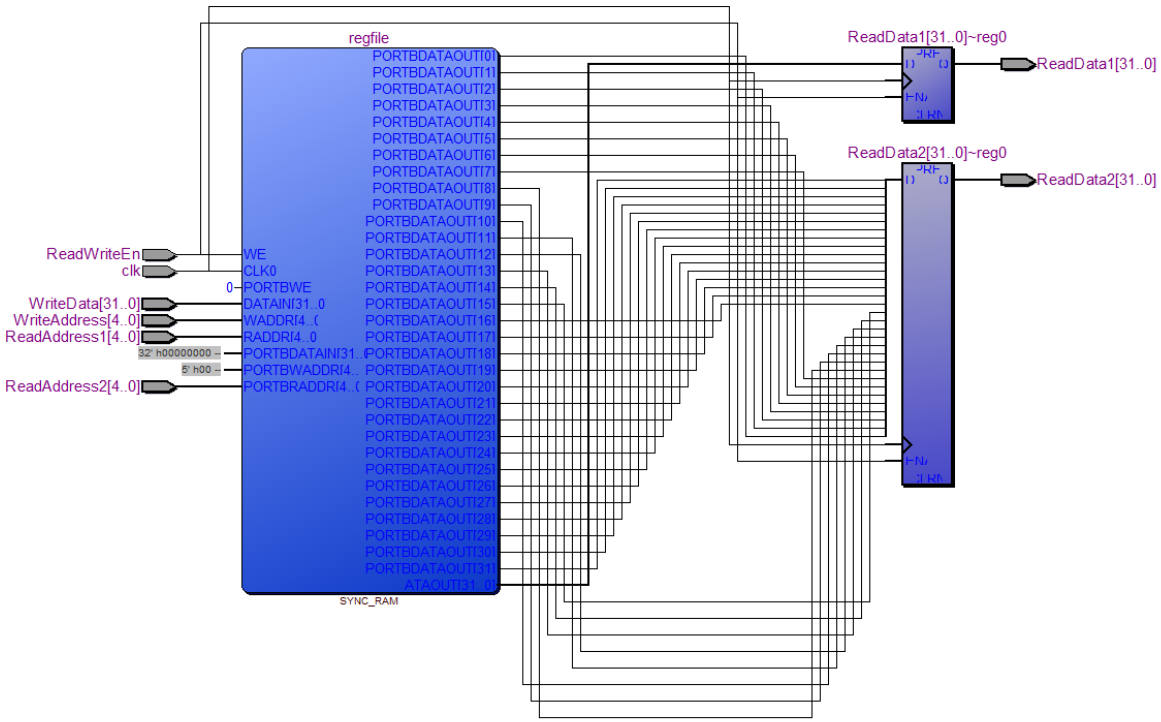
Waveform test function:

2) Thiết kế thanh ghi

Code:

```
 1  module lab_2_2 (ReadAddress1, ReadAddress2,
 2  WriteAddress, WriteData, ReadData1, ReadData2,
 3  ReadWriteEn, clk);
 4
 5  input [4:0] ReadAddress1, ReadAddress2, WriteAddress;
 6  input [31:0] WriteData;
 7  input ReadWriteEn;
 8  input clk;
 9  output reg [31:0] ReadData1, ReadData2;
10  reg [31:0] regfile [0:31];
11
12  always @ (posedge clk)
13     begin
14        if (ReadWriteEn)
15        begin
16           regfile[WriteAddress] <= WriteData;
17           ReadData1 <= regfile[ReadAddress1];
18           ReadData2 <= regfile[ReadAddress2];
19        end
20     end
21  endmodule
```

RTL:



Waveform test function: