Kamyashree T

8151038686 — kamyashree.t@gmail.com — linkedin.com/in/kamyashree-t — GitHub — Portfolio

Summary — Embedded Systems Engineer working on production Intel client SoC firmware, focusing on low-level platform configuration, feature enablement, and cross-layer debugging. Engaged in analyzing hardware–software interactions across firmware initialization flows, power configuration paths, and platform-specific SKUs. Strong foundation in C/C++, system architecture, and structured validation workflows, with growing interest in OS-level driver architecture and device-level software integration.

Experience

Intel Corporation, Bengaluru **July 2025 – Present**
Graduate Technical Trainee – SoC Firmware

- Contributing to client SoC firmware development within graphics-related configuration and feature enablement flows in production firmware.
- Designed and integrated **Dynamic Graphics Branding** feature, implementing platform-specific configuration logic across multiple client SKUs.
- Investigated and resolved a **PL4 power limit Hardware Status Debug (HSD)** issue by tracing configuration paths across firmware source, build artifacts, and generated binaries.
- Performed low-level debugging and root-cause analysis involving configuration flags, soft straps, and firmware initialization sequences.
- Participated in structured code reviews, architectural discussions, and cross-team issue triage in a large, modular firmware codebase.
- Analyzed workstation-class firmware variants (Razor Lake platform) to understand platform-specific deltas and reuse boundaries.
- Working on refactoring the firmware-to-ucode mailbox subsystem to remove deprecated HGS command handling by eliminating inheritance coupling and resolving associated build and dependency impacts in production firmware.

Skills

Programming: C, C++, Embedded C, Python

Firmware & Embedded: SoC firmware configuration, feature enablement, hardware–software interaction, ARM Cortex-M

RTOS Concepts: Task scheduling, multi-threading, IPC, Zephyr RTOS

Architecture Exposure: Power configuration flows, platform SKUs, firmware initialization logic

Tools: Git, Makefiles, Linux development environment, Visual Studio, CLion

Hardware / HDL (Academic): Verilog, VHDL, FPGA basics

Projects

RTOS-Based Task Management for Electric Vehicles **2024 – 2025**

- Designed an embedded task management framework using Zephyr RTOS to simulate EV subsystem coordination.
- Implemented multi-threaded task scheduling and IPC mechanisms with timing and memory analysis.
- Evaluated deterministic behavior and system responsiveness under varying load conditions.

Solar-Based Wireless EV Charging Station **2024**

- Designed a wireless power transfer system integrated with solar energy harvesting and storage management.
- Performed system-level efficiency analysis across varying load and environmental conditions.
- Optimized power transfer parameters through structured experimental validation.

PCB Defect Detection using Image Processing **2023**

- Developed an image-processing pipeline for detecting PCB manufacturing defects using pattern comparison techniques.
- Implemented noise filtering and threshold optimization to improve detection accuracy.
- Conducted controlled experimental validation to evaluate robustness under varying lighting and surface conditions.

Education

Vellore Institute of Technology (VIT) **2024 – 2026**
M.Tech — Embedded Systems

Sir M. Visvesvaraya Institute of Technology, Bengaluru **2020 – 2024**
B.E — Electronics and Communication Engineering