Counter Design

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The problem is due October 25, 2023, by 11:59 pm. Please submit original work.

Design a 16-bit program counter (PC) that supports features to: (1) increment the current PC value for the next clock cycle; (2) load a new value into the PC for the next clock cycle; and (3) reset the PC to zero for the next clock cycle. You may design the PC using the various built-in chips available under nand2tetris/tools/builtInChips, including the `Inc16` and `Register16` chip parts.

You have been provided with the `PC.hdl` file as a starting point to develop your solution. Your chip design will be tested using the supplied `PC.tst` file. When loaded into the hardware simulator, `PC.tst` loads your HDL design, and supplies a battery of test inputs to it and stores the output responses in `PC.out`. Contents of `PC.out` must match the outputs listed in the supplied `PC.cmp` file exactly. If not, the simulator will display an error.

Please submit the completed `PC.hdl` file via BBLearn. Do not include any other files.