Adder Design

Prof. Naga Kandasamy
ECE Department, Drexel University

The problems in this set are due October 11, 2023, by 11:59 pm. Please submit original work.

Design the following adder components in HDL:

1. **(5 points)** Half-adder stage.
   - Build this circuit using the basic gates (or, and, not, and xor).
2. **(5 points)** Full-adder stage.
   - Build this circuit using the basic gates (or, and, not, and xor).
3. **(5 points)** Four-bit ripple-carry adder.
   - Build this circuit using the previously built half-adder and full-adder stages.
4. **(5 points)** Four-bit carry lookahead adder.
   - Generate the required generate signals (g_0, g_1, g_2, g_3) and propagate signals (p_0, p_1, p_2, p_3). Use these signals to generate the carry bits (c_0, c_1, c_2, c_3). Supply the carry bits to the full adder stages to generate the sum bits. The carry-out signals generated by the full adders can be assigned to dummy wires which are never used, that is, discarded.

Using the above adder components, build the following larger components:

1. (**10 points**) 16-bit ripple-carry adder by linking up four 4-bit ripple-carry adders.
2. (**10 points**) 16-bit carry lookahead adder by linking up four 4-bit carry lookahead adders in carry-ripple style.

Use the provided `.hdl` files as a starting point to develop your solutions. Submit the completed `.hdl` files via BBLearn as a single zip file. Do not submit any other files.

Note: Testing scripts are not supplied for this assignment to test your designs; you must do so by manually providing inputs via the Hardware Simulator.

When provided with 4-bit inputs, the simulator does not treat these numbers as belonging to the 2s complement system. Therefore, test the 4-bit adder designs by having them perform unsigned arithmetic on positive numbers in the range 0 to 15. Do not supply negative numbers to the 4-bit adders since the simulator does not know how to interpret them correctly. For 16-bit designs, however, the simulator knows how to correctly treat them within the twos complement system. You may test the 16-bit designs using both negative and positive numbers.