Memory Design

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The problems in this set are due October 25, 2023 by 11:59 pm. Please submit original work.

Using HDL, design the following memory components in recursive fashion.

1. **(5 points)** Memory cell to store a single bit. Design the cell from first principles using only basic built-in gates (includes the multiplexer) and a D flip-flop.
2. **(5 points)** A 16-bit parallel-load register. Build this unit using the single-bit memory cells that you previously designed.
3. **(5 points)** Random-access data memory containing eight 16-bit registers (RAM8). Build the RAM8 unit using registers that you previously designed.
4. **(5 points)** Random-access data memory containing sixty four registers (RAM64). Build the RAM64 unit using the RAM8 units that you previously designed.

You have been provided with `.hdl` files as a starting point to develop your solutions. Your chip design will be tested using the supplied `.tst` file. When loaded into the hardware simulator, the `.tst` file loads your HDL design, and supplies a battery of test inputs to it and stores the output responses in a `.out` file. The contents of the `.out` file must match the outputs listed in the supplied `.cmp` file exactly. If not, the simulator will display an error.

Please submit the completed `.hdl` files via BBLearn as a single `.zip` file. Do not include the `.tst`, `.cmp`, and `.out` files.