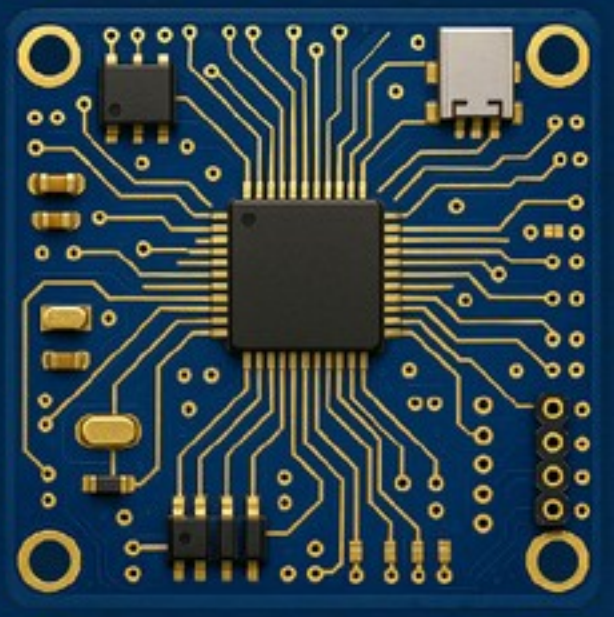
PREDICTABLE DESIGNS

DESIGN REVIEW CHECKLIST

PRINTED CIRCUIT BOARD (PCB) LAYOUT



PCB Layout Review Checklist

Board Owner:	
Reviewer:	
Date:	

1. Board Structure & Outline

- [ ] Board outline is closed and valid

- [ ] Board dimensions appear reasonable for application

- [ ] Mounting holes present and properly sized

- [ ] Mounting holes have keepout for screws/standoffs

- [ ] Corner radius appropriate for manufacturability

- [ ] PCB thickness specified in stackup

2. Component Placement

- [ ] Components grouped logically by function

- [ ] High-power components not clustered together

- [ ] Tall components positioned to avoid mechanical interference

- [ ] Connectors accessible (not blocked by other components)

- [ ] Polarized components oriented consistently where possible

- [ ] Components with thermal pads positioned for heat management

- [ ] Adequate spacing between components for assembly

- [ ] No components too close to board edges

3. Power Distribution

- [ ] Power traces appropriately sized for current (wider for high current)

- [ ] Power connector pins/traces sized for expected current

- [ ] Multiple vias used for high-current connections

- [ ] Decoupling capacitors placed immediately adjacent to IC power pins

- [ ] Bulk capacitors positioned near power input

- [ ] Ground plane present and continuous

- [ ] Power planes used appropriately

- [ ] No long thin power traces creating bottlenecks

- [ ] Star-point grounding implemented if design uses split ground

4. Switching Power Supply Layout

- [ ] Switching regulator follows manufacturer layout guidelines

- [ ] Input capacitor close to regulator input pin

- [ ] Output capacitor close to regulator output pin

- [ ] Feedback trace routed away from switching node

- [ ] Switching node trace/copper area minimized

- [ ] Ground connections solid (not thin traces)

- [ ] Hot loop area minimized

5. High-Speed & Critical Signals

- [ ] Differential pairs routed together with consistent spacing

- [ ] Differential pair lengths matched (equal length)

- [ ] High-speed signals have continuous ground plane beneath

- [ ] High-speed traces avoid crossing splits in ground plane

- [ ] Clock signals kept short and direct

- [ ] Clock traces not running parallel to other signals

- [ ] No stubs on high-speed or clock traces

- [ ] Via count minimized on critical signals

- [ ] Controlled impedance traces have appropriate width

6. RF Layout (if applicable)

- [ ] RF traces are 50Ω controlled impedance

- [ ] RF trace has ground plane underneath

- [ ] Antenna keepout area maintained (no copper beneath)

- [ ] RF section has ground stitching vias

- [ ] RF traces kept away from digital signals

- [ ] Matching network layout matches reference design

7. Analog Signal Routing

- [ ] Analog traces routed away from digital/switching signals

- [ ] Analog ground separate or star-connected if used

- [ ] ADC input traces kept short and direct

- [ ] Guard rings around sensitive analog inputs if needed

- [ ] Differential analog signals routed as pairs

8. Thermal Management

- [ ] Thermal vias present under power components (ICs, regulators)

- [ ] Thermal vias adequate count (typically 9+ for high power)

- [ ] Thermal vias not tented (open for heat transfer)

- [ ] Copper area around hot components for heat spreading

- [ ] Heatsink mounting provisions if pads present

- [ ] Thermal reliefs on ground plane connections (for soldering)

9. Crystal/Oscillator Layout

- [ ] Crystal placed very close to IC

- [ ] Crystal load capacitors placed immediately adjacent

- [ ] Ground plane solid under crystal

- [ ] Crystal traces kept short with no vias if possible

- [ ] No high-speed signals routed near crystal

10. EMI & Grounding

- [ ] Ground plane coverage good (>70% on ground layers)

- [ ] Ground stitching vias around board perimeter

- [ ] Ground stitching vias near RF circuits and high-speed

- [ ] No long parallel trace runs (creates coupling)

- [ ] Traces not running along board edges

- [ ] Isolated copper islands removed or grounded

- [ ] Return current paths not interrupted

11. Manufacturing & Assembly

- [ ] Fiducials present (minimum 3, asymmetrically placed)

- [ ] Fiducials in clear area (not obscured)

- [ ] Tooling holes present if needed

- [ ] Component orientation consistent (same direction where possible)

- [ ] Fine-pitch components oriented for easier inspection

- [ ] Panelization appropriate if multiple boards per panel

- [ ] Breakaway tabs or V-scoring visible if panelized

12. Silkscreen & Markings

- [ ] All ICs have pin 1 marked clearly

- [ ] Polarized components have polarity marked (+/-, cathode stripe)

- [ ] Component reference designators present and readable

- [ ] Silkscreen not covering pads or vias

- [ ] Board revision number visible on silkscreen

- [ ] Company name or logo present if appropriate

- [ ] Test point labels present where applicable

- [ ] Connector pin numbering marked if helpful

- [ ] Silkscreen text size readable (>1mm height)

13. Layer Stackup

- [ ] Layer count appropriate (not excessive)

- [ ] Ground layers positioned for signal return paths

- [ ] Power planes present where appropriate

- [ ] Stackup appears symmetrical (prevents warping)

- [ ] Layer thicknesses reasonable

14. Final Verification

- [ ] No obvious DRC violations visible

- [ ] All component footprints appear correct

- [ ] Net names visible and make sense

- [ ] BOM count matches components on board

- [ ] Test points accessible

- [ ] Programming header accessible and properly connected

- [ ] No obvious routing errors (traces going wrong direction)