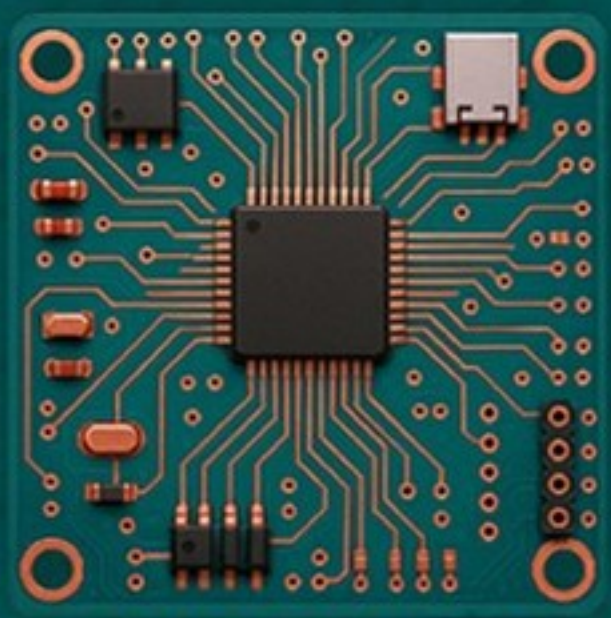
PREDICTABLE DESIGNS

DESIGN REVIEW CHECKLIST

Schematic Circuit



Schematic Design Review Checklist

Board Owner:

Reviewer:

Date:

1. Component Selection & Ratings

- [ ] All components are currently in production (not obsolete/NRND)

- [ ] Second sources available for critical single-source components

- [ ] Package types are appropriate (SMT sizes reasonable, THT where needed)

- [ ] Voltage ratings have adequate margin (check against net voltages)

- [ ] Power ratings have adequate margin for resistors/regulators

- [ ] Capacitor voltage ratings include derating (typically 2x minimum)

2. Power Supply & Protection

- [ ] Input protection present (reverse polarity, overvoltage)

- [ ] Inrush current limiting components present if needed

- [ ] Power supply voltages are reasonable for the circuitry

- [ ] Switching regulator has input and output capacitors per datasheet

- [ ] Linear regulator input/output voltage differential appropriate

- [ ] ESD protection diodes/TVS on all external-facing connections

- [ ] Fuses or PTC devices sized appropriately if present

3. Bypass & Decoupling

- [ ] Every IC has at least one decoupling capacitor per power pin

- [ ] Decoupling capacitor values match IC datasheet recommendations

- [ ] Mix of capacitor values present (bulk + ceramic) where appropriate

- [ ] Analog ICs have separate decoupling from digital where recommended

4. Clock & Timing

- [ ] Crystal has correct load capacitors (verify with datasheet)

- [ ] Crystal load capacitor calculation is correct (CL = (C1*C2)/(C1+C2) + Cstray)

- [ ] Oscillator circuits match datasheet reference design

- [ ] Clock distribution buffers present if needed for fanout

5. Digital Interfaces

- [ ] I2C buses have pullup resistors (typically 2.2kΩ - 10kΩ)

- [ ] I2C pullup values appropriate for bus speed and capacitance

- [ ] SPI signals have correct connections (MISO/MOSI not swapped)

- [ ] SPI chip selects are active-low with pullups where needed

- [ ] UART connections correct (TX to RX, RX to TX)

- [ ] USB data lines have correct termination (22Ω series resistors)

- [ ] USB has correct pullup on D+ (1.5kΩ for full-speed)

- [ ] Ethernet has magnetics and correct termination resistors

- [ ] CAN bus has 120Ω termination at both ends only

- [ ] Level shifters present where signals cross voltage domains

- [ ] Logic levels compatible between connected ICs

6. Analog Circuits

- [ ] Op-amp feedback networks appear reasonable (gain, stability)

- [ ] ADC reference voltage is stable (buffered, filtered)

- [ ] ADC input range matches expected signal levels

- [ ] Input protection present on ADC inputs (clamp diodes, series R)

- [ ] Anti-aliasing filters present before ADC inputs where needed

- [ ] DAC output has appropriate load/buffer

- [ ] Sensor signal conditioning appears appropriate

- [ ] Analog ground separate from digital if used

7. IC Pin Configuration

- [ ] Configuration/strapping pins set with resistors (not left floating)

- [ ] Unused inputs have pullups/pulldowns (not left floating)

- [ ] Multi-function pins configured appropriately

- [ ] Reset pins have pullups if active-low

- [ ] Enable pins configured correctly

- [ ] Mode/configuration pins set per intended operation

8. RF/Wireless (if applicable)

- [ ] RF section has appropriate antenna connection (connector or chip antenna)

- [ ] Antenna feed has 50Ω impedance matching network

- [ ] RF section has appropriate filtering

- [ ] Balun/matching network matches reference design

9. Schematic Documentation & Clarity

- [ ] All components have unique reference designators

- [ ] Component values clearly labeled and readable

- [ ] Net names are meaningful (not default names)

- [ ] Power nets clearly labeled with voltages (3V3, 5V0, etc.)

- [ ] All IC pins are connected or explicitly marked NC (no connect)

- [ ] No obvious missing connections or floating nets

- [ ] Connector pin numbering is clear

- [ ] Schematic is organized logically by function

10. Test & Debug Access

- [ ] Programming header present (JTAG, SWD, ISP, etc.)

- [ ] Programming header pins correctly connected per standard

- [ ] Serial debug port accessible (UART/USB)

- [ ] Test points or headers on critical signals

- [ ] LED indicators present for power and status