Karthikeyan Renga Rajan

DOB: November 2, 2001

College Of Engineering Guindy(CEG), Anna University

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Indian Citizenship

Social Network

Github Projects Page Link

LinkedIn Link

Skills

Linux

C/C++

Verilog

Python

SystemVerilog

Vivado

Tensorflow

PyTorch

Matlab

CUDA

Computer Vision

Vim

HTML

CSS

Languages

English — TOEFL - 116/120

Hindi — Native

Tamil — Native

Education

2019 - 2023 — **Bachelor of Engineering in Electronics and Communication Engineering** — CEG,Anna University

Cumulative GPA : 9.41 out of 10

2019 — **Class XII** — National Victor Public School, Delhi

Aggregate : 95.2%

2017 — **Class X** — National Victor Public School, Delhi

Cumulative GPA : 10 out of 10

Work Experience

December 2022 - Present — **Co-founder and Digital Design Engineer at HelixLogic** — Chennai, India

- Designed and Implemented an ASIC in SystemVerilog to decode DNA sequences based on signals derived from a Nanopore Membrane.
- Startup funded by the Indian Government's BIRAC EYUVA program.
- Managing a two-member student team.

May 2022 - August 2022 — **Summer Internship at University of Toronto, Canada (In-person)** — ISM Laboratory

- Summer Internship under Prof. Roman Genov at the University of Toronto funded by MITACS.
- Developed a RISC-V core(in SystemVerilog) to create custom mask sequences on the fly for the coded-exposure image sensors.
- Worked on mask generation and mask decompression modules for generating hard-coded masks and receiving compressed masks.
- Completed a Continuous Integration flow for the project.
- Completed an Automatic Documentation engine for the project.

June 2021 - July 2021 — **Research Internship at the Indian Academy of Sciences(IASc), Bengaluru** — Integrated Systems Laboratory

Project under Summer Research fellowship: Image-Based-Rendering based Reinforcement learning environment for end-to-end training to avoid sim2real, domain adaptation or domain randomization etc using CUDA and OpenGL

May 2021 - January 2022 — **Research Internship at Anna University, Chennai, India** — Integrated Systems Laboratory

- Implemented RTL changes(in Verilog) to accommodate the modified architecture of the ASIC.
- Wrote test benches to simulate and verify the behavioral functioning of any given module.

Projects

January 2023 - April 2023 — **Implementation of a Machine Learning Inference Accelerator with a Hierarchical Mesh-based NoC**

A SystemVerilog Implementation of the Eyeriss CNN architecture with a Hierarchical Mesh-based Network-on-Chip(NoC) optimization to maximize data reuse and approximate multipliers to increase speed and energy efficiency.

August 2021 - January 2023 — **Metis(V1 & V2)**

A programmable 256-neuron, 2048-synapse neuromorphic chip in 130nm CMOS was developed to accelerate inference and learning for various types of recurrent spiking neural networks(RSNNs). The chip features an analog circuit for leaky integrate-and-fire neurons and on-chip e-prop learning. The on-chip e-prop trains a spiking neural network to achieve an accuracy of 98.96% on the MNIST dataset with a power efficiency of 4.78pJ/SOP at 1.8V.

August 2022 - December 2022 **H.264 Video Codec Accelerator**
An Verilog Implementation of the H.264 Video Codec accelerator over PCIe. Simulated using Verilator, SystemC-TLM, and QEMU. Includes Device Drivers for Linux using DMA and Verilog.

August 2022 - December 2022 **Hardware-Software Codesign for Verilog development over PCIe**
Developed a PCIe-Verilog verification setup for codesign using QEMU and SystemC-TLM. Used to develop Firmware and Hardware simultaneously. Uses Remote Port IPC to connect the QEMU Virtual machine and the Verilator simulation

June 2020 - October 2020 **Tyche**
Adaptive traffic control using Deep Reinforcement Learning: Deep Q-Network and Cityflow OpenAI gym environment. Uses Q-learning(and PPO) to learn optimal traffic flow control

June 2020 - October 2020 **Machine Learning Assisted Verification Methodology for Analog and Mixed Signal Circuits**
Semiconductor Research Corporation(SRC)- Task 2982.001. The goal of the proposed work for AMS (Analog and Mixed Signal circuits) verification was to characterize the input space, the output space, and the mapping between the two using ML techniques, in such a manner that the quality and efficiency of design verification are improved.

Achievements

2024 **Anna University Guindy Engineers 65 Project Award Endowment**- Award for the best bachelor thesis project

2022 **BIRAC Startup Grant**- Funding for 'Ultrafast, Accurate Nanopore DNA sequencing using custom ASIC' Startup

2021 **First Position**- Techstars Startup Weekend Chennai: A startup pitch competition

2021 **First Position**- MATRIMAZE: An Advanced Matlab Competition, Vision 2021

2021 **First Position**- Web development Hackathon, Abacus CEG 2021

2018 - 2019 **Third Prize**- Silicon Battles Delhi, Senior Quiz

Positions

April 2021 - April 2023 **Student director**- Computer Society of Anna university
- Conducted workshops for junior students to teach them the technical skills required and plan their careers ahead

April 2021 - April 2023 **Student director**- National Service Scheme(NSS), India
- Contributed to the distribution of vaccines for those in need during the COVID-19 pandemic

December 2020 - April 2023 **Member**- Robotics Club of CEG

Workshops Attended

2020 **Operating Systems Workshop, Kurukshetra 2020**
A Deep look at Unix/Linux internals and File Systems

2020 **Basic Robotics Workshop**
A Basic Robotics workshop with hands-on experience