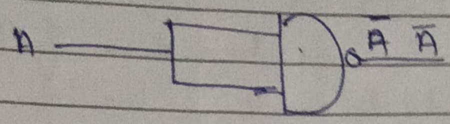
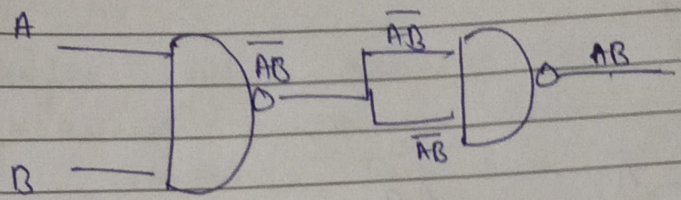
Mission 1

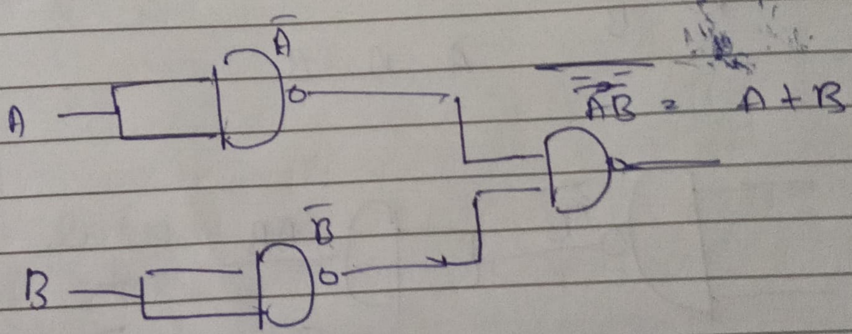
1) NOT



2) ~~A~~ AND



3) OR



Mission - 2

truth table

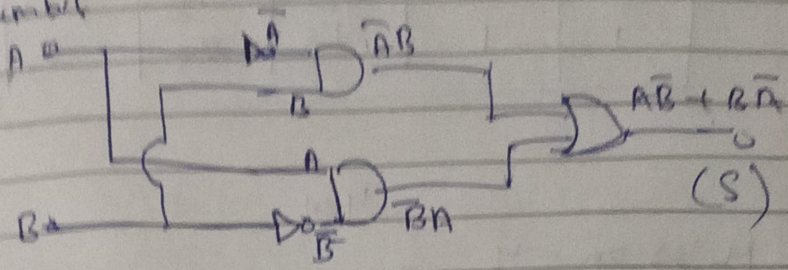
a)

Input		output	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

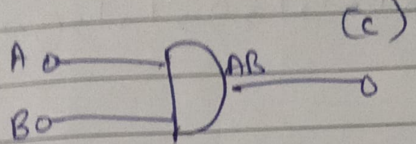
(b) $S = A\bar{B} + B\bar{A}$

$C = AB$

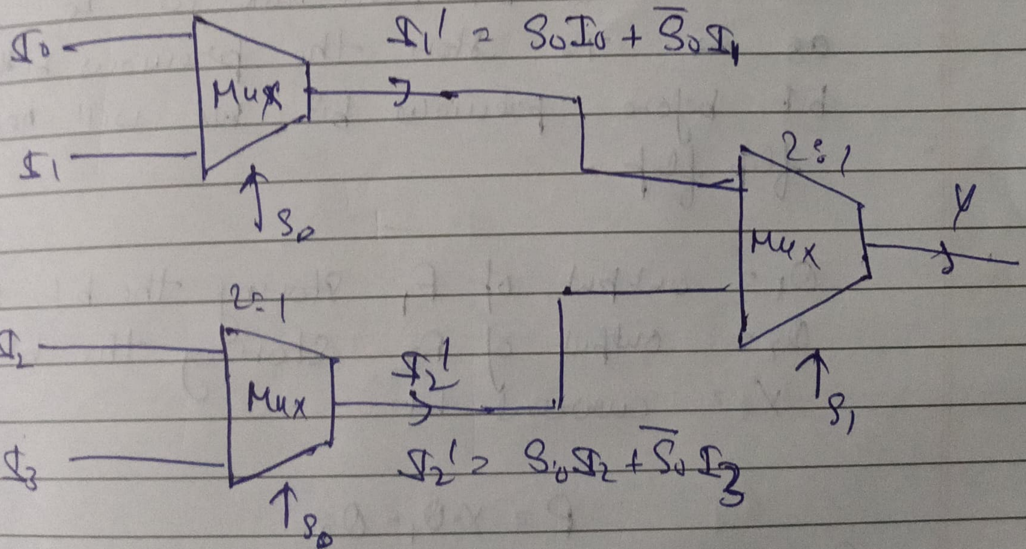
(c) (S) Sum bit



Carry bit



...ssion - 3



$y = S_1 I_1' + \bar{S}_1 I_2'$

4:1 MUX truth table

S_0	S_1	I_1'	I_2'	Y (output)
		I_1	I_3	I_3
0	0	I_1	I_3	I_1
0	1	I_0	I_2	I_2
1	0	I_0	I_2	I_0
1	1			

4:1

Mission - 4

a) Input stream

0, 1, 1, 1, 0, 1, 1, 1, 0

output

0, 0, 0, 1, 0, 0, 0, 1, 0

We would need 2 flip flop.
The current bit need not to be stored
~~as~~ ~~as~~ To store the previous bit and
bit before previous bit we will need two
flip flop.

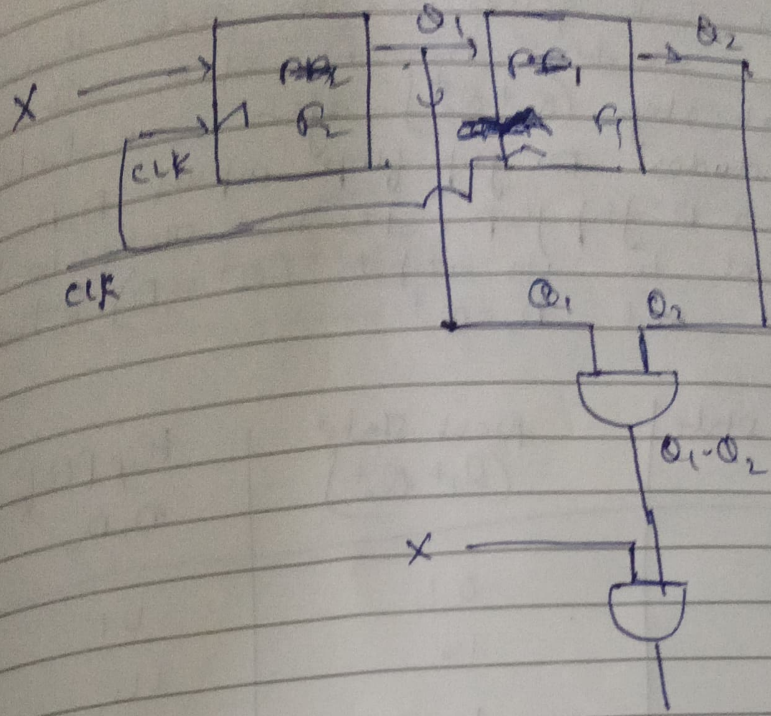
Q_1 = output of F_1 storing the bit 1 cycle old
Q_2 = output of F_2 storing the bit 2 cycle a
X = current bit

$$P = X \cdot Q_1 \cdot Q_2$$

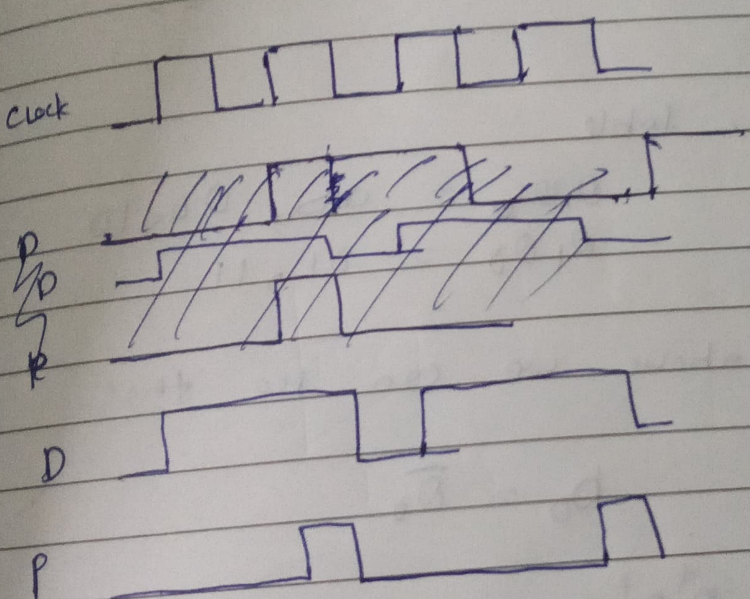
So ~~where~~ when

$X = 1$, $Q_1 = 1$, $Q_2 = 1$

only then $P = 1$



$P = Q_1 \cdot Q_2 \cdot X$



PAGE

Mission - 5

~~After 1 clock pulse~~, the state transition

a) Table relates current state $(Q_1 Q_0)$ to next stage $(Q_1^+ Q_0^+)$ after one clock pulse. It includes D flip-flop inputs $D_1 D_0$. Since for a D flip flop, the next state is equal to in input $(Q^+ = D)$. Therefore, $D_1 = Q_1^+$ and $D_0 = Q_0^+$

Current state $Q_1 Q_0$	Next State $(Q_1^+ . Q_0^+)$	flip flop $D_1 D_0$
00	01	01
01	10	10
10	11	11
11	00	00

b) from the table

$D_0 = 1$ $\quad Q_1 Q_0 =$ 00, 10

$D_0 = 0$ $\quad Q_1 Q_0 =$ 01, 11

from above we can see that

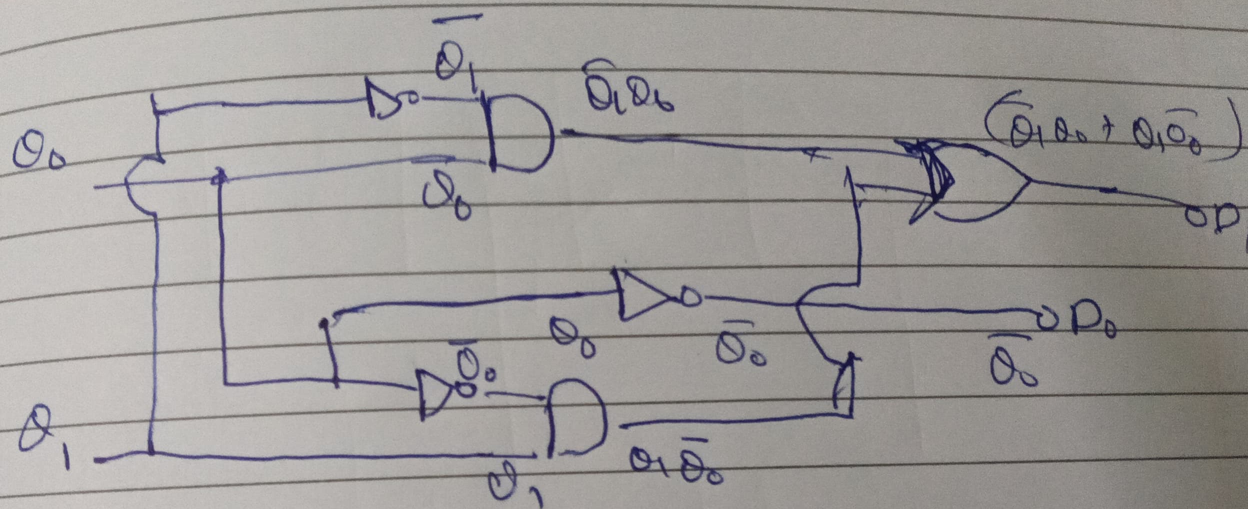
$$D_0 = \overline{Q_0}$$

$D_1 = 0$ $\quad Q_1^+ Q_0^+$ 00, 11

$D_1 = 1$ $\quad Q_1^+ Q_0^+$ 01, 10

$$D_1 = Q_1 \overline{Q_0} + \overline{Q_1} Q_0$$

(XOR)


Q_0
$\bar{Q}_1$
$\bar{Q}_1 Q_0$
Q_0
$(\bar{Q}_1 Q_0 + Q_1 \bar{Q}_0)$
D_1
Q_0
$\bar{Q}_0$
D_0
$\bar{Q}_0$
$\bar{Q}_0$
Q_1
$Q_1 \bar{Q}_0$
Q_1