SN75174
QUADRUPLE DIFFERENTIAL LINE DRIVER

- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11.**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Active-High Enable**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**
- **Functionally Interchangeable With MC3487**

N PACKAGE
(TOP VIEW)

1A	1	16	V_{CC}
1Y	2	15	4A
1Z	3	14	4Y
1,2EN	4	13	4Z
2Z	5	12	3,4EN
2Y	6	11	3Z
2A	7	10	3Y
GND	8	9	3A

DW PACKAGE
(TOP VIEW)

1A	1	20	V_{CC}
1Y	2	19	4A
NC	3	18	4Y
1Z	4	17	NC
1,2EN	5	16	4Z
2Z	6	15	3,4EN
NC	7	14	3Z
2Y	8	13	NC
2A	9	12	3Y
GND	10	11	3A

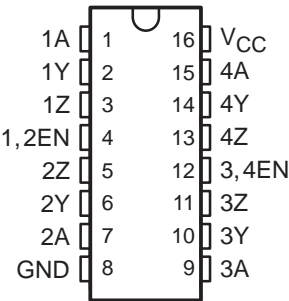NC – No internal connection

description

The SN75174 is a monolithic quadruple differential line driver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.
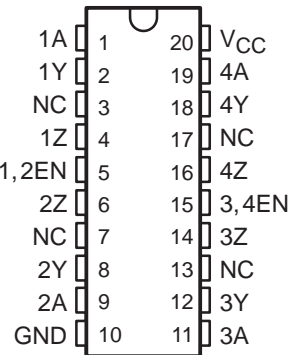
The SN75174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75174 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

INPUT	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = TTL high level, X = irrelevant,
L = TTL low level, Z = high impedance (off)

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TEXAS INSTRUMENTS

SN75174
QUADRUPLE DIFFERENTIAL LINE DRIVER

logic symbol†

1,2EN **4**	EN
1A **1**	▷ 2 1Y / 3 1Z
2A **7**	6 2Y / 5 2Z
3,4EN **12**	EN
3A **9**	▷ 10 3Y / 11 3Z
4A **15**	14 4Y / 13 4Z
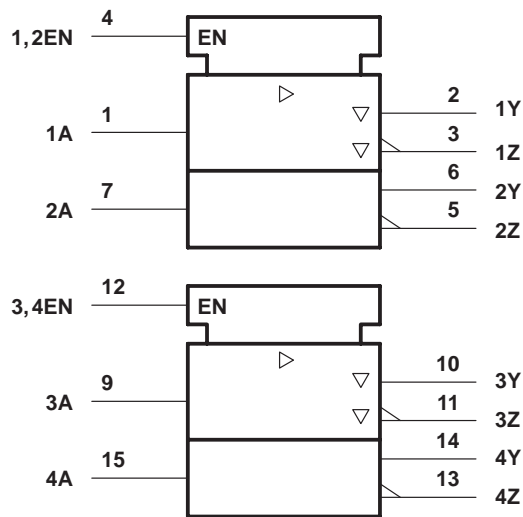
logic diagram, each driver (positive logic)

A ────▷──── Y
              ○ ── Z
EN ──▷──
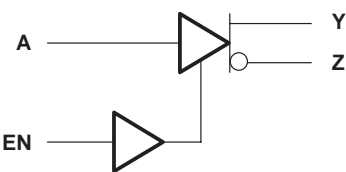
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs
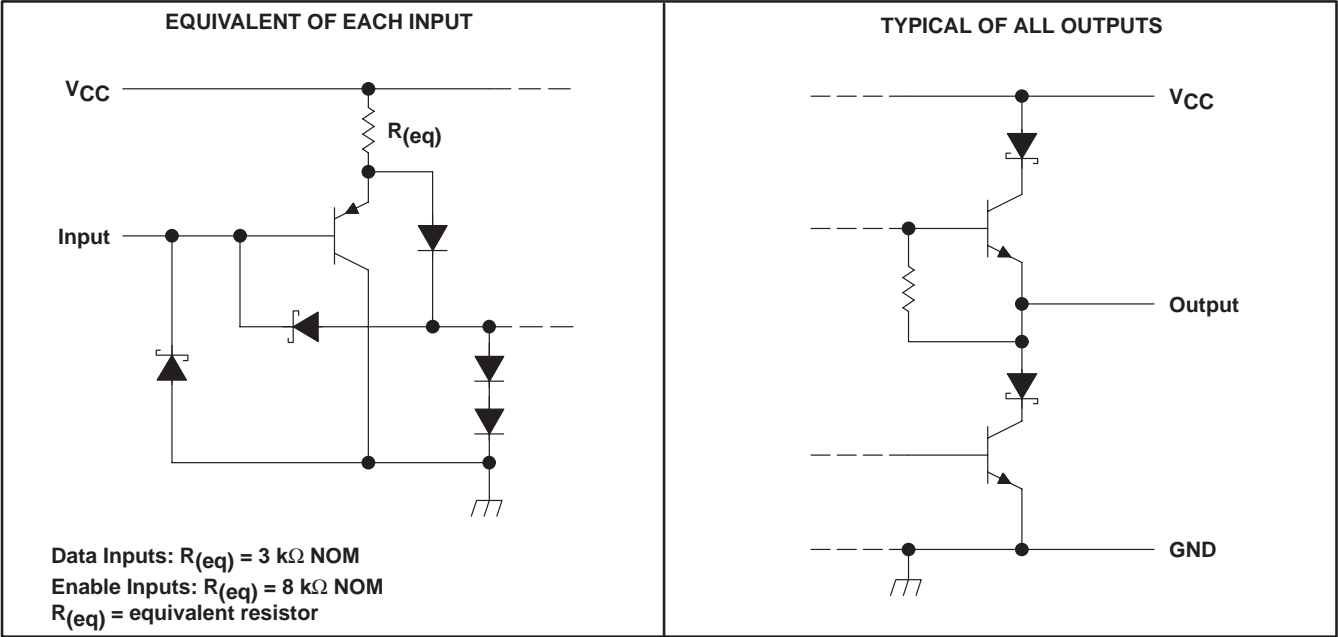
EQUIVALENT OF EACH INPUT	TYPICAL OF ALL OUTPUTS
V_{CC} — $R_{(eq)}$ — Input	V_{CC} — Output — GND

Data Inputs: $R_{(eq)}$ = 3 kΩ NOM
Enable Inputs: $R_{(eq)}$ = 8 kΩ NOM
$R_{(eq)}$ = equivalent resistor

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Output voltage range, V_O . . . . −10 V to 15 V
Input voltage, V_I . . . . 5.5 V
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1:   All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			−7 to 12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	$V_{IH} = 2$ V, $I_{OH} = -33$ mA	$V_{IL} = 0.8$ V,		3.7		V
V_{OL}	Low-level output voltage	$V_{IH} = 2$ V, $I_{OL} = 33$ mA	$V_{IL} = 0.8$ V,		1.1		V
V_O	Output voltage	$I_O = 0$		0		6	V
$|V_{OD1}|$	Differential output voltage	$I_O = 0$		1.5	6	6	V
$|V_{OD2}|$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1	1/2 V_{OD1} or 2[‡]			V
		$R_L = 54\ \Omega$,	See Figure 1	1.5	2.5	5	
V_{OD3}	Differential output voltage	See Note 2		1.5		5	V
$\Delta|V_{OD}|$	Change in magnitude of differential output voltage[§]					±0.2	V
V_{OC}	Common-mode output voltage[¶]	$R_L = 54\ \Omega$ or $100\ \Omega$,	See Figure 1			+3 −1	V
$\Delta|V_{OC}|$	Change in magnitude of common-mode output voltage[§]					±0.2	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7$ V to 12 V			±100	µA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V				±100	µA
I_{IH}	High-level input current	$V_I = 2.7$ V				20	µA
I_{IL}	Low-level input current	$V_I = 0.5$ V				−360	µA
I_{OS}	Short-circuit output current	$V_O = -7$ V				−180	mA
		$V_O = V_{CC}$				180	
		$V_O = 12$ V				500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Outputs disabled		18	40	

[†] All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

[‡] The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

[§] $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

[¶] In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

NOTE 2: See EIA Standard RS-485.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	$R_L = 54\ \Omega$,	See Figure 2		45	65	ns
$t_{t(OD)}$	Differential-output transition time				80	120	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$,	See Figure 3		80	120	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$,	See Figure 4		55	80	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$,	See Figure 3		75	115	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$,	See Figure 3		18	30	ns

TEXAS
INSTRUMENTS

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$|V_{OD1}|$	V_o	V_o
$|V_{OD2}|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$|V_{OD3}|$		V_t (Test Termination) Measurement 2)
$\Delta|V_{OD}|$	$||V_t| - |\overline{V}_t||$	$||V_t| - |\overline{V}_t||$
V_{OC}	$|V_{os}|$	$|V_{os}|$
$\Delta|V_{OC}|$	$|V_{os} - \overline{V}_{os}|$	$|V_{os} - \overline{V}_{os}|$
I_{OS}	$|I_{sa}|, |I_{sb}|$	
I_O	$|I_{xa}|, |I_{xb}|$	I_{ia}, I_{ib}

PARAMETER MEASUREMENT INFORMATION
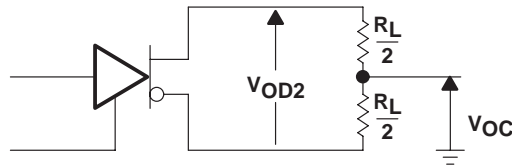
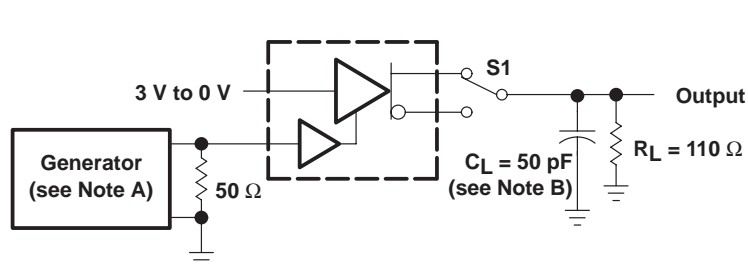**Figure 1. Differential and Common-Mode Output Voltages**

TEST CIRCUIT
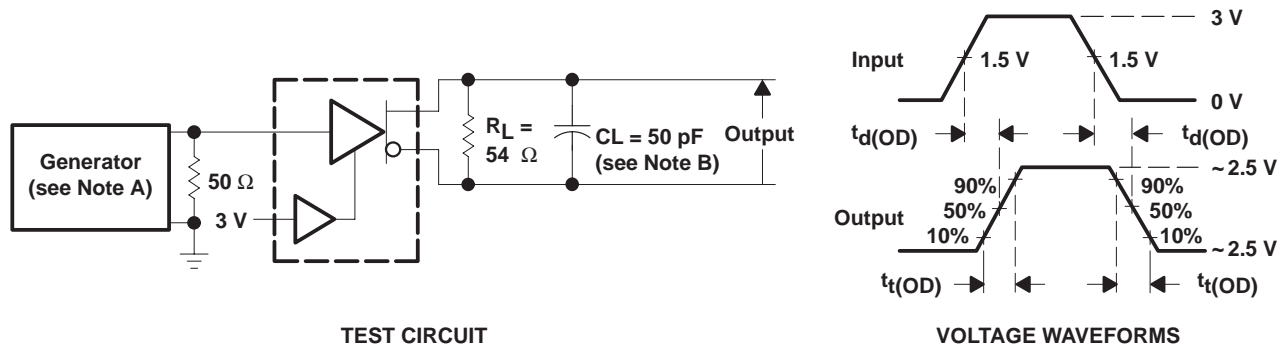
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50$ Ω.
       B. C_L includes probe and stray capacitance.

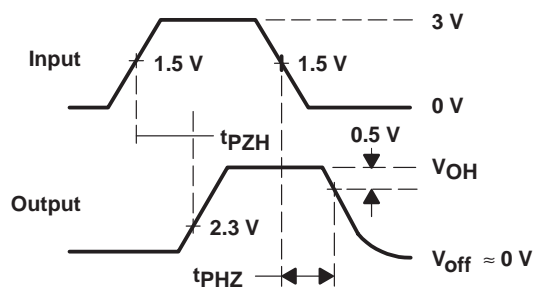**Figure 2. Differential-Output Test Circuit and Voltage Waveforms**

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PARAMETER MEASUREMENT INFORMATION

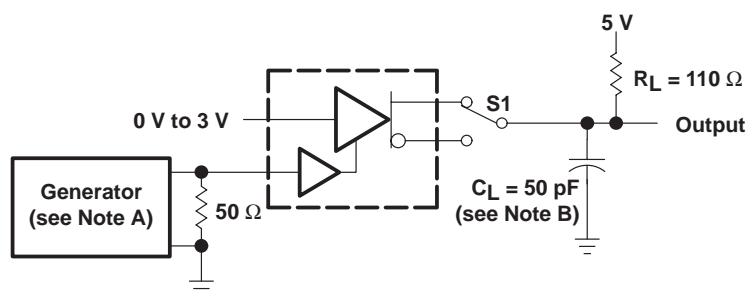**TEST CIRCUIT**   **VOLTAGE WAVEFORMS**
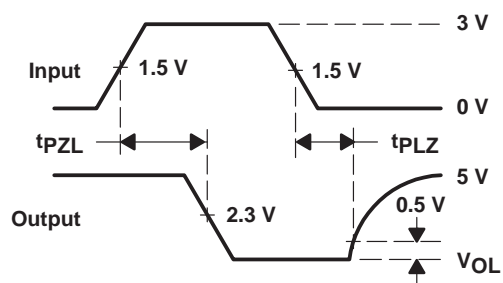
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, duty cycle = 50%, $t_r \leq$ 5 ns, $t_f \leq$ 5 ns, Z_O = 50 Ω.
   B. C_L includes probe and stray capacitance.

Figure 3. Test Circuit and Voltage Waveforms

TEST CIRCUIT   **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, duty cycle = 50%, $t_r \leq$ 5 ns, $t_f \leq$ 5 ns, Z_O = 50 Ω.
   B. C_L includes probe and stray capacitance.

Figure 4. Test Circuit and Voltage Waveforms
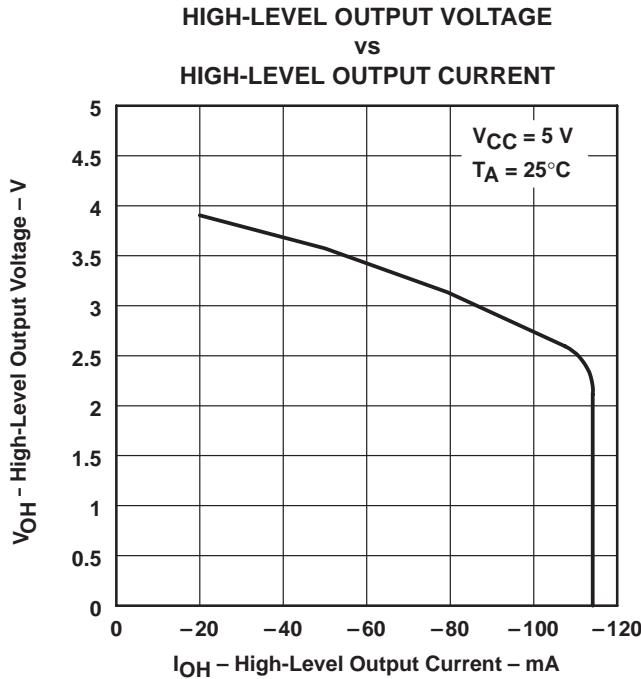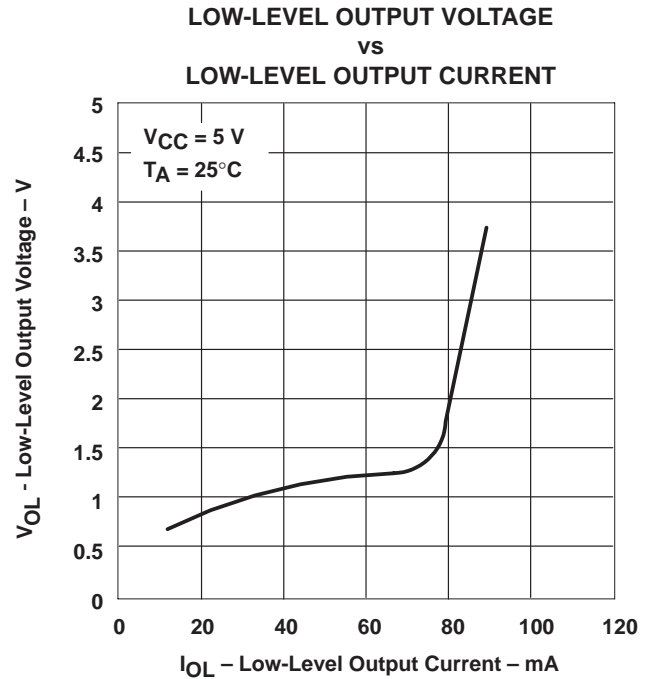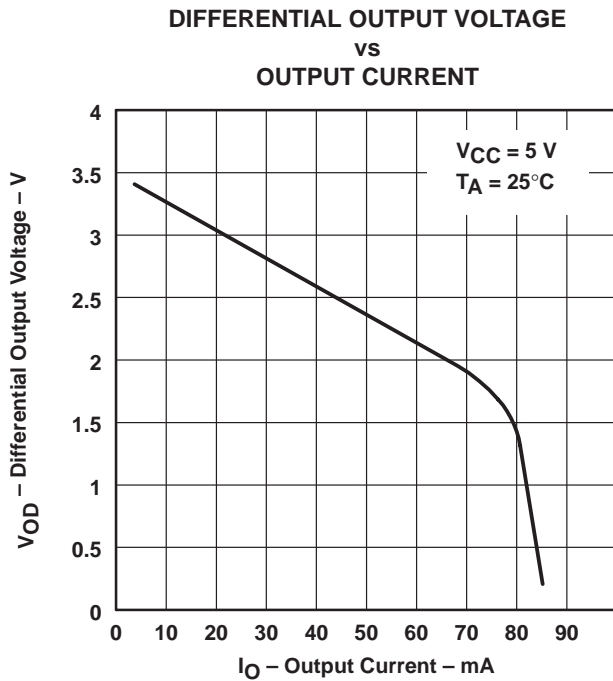
TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

V_{CC} = 5 V
T_A = 25°C

V_{OH} – High-Level Output Voltage – V

I_{OH} – High-Level Output Current – mA

Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

V_{CC} = 5 V
T_A = 25°C

V_{OL} - Low-Level Output Voltage – V

I_{OL} – Low-Level Output Current – mA

Figure 6

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

V_{CC} = 5 V
T_A = 25°C

V_{OD} – Differential Output Voltage – V

I_O – Output Current – mA

Figure 7

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

Output Disabled
T_A = 25°C

I_O – Output Current – μA

V_{CC} = 0 V

V_{CC} = 5 V

V_O – Output Voltage – V

Figure 8

TEXAS
INSTRUMENTS

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

No Load
Outputs Enabled
$T_A = 25°C$

Inputs Open

Inputs Grounded

I_{CC} – Supply Current – mA

V_{CC} – Supply Voltage – V

Figure 9

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

No Load
Input Open
Outputs Disabled
$T_A = 25°C$

I_{CC} – Supply Current – mA

V_{CC} – Supply Voltage – V

Figure 10

APPLICATION INFORMATION

1/4 SN75172

1/4 SN75173

R_T

Up to 32
RS-485 Unit Loads

1/4 SN75172

1/4 SN75173

1/4 SN75173

R_T

1/4 SN75174

1/4 SN75175

1/4 SN75174
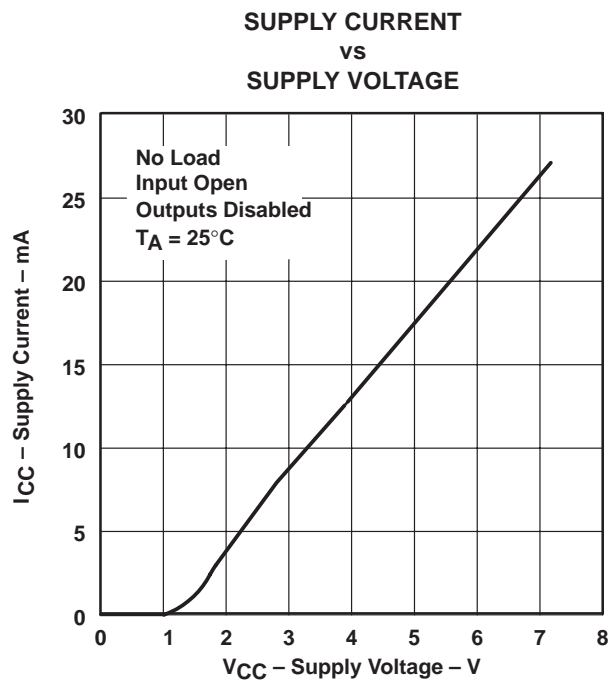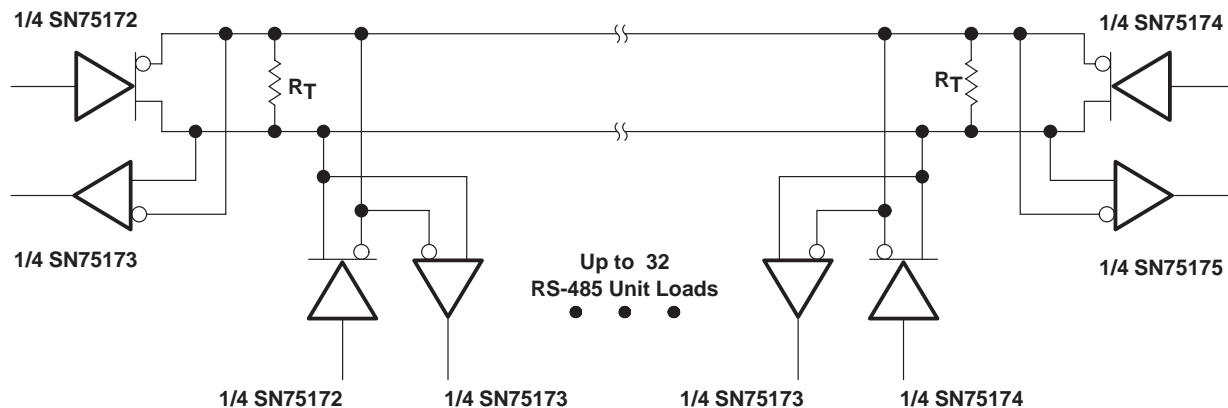
NOTE: The line length should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 11. Typical Application Circuit

![Texas Instruments logo]

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN75174DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75174DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75174DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75174J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN75174N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75174NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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	PINS **	14	16	18	20
DIM					
A		0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX		0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN		——	——	——	——
C MAX		0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN		0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\dfrac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\dfrac{0.060\ (1,52)}{0.015\ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

A

0°−15°

$\dfrac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

$\dfrac{0.014\ (0,36)}{0.008\ (0,20)}$

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
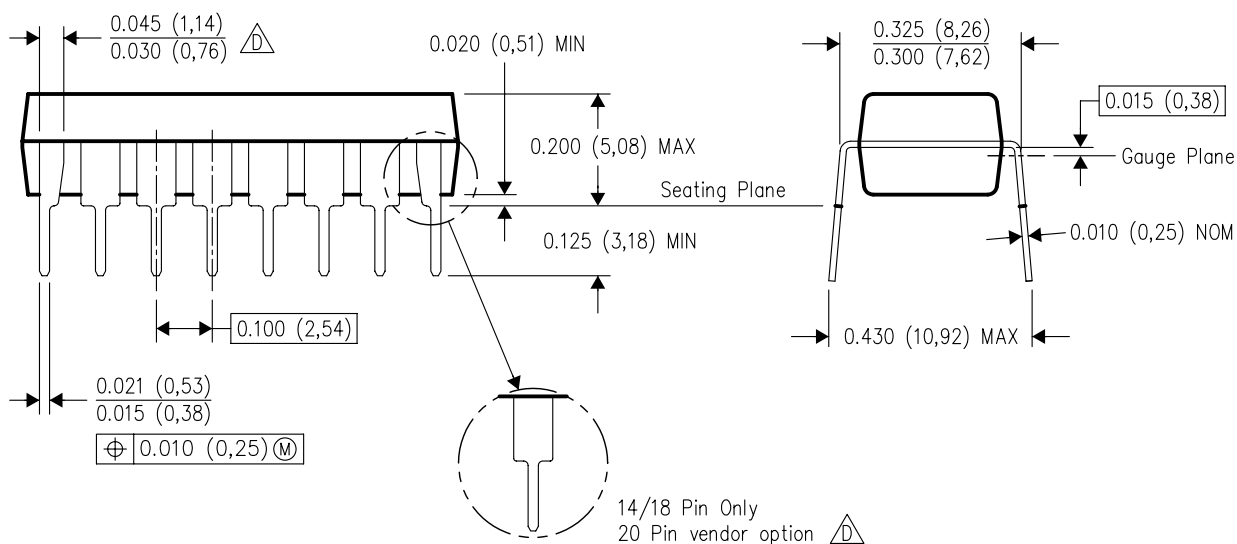   E.   Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

N (R−PDIP−T**) PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

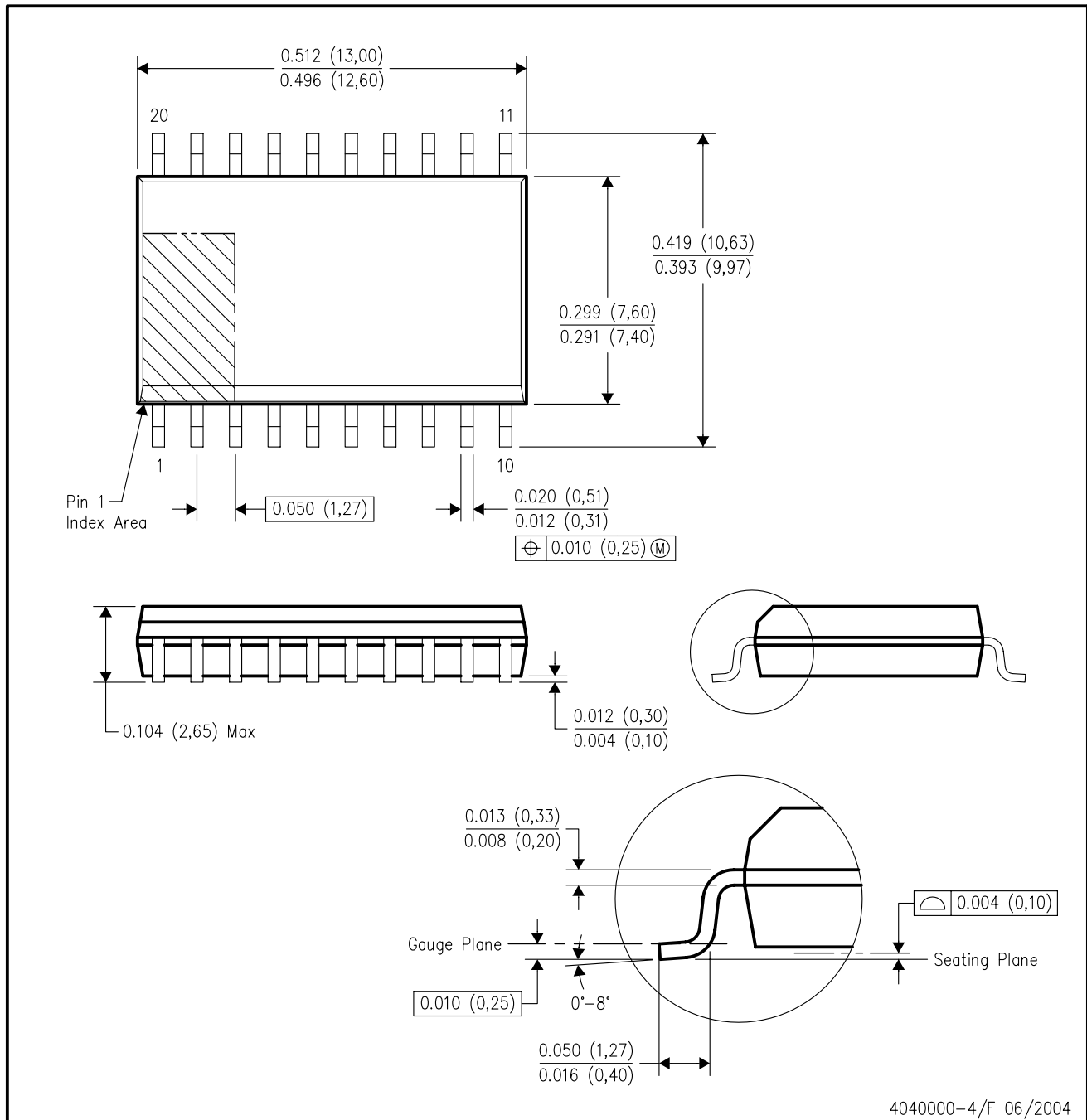| PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

Gauge Plane

0.010 (0,25)

0°−8°

⌂ 0.004 (0,10)

Seating Plane

0.050 (1,27)
0.016 (0,40)

4040000−4/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS−013 variation AC.

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