

BJT Biasing and Thermal Stabilization

Transistor Biasing

The application of DC voltage to establish fixed level of current & voltage is known as biasing.

Transistor must be properly biased in order to utilize a device as an amplifier or a digital switch. A desirable DC voltage or DC current applied to set the operating point.

Types of Biasing Circuits

A transistor is biased with the help of an external DC source. The circuit used for transistor biasing is called a biasing circuit. There are various ways to bias a transistor.

- 1) Fixed bias
- 2) Emitter feedback biasing
- 3) Collector feedback biasing
- 4) Voltage divider or self biasing

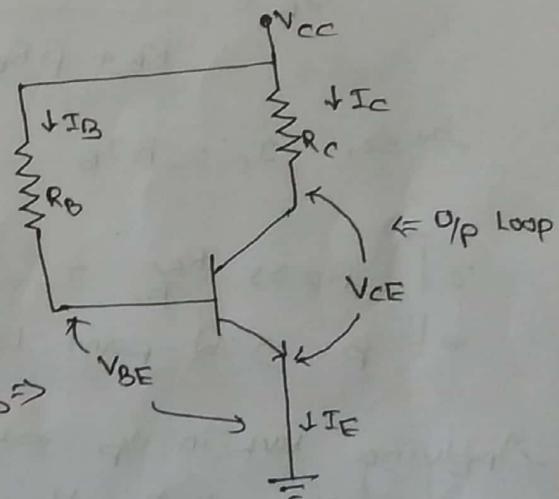
1) Fixed Biasing Circuit

The fixed bias circuit is,

Applying KVL in I/P loop,

$$V_{CC} = I_B R_B + V_{BE}$$

$$\text{or, } I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \xrightarrow{\text{I/P loop}} \quad (1)$$



If $V_{CC} \gg V_{BE}$

$$I_B \approx \frac{V_{CC}}{R_B} = \text{constant}$$

For a given Q-point I_B is constant. So it is called fixed biasing method.

$$I_C = \beta I_B = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right) \quad (2)$$

Applying KVL in O/P loop, we get

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C \quad (3)$$

Variation of β due to temp can cause I_C & V_{CE} to change. This changes Q-point of transistor. This makes fixed biasing extremely β dependent, which is highly undesirable.

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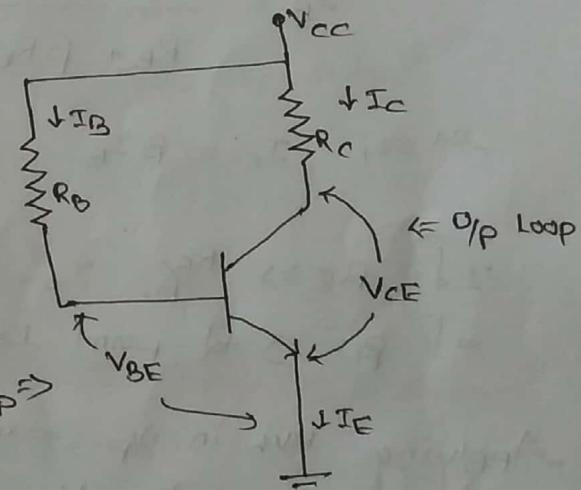
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Variation of β due to temp can cause I_C & V_{CE} to change. This changes Q-point of transistor. This makes fixed biasing extremely β dependent, which is highly undesirable.

2) Emitter Feedback Biasing

Applying KVL in I/p loop or Base ckt,

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E \quad (1)$$

$$\text{But, } I_E = I_B + I_C = I_B + \beta I_B \\ = (1 + \beta) I_B \quad (2)$$

From eqn (2)

$$V_{CC} = I_B R_B + V_{BE} + (1 + \beta) I_B R_E$$

$$\text{or, } I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_E}$$

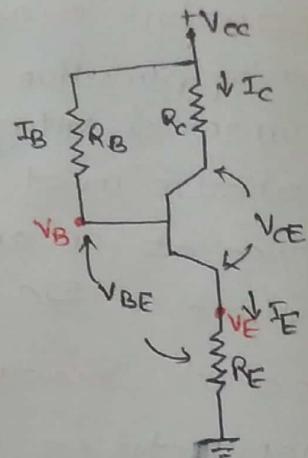


Fig: Emitter feedback bias

If $\beta \gg 1$,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_E}$$

$$\text{Also, } I_C = \beta I_B = \frac{V_{CC} - V_{BE}}{R_B / \beta + R_E}$$

If $R_E \gg R_B$, $I_C = \text{constant}$ & is independent of β . \Rightarrow Q-point is stable.

Applying KVL in O/P circuit,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\text{or, } V_{CE} = V_{CC} - I_C R_C - I_E R_E \quad (3)$$

$$\Rightarrow \text{As, } V_E = I_E R_E \approx I_C R_E \quad (\because I_C \approx I_E)$$

From eqn (3)

$$V_E = V_{CC} - I_C R_C - V_{CE}$$

$$\text{Since } V_E = I_C R_E$$

If I_C tries to increase, V_E also increases.

So that, $V_B = V_{BE} + V_E$ also increases.

$$\& I_B = \frac{V_{CC} - V_B}{R_B} \text{ decreases.}$$

which in turn decreases I_C .

Thus this negative feedback cancels any attempted change in collector current with an opposing change in base voltage.

$$\text{i.e. } I_C \uparrow \Rightarrow V_E \uparrow \Rightarrow V_B \uparrow \Rightarrow I_B \downarrow \Rightarrow I_C \downarrow$$

3) Collector Feedback Biasing

Applying KVL at i/p loop (or base circuit)

$$V_{CC} = I_C R_C + I_B R_B + V_{BE} \quad \text{--- (1)}$$

$$\text{or, } V_{CC} = I_C R_C + \frac{I_C}{B} R_B + V_{BE} \quad (\because I_C = B I_B)$$

$$\text{or, } I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{B}} \quad \text{--- (2)}$$

If $R_C \gg \frac{R_B}{B}$,

$$I_C = \frac{V_{CC} - V_{BE}}{R_C}$$

If I_C tries to increase,

$$V_C = V_{CC} - I_C R_C \text{ decreases}$$

$$I_B = \frac{V_C - V_{BE}}{R_B} \text{ also decreases}$$

which will then reduce I_C . (\uparrow As $I_C = B I_B$)

Applying KVL at o/p loop,

$$V_{CC} = I_C R_C + V_{CE}$$

$$\text{or, } V_{CE} = V_{CC} - I_C R_C \quad \text{--- (3)}$$

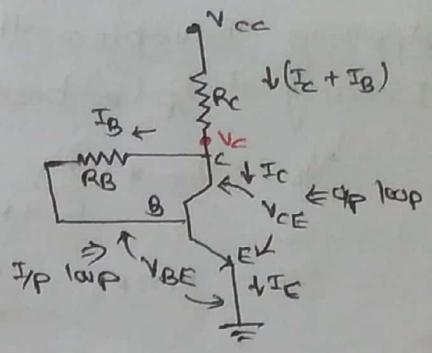


Fig: Collector feedback Bias

$$\textcircled{1} \quad V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE}$$

As $I_C = B I_B$ or,
 $I_B \ll I_C$, so
 $V_{CC} = I_C R_C + I_B R_B + V_{BE}$

4) Voltage divider Biasing / Self Biasing / Universal Biasing β-independent Biasing

The voltage-divider circuit is also called β-independent biasing method.

This one is most stable biasing method among the circuits discussed.

Previously for various temp condition & β value of transistor.

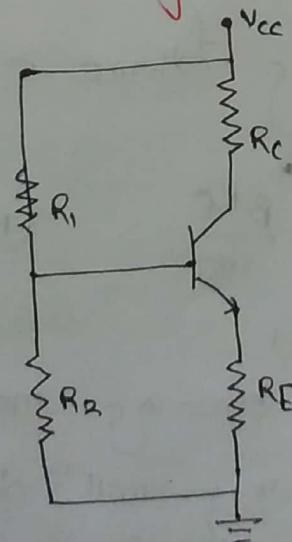


Fig: Voltage divider Biasing

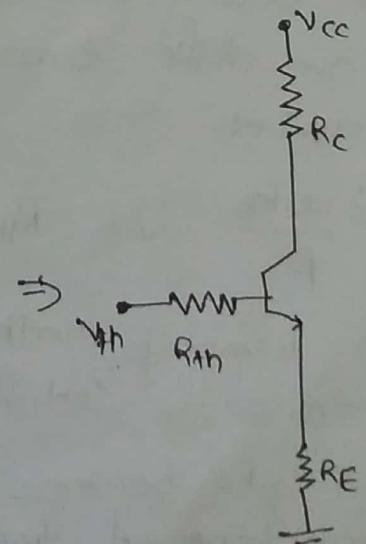


Fig: Thevenins equivalent circuit

Applying Thevenin's theorem to analyze this circuit.

Looking at i_p (or base) terminal,

$$V_{Th} = V_{CC} * \frac{R_2}{R_1 + R_2}$$

$$R_{Th} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Applying KVL through Base-Emitter loop,

$$V_{Th} = I_B \cdot R_{Th} + V_{BE} + I_E R_E$$

$$\text{on } V_{Th} - V_{BE} = \frac{I_C}{\beta} R_{Th} + I_C R_E$$

or, $\frac{V_{Th} - V_{BE}}{R_{Th}/\beta + R_E} = I_C$

$$\therefore I_C = \frac{V_{Th} - V_{BE}}{R_{Th}/\beta + R_E}$$

This con. shows that collector current is almost independent of β , when $R_E \gg R_{Th}$

The voltage divider biasing method can be described in two ways:

- i) Stiff biasing method
- ii) Firm biasing method.

Stiff Biasing method.

To achieve stiff biasing following condition must be occupied.

$$R_E \geq 100 R_{Th} \quad \text{i.e. } R_{Th} \leq \frac{\beta R_E}{100} \quad (R_{Th} \leq 0.01 \beta R_E)$$

Firm Biasing method

Sometimes in stiff biasing method, the value of R_1 & R_2 becomes very small due to which I/P impedance of transistor is very small and may create problems.

In this case firm biasing is used to achieve this.

$$\frac{V_{Th}}{R_E} \leq RE \quad , \quad R_{Th} = 0.1 BRE$$

When $V_{Th} \gg V_{BE}$, $V_{Th} - V_{BE}$ becomes almost constant.

For this achievement, following guidelines are used.

Guideline No.1

\Rightarrow popular for low voltage power supply. ($V_{CC} < 10V$)

$$\Rightarrow \text{choose, } V_{Th} = \frac{V_{CC}}{R_C} \quad \& \quad V_{RC} = \frac{V_{CC}}{3}$$

which will then lead to,

$$R_1 = 2R_2 \quad \& \quad R_{Th} = \frac{2}{3} R_2$$

$$V_{Th} = V_{CC} + \frac{R_2}{R_1 R_2} = \frac{1}{3} V_{CC} \quad , \quad R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{2 R_2 \times \frac{2}{3} R_2}{2 R_2 + R_2} = \frac{2 R_2 \times \frac{2}{3} R_2}{3 R_2} = \frac{4}{3} R_2$$

$$3R_2 = R_1 + R_2$$

$$\Rightarrow R_1 = 2R_2$$

[$I_1 = \alpha IB$ (selection of R_1 & R_2)]

Now, Biasing becomes,

$$R_{Th} = 0.1 B RE = \frac{2}{3} R_2 \text{ for firm biasing}$$

$$R_{Th} = 0.01 BRE = \frac{2}{3} R_2 \text{ for stiff biasing.}$$

Guideline No.2

\Rightarrow popular for high power supply. ($V_{CC} > 10V$)

$$V_E = I_E R_E \approx 0.1 V_{CC}$$

$$V_{CE} = 0.5 V_{CC}$$

$$(V_{RC}) = V_{RC} = I_C R_C = 0.1 V_{CC}$$

$$R_{Th} = R_2$$

Because V_E is much smaller compared to V_{CC} , V_{Th} is also much smaller than V_{CC} & leads to $R_{Th} = R_2$ & biasing becomes

$$R_{Th} = 0.1 BRE \approx R_2 \text{ for Firm biasing}$$

$$R_{Th} = 0.01 BRE \approx R_2 \text{ for Stiff biasing.}$$

Design a CE self-bias circuit for $I_C = 2\text{mA}$.
Assume $V_{CC} = 20\text{V}$ & $\beta = 100$.

Soln: The CE self-bias circuit is,

(i) Let $V_{RE} = 10\text{V}$ of V_{CC}

i.e. $I_E R_E = 10\text{V}$ of $20\text{V} = 2\text{V}$

$$\Rightarrow R_E = \frac{2}{I_E} = \frac{2}{I_C} \quad (\because I_E \approx I_C)$$

$$\therefore R_E = \frac{2}{2 \times 10^{-3}} = 1\text{k}\Omega$$

(ii) $V_E = 50\%$ of V_{CC}

i.e. $V_{CE} = 50\%$ of 20V

= 10V , to locate Q-point at the center of DC load line.

(iii) Applying KVL in O/P loop,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\text{or, } 20 - 10 - 2 = I_C R_C$$

$$\Rightarrow R_C = \frac{8}{2 \times 10^{-3}} = 4\text{k}\Omega$$

(iv) Also, $V_B = V_{CC} - I_1 R_1$,

where, $I_1 = 10 I_B = 10 \times \frac{I_C}{\beta} = 10 \times \frac{2 \times 10^{-3}}{100} = 2 \times 10^{-4}$
 $= 200 \times 10^{-6} = 200\mu\text{A}$

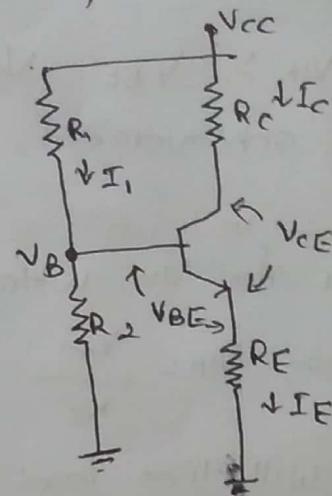
$$\therefore V_B = 20 - 200 \times 10^{-6} \times R_1$$

$$\text{But } V_B = V_{BE} + I_E R_E = 0.7 + 2 \times 10^{-4} = 2.7\text{V}$$

$$\text{So, } 2.7 = 20 - 200 \times 10^{-6} \times R_1$$

$$\Rightarrow R_1 = \frac{20 - 2.7}{200 \times 10^{-6}} = 86.5\text{k}\Omega$$

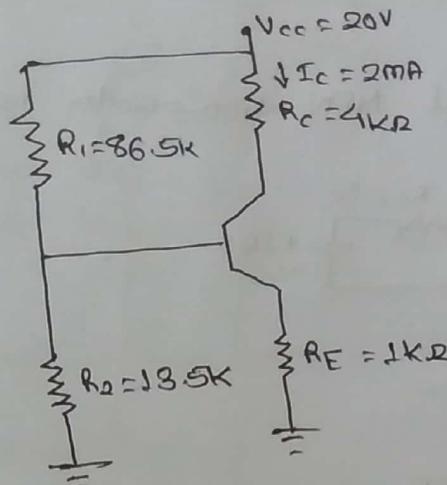
v) $V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}$ or, $2.7 = \frac{20 R_2}{R_1 + R_2} = \frac{20 R_2}{86.5 + R_2}$



$$\text{or}, 233.25 + 2.7 R_2 = 20 R_2$$

$$\Rightarrow R_2 = 18.5 \text{ k}\Omega$$

Now, the CE self-bias circuit is,



Find the Q-point / bias point of a ^{Germanium} transistor given.

Assume $B = 99$.

Soln: Applying KVL in I/P loop,

$$V_{cc} = I_B R_B + V_{BE} + I_E R_E$$

$$\text{or}, 16 = I_B R_B + V_{BE} + (B+1) I_B R_E$$

$$\text{or}, 16 = I_B [R_B + (B+1) R_E] + V_{BE}$$

$$\Rightarrow I_B = \frac{16 - 0.3}{(120 + 100 \times 1) \times 10^3} = 7.136 \times 10^{-6}$$

$$\therefore I_B = 7.136 \mu\text{A}$$

$$\text{Also, } I_E = (B+1) I_B = 100 \times 7.136 \mu\text{A} = 7.136 \text{ mA}$$

Again, applying KVL in O/P loop,

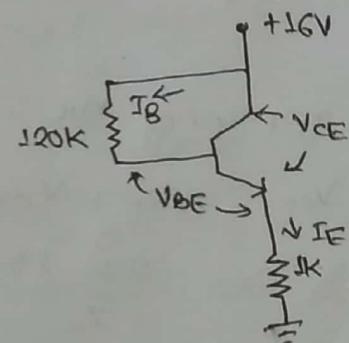
$$V_{cc} = V_{CE} + I_E R_E$$

$$\Rightarrow V_{CE} = V_{cc} - I_E R_E = 16 - 7.136 \times 10^{-3} \times 1 \times 10^3$$

$$= 8.86 \text{ V}$$

Thus, Q-point or bias point is,

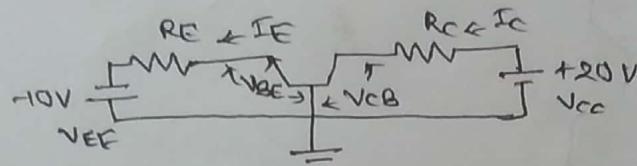
$$I_{EQ} = 7.136 \text{ mA} \quad \& \quad V_{CEQ} = 8.86 \text{ V}$$



A common base ckt is to be designed for an NPN transistor to be used in a system having DC power supplies of +20V & 10V. The bias point is to be $I_E = 1.5\text{mA}$ & $V_{CB} = 10\text{V}$.

Soln:

The CB configuration of NPN transistor is,



Applying KVL in I/P loop,

$$V_{EE} = I_E R_E + V_{BE}$$

$$\Rightarrow R_E = \frac{10 - 0.7}{1.5 \times 10^{-3}} = 6.2 \text{ k}\Omega$$

Again, applying KVL in I/P loop,

$$V_{CC} = I_C R_C + V_{CB}$$

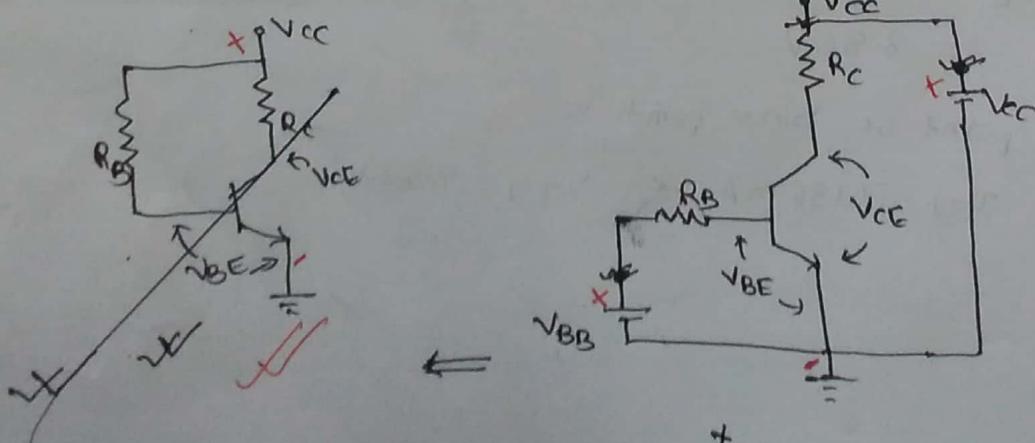
$$\Rightarrow R_C = \frac{20 - 10}{I_C} = \frac{10}{1.5 \times 10^{-3}} = 6.67 \text{ k}\Omega$$

An NPN Si transistor having a nominal B of 100 is to be used in a CE configuration with $V_{CC} = 12\text{V}$. The bias point or operating point (Q-point) is to be $I_C = 2\text{mA}$ & $V_{CE} = 6\text{V}$.
i) Design the circuit.

ii) Find the range of possible base values if B of the transistor can change to any value between 50 & 150.

Soln:

The NPN CE configuration transistor is,



Applying KVL in IP loop,

$$V_{BB} = I_B R_B + V_{BE}$$

$$\Rightarrow R_B = \frac{V_{BB} - V_{BE}}{I_B} = \frac{V_{BB} - V_{BE}}{I_c/B} = \frac{12 - 0.7}{\frac{2 \times 10^{-3}}{100}} = \frac{11.3 \times 100}{2 \times 10^{-3}} = 565 \text{ k}\Omega$$

Applying KVL in O/P loop,

$$V_{CC} = I_C R_C + V_{CE}$$

$$\Rightarrow R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{12 - 6}{2 \text{ mA}} = 3 \text{ k}\Omega$$

Now, if B changes from 50 to 150,

$$\text{Then, } I_{C\min} = \beta_{min} I_B$$

$$\text{Where, } I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{560 \text{ k}\Omega} = 20.18 \mu\text{A}$$

(Here, as the standard value of R_B closest to the calculated value of 565k is 560k).

And,

$$I_{C\max} = \beta_{max} I_B = 50 \times 20.18 \mu\text{A} = 1.01 \text{ mA}$$

$$I_{C\max} = \beta_{max} I_B = 150 \times 20.18 \times 10^{-6} = 3.03 \text{ mA}$$

$$\text{Now, } V_{CE\min} = V_{CC} - I_{C\max} R_C = 12 - 3.03 \times 10^3 \times 3 \times 10^3 \\ = 2.92 \text{ V}$$

Similarly,

$$V_{CE\max} = V_{CC} - I_{C\min} R_C = 12 - 1.01 \times 10^3 \times 3 \times 10^3 \\ = 8.97 \text{ V}$$

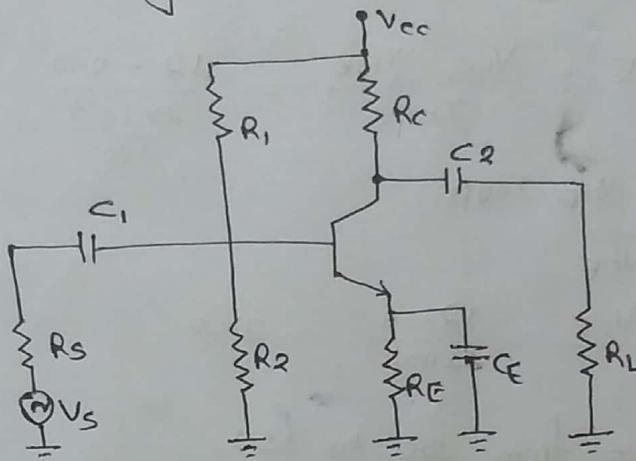
i.e. there is a large variation of V_{CE} from 2.92V to 8.97V, which is not tolerable.

Load Line Circuit

Consider O/P characteristic curve of a common emitter amplifier circuit which indicates the relationship between V_{CE} & I_C . The relationship is linear so that it can be represented by a straight line on the O/P characteristic & this straight line is called Load line. The point lying on the load lines give the possible values of V_{CE} & I_C in O/P ckt. There are 2 types of load lines: DC & AC load line.

DC Load Line, AC Load Line & Q-point

Consider a voltage-divider bias circuit as:



DC Load Line \Rightarrow Fig: Voltage divider bias circuit

For DC equivalent circuit, all capacitors are opened since $X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi \times 0 \times C} = \infty$, & all the ac voltage sources are grounded. Then its DC equivalent circuit & thevenins equivalent circuits are,

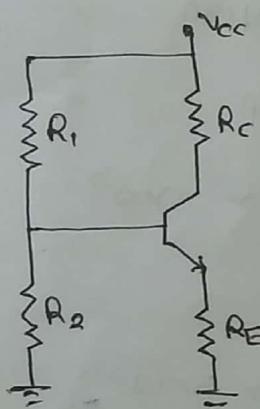


Fig: DC equivalent circuit

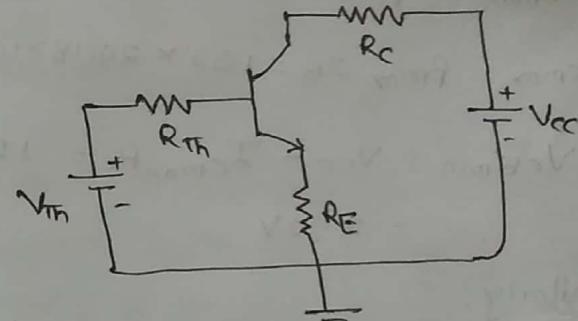
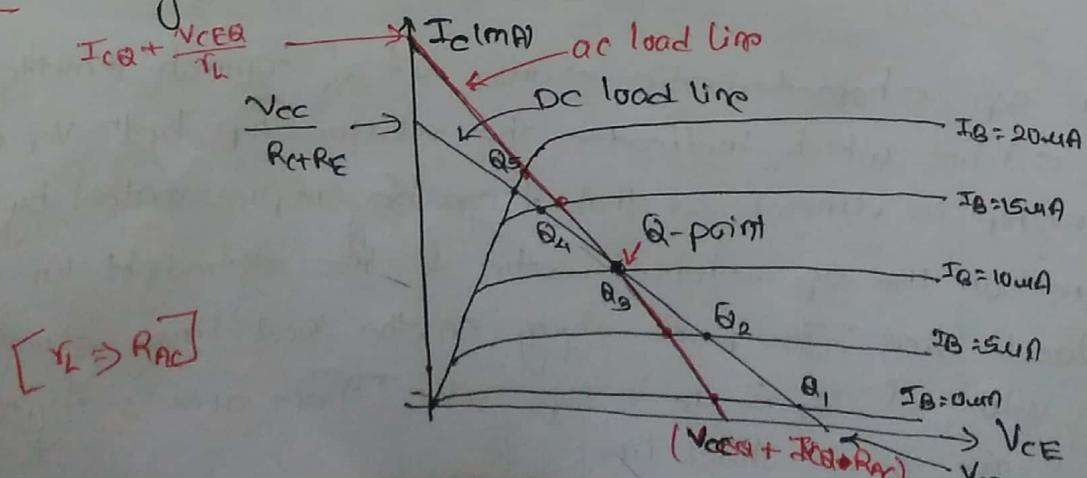


Fig: Thevenin's equivalent ckt

\Rightarrow

DC load line is the line on the O/P characteristics of the transistor circuit which gives the value of I_C & V_{CE} corresponding to zero ac signal or DC conditions.



$$\text{Here, } V_{CC} = I_C (R_{CE} + R_E) + V_{CE} \quad (\because I_C \approx I_E)$$

$$\text{For } V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_{CE} + R_E} \quad \text{--- (i)}$$

$$\text{For } I_C = 0, \quad V_{CE} = V_{CC} \quad \text{--- (ii)}$$

$$\text{Here, } V_{TH} = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

$$\text{and } V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

$$V_{TH} = V_{BE} + R_{TH} I_B + (\beta + 1) I_B R_E$$

$$\Rightarrow I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E}$$

Now, the op characteristics curves of CE transistor configuration is as shown above.

In a figure, two points $(V_{CC}, 0)$ & $(0, \frac{V_{CC}}{R_{CE} + R_E})$ are joined & that straight line is called DC load line.

Let $I_B = 10mA$. Then this DC load line cuts $I_B = 10mA$ line at a point, which is called operating point or Q-point.

The corresponding current & voltage at Q-point are I_{CQ} & V_{CEQ} respectively.

3 cases: case I: I_B increased, Q shift towards upper left.

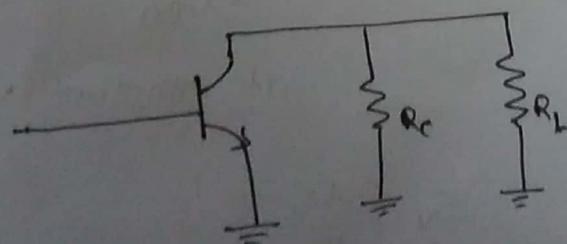
case II: R_E increased, Q shift more towards left

case III: V_{CC} increased, Q shift right.

AC Load Line

This is line on op characteristics of transistor circuit which gives the values I_C & V_{CE} when signal applied is considering.

AC equivalent circuit is,



The AC load line passes through the Q-point & its slope is $-\frac{1}{r_L}$, where $r_L = R_C // R_L$. The eqn of ac load line is,

$$I_C - I_{CQ} = -\frac{1}{r_L} (V_{CE} - V_{CEQ})$$

The points for ac load lines are,

	I_C	V_{CE}
i)	0	$V_{CEQ} + I_{CQ} \cdot r_L$
ii)	$I_{CQ} + \frac{V_{CEQ}}{r_L}$	0

Transistor Stability

The collector current I_C of a transistor varies with

i) temp of operation of transistor

ii) physical parameter like V_{BE} & β of the transistor.

The process of making I_C independent of temperature & physical parameter variation is called transistor stabilization.

If the transistor is not stabilized it may be destroyed due to thermal runaway. So, we must stabilize a transistor.

To stabilize a transistor we have to use various transistor biasing methods.

The effectiveness of transistor biasing method to stabilize a transistor is measured by the stability factor (S).

Stability Factor

It is defined as the rate of change in collector current I_C with respect to the change in collector base leakage current, I_{CBO} .

$$\text{i.e., Stability factor, } S = \frac{dI_C}{dI_{CBO}} \quad (1)$$

at constant V_{BE} & β .

My,

$$S = \frac{dI_C}{dB} \quad \left| \begin{array}{l} I_{CBO} = \text{const} \\ V_{BE} = \text{const} \end{array} \right.$$

$$S_V = \frac{dI_C}{dV_{BE}} \quad \left| \begin{array}{l} V_{CBO} = \text{const} \\ \beta = \text{const} \end{array} \right.$$

The relationship b/w I_c & I_{cBO} is given by the eqn,

$$I_c = \beta I_B + (\beta+1) I_{cBO}$$

On differentiating w.r.t I_c

$$\frac{dI}{dI_c} = \beta \frac{dI_B}{dI_c} + (\beta+1) \frac{dI_{cBO}}{dI_c}$$

$$\text{or, } \frac{1}{\beta+1} - \beta \frac{dI_B}{dI_c} = (\beta+1) \frac{dI_{cBO}}{dI_c} = \beta+1 * \frac{1}{S}$$

$$\text{or, } S = \frac{\beta+1}{1 - \beta \frac{dI_B}{dI_c}} \quad \text{--- (2)}$$

Also, $I_c = \beta I_B + (\beta+1) I_{cBO}$

i.e. Lesser the change in I_{cBO} \Rightarrow more will be stable
Higher " " " " " \Rightarrow Less " " "

Thermal Instability & Thermal Runaway

We know that, $I_c = \beta I_B + (\beta+1) I_{cBO}$

As temp $\uparrow \Rightarrow I_{cBO} \uparrow \Rightarrow I_c \uparrow$

Also, as $I_c \uparrow \Rightarrow$ junction temp $\uparrow \Rightarrow I_{cBO} \uparrow \uparrow$ (more).

This process goes on in a cumulative way. As a result large collector current flows. This process is called thermal instability & thermal runaway.

Thermal runaway can be avoided by a suitable design.

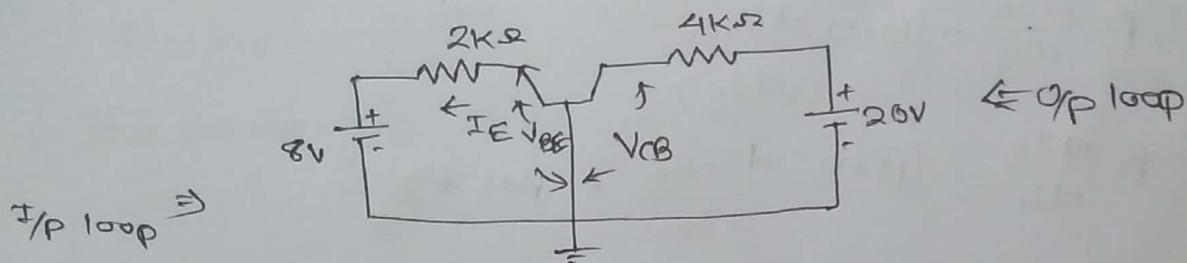
To avoid thermal runaway, following condition must be satisfied.

$$\text{i.e. } \frac{dP_c}{dT_j} < \frac{dP_D}{dT_j}$$

where P_c is the heat generated at collector junction

& P_D is maximum heat generated.

Find I_E , I_B , I_C & V_{CE} for the given CB transistor amplifier. Also draw a DC load line & locate the Q-point. Given $\alpha = 0.9$.



Soln: Applying KVL on I/P loop,

$$8 = 2I_E + V_{BE}$$

$$\Rightarrow I_E = \frac{8 - V_{BE}}{2 \times 10^3} = \frac{8 - 0.7}{2 \times 10^3} = 3.65 \text{ mA}$$

As we know,

$$I_C = \alpha I_E + I_{CBO}$$

$$\therefore I_C = \alpha I_E = 0.9 \times 3.65 = 3.28 \text{ mA}$$

Also,

$$I_E = I_B + I_C$$

$$\therefore I_B = I_E - I_C = 3.65 - 3.28 = 0.365 \text{ mA}$$

Applying KVL on O/P loop

$$V_{CC} = I_C R_C + V_{CB}$$

$$\text{or, } V_{CB} = V_{CC} - I_C R_C = 20 - 3.28 \text{ mA} * 4 \text{ k}\Omega = 6.86 \text{ V}$$

And,

$$V_{CE} = V_{CB} + V_{BE} = 6.86 + 0.7 = 6.93 \text{ V}$$

The O/P characteristics of CB configuration is shown in figure,

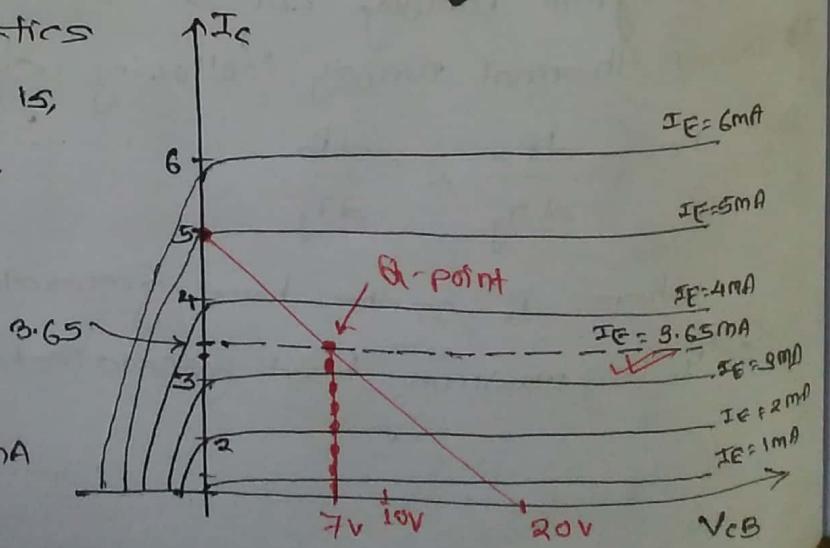
We know,

$$V_{CC} = I_C R_C + V_{CB}$$

$$\text{when } I_C = 0, V_{CB} = 20 \text{ V}$$

$$\text{when } V_{CB} = 0 \text{ V},$$

$$I_C = \frac{V_{CC}}{R_C} = \frac{20}{4} = 5 \text{ mA}$$



Now, let's draw a straight line joining two points (20,0) & (0,5mA). This st. line is the DC load line.

This DC load line intersects the $I_E = 3.65mA$ line at point Q which is called its operating point or Q-point or quiescent point.

From graph, at Q-point,

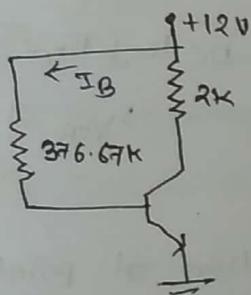
$$I_{CQ} = 3.65mA$$

$\& V_{CEQ} \approx 7V$.

The silicon transistor in CE configuration is as shown.

i) Determine I_B , I_C , I_E , V_{CE} & Q-point.

ii) Determine Q-point graphically.



iii) Repeat (ii) if R_B changes to 161.43kΩ.

SOLN:

j) Applying KVL in I/P loop,

$$V_{CC} = I_B R_B + V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{376.67} = 30mA$$

Also, we know that

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

$$= \beta I_B$$

$$= 100 \times 30mA$$

$$= 9mA$$

(As I_{CBO} is very small, so neglected)

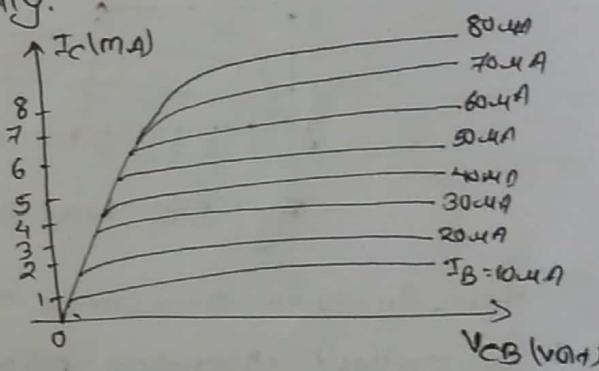
Applying KVL in O/P loop,

$$V_{CC} = I_C R_C + V_{CE}$$

$$\Rightarrow V_{CE} = 12 - 3mA \times 2k\Omega = 6V$$

Thus, Q-point is, $V_{CEQ} = 6V$ & $I_{CQ} = 3mA$.

Since V_{CE} is +ve & $V_{CE} > 1V$, transistor operates in active region.



∴ As we have,

$$V_{CE} = I_C R_C + V_{CE}$$

When $V_{CE} = 0V$,

$$I_C = \frac{V_{CC}}{R_C} = \frac{12}{2 \times 10^3} = 6mA$$

When $I_C = 0mA$,

$$V_{CE} = V_{CC} = 12V$$

Now, plot two points, $(12, 0)$ & $(0, 6)$ in given up characteristic curve as shown below.

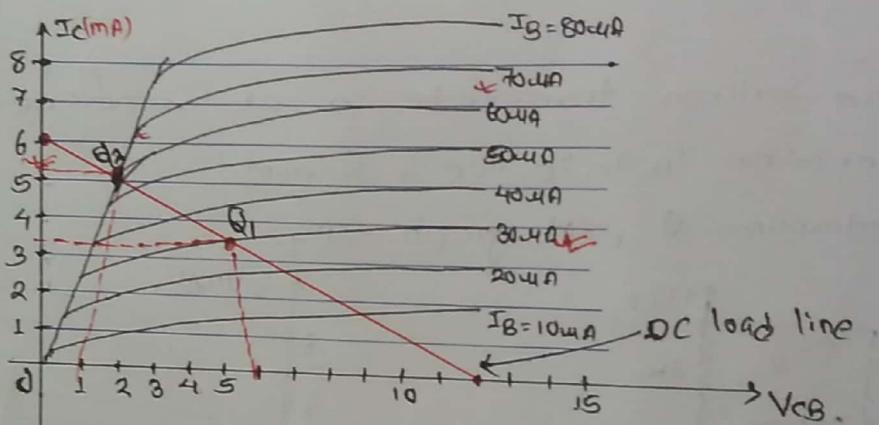


Fig: DC load line & Q-point

Here, $I_B = 30mA$ intersects the DC load line at point Q_1 , which is called operating point / Q-point or quiescent point.

From graph, $I_{CQ} = 3.2mA$

& $V_{CEQ} \approx 6V$, which are close to calculated value.

Now for $R_B = 161.43k\Omega$

$$I_B = \frac{12 - 0.7}{161.43 \times 10^3} = 70mA$$

$$\text{Also, } I_C = \beta I_B = 100 \times 70 \times 10^{-3} = 7 \times 10^{-2} = 7mA$$

$$V_{CE} = V_{CC} - I_C R_C = 12 - 7 \times 2 = -2V$$

$$\therefore V_{CB} = V_{CE} - V_{BE} = -2 - 0.7 = -2.7V$$

Since V_{CB} is -ve, the CB junction is also forward biased (NPN). i.e. both EB & CB junction are forward-biased, so that transistor is in the saturation region. Then Q-point is shifted from Q_1 to Q_2 , which is in saturation region.

$I_C = \beta I_B$ is valid only when the transistor operates in a active region.

Thus, for a transistor is in saturation region, I_B & I_C can be obtained as,

$$V_{CC} = I_{Bsat} R_B + V_{BEsat}$$

$$\Rightarrow I_{Bsat} = \frac{12 - 0.8}{161.43k} \approx 70mA$$

$$\& I_{Csat} = \frac{V_{CC} - V_{CEsat}}{R_C} = \frac{12 - 0.2}{2k} = 5.9mA$$

Calculate I_B , I_C , V_{CE} & stability factor for collector-to-base bias (collector-feedback bias) circuit given below.

Soln:

Applying KVL in I/P loop,

$$V_{CC} = I_B R_E + I_B R_B + V_{BE}$$

$$= I_B (R_E + R_B) + I_C R_C + V_{BE}$$

$$\text{or, } V_{CC} = I_B (100 + 2) + \beta I_B \times 2 + 0.7$$

$$\text{or, } 20 - 0.7 = 102 I_B + 200 I_B = 302 I_B$$

$$\Rightarrow I_B = \frac{19.3V}{302k\Omega} = \frac{19.3}{302 \times 10^3} = 63.90mA$$

$$\text{And, } I_C = \beta I_B = 6.39mA \quad (\because I_{CBO} = 0A)$$

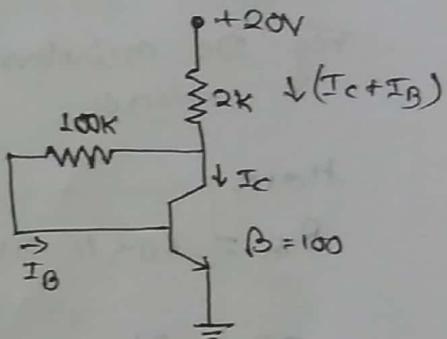
$$I_E = I_B + I_C = 6.39mA + 63.90mA \\ = 6.45mA$$

Again, applying KVL in O/P loop

$$V_{CE} = (I_B + I_C) R_C + V_{CE}$$

$$\text{or, } V_{CE} = 20 - 6.45mA \times 2k$$

$$\therefore V_{CE} = 7.1V$$



Find I_B , I_C , V_{CE} & s for the voltage divider circuit given in figure.

SOLN: The DC equivalent and Thevenin's equivalent circuit of the given circuit is

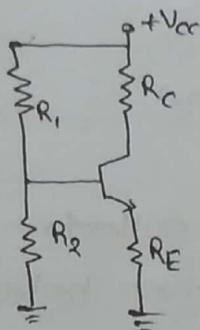


Fig: DC equivalent circuit

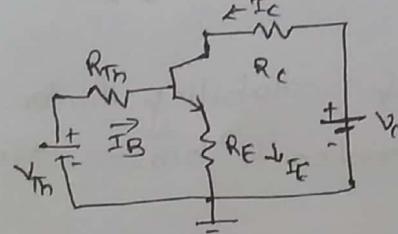


Fig: Thevenin's equivalent circuit.

Here,

$$R_{TH} = 60K \parallel 15K = \frac{60 \times 15}{60+15} = 12K\Omega$$

$$\text{and } V_{TH} = \frac{15}{15+60} \times 20 \approx 4V$$

Applying KVL in I/P loop, (Thevenin's equivalent circuit)

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E = I_B R_{TH} + V_{BE} + (B+1) I_B R_E$$

$$\Rightarrow I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + R_E(B+1)} = \frac{4 - 0.7}{12 + (100+1) \times 2} = \frac{3.3V}{214 \Omega} = 15.42 \mu A$$

Also, we know that

$$I_C = B I_B + (B+1) I_{CBO}$$

$$= 100 \times 15.42 \times 10^{-6} + 101 \times 100 \times 10^{-9}$$

$$\Rightarrow I_C = 1.55mA \quad (1.542mA)$$

$$\text{Also, } I_E = I_C + I_B = 1.55mA \quad (1.542mA)$$

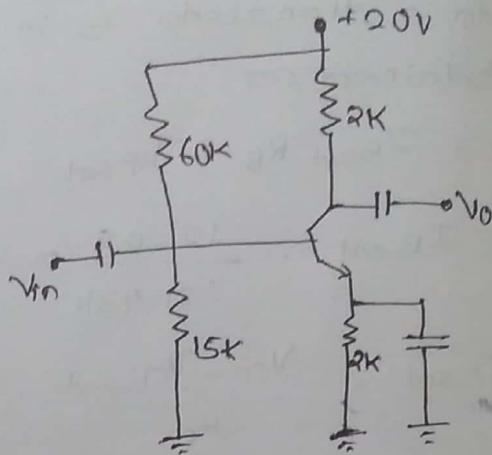
$(I_{CBO} = 10 \text{ or } 100 nA)$
 I_{CBO} is very small
 so can be neglected

Applying KVL at O/P loop,

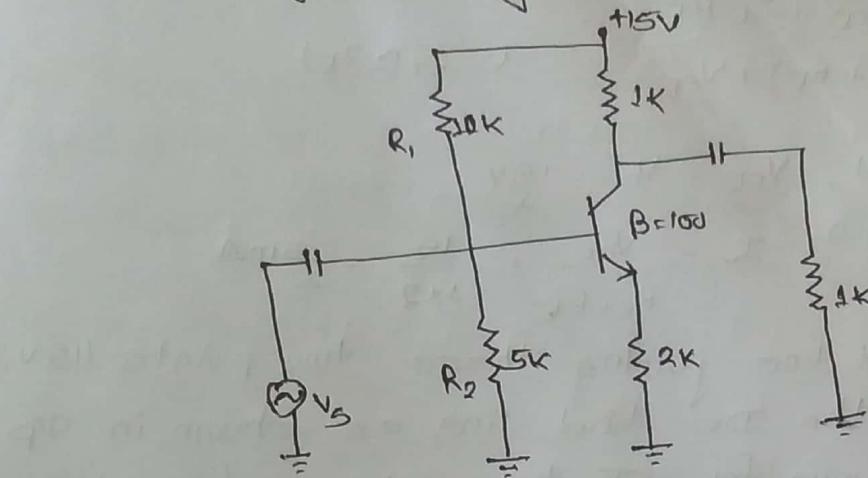
$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C - I_E R_E = 15 - 1.55 \times 2 - 1.56 \times 2 \\ = 8.76V$$

Thus, transistor operates in the active region.



Draw the dc load line & the Q-point for the given voltage divider bias circuit.



Solution:

DC Load Line:

The DC equivalent circuit & its Thvenins equivalent circuit is,

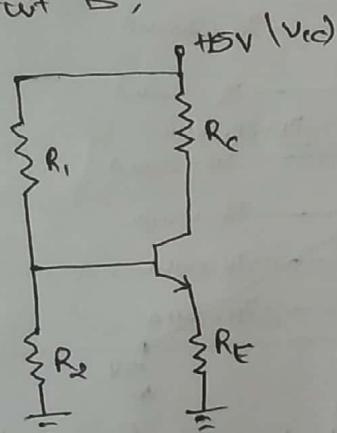


Fig: DC equivalent ckt

$$\text{Here, } R_{TH} = R_1 // R_2 = \frac{10 \times 5}{10+5} = 3.33 \text{ k}\Omega$$

$$\& V_{TH} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{5}{5+10} \times 15 = 5V$$

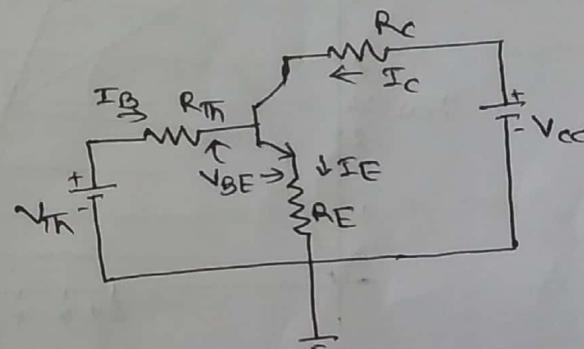


Fig: Thvenins equivalent ckt

Applying KVL in IP loop on Thvenins equivalent ckt,

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

$$\text{or, } V_{TH} = I_B R_{TH} + V_{BE} + (B+1) I_B R_E$$

$$\Rightarrow I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (B+1) R_E} = \frac{5 - 0.7}{[3.33 + (100+1) \times 2] \times 10^3}$$

$$= 20.94 \times 10^{-6}$$

$$\text{or, } I_B = 20.94 \mu A$$

Again applying KVL in OP loop,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\text{or, } V_{CC} = I_C (R_C + R_E) + V_{CE}$$

($\because I_C \approx I_E$)

When $I_C = 0$, $V_{CE} = V_{CC} = 15V$

$$\text{when } V_{CE} = 0, I_C = \frac{V_{CC}}{R_C + R_E} = \frac{15}{1+2} = 5\text{mA}$$

Now, the straight line joining these two points (15V, 0) & (0, 5mA) is the DC load line, as shown in OP characteristic curve for CE transistor configuration.

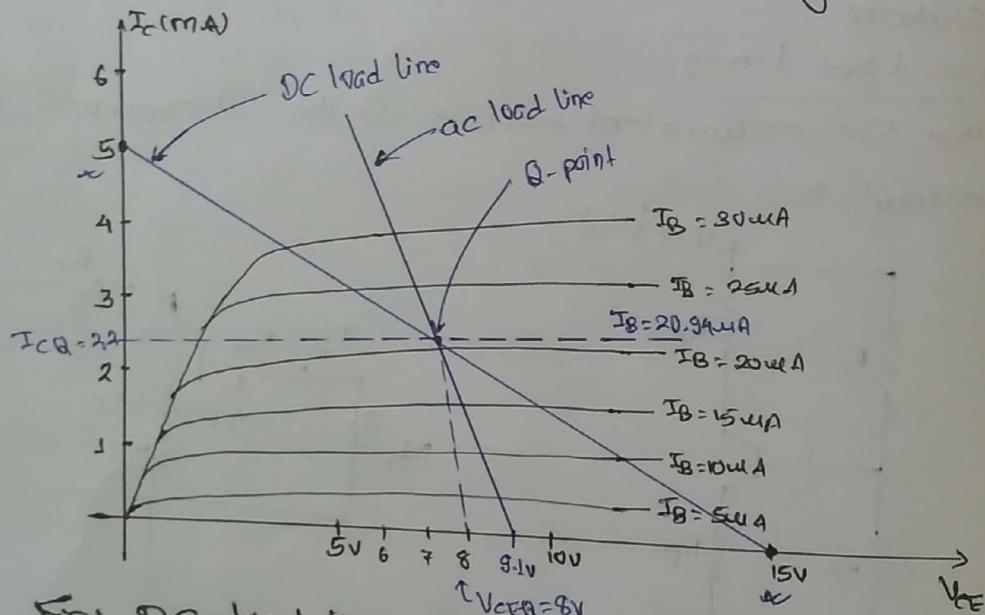


Fig: DC load line, AC load line & Q-point

Q-point:

It is the point at which the dc load line intersects with $I_B = 20.94\mu\text{A}$ curve. At Q-point, the corresponding current & voltages are:

$$I_{CQ} \approx 2.2\text{mA}$$

$$\text{&} V_{CEQ} \approx 8V$$

AC Load Line:

For ac equivalent circuit, all capacitors are shorted and DC voltage sources are grounded & the resultant ac equivalent circuit is as given below:

The ac load line passes through a Q-point & its slope is $-\frac{1}{R_L}$, such that

$$r_L = R_C // R_L$$

$$= \frac{1 \times 1}{1+1} = 0.5 \text{ k}\Omega$$

We have, eqn of ac load line is,

$$I_C - I_{CQ} = -\frac{1}{r_L} (V_{CE} - V_{CEQ})$$

when, $I_C = 0$

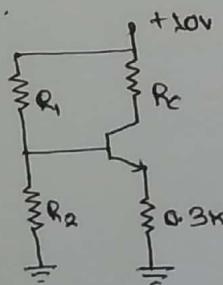
$$\begin{aligned} V_{CE} &= V_{CEQ} - I_{CQ} \cdot r_L \\ &= 8 + 2.2 \times 0.5 \\ &= 9.1 \text{ V} \end{aligned}$$

when, $V_{CE} = 0$,

$$I_C = I_{CQ} + \frac{V_{CEQ}}{r_L} = 2.2 + \frac{8}{0.5} = 18.2 \text{ mA}$$

Now, the straight line joining two points (0, 9.1V) & (9.1V, 0) & (0, 18.2mA) is the ac load line, which is shown in o/p characteristic curve for CE transistor configuration.

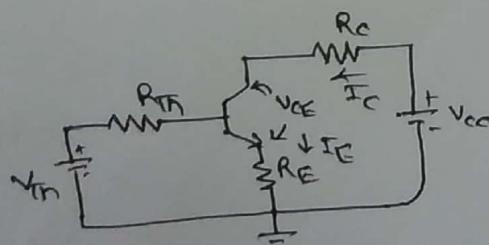
Calculate R_1 & R_C for the circuit given if $I_C = 1 \text{ mA}$, $V_{CE} = 2.5 \text{ V}$ & given $h_{FE} = 100$ & $I_{CQ} = 0$.



Soln:

The Thevenin's

equivalent circuit is,



Applying KVL on o/p loop,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\Rightarrow R_C = \frac{V_{CC} - V_{CE} - I_E R_E}{I_C} = \frac{V_{CC} - V_{CE} - I_C R_E}{I_C}$$

$$\text{or, } R_C = \frac{10 - 2.5 - 1 \times 10^{-3} \times 0.3 \times 10^3}{1 \times 10^{-3}} = \frac{10 - 2.8}{1 \times 10^{-3}}$$

$$\Rightarrow R_C = 7.2 \text{ k}\Omega$$

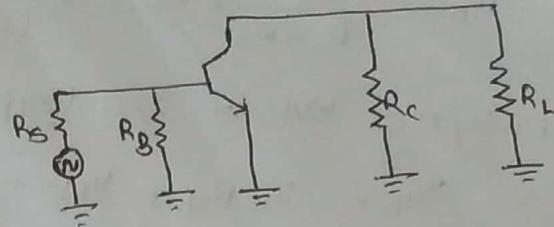


Fig: AC equivalent circuit

Also, we know,

$$V_{Th} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{10K}{(10 + R_1)K} \times 10V$$

Applying KVL at I/P loop,

$$V_{Th} = I_B R_{Th} + V_{BE} + I_E R_E$$

Since Base current is very small,

$$V_{Th} = V_{BE} + I_E R_E$$

$$= 0.7 + 1 \times 10^3 \times 0.8 \times 10^3 = 1V$$

$$\text{Thus, } V_{Th} = 1 = \frac{10 \times 10^3 \times 10}{R_1 + 10 \times 10^3}$$

$$\text{or, } R_1 = 100 \times 10^3 - 10 \times 10^3 = 90K\Omega$$

Thus,

$$R_1 = 90K\Omega \text{ & } R_C = 7.2K\Omega$$