

QN1. Ans :-

current flow mechanism of NPN transistor :-

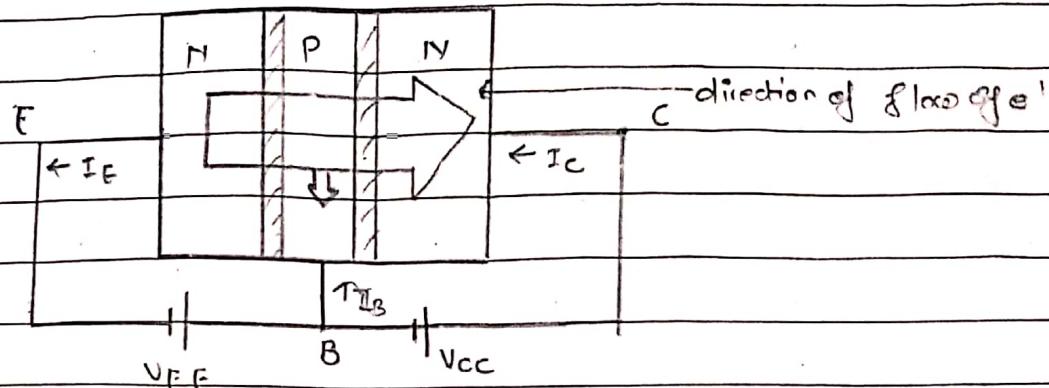
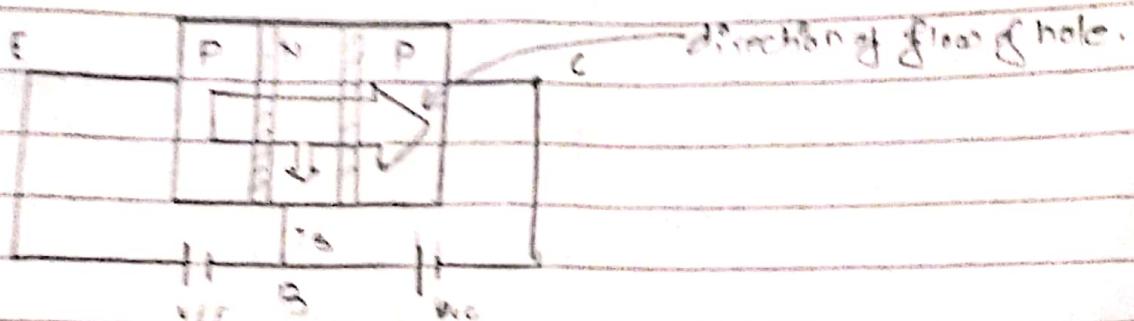


Fig: Basic operation of NPN transistor.

- For normal operation of transistor EB junction must be forward biased & CB junction must be reverse biased.
- The forward bias raises e^- from N-type emitter to flow towards Base & gives emitter current (I_E)
- Among these e^- 's coming from Emitter to base only few e^- 's (about 5%) recombine with hole of P-type Base & give rise to Base current (I_B).
- The remaining e^- 's (about 95%) cross the base region & moves towards collector. As collector is reverse biased e^- crossing the junction is attracted towards +ve terminal of a source V_{CC} . i.e. e^- moves from collector towards source & gives collector current (I_C).

therefore, for a transistor, emitter current is = sum of Base & collector current. i.e. $I_E = I_B + I_C$

Operation of PNP transistor.



Basic operation of PNP transistor.

- For normal operation of transistor, FB junction must be forward biased & CB junction must be reverse biased.
- The forward bias causes e- from P+ type emitter to flow towards base & gives emitter current (I_E).
- Among these e-, if coming from emitter
- The top terminal of a source V_{EE} repels the holes from p-type emitter - so the holes starts to move from emitter towards a base & gives rise to emitter current (I_E).
- Among the holes coming from emitter to base, only few holes (about 5+) recombine with the e- of N-type base & gives rise to Base current (I_B).

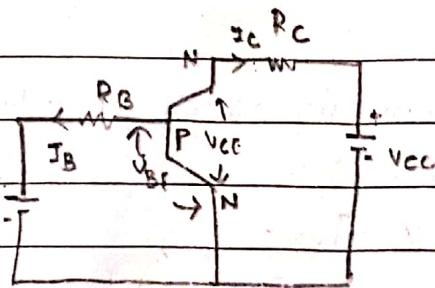
→ The remaining holes (about 95%) cross the Base region and move to the collector. so that holes moves from collector towards the source V_{CC} . This gives rise to collector current (I_C). Thus for a transistor, emitter current is sum of Base current & collector current i.e.

$$I_E = I_C + I_B$$

Q(2) Ans:-

Arrangement of IIP & o/p terminal in a diot is called transistor configuration. It can be performed in 3 ways:-

i) Common Emitter configuration:

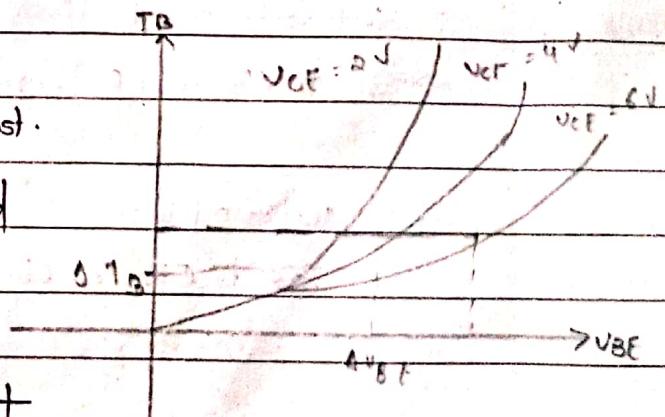


Graph of V_{BF} & I_B for $V_{CE} = \text{const}$

→ Similar to that of forward biased diode.

fig: common emitter configuration

→ IIP resistance, $r_{in} = \frac{\partial V_{BE}}{\partial I_B} \quad | \quad V_{CE} = \text{const.}$



Hence, I_B increases less as compared to V_{BF} so, $r_{in} = \text{high.}$

→ As $V_{CE} \rightarrow$ reverse bias voltage at

collector-base junction (\uparrow) =

depletion width of CB junction (\uparrow) =

Base region (\uparrow) & effective Base width (\downarrow) =

$$I_B (\uparrow)$$

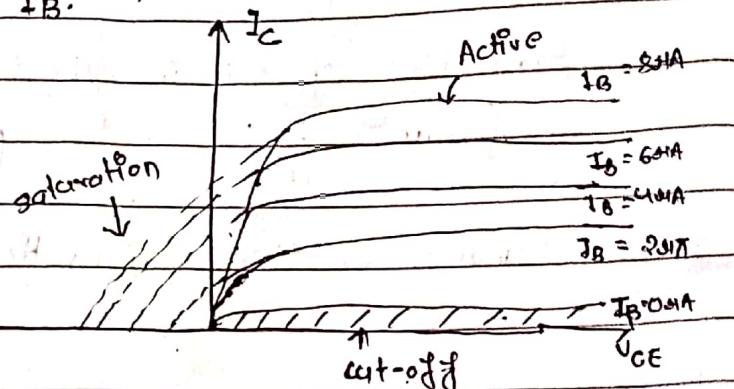
fig: output characteristics for CE configuration.

This effect is called Early effect or Base width modulation.

→ If reverse bias voltage, V_{BE} is further increased effective base width tends to zero, causing excessive rise in collector current I_C . This phenomena is punch through.

Output characteristics:-

Plot of V_{CE} & I_C of constant I_B .



→ Three region of operation

(i) Active

→ EB is F.B & CB is reverse biased. configuration.

Fig: Op characteristics of CE

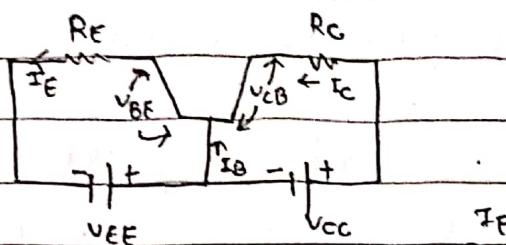
(ii) saturation

→ Both EB & CB are F.B.

(iii) cut-off

Both EB & CB are R.B.

2) Common Base Configuration:-



I_P characteristics:

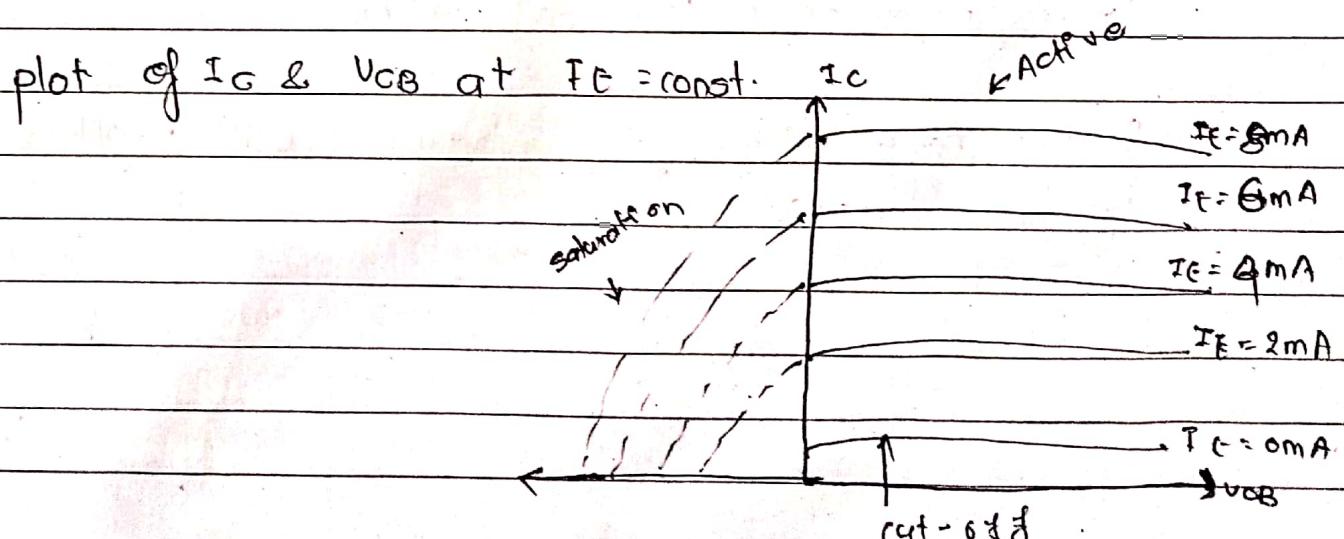
→ plot of I_F & V_{BF} at $V_{CB} = \text{const.}$

→ for a given I_P voltage V_{BE} , I_P current $I_F(\tau)$ when higher value of CB voltage (V_{CB}) is applied.

→ As $V_{CB} \uparrow$ from 0 to 10V I_F also (\uparrow), of CB configuration which is due to reduction of effective base width.

$$r_{in} = \left| \frac{\partial V_{BE}}{\partial I_E} \right|_{V_{CB}=\text{const.}} = 1000$$

O_P characteristics:-



- $I_C \ll I_E$ in active region. So o/p resistance is very high.
- $I_C = 0$ at cut-off region.
- For small $-v_{CE}$ voltage of v_{CB} , both function will be forward biased & will be in saturation.

3) Common Collector Configuration:

IIP characteristics:

plot of v_{CB} & I_B at

$v_{CE} = \text{const.}$

Hence,

$$v_{BE} = v_{FE} - v_{CB}$$

As $v_{CB} (\uparrow)$ with, $v_{CE} = \text{const.}$

$$v_{BE} (\downarrow) = I_B (\downarrow)$$

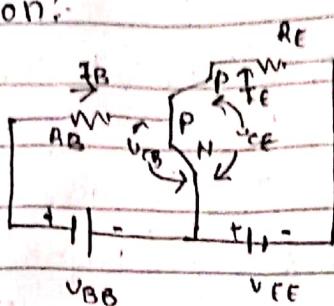
Also, when $v_{CB} = v_{CE}$

$$v_{BF} = 0 \Rightarrow I_B = 0.$$

O/p characteristics,

⇒ plot of v_{CE} & I_E at $I_B = \text{const.}$

Fig: common collector configuration.



$$I_B \text{ vs } v_{CE} = 5, 10, 15 \text{ V}$$

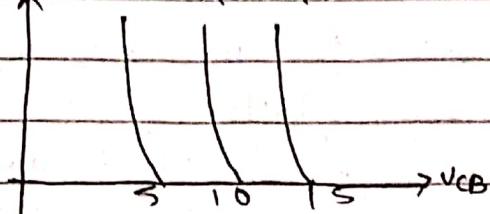


Fig: IIP characteristics of CC configuration.

⇒ similar to common emitter configuration.

→ Is also known as emitter follower because emitter voltage follows the base voltage.

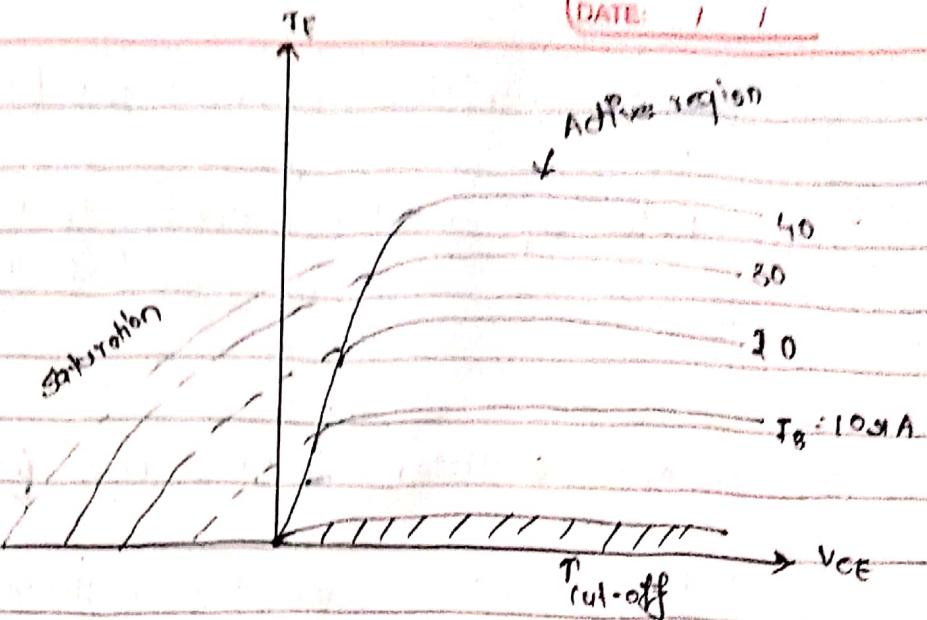


Fig: O/P characteristics of CC configuration.

- 3.) Compare CB, CC & CE configuration of BJT in terms of current gain, Z_{in} impedance, voltage gain & its application.

① Common Base current Gain (α)

ratio of collector current resulting from carrier injection to the total emitter current.

$$\text{current gain } (\alpha) = \frac{\text{O/p current}}{\text{I/p current}}$$

$$\text{or, } \alpha = \frac{I_C (\text{INJ})}{I_E}$$

$$I_C (\text{INJ}) = \alpha I_E$$

Total collector current I_C :

$$I_C = I_C (\text{INJ}) + I_{CBO}$$

$$\Rightarrow I_C = \alpha I_E + I_{CBO}$$

② Common Emitter current Gain (β)

ratio of collector current to base current :-

$$\beta = \frac{I_C}{I_B}$$

③ Common collector current Gain (γ)

ratio of emitter current to collector to

$$\gamma = \frac{I_E}{I_B} = \frac{I_B + I_C}{I_B} = 1 + \beta.$$

Input impedance is very high (200 to 750k Ω) voltage gain is less than unity.

Application :

switching circuits.

Q4.) What are modes of operation of transistor. Show that, $I_C = \beta I_B + (\beta + 1) I_{EB}$, where the symbols have their usual meanings.

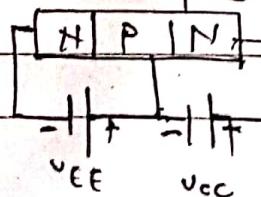
→ Ans:-

BJT can operate in any of following modes :-

a.) Active mode :-

If EB junction is forward biased & CB junction is reverse biased then its mode of operation is called active mode.

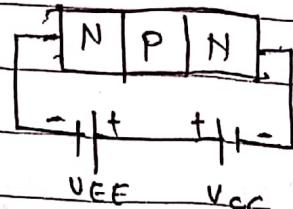
In this mode BJT works as an amplifier.



b) Saturation mode

- Both EB and CB junction of BJT is forward biased.

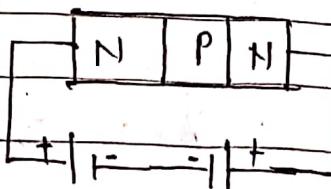
→ works as close switch i.e. switch ON.



c) Cut-off mode

→ both EB & CB junctions are reverse biased.

→ works as open switch OFF.



Given,

$$I_c = \beta I_B + (\beta + 1) I_{CBO}$$

In collector-base leakage current (I_{CBO})

$$\begin{aligned} I_c &= \alpha I_B + I_{CBO} \quad [I_{CBO} \text{ is the common base current}] \\ &= \alpha (I_C + I_B) + I_{CBO} \\ \text{or } (1-\alpha) I_c &= \alpha I_B + I_{CBO} \end{aligned}$$

$$I_c = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \quad \text{--- (1)}$$

where I_{CBO} is the common base leakage current.

From the relation of common Base current gain (α) and common emitter current gain (β).

$$I_E = I_B + I_C$$

$$\frac{I_E}{I_C} = \frac{I_B + I_C}{I_C}$$

$$\frac{1}{I_C/I_B} = \frac{1}{I_C/I_B} + 1$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 = \frac{\beta + 1}{\beta}$$

$$\alpha = \frac{\beta + 1}{\beta}$$

$$1/\beta = 1/\alpha - 1 = 1 - \alpha$$

$$\beta = \frac{1 - \alpha}{\alpha} \quad \text{---(2)}$$

from the eqn ① & ②

$$I_O = \beta I_B + \beta I_{CBO}$$

- 5) With neat sketch & its significance, explain BJT switching time. What is early effect & punch through.



BJT can be used as a switch when it is operated in saturation & open switch (switch OFF) when operated in cut-off region.

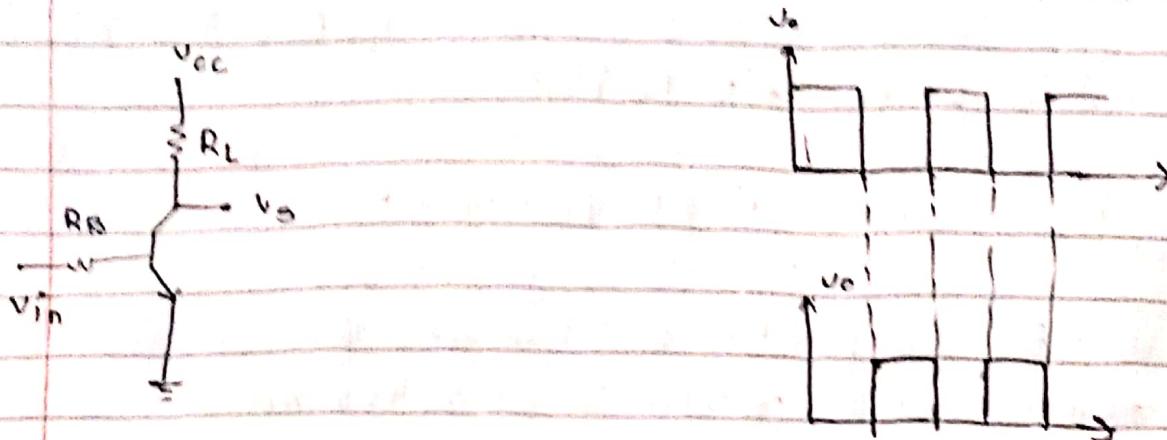


Fig: Transistor as switch

→ If $v_{in} = 0V$ or (v_{in} is less than Barrier potential) it is not sufficient to forward bias EB junction & CB junction is reverse biased.

Case I :- When $v_{in} \neq 0V$

→ If $v_{in} = 0V$ or (v_{in} is less than Barrier potential) it is not sufficient to forward bias EB junction & CB junction is reverse biased.

→ Both FB & CB junction are reverse biased, & transistors will operate in cut-off mode.

In cut off, transistor doesn't conduct from collector to emitter i.e. open circuited.

→ v_o becomes high & works as switch ON.

$$\begin{cases} v_o = V_{cc} \\ v_o = 0 \end{cases}$$

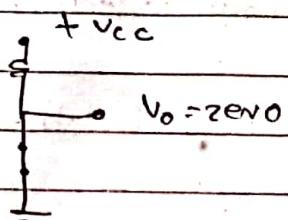
(Case II :- When I_{Dp} is high)

\rightarrow If $V_{in} = SV$ (or $V_{in} >$ Barrier Potential)

Both CB & EB junction will become forward biased
& transistor will operate in saturation mode.

\rightarrow Transistor conducts & works as close switch.

\rightarrow O_{Dp} becomes low & behaves a switch OFF.



Early Effect:-

As $V_{CE}(T) \rightarrow$ reverse bias voltage at collector - base junction (T) \Rightarrow depletion width of CB junction (T) \Rightarrow Base region (n) & effective Base width (J) $= J_B(n)$.
This effect is called Early Effect or Base width modulation.

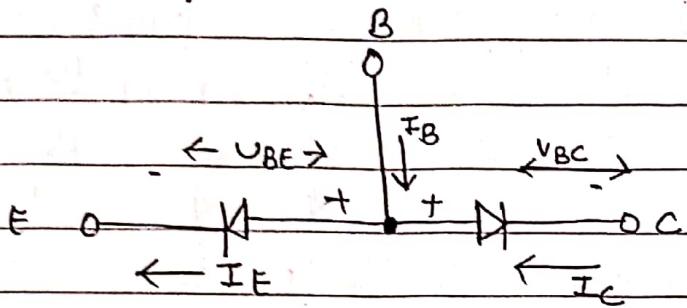
Punch through:-

If reverse bias voltage is further increased, effective base width tends to zero, causing excessive rise in collector current I_C . This phenomenon is Punch through.

- c.) Describe Ebers-Moll Model of transistor. Transistor can be used as a switch and as an amplifier. Explain.

→ Ans:-

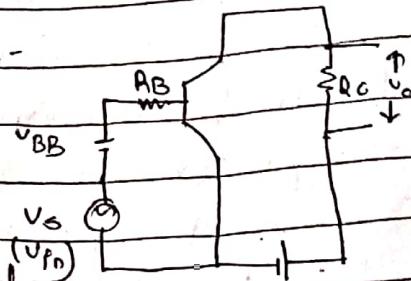
The bipolar junction transistor can be considered essentially as two pn junctions placed back to back, with the base p-type region being common to both diodes. This can be viewed as two diodes having a common third terminal as shown in fig.



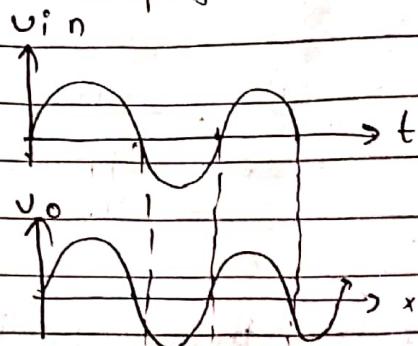
However, the two diodes are not in isolation, but are independent. This means that the total current flowing in each diode is influenced by the conditions prevailing in the other. In isolation, the two junctions would be characterized by the normal diode equation with a suitable notation used to differentiate between the two junctions ~~as can~~. When the two junctions are combined, however, to form a transistor, the base region is shared internally by both diodes even though there is external connection to it.

Transistor as a switch -

Transistor as an Amplifier -



To use Transistor as an amplifier it must be operated in active mode, i.e. EB junction is forward biased & CB junction is reversed.



- Consider a CE transistor amplifier with low amplitude AC signal v_s is applied as TIP to be amplified.
- DC voltages sources V_{BB} & V_{CC} are connected in such a way that EB junction is forward biased and CB junction is reverse biased.
- The TIP ckt being forward biased has low resistance so that a small change in TIP voltage can cause large change in T_B & cause almost same change in T_C ($I_C = \beta I_B$)
- This large collector current flowing through R_C develops large voltage across it.

→ Thus a weak signal applied at I_{BP} port appears in the amplified form at the o/p.

In this way, transistor can be used as an amplifier.

Q. What is stability factor? Derive stability factor for self biased NPN transistor.

→ Ans:-

Stability factor is the rate of change in collector base leakage current I_{CBO} i.e.

$$s = \frac{dI_C}{dI_{CBO}}$$

We have,

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

on differentiating w.r.t. to I_C

$$1 = \frac{\beta \cdot dI_B}{dI_C} + (\beta + 1) \frac{dI_{CBO}}{dI_C}$$

$$\text{or, } 1 - \frac{\beta dI_B}{dI_C} = (\beta + 1) \frac{dI_{CBO}}{dI_C}$$

$$= (\beta + 1) \times \frac{1}{s}$$

$$\therefore s = \frac{\beta + 1}{1 - \beta dI_B} \frac{1}{dI_C}$$

This is the required stability factor for self biased NPN transistor.

QN 89.) Avalanche / Breakdown effect on transistor:

The breakdown region of a transistor is the region where the collector voltage V_{CC} is so large that the collector-base diode breaks down, causing a large undesired collector current to flow.

When the collector-base voltage is too large, the collector-base diode breaks down so that the collector conducts electricity. So even though the base of the transistor doesn't receive any current, the transistor still conducts across the collector. This is called the breakdown region.

b.) Relationship between α , B & β .

We know that,

$$I_E = I_B + I_C$$

$$\text{Or, } \frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\text{Or, } \frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\alpha = \frac{\beta + 1}{\beta}$$

$$\text{Or, } \frac{1}{\beta} = \frac{1 - \alpha}{\alpha}$$

$$\therefore \beta = \frac{1 - \alpha}{\alpha}$$

$$\text{or}, \quad \beta = \frac{I_E}{I_B} = \frac{I_B + I_C}{I_B} = 1 + \beta.$$

$$\beta = 1 + \beta$$

$$\therefore \beta = \beta - 1$$

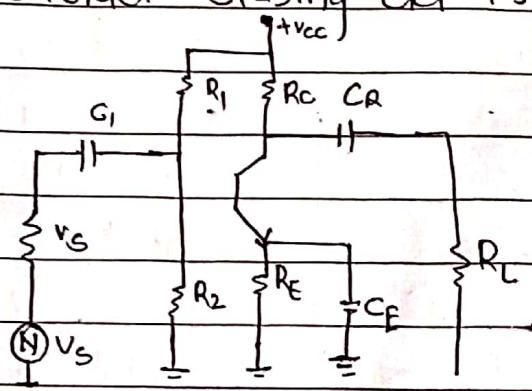
$$\beta - 1 = \beta = \frac{1}{\alpha}$$

This is the

required relationship between α , β & γ .

c) AC & DC load line and Q-point:

Consider a voltage divider biasing circuit is,



DC load line!

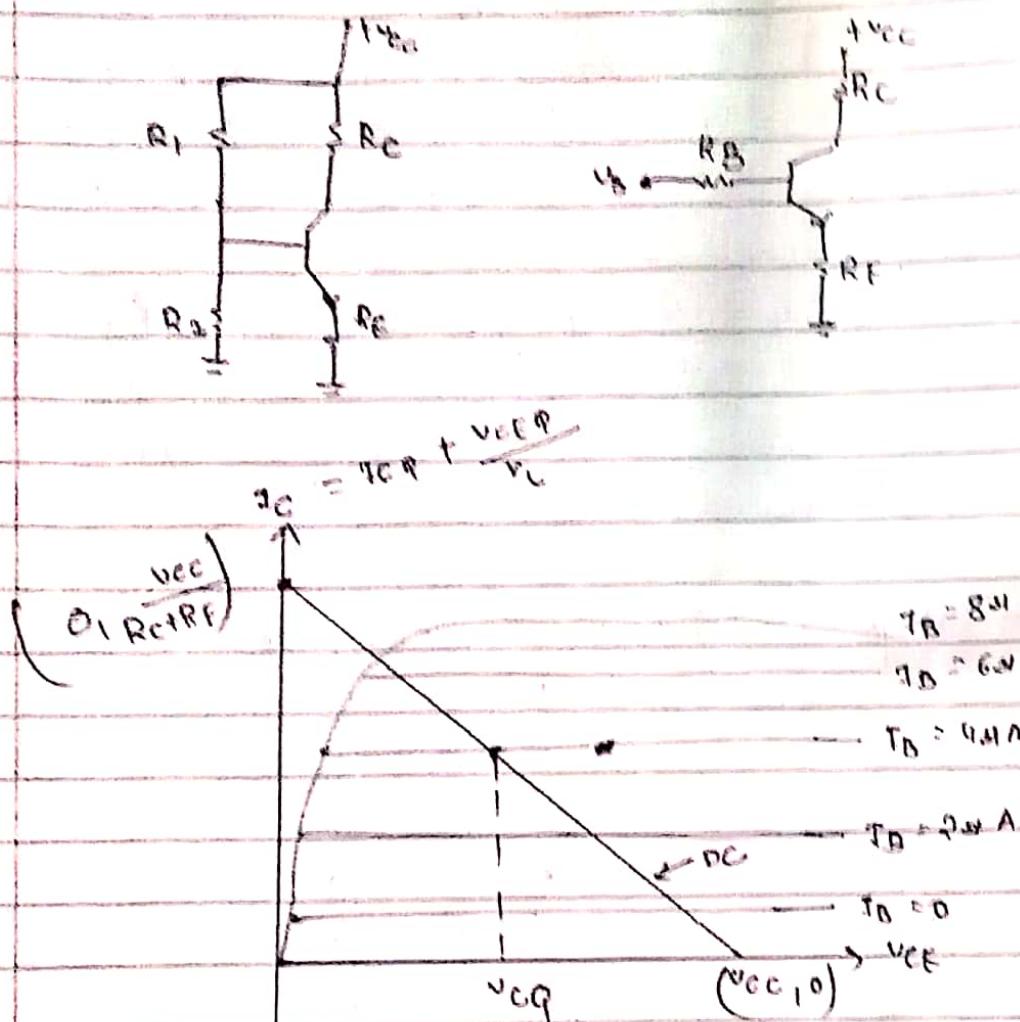
DC load line is the on o/p characteristics of transistor or ckt which gives the value of I_C & V_{CE} corresponding to zero AC signal or DC condition.

For DC equivalent ckt, all capacitor are opened. Since

$$X_C = \frac{1}{2\pi f C} = \frac{1}{0} = \infty \quad \& \text{ all AC voltage sources are}$$

grounded.

Then DC. equivalent circuit of the transistor and eqn I_C ,



Applying KVL at OIP loop:

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E = I_C (R_C + R_E) + V_{CE}$$

$$\text{if } V_{CE} = 0, I_C = \frac{V_{CC}}{R_C + R_E}$$

$$\text{if } I_C = 0, V_{CE} = V_{CC}$$

In above graph two points $(V_{CC}, 0)$ & $(0, \frac{V_{CC}}{R_C + R_E})$ are joined by that straight line is called DC load line.

joined by that straight line is called DC load line.

AC load line:

This is a line on O/P characteristics of transistor or ckt that gives the value of i_C & V_{CE} when AC signal applied is considered.

AC load line passes through Q-point i.e. its slope is $\frac{1}{r_L}$, where $r_L = R_C \parallel R_L$.

The eqn of AC load line is,

$$I_O - I_{CQ} = \frac{1}{r_L} (V_{CE} - V_{CEQ})$$

when $i_C = 0$

$$V_{CE} = 0 \quad I_O = r_L + V_{CEQ}$$

& when $V_{CE} = 0$

$$I_O = I_{CQ} + \frac{V_{CEQ}}{r_L}$$

on joining these two points ($I_{CQ}, r_L + V_{CEQ}, 0$) & ($0, I_{CQ} + \frac{V_{CEQ}}{r_L}$) a straight line is obtained which is known as AC load line.

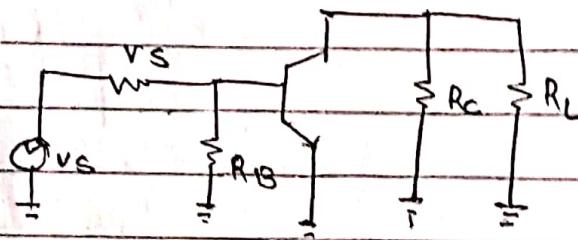


Fig: AC equivalent ckt of given transistor ckt.

d) Thermal instability & thermal runaway:

This process goes in cumulative way & as a result large current flows. This process is called thermal instability & thermal runaway.

Thermal runaway can be avoided by suitable design. To avoid thermal runaway, following condition must be satisfied.

$$\frac{dP_c}{dT_j} < \frac{dP_o}{dT_j}$$

whence, $\frac{dP_c}{dT_j}$ is variation of power dissipated

at collector due to temperature variation,

$\frac{dP_o}{dT_j}$ is variation of power dissipated at collector that is allowed by manufacturer with respect to junction temperature variable.

1.) Design a CE self-bias circuit for $I_C = 20mA$, $V_{CC} = 20V$, $B = 100$.
 → Soln:-

The CE self-bias ckt is,

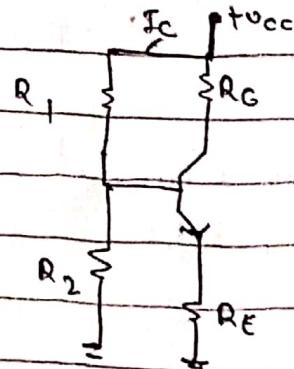
$$\text{let, } V_{BE} = 10\% \text{ of } V_{CC}$$

$$\text{or, } I_{ERE} = 10\% \text{ of } 20V = 2V$$

$$R_E = \frac{2V}{I_E} = \frac{2V}{2mA} = \frac{2V}{2mA}$$

$$= 1k\Omega$$

$$\text{let, } V_{CE} = 50\% \text{ of } V_{CC} = 10V.$$



Applying KVL at op loop, $V_{CC} = I_C R_C + V_{CE} + I_{ERE}$

$$20 = I_C R_C + 10 + 2$$

$$R_C = \frac{8V}{2mA} = 4k\Omega$$

$$\text{And } V_B = V_{CC} - I_1 R_1$$

$$\text{where } I_1 = 10I_B = 10 \frac{I_C}{B} = 10 \times \frac{2mA}{100}$$

$$= 2 \times 10^{-4} A.$$

$$V_B = V_{CC} - 2 \times 10^{-4} \times R_1$$

$$\& V_B = V_{BE} + I_{ERE}$$

$$= 0.7 + 2 = 2.7$$

$$\text{or, } 2.7 = 20 - 2 \times 10^{-4} \times R_1$$

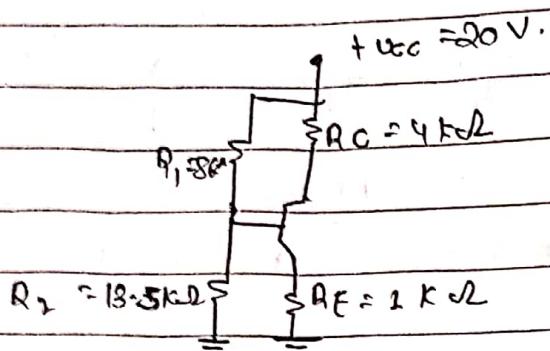
$$R_1 = 86.5 k\Omega$$

$$\text{Again } V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

$$2.7 = \frac{R_2}{86.5 + R_2} \times 20$$

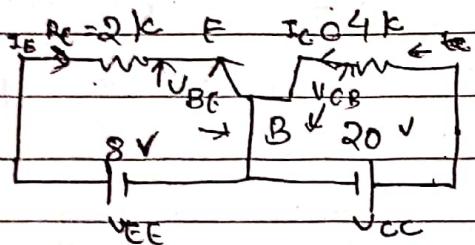
$$\therefore R_2 = 13.5 \text{ k}\Omega$$

The required self-bias circuit for $I_0 = 2 \text{ mA}$ & $V_{CC} = 20 \text{ V}$ is,



2. Find emitter, Base & collector current as well as V_{CE} for given CB transistor amplifier. Also draw no load line and locate Q-point. Assume $\alpha = 0.9$.

→ Soln:-



→ Soln:-

Applying KVL at top loop:-

$$V_{EE} = I_E R_E + V_{BE}$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{(8 - 0.7)}{2 \text{ k}\Omega} = 3.65 \text{ mA}$$

we have,

$$I_C = \alpha I_E$$

$$= 0.9 \times 3.65 \text{ mA}$$

$$= 3.28 \text{ mA.}$$

$$I_B = I_E - I_C$$

$$= 3.65 - 3.28$$

$$= 0.365 \text{ mA.}$$

KVL at OIP loop

$$V_{CC} = I_C R_C + V_{CB}$$

$$V_{CB} = 20 - 4 \times 10^3 \times 3.28 \times 10^{-3}$$

$$\therefore V_{CB} = 6.88 \text{ V}$$

The OIP characteristics of CB transistor or amp is :-

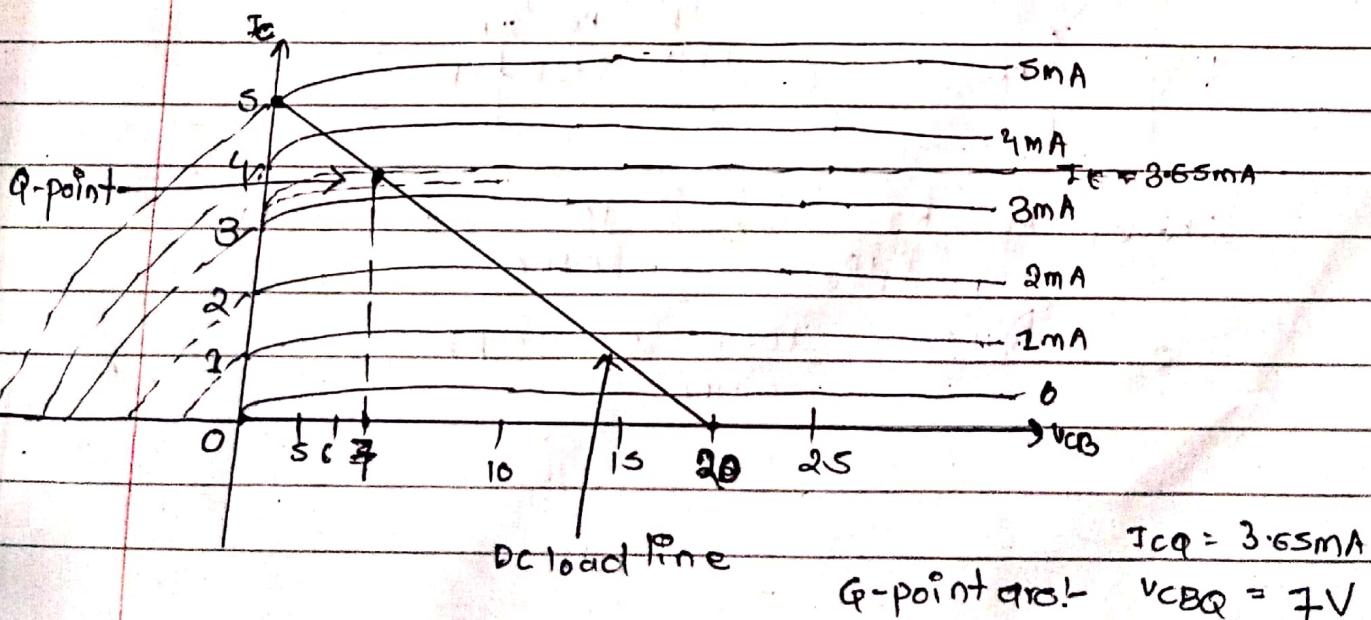
we have,

$$V_{CC} = I_C R_C + V_{CB}$$

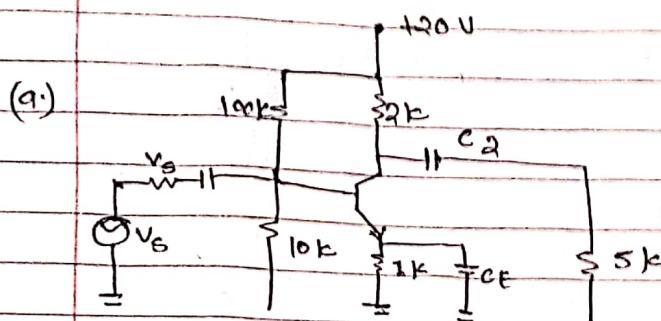
$$\text{when } I_C = 0, V_{CB} = 20 \text{ V} = V_{CC}$$

$$\text{when, } V_{CC} = 0, I_C = \frac{V_{CC}}{R_C} = \frac{20}{4} = 5 \text{ mA.}$$

(20V) & (0, 5mA)

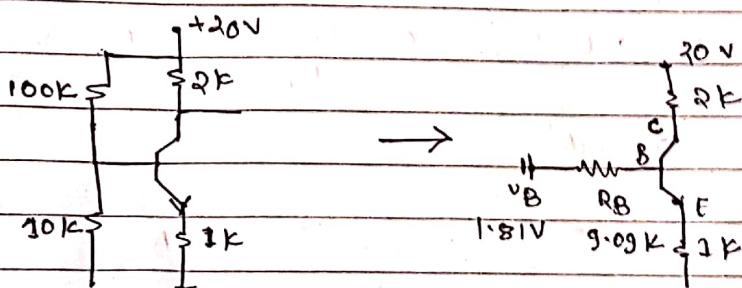


- 3.) For the circuit shown below, draw DC load line & final operating point. Also locate operating point on DC load line & find the stability factor of ch. Assume silicon transistor with $\beta = 300$
 \rightarrow Soln.



For DC load line capacitor C_2 is open circuited.

DC equivalent circuit is



$$\text{Here, } V_B = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{10}{10+100} \times 20 = 1.81V.$$

$$R_B = R_1 // R_2 = \frac{10 \times 100}{10+100} = 9.09k\Omega.$$

Applying KVL at Input,

$$V_B = I_B R_B + V_{BE} + I_E R_E$$

$$1.81 = I_B \times 9.09 \times 10^3 + 0.7 + (\beta+1) I_B \times 1 \times 10^3$$

$$1.81 - 0.7 = I_B (9.09 \times 10^3 + 100 + 1) \times 1 \times 10^3$$

$$\begin{aligned} I_B &= \frac{1.81 - 0.7}{(9.09 \times 10^3 + 101 \times 10^3)} \\ &= 1.008 \times 10^{-5} \text{ Amp.} \approx 1.008 \text{ mA} \end{aligned}$$

& we have,

$$I_C = \beta I_B$$

$$= 100 \times 1.008 \times 10^{-5}$$

$$= 1.008 \text{ mA.}$$

Now,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CC} = I_C (R_C + R_E) + V_{CE}.$$

$$\text{where } V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_C + R_E} = \frac{20}{2 + 1} = 6.66 \text{ mA.}$$

When $I_C = 0$, $V_{CC} = V_{CE} = 20 \text{ V.}$

I_C

(0, 5)

8

6

4

2

0

-2

-4

-6

-8

-10

5

10

15

20

(20, 0)

$I_B = 0$

V_{CE}

Q-point

50 mA

40 mA

30 mA

20 mA

10 mA

0 mA

For the given circuit,

$$V_{CG} = 14 \text{ V.}$$

$$I_{CA} = 108 \text{ mA.}$$