Design and Simulation of CMOS Inverter in Cadence Virtuoso and Layout Implementation

Self Project Report

1. Introduction

The CMOS inverter is one of the most fundamental building blocks of digital integrated circuits. Its functionality and performance directly influence the efficiency of logic families, processors, and VLSI systems.

The objective of this project was to design, simulate, and implement the layout of a CMOS inverter using the *gpdk90* technology library in Cadence Virtuoso. The project involved schematic creation, transient and DC analysis, corner analysis, and physical layout implementation, followed by DRC and LVS verification.

2. Methodology

2.1. Schematic Design

- The CMOS inverter was designed using the *gpdk90* technology library.
- One PMOS and one NMOS transistor were connected in the standard pull-up and pull-down configuration.
- Proper power (VDD) and ground (GND) connections were established.
- The schematic was verified for errors before proceeding to simulation.

2.2. Simulation and Analysis

- **Transient Analysis:** Performed in Cadence ADE to study switching characteristics using a square-wave input.
- **DC Analysis:** Conducted to obtain Voltage Transfer Characteristics (VTC) and threshold voltage.
- **Corner Analysis:** Conducted in ADE XL with variations in process corners, temperature, and PMOS widths.

2.3. Layout Implementation

- Using Virtuoso Layout XL, the inverter layout was drawn with minimum feature size of 1 μm separation as per design rules.
- Metal layers, poly, active regions, and contacts were carefully placed to match the schematic.

2.4. Verification

- **Design Rule Check (DRC):** Run using Assura to ensure compliance with gpdk90 rules.
- **Layout Versus Schematic (LVS):** Verification confirmed that the layout matched the schematic.

3. Results

- The inverter produced the expected inverted output with negligible propagation delay in transient analysis.
- The VTC showed a sharp transition near VDD/2, confirming good noise margins.
- Corner analysis validated stable performance across varying conditions.
- The layout passed DRC and LVS successfully, confirming correctness.

4. Conclusion

This project successfully demonstrated the complete design cycle of a CMOS inverter in Cadence Virtuoso, starting from schematic entry, simulation, and layout, to verification.

The study of transient, DC, and corner analysis reinforced understanding of inverter switching characteristics and robustness. The layout implementation, along with successful DRC and LVS checks, confirmed the correctness of design with respect to both logical and physical domains.

This hands-on project provided valuable exposure to industrial EDA tools and strengthened the understanding of CMOS fundamentals, serving as a foundation for advanced VLSI design.