32-Bit RISC Processor Pipeline

Requirements

The RISC-style 32-bit processor pipeline should support the following instructions:

- MOVE R_i, R_j \\The content of R_j is transferred to R_i.
- MOVE R_i, Immediate (16-bit) \\The immediate value (32-bit unsigned extended) will be transferred to R_i.
- LOAD R_i, X (R_j) \\ The content of memory location [[R_j] + X] is loaded into R_i, where X is a 16-bit unsigned immediate value.
- STORE R_i, X (R_j) \\ The content of register R_i is stored in memory [[R_j] + X], where X is a 16-bit unsigned immediate value.
- ADD R_i, R_j, R_k \\ $R_i = R_j + R_k$.
- ADI R_i, R_j, Immediate (16-bit) \\ $R_i = R_j$ + Immediate Value (32-bit unsigned extended)
- SUB R_i, R_j, R_k \\ $R_i = R_j - R_k$
- SUI R_i, R_j, Immediate (16-bit) \\ $R_i = R_j$ - Immediate Value (32-bit unsigned extended)
- AND R_i, R_j, R_k \\ $R_i = R_j$ AND R_k.
- ANI R_i, R_j, Immediate (16-bit) \\ $R_i = R_j$ AND Immediate Value (32-bit unsigned extended)
- OR R_i, R_j, R_k \\ $R_i = R_j$ OR R_k.
- ORI R_i, R_j, Immediate (16-bit) \\ $R_i = R_j$ OR Immediate Value (32-bit unsigned extended)
- HLT (Stops the execution).

Additional Information: The instructions will be executed sequentially. So, the next instruction will be fetched from the memory only after the current instruction completes its execution. Each instruction will go through the conventional 5 stages of the pipeline as discussed in the class. All registers are 32-bit. The intermediate registers needed for the pipeline execution can be decided as per your design. There is no need to exactly follow the pipeline discussed in the class. You can use any built-in components (including memory) available in the Logisim for designing the circuit. Ensure each instruction takes exactly 5 clock pulses to complete. There will be 32 GPRs in the system. Other special-purpose registers may be included as needed. The control unit designing is not mandatory as the instruction decoder (ID) can directly be used to generate the control signals. Register file (RF) implementation is also up to your choice. The design will be tested against assembly codes (machine codes) written in the memory. The number of memory locations can be decided by you, but ensure it has sufficient space to that a typical program of 32 instructions and 32 data items can be stored. Provide a reset signal that will set the value of PC to 0.