32-Bit RISC Processor Pipeline

Design Overview

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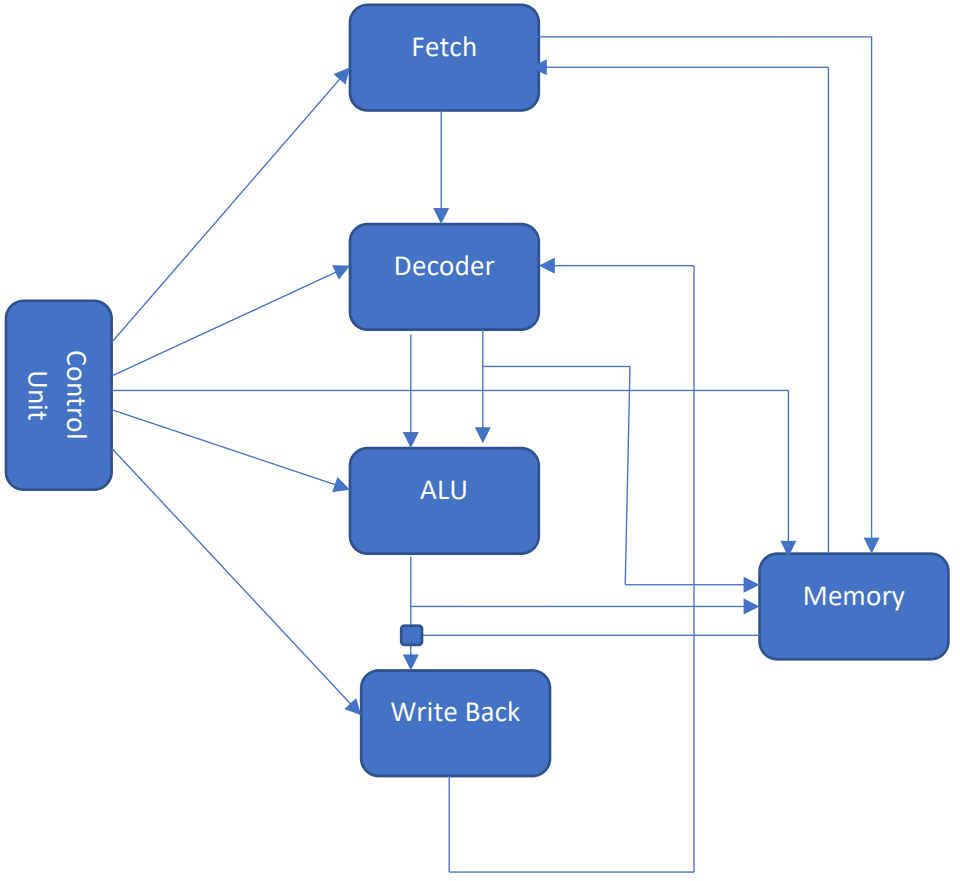
Block Level Diagram:



5-Stage Architecture: