T9.- MEMORIAS

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Nafarroako Unibertsitate Publikoa

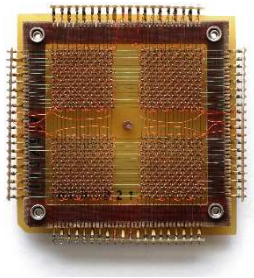
LA MEMORIA

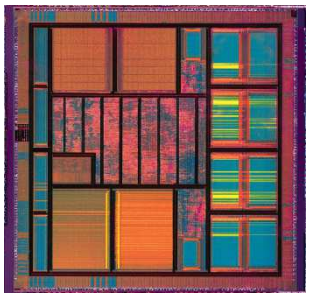
Necesidad de almacenar información ⇨ **Sistemas más complejos**
Aplicaciones más sofisticadas

Distintas tecnologías / soportes para almacenar

- **Analógicas**

- **Digitales**





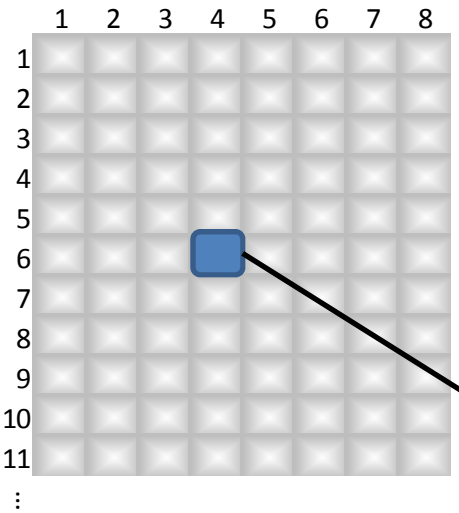
LA MEMORIA

Memorias digitales semiconductoras

- Rapidez: Interacción directa con circuitos digitales
- Tamaño: Alta capacidad de integración
- Integración: fabricación en el chip
- Diferentes topologías/tecnologías de implementación, distinta aplicación de cada memoria

MEMORIA: CONCEPTOS BÁSICOS

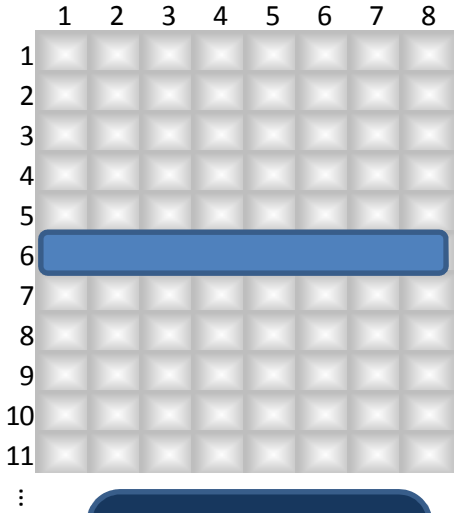
- **Celdas**: Unidad repetitiva capaz de almacenar un 1 ó un 0
- **Bancos de datos**: organizadas en forma de matrices
- **Capacidad de una memoria**: número total de celdas de datos



- Las celdas se organizan en matrices en función de la organización de los datos (8, 16 bits, etc.)

- Para acceder a un elemento de la matriz: DIRECCIÓN

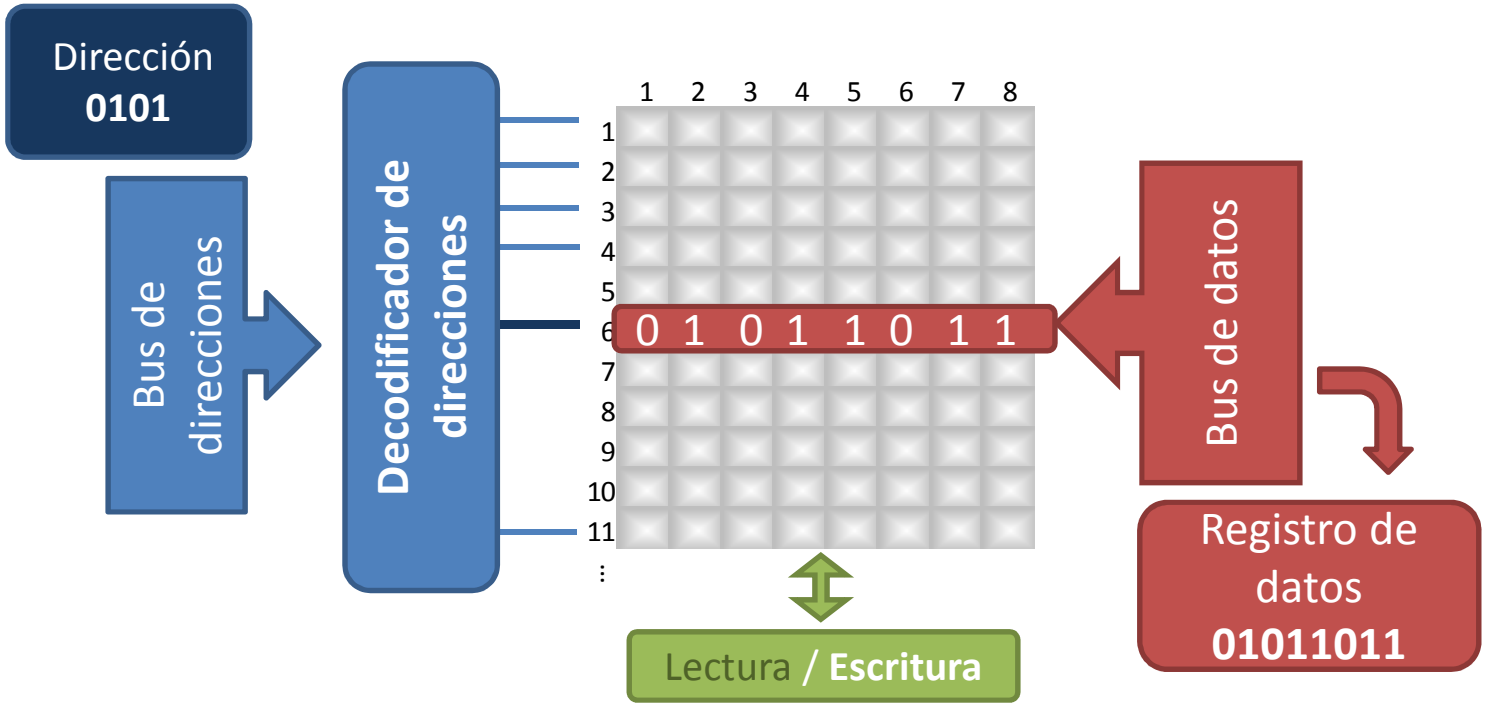
Ejemplo



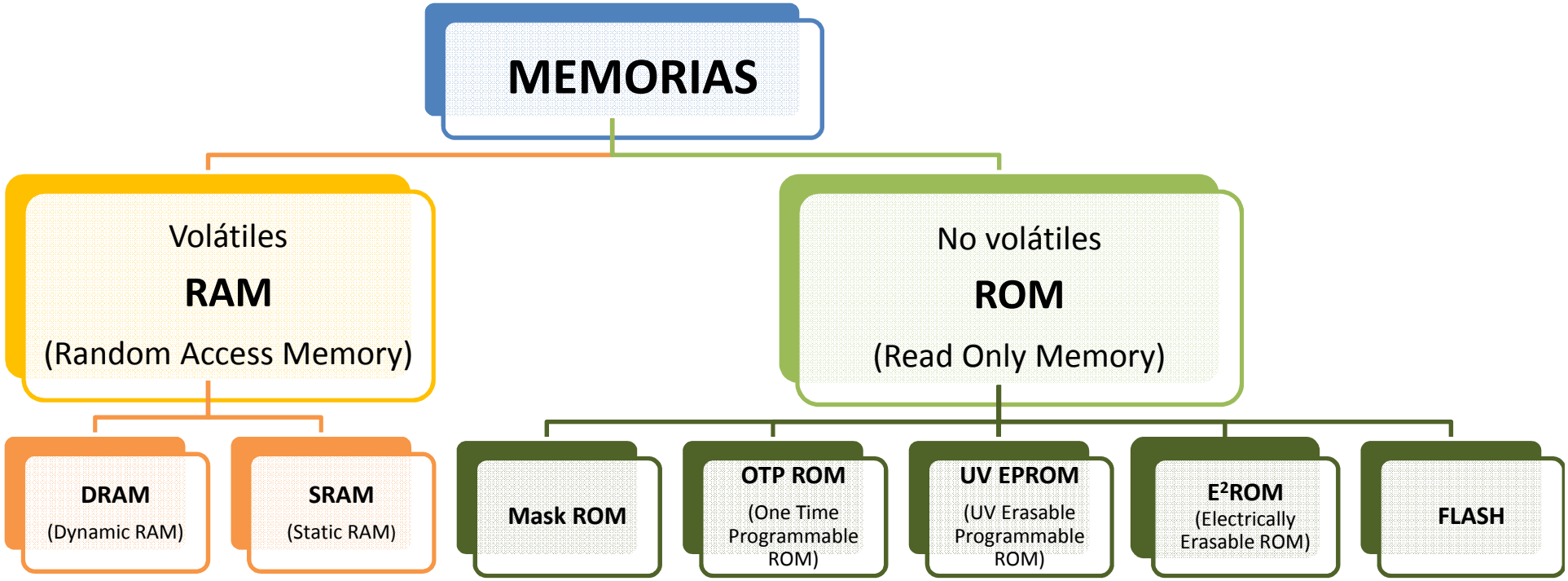
¿Cómo se LEE la información contenida en la dirección 5?

- **Medida de la capacidad de una memoria**:
  - Kb = 2^{10} bits = 1024 bits KB= 2^{10} bytes = 1024 bytes = 8192bits
  - Mb = 2^{10} Kb = 2^{20} bits = 1,048,576 bits

MEMORIA: CONCEPTOS BÁSICOS



Distintos tipos de memoria en función de su construcción: Diferentes aplicaciones


MEMORIAS
Volátiles
RAM
(Random Access Memory)
No volátiles
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(Read Only Memory)
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(Dynamic RAM)
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Mask ROM
OTP ROM
(One Time Programmable ROM)
UV EPROM
(UV Erasable Programmable ROM)
E²ROM
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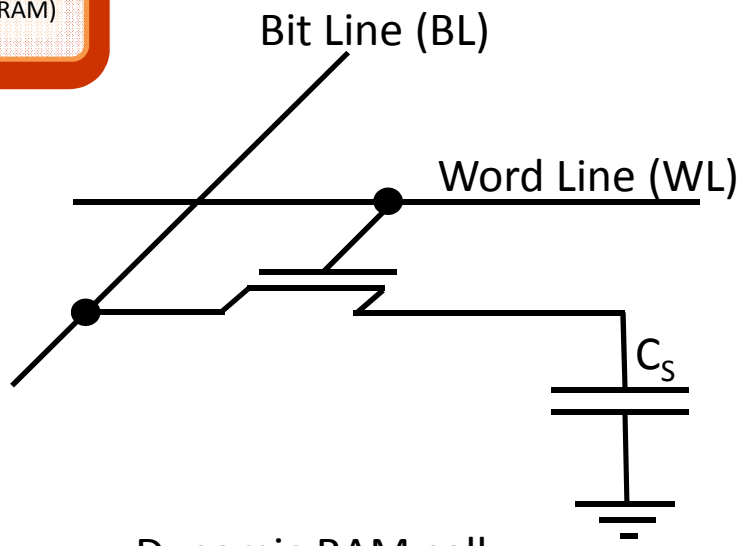
FLASH

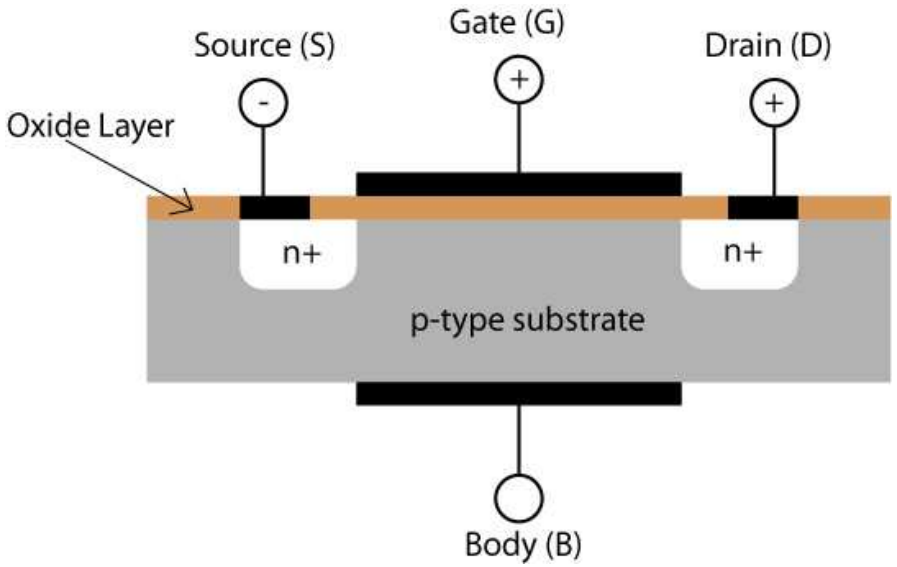
DRAM
(Dynamic RAM)

• asynchronous DRAM



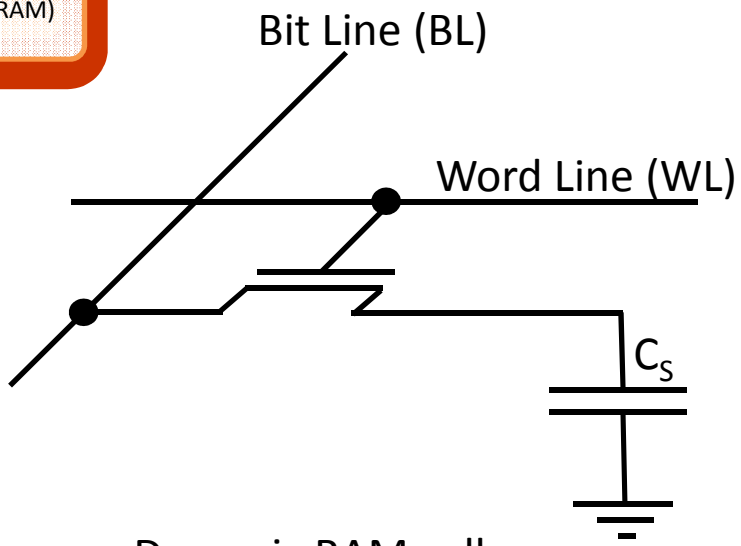
Dynamic RAM cell

- OFF
- ON

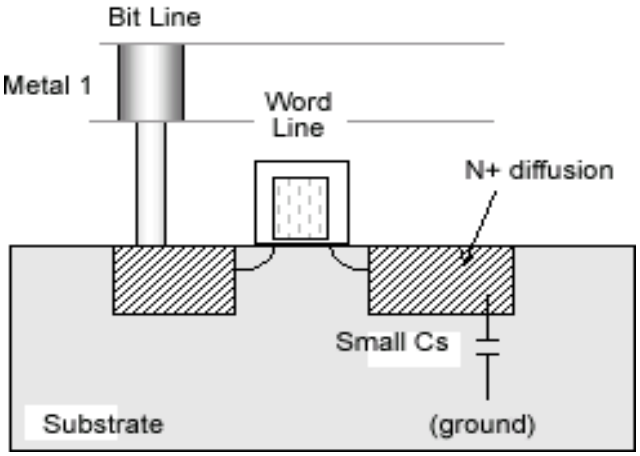


DRAM
(Dynamic RAM)

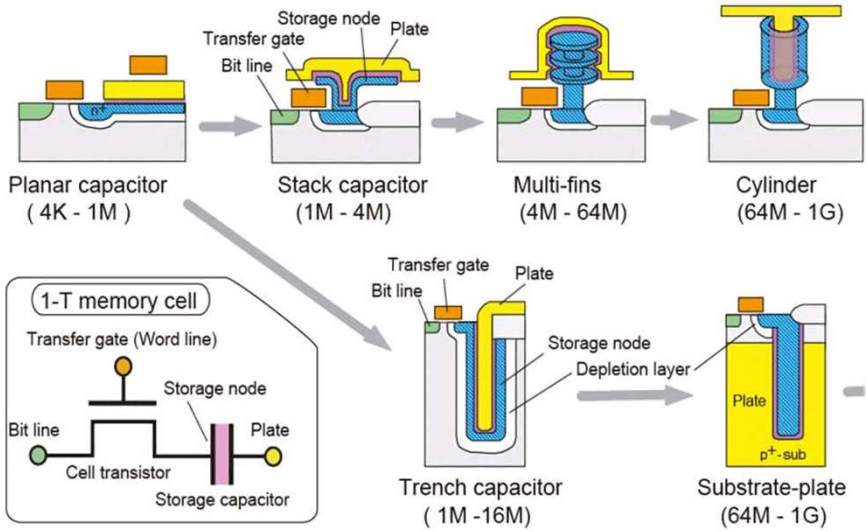
- **asynchronous DRAM**



Dynamic RAM cell



Fuente: Insa-toulouse.fr

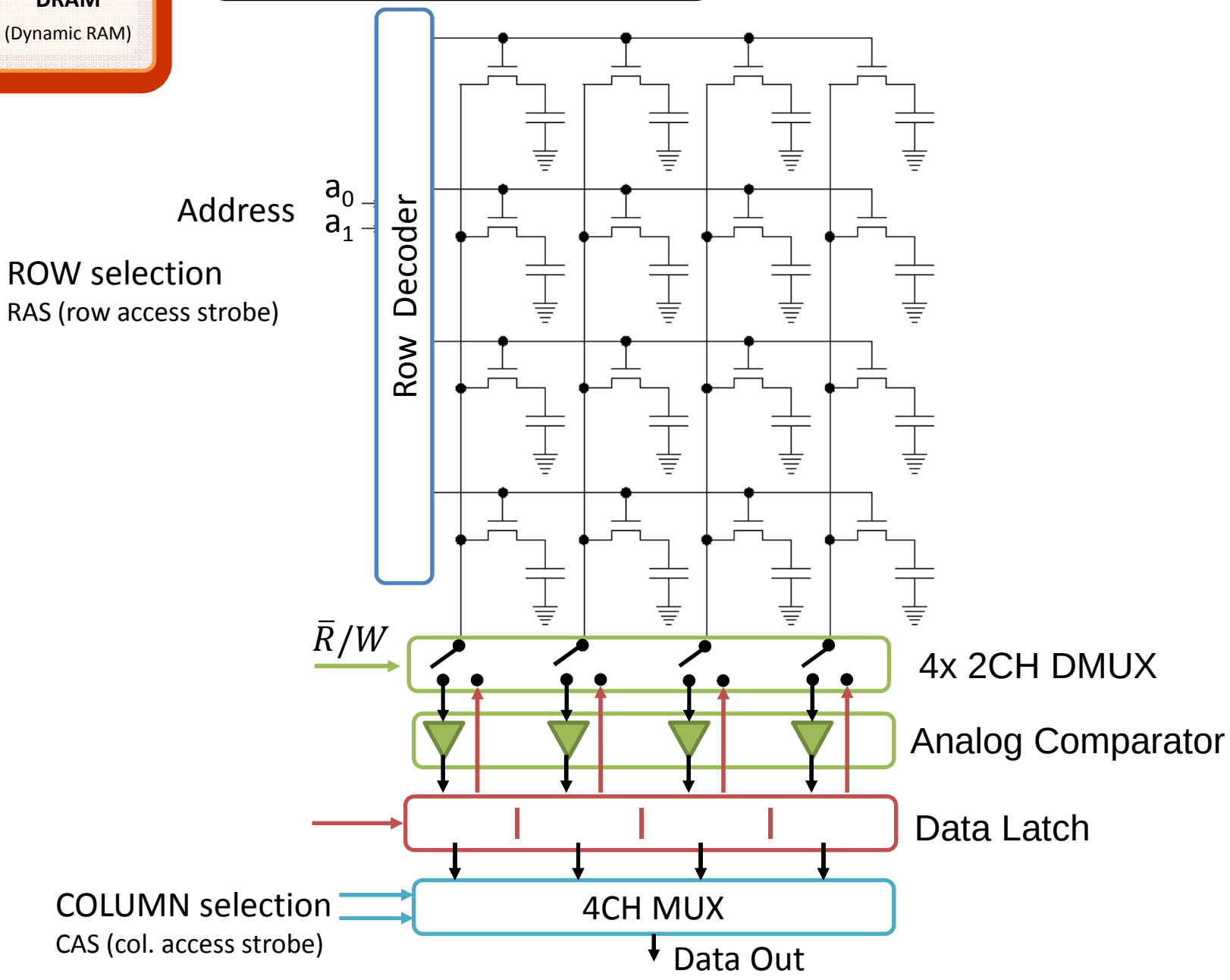


Fuente: Hideo Sunami, "The Role of the Trench Capacitor in DRAM Innovation", Solid-State Circuits Newsletter, IEEE, 2008

DRAM:
(1 Transistor + 1 condensador) / bit
Alta integración de datos
Condensador ≈ de 10fF a 50fF
Es necesaria una operación de refresco

DRAM
(Dynamic RAM)

• asynchronous DRAM



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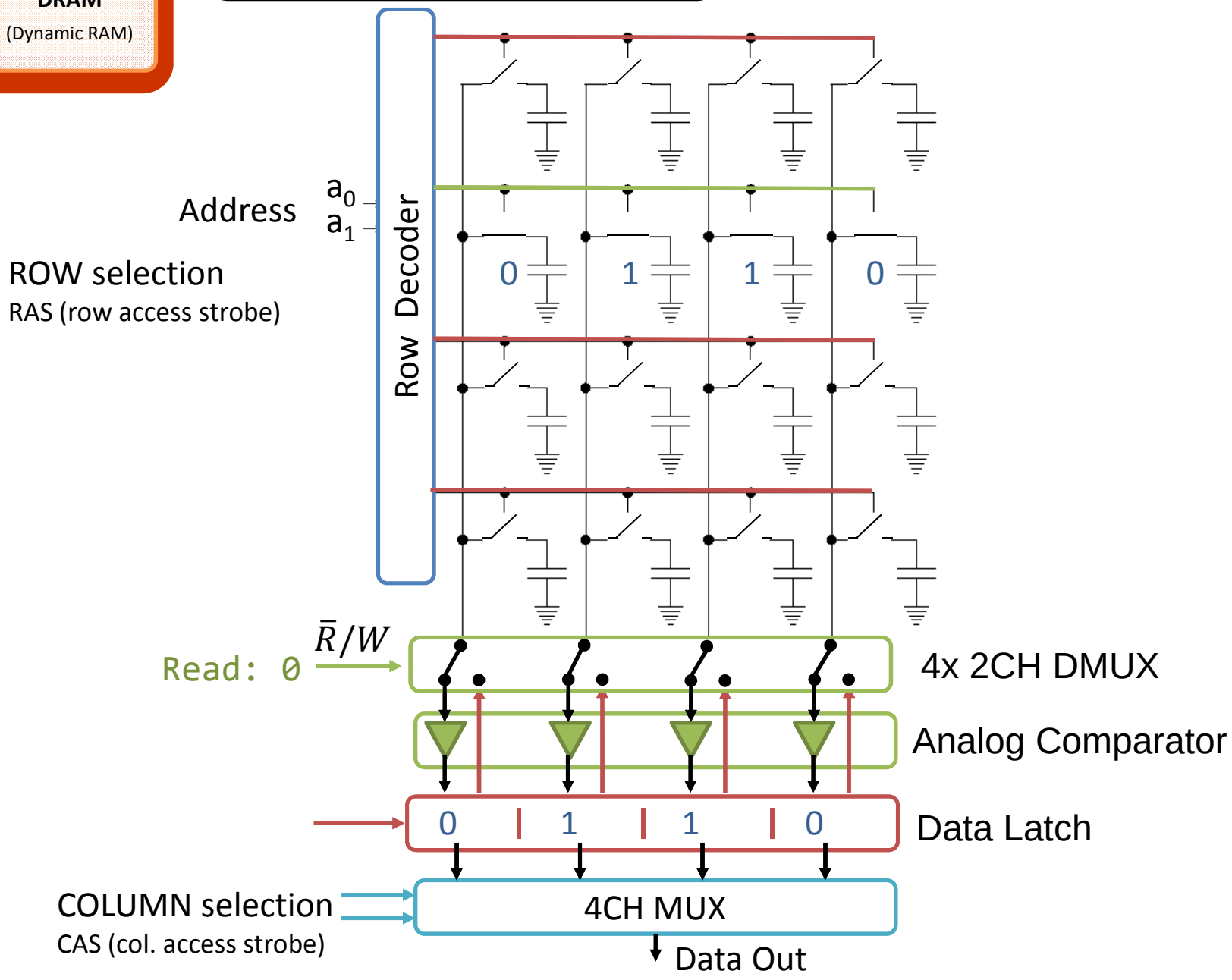

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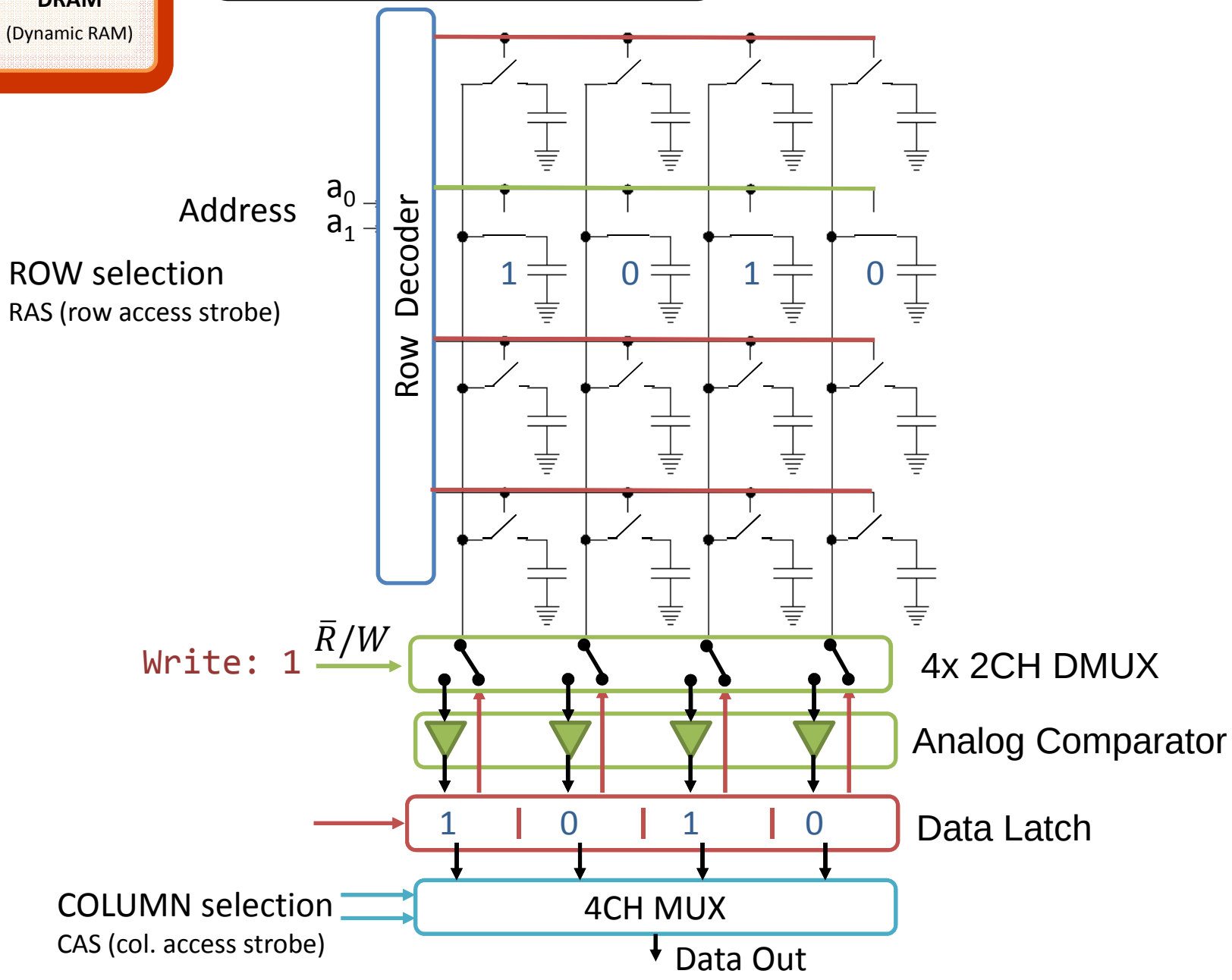

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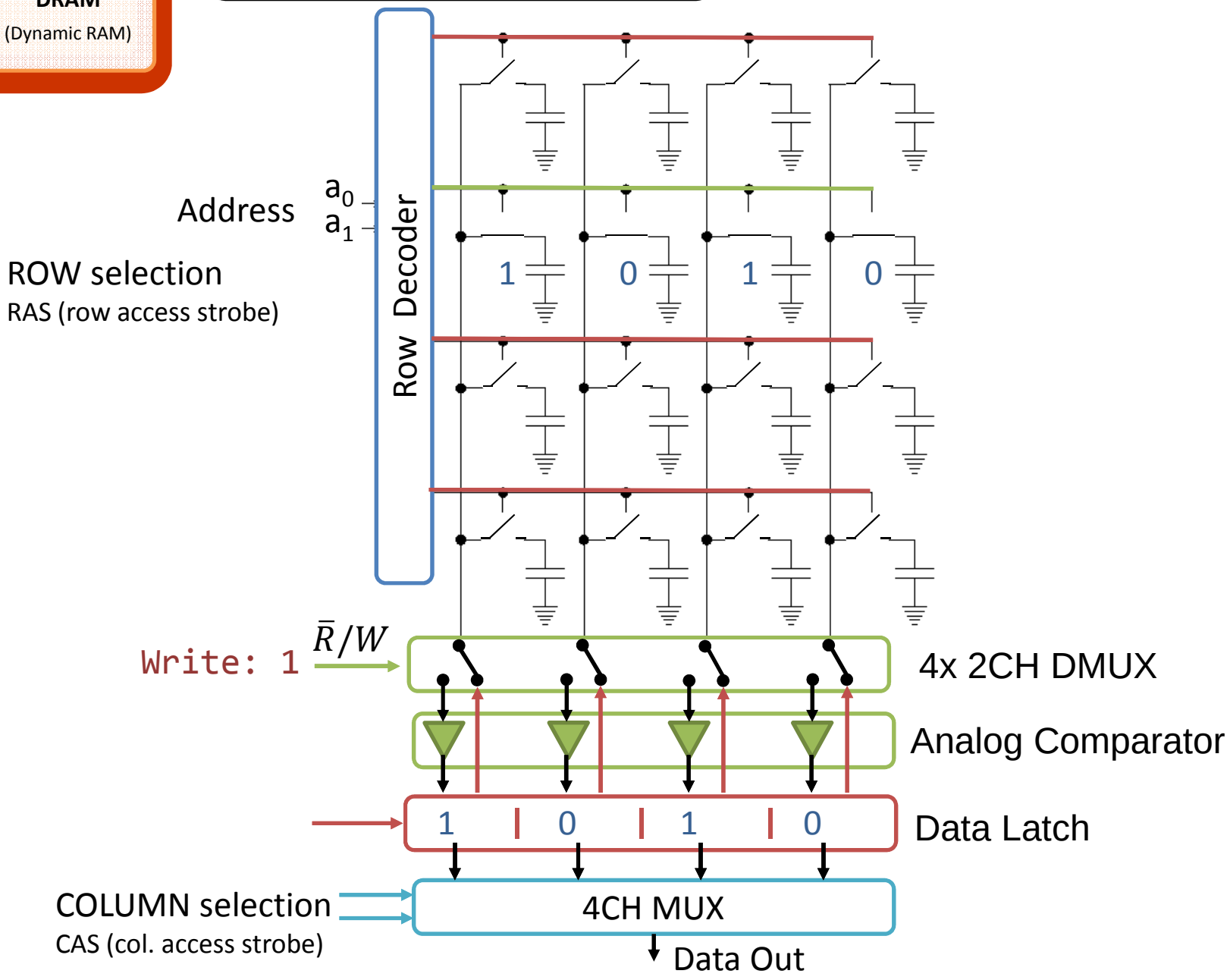
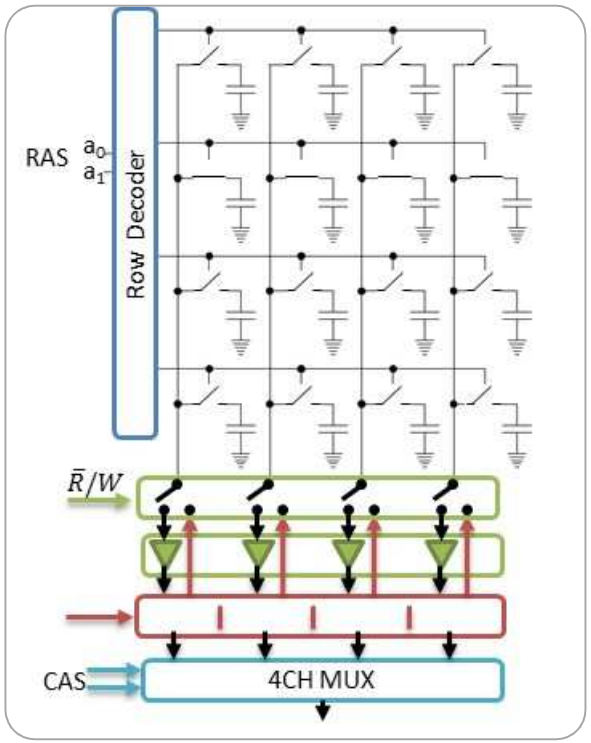


DRAM
(Dynamic RAM)

•SDRAM synchronous



LIMITATIONS OF DRAM:
•Latency.- time delay required to complete an operation
•Refresh cycles
Slow down the memory speed

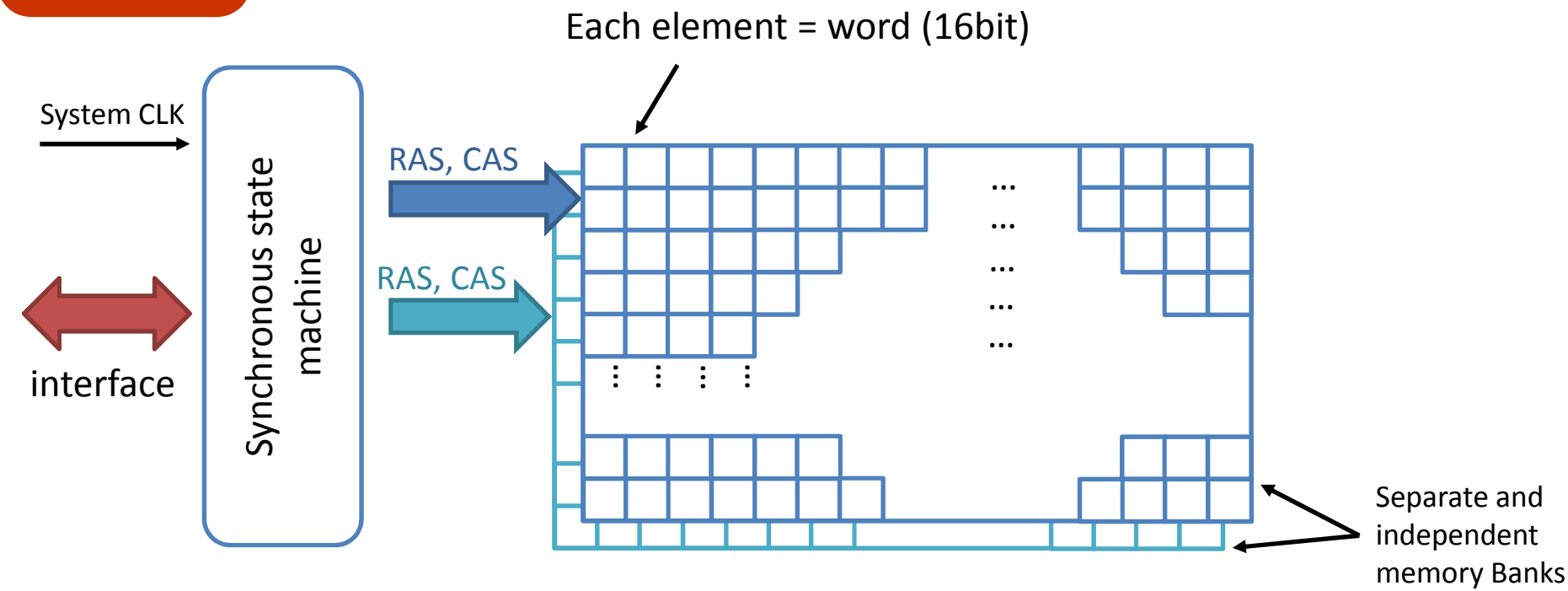
¿HOW IS IT POSSIBLE TO INCREASE THE NUMBER OF MEMORY ACCESSES PER SECOND?

- Reducing the frequency of the refresh cycles
- Shorter latency times
- PIPELINING

SDRAM

DRAM
(Dynamic RAM)

•SDRAM synchronous

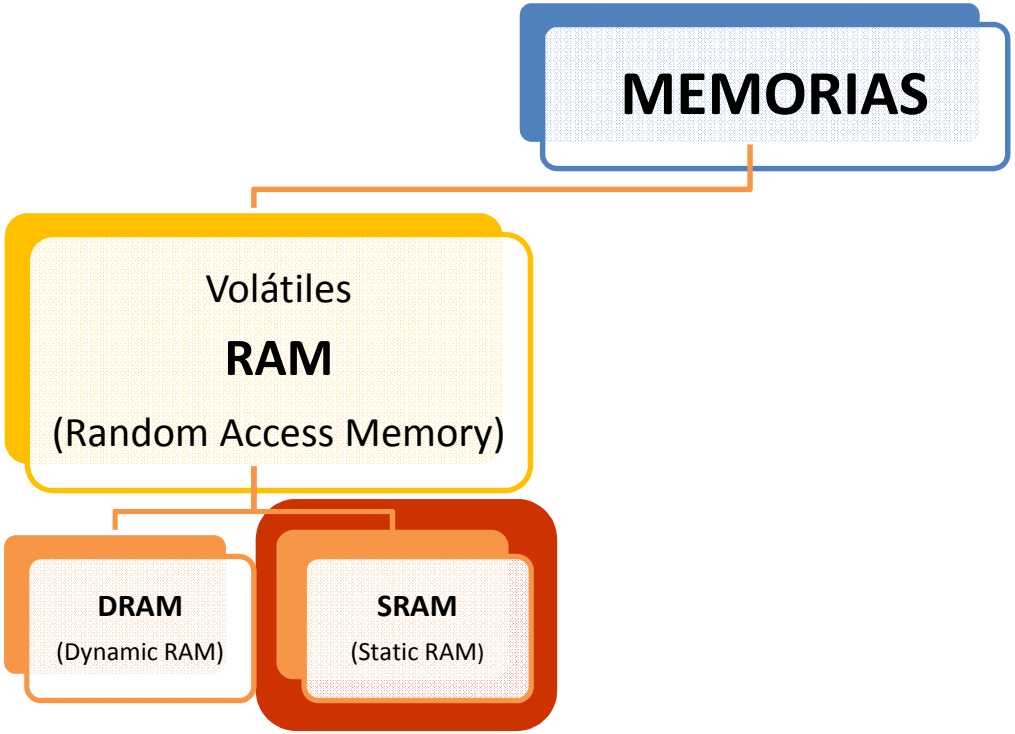


512MB DIMM = 8 x 64MB chips

Each 64MB chip =
32M x 16bit = 32 x 2^{20} x 16bit =
536,870,912bits
2 Memory Banks, with 8192 rows and 2048 columns

For example: IS42S16400J-7TL: DRAM 64M (4Mx16) 143MHz SDR

SDRAM Generation
- SDR (Single Data Rate)
- DDR (Double Data Rate)
- DDR2 (Double Data Rate type2)
- DDR3 (Double Data Rate type3)
- …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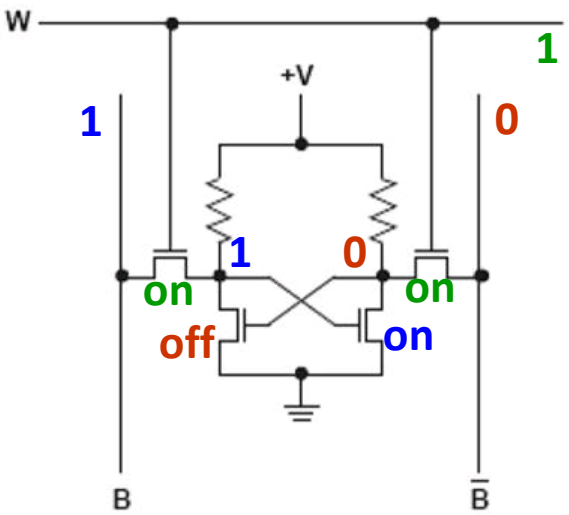
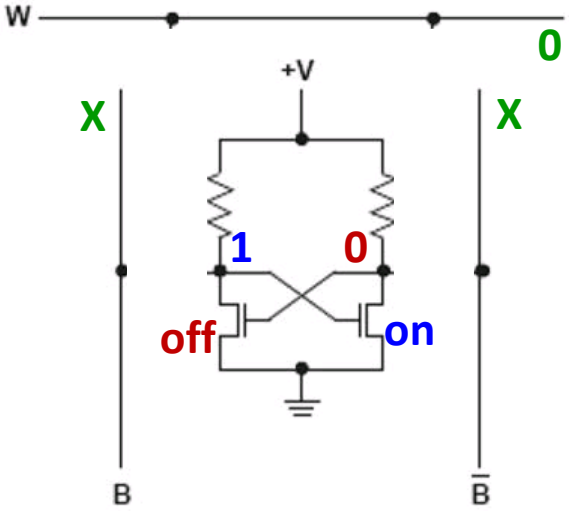
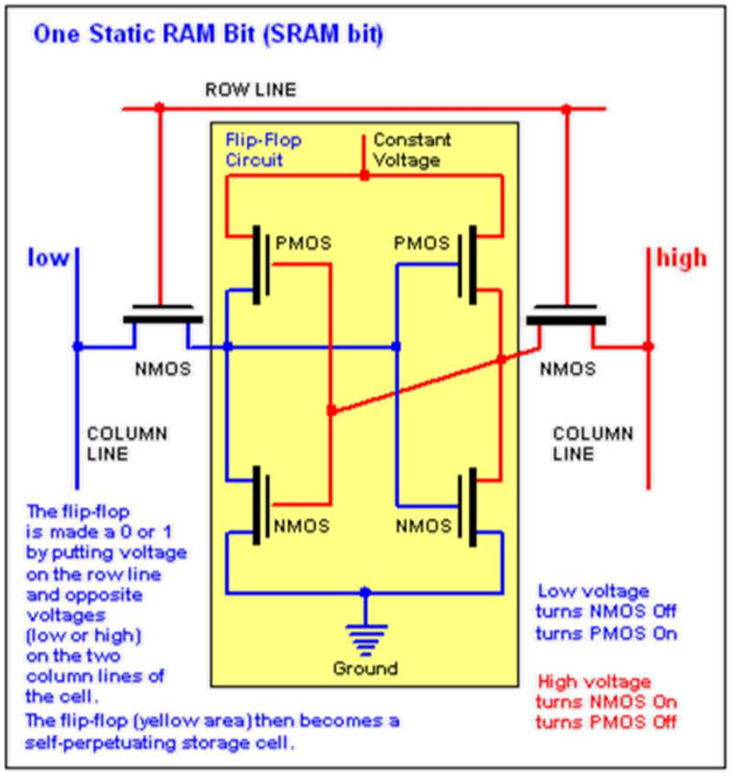






Fuente: Computer Desktop Encyclopedia. The Computer Language Co. Inc.

SRAM:

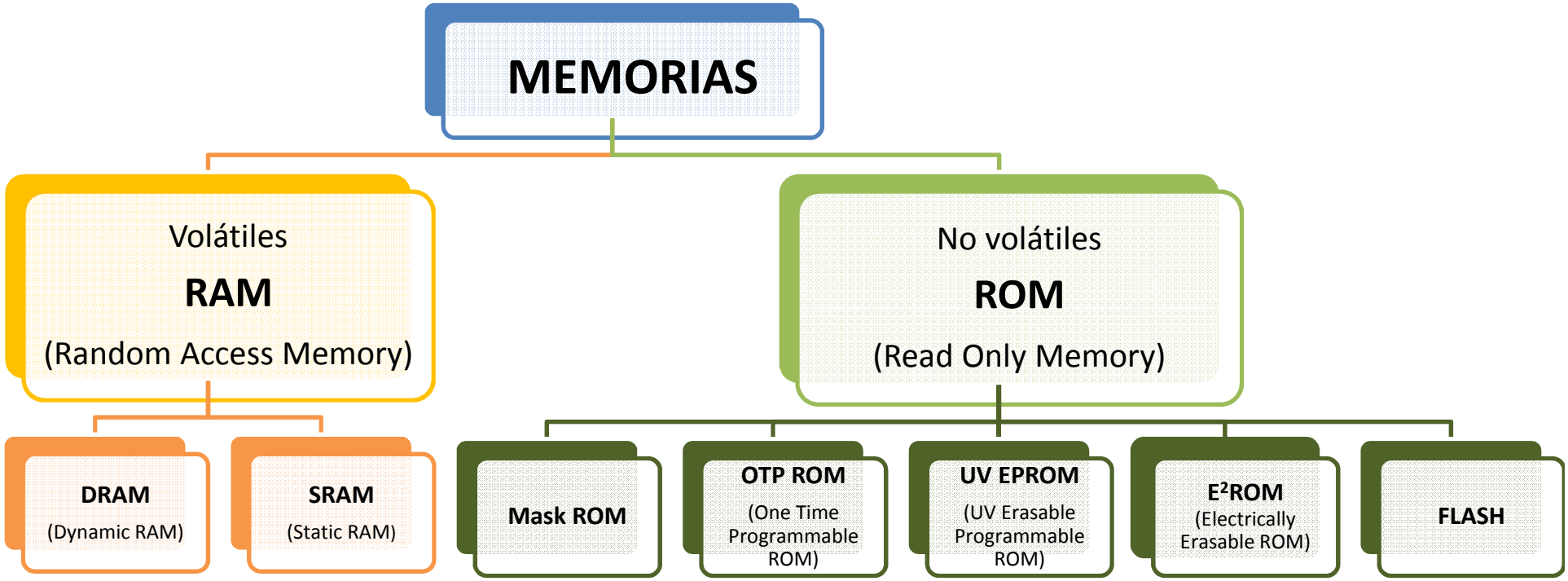
4-6 Transistores / bit

Menos integración de datos que DRAM

Precio/bit mayor que DRAM

NO es necesario el refresco de datos

Más rápida que DRAM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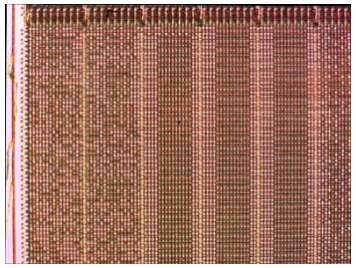
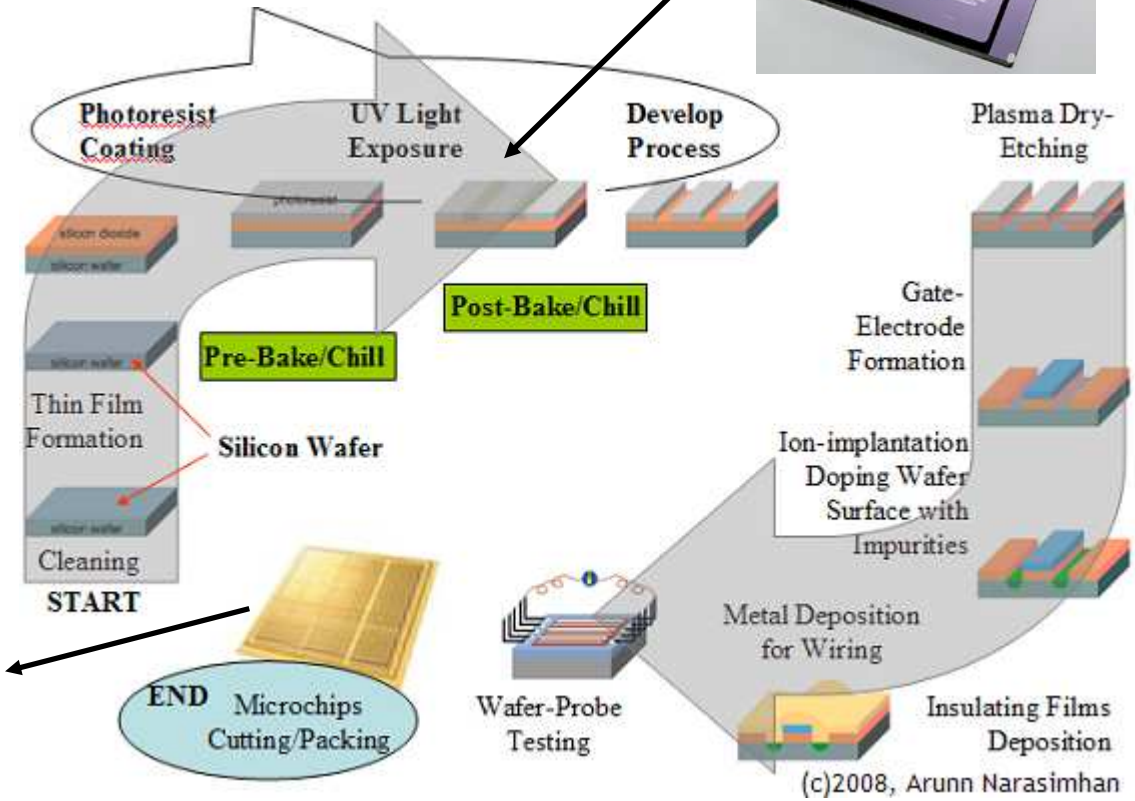
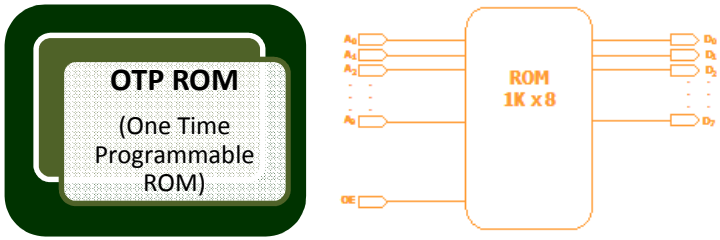
Mask ROM

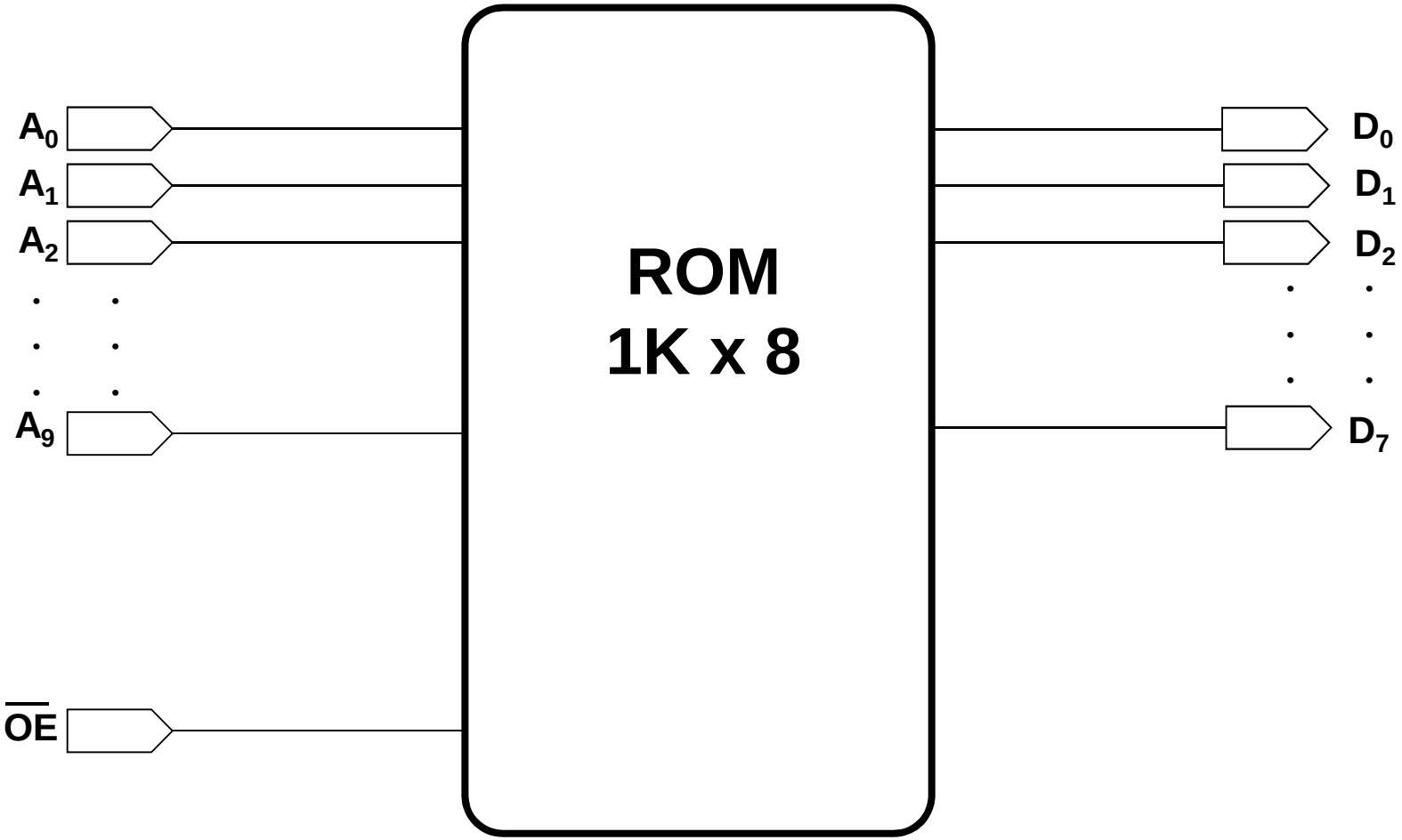
http://youtu.be/4Q_n4vdyZzc

Semiconductores:
Proceso fabricación
FOTOLITOGRAFIA



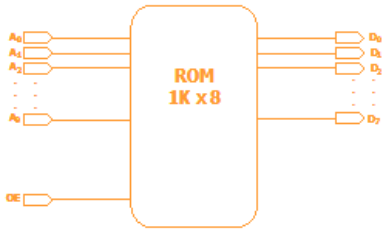


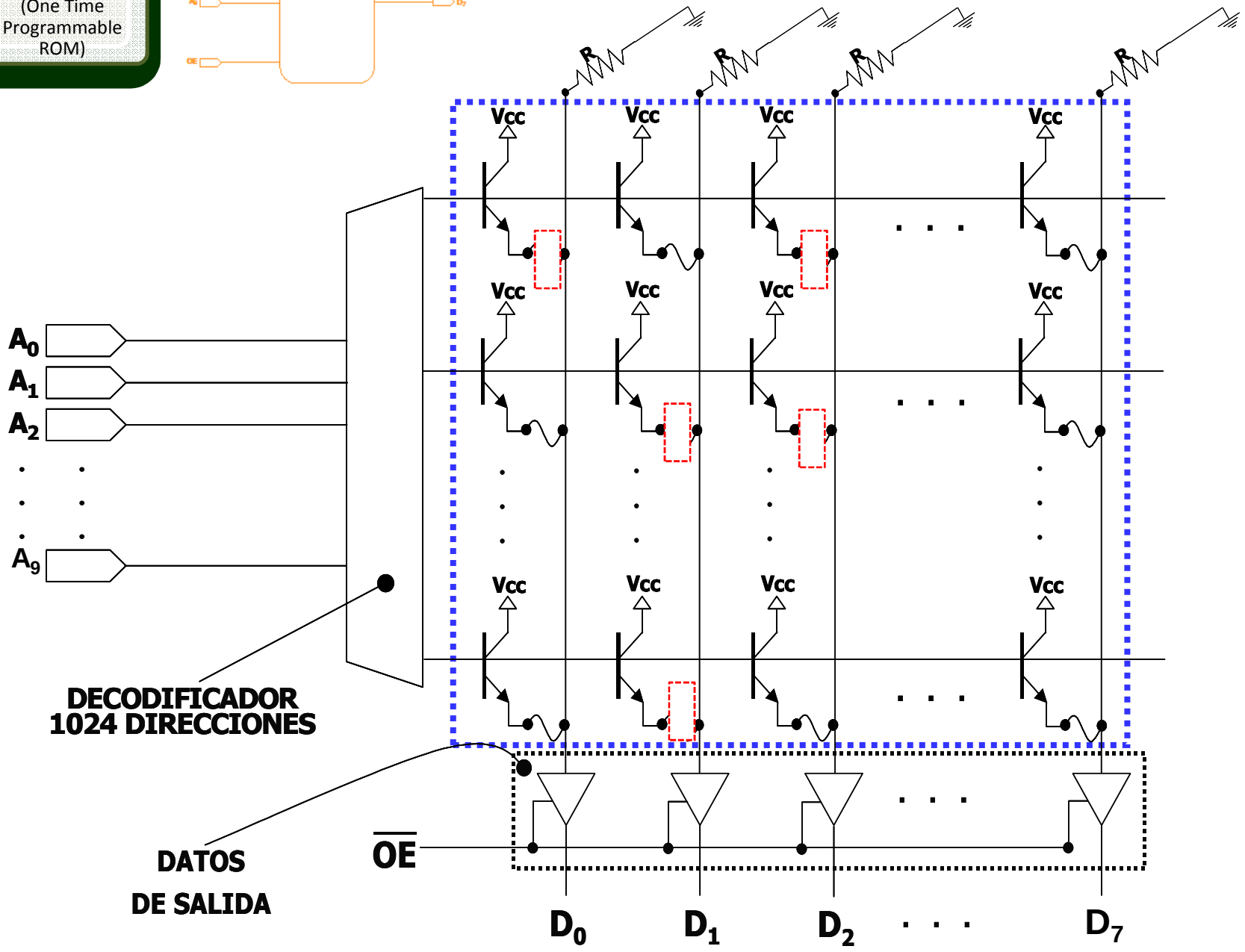

OTP ROM
(One Time Programmable ROM)
ROM
1K x 8


A0
A1
A2
A9
OE
ROM
1K x 8
D0
D1
D2
D7

OTP ROM

(One Time Programmable ROM)





http://youtu.be/4Q_n4vdyZzc

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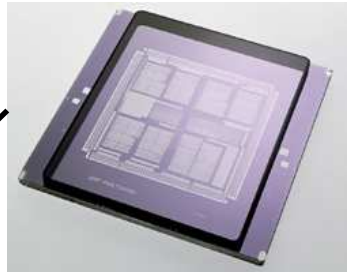
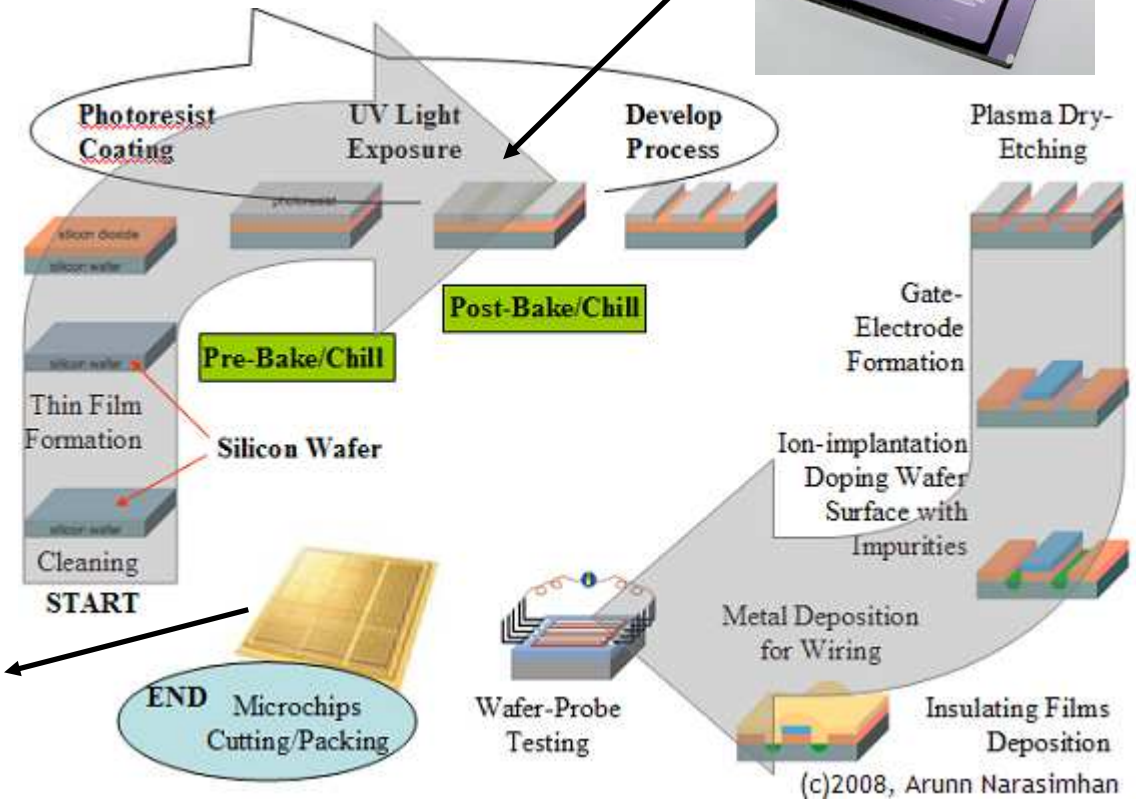
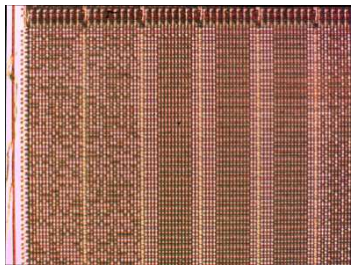
Proceso fabricación
FOTOLITOGRAFIA

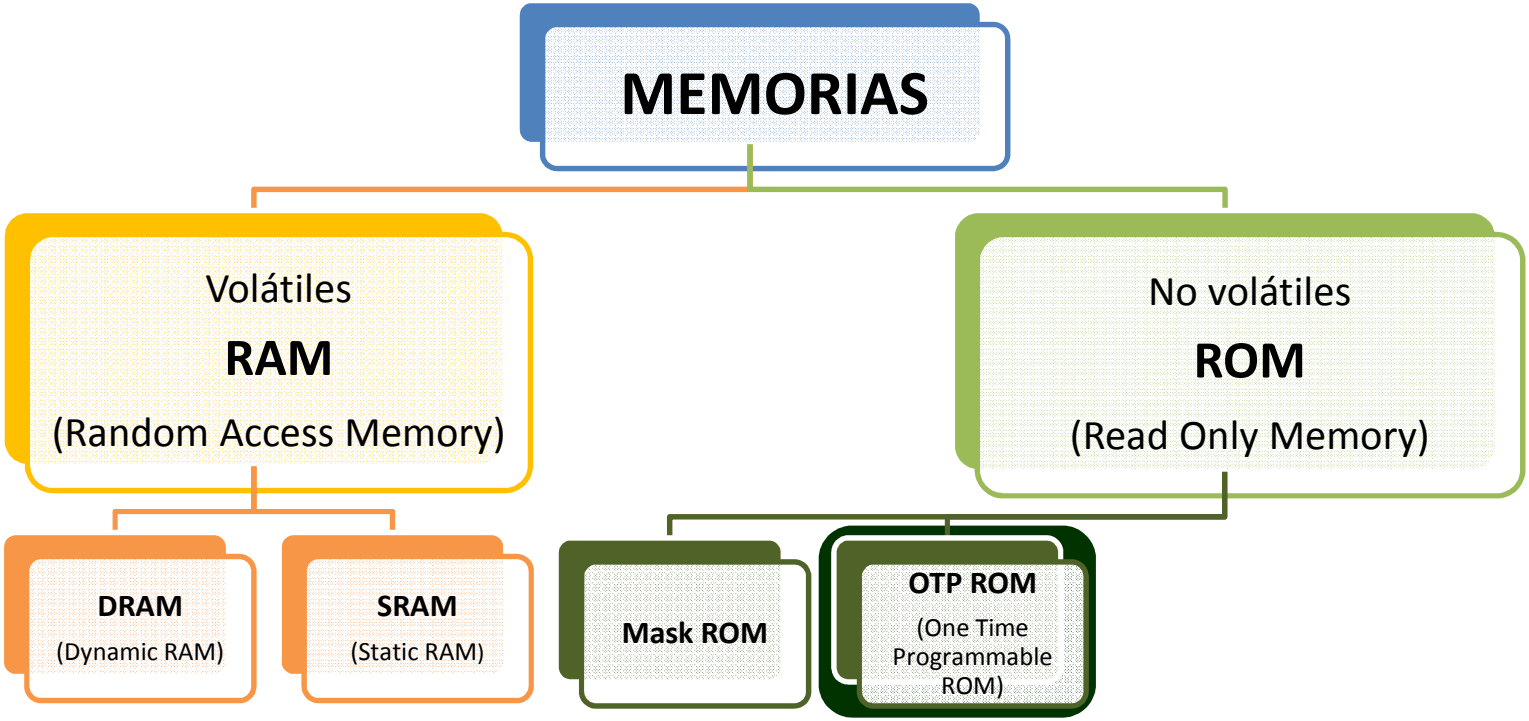






Contenidos ya programados por el fabricante
Menor costo por bit (es la memoria semiconductora más compacta)
Se utiliza en producción final
Ninguna flexibilidad: un error en el diseño provoca el reemplazo de la Mask ROM

Los microprocesadores suelen utilizar una Mask ROM integrada para almacenar su micro-código, también para almacenar el firmware o el “cargador de arranque” o “gestor de arranque” (bootloader).



OTP ROM:

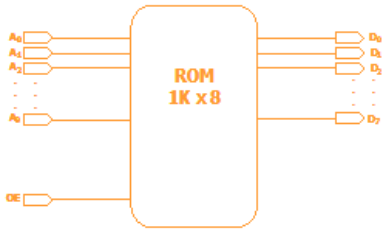
Programables una única vez

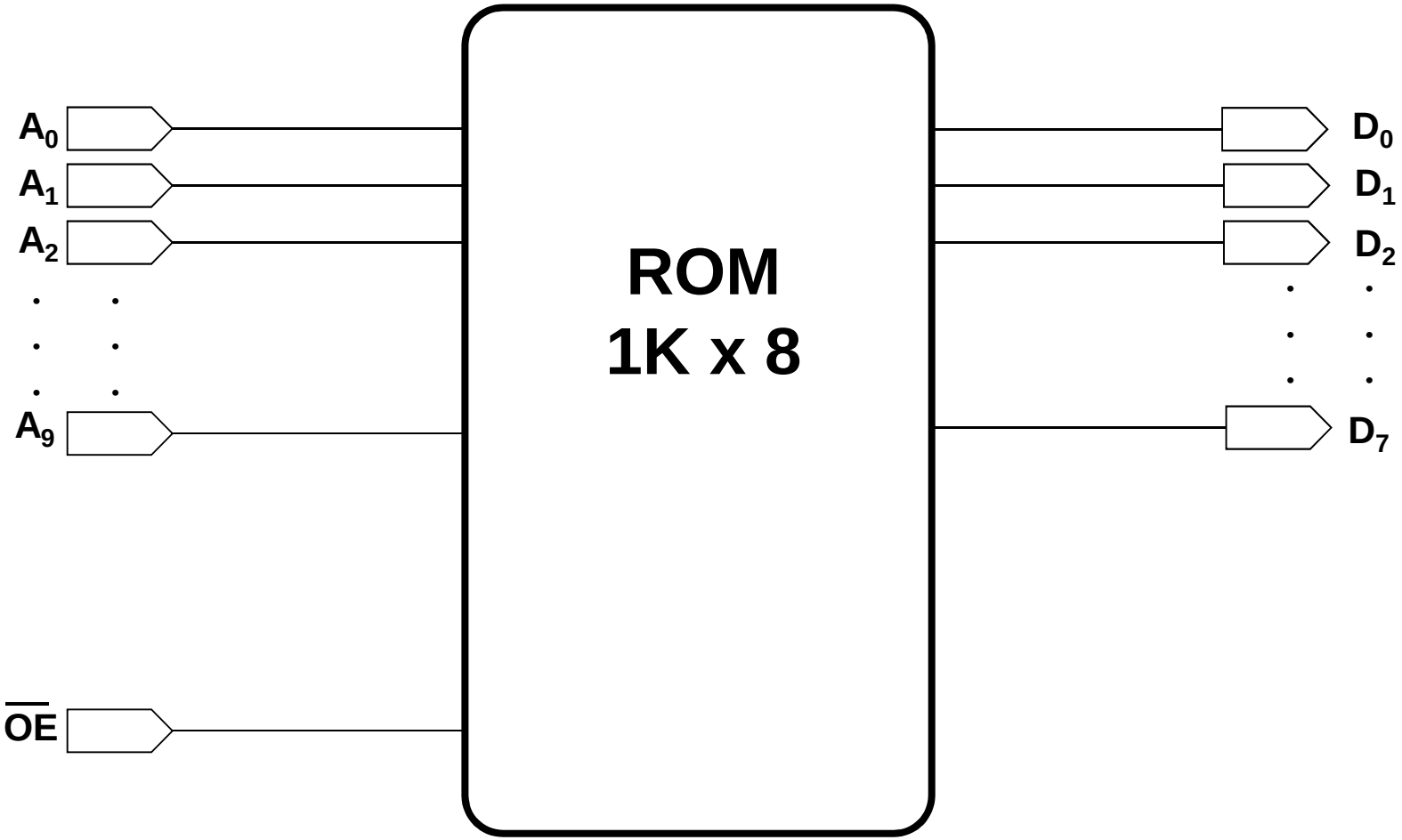
Los contenidos pueden ser programados en el sistema (utilizando un programador especial)

Permite a las compañías configurar los equipos de manera personalizada a bajo coste

OTP ROM

(One Time Programmable ROM)





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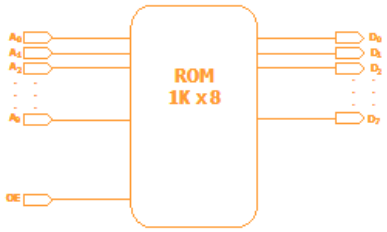

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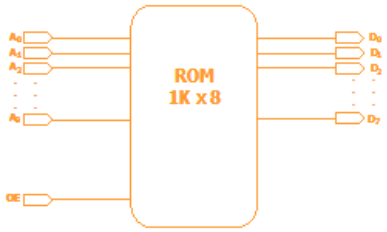

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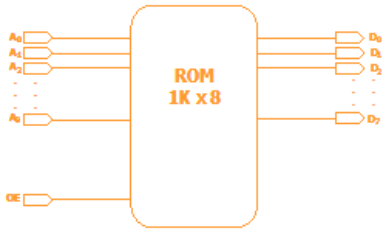

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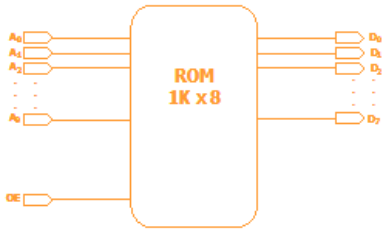

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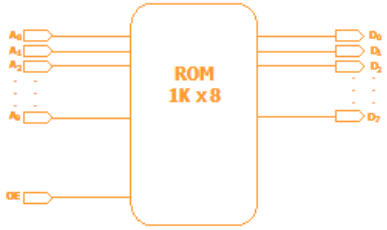

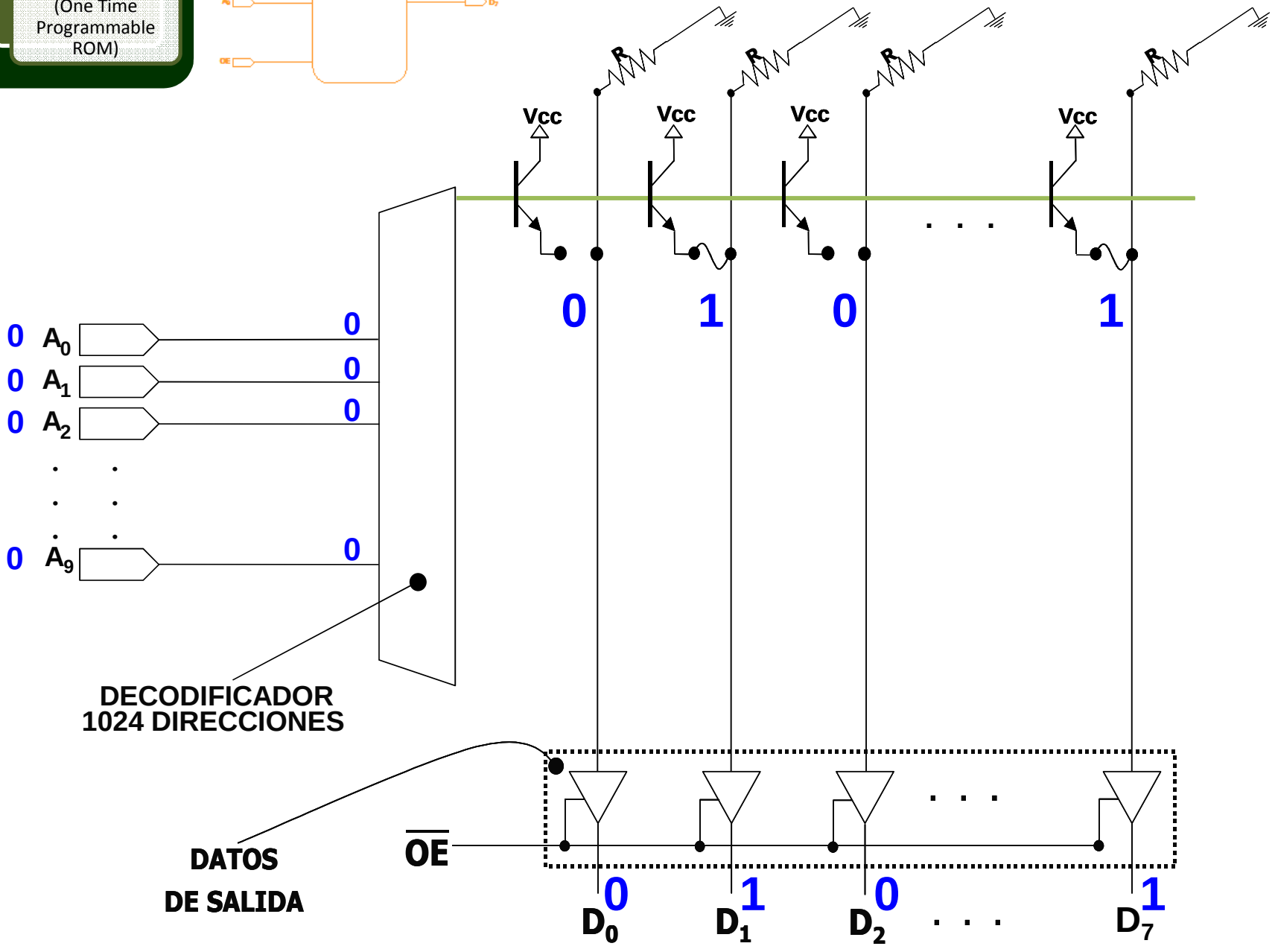

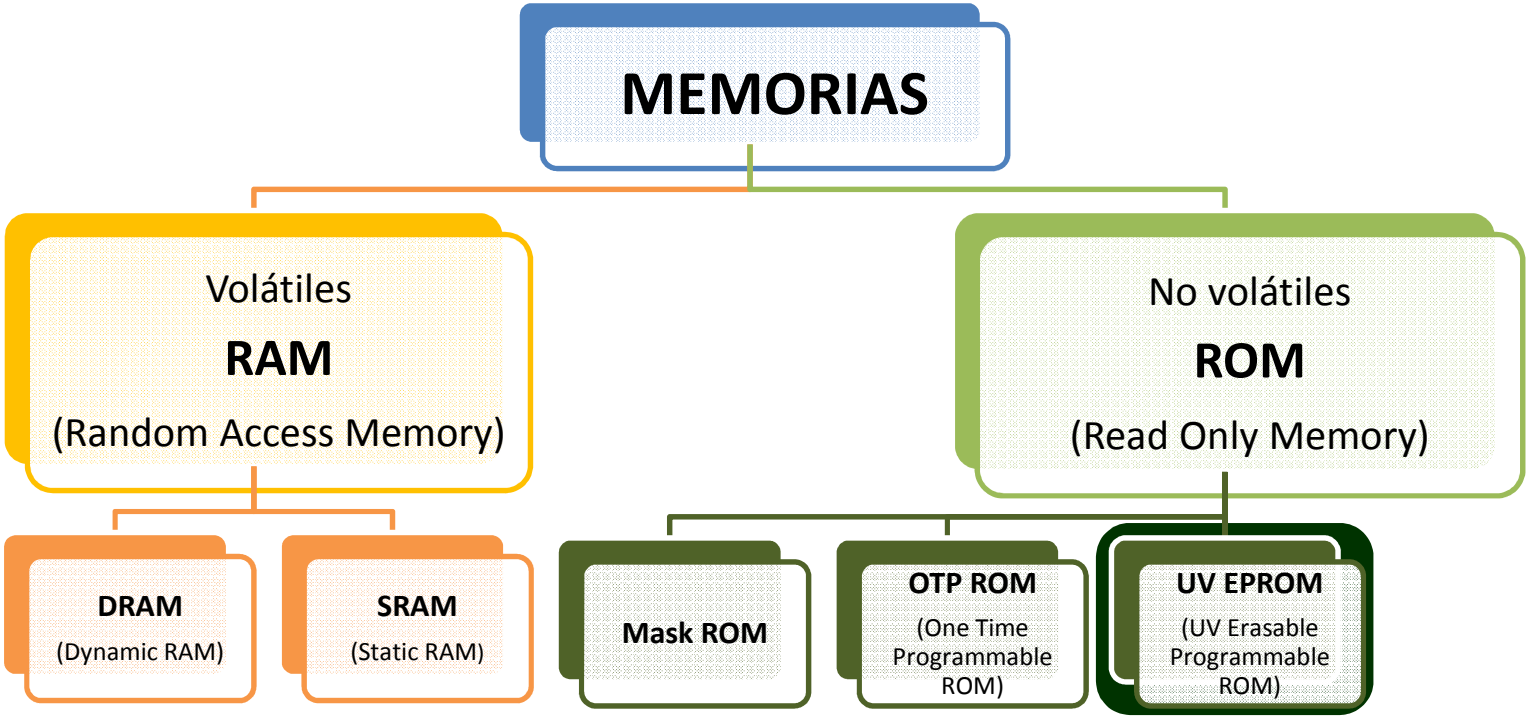
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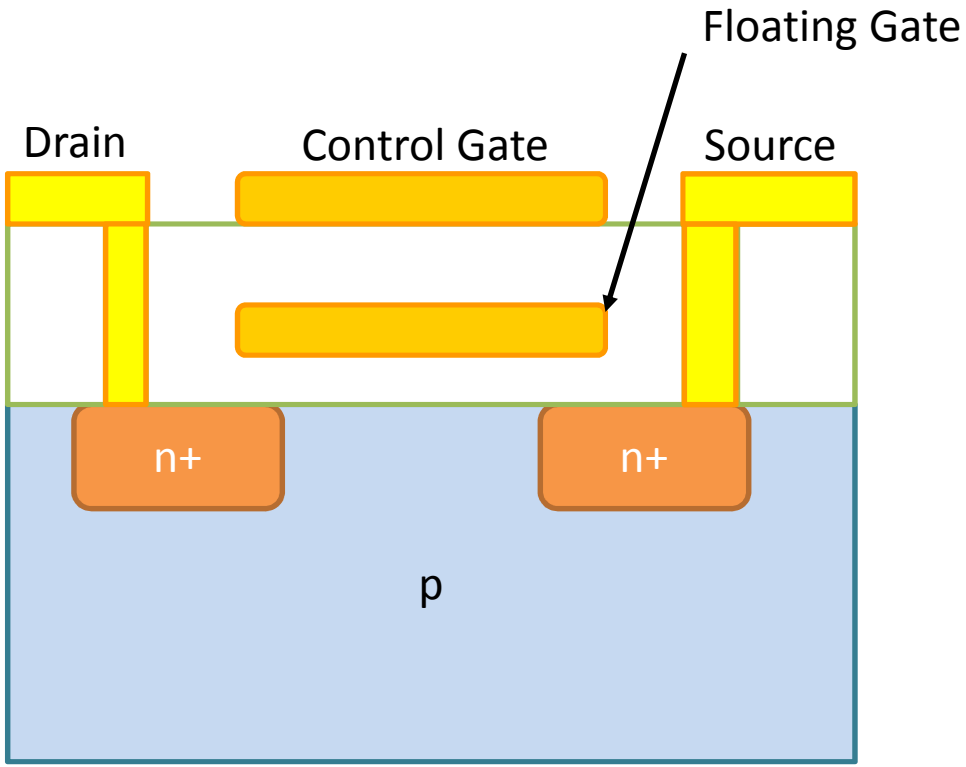


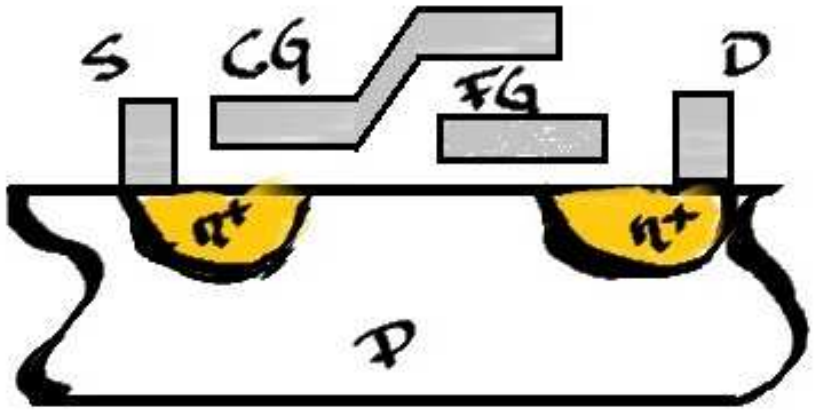
Similar a las Mask ROMs (en cuanto a su estructura matricial) pero en este caso, la existencia o no de un contacto eléctrico es programmable mediante un transistor especial

FLOATING GATE MOSFET

La programación de una EPROM se realiza mediante el fenómeno de "hot carrier injection"

UV EPROM

(UV Erasable Programmable ROM)



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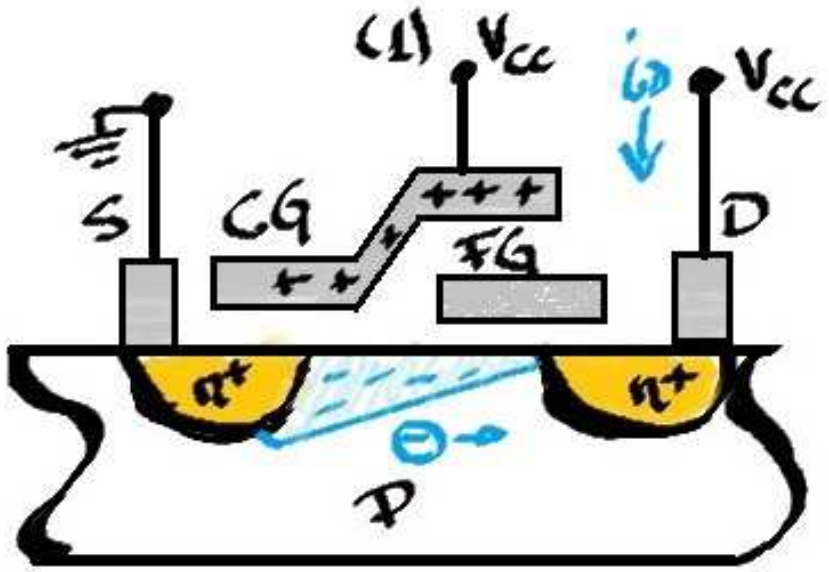
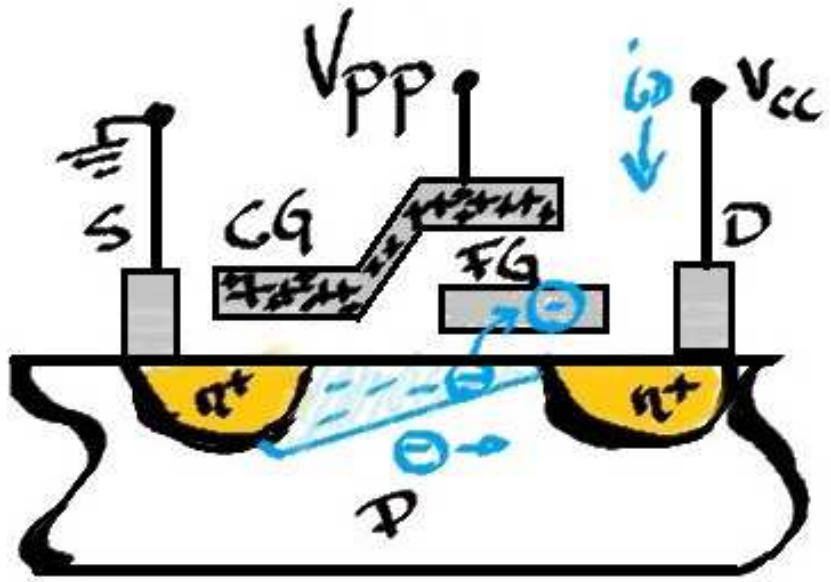


FLOATING GATE MOSFET

READ when FG is uncharged

La programación de una EPROM se realiza mediante el fenómeno de "hot carrier injection"



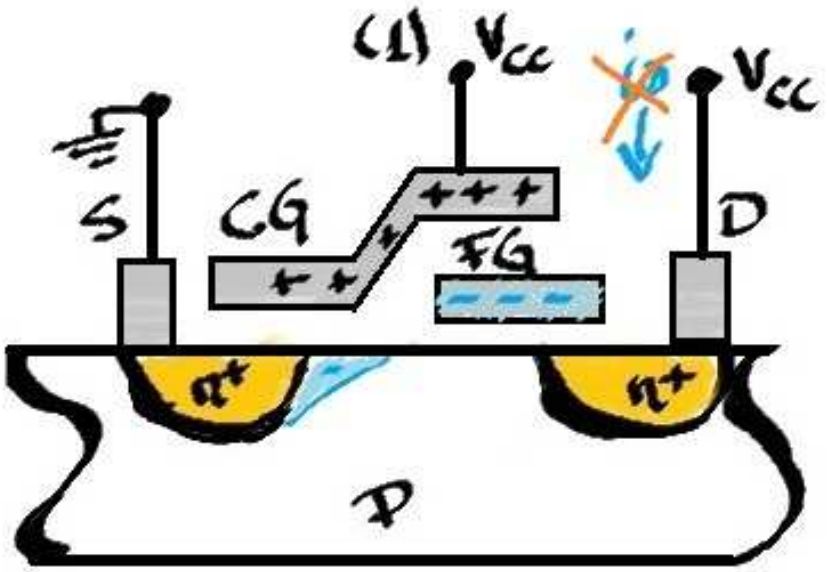
FLOATING GATE MOSFET

WRITE

La programación de una EPROM se realiza mediante el fenómeno de "hot carrier injection"

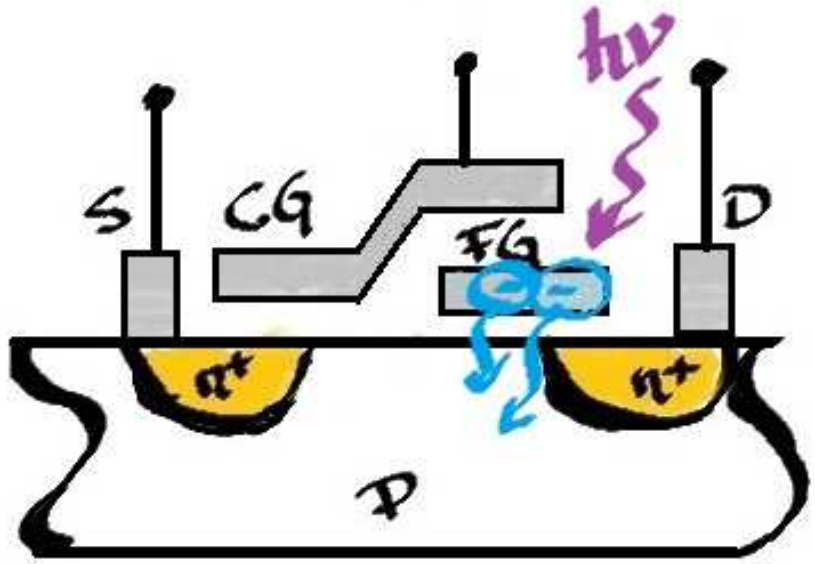
UV EPROM

(UV Erasable Programmable ROM)



FLOATING GATE MOSFET

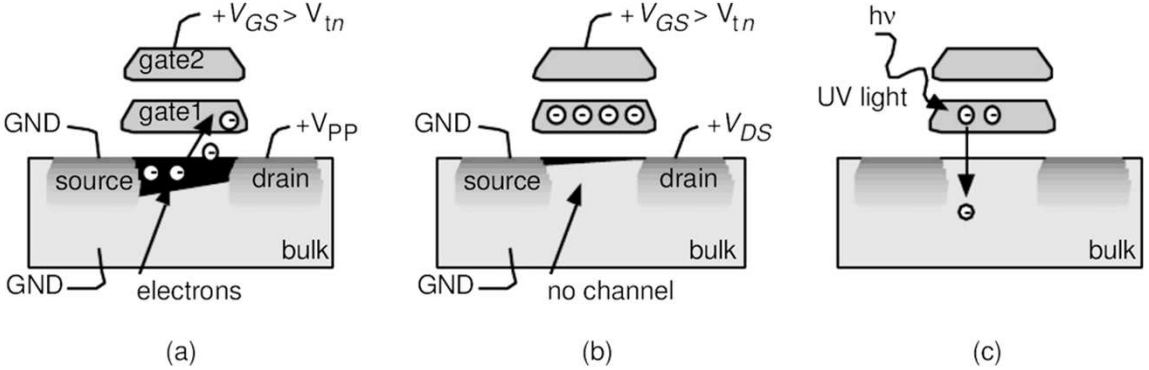
READ when FG is charged



FLOATING GATE MOSFET

ERASING

UV EPROM
(UV Erasable Programmable ROM)



An EPROM transistor. (a) With a high (> 12 V) programming voltage, V_{PP} , applied to the drain, electrons gain enough energy to "jump" onto the floating gate (gate1). (b) Electrons stuck on gate1 raise the threshold voltage so that the transistor is always off for normal operating voltages. (c) Ultraviolet light provides enough energy for the electrons stuck on gate1 to "jump" back to the bulk, allowing the transistor to operate normally.

Fuente: Application-Specific Integrated Circuits Copyright © 1997 by Addison Wesley Longman, Inc.

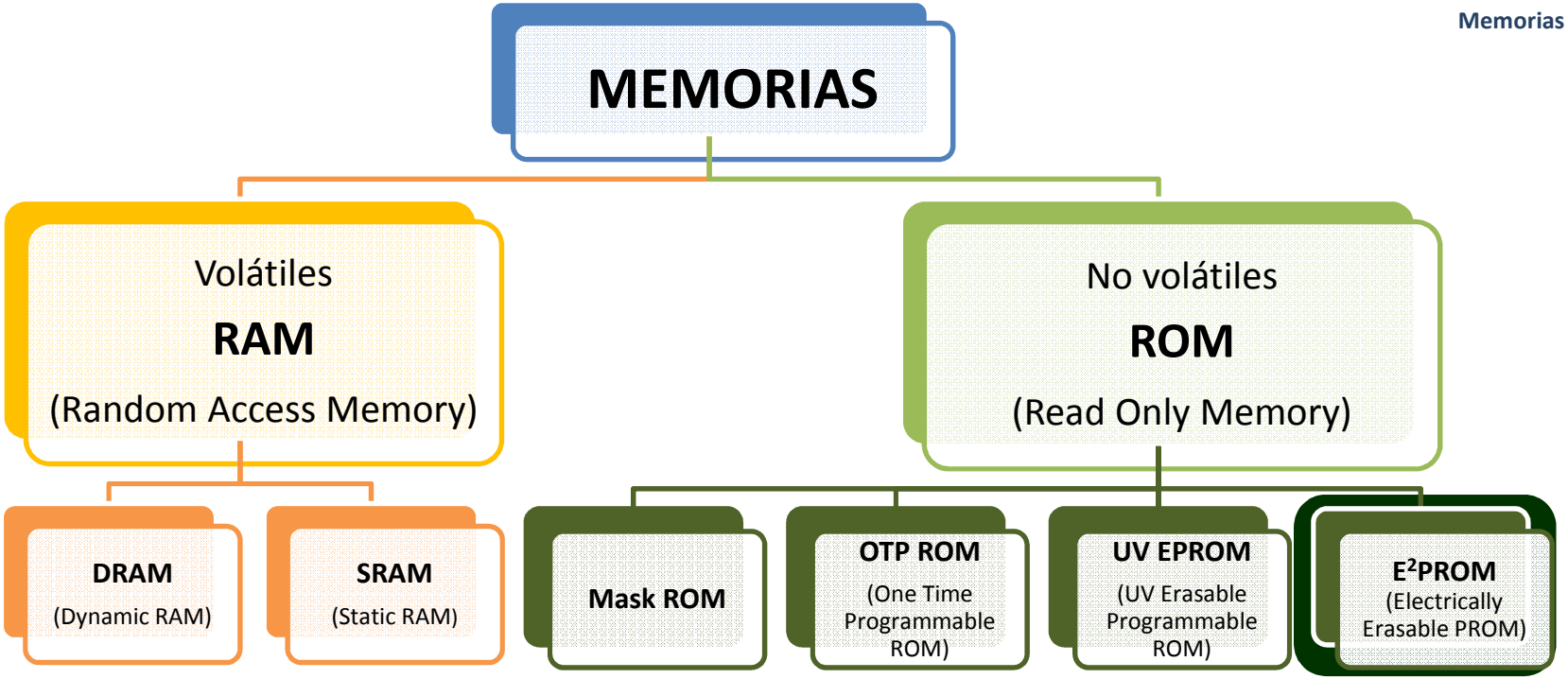
La programación de una EPROM se realiza mediante el fenómeno de "hot carrier injection"

UV EPROM:

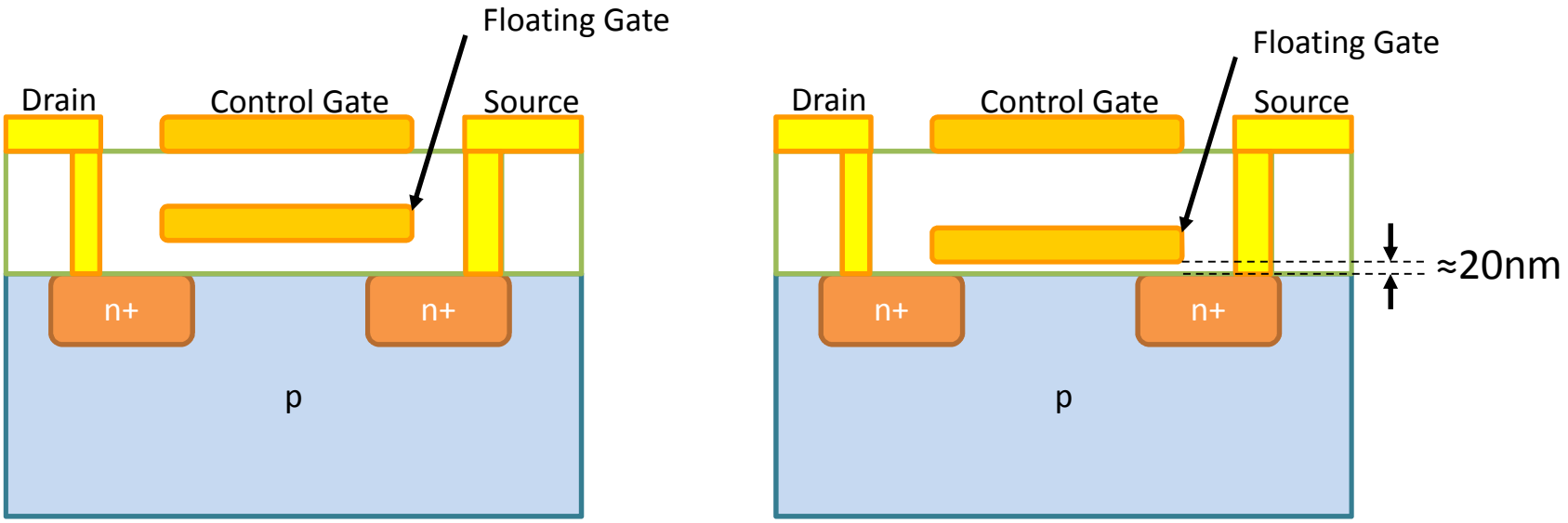
Programables eléctricamente en programador especial (Vpp ≈ 12 V)

Se pueden borrar mediante luz UV en borrador especial

Reprogramables, pero es necesario sacarlas de su circuito para borrar y reprogramar

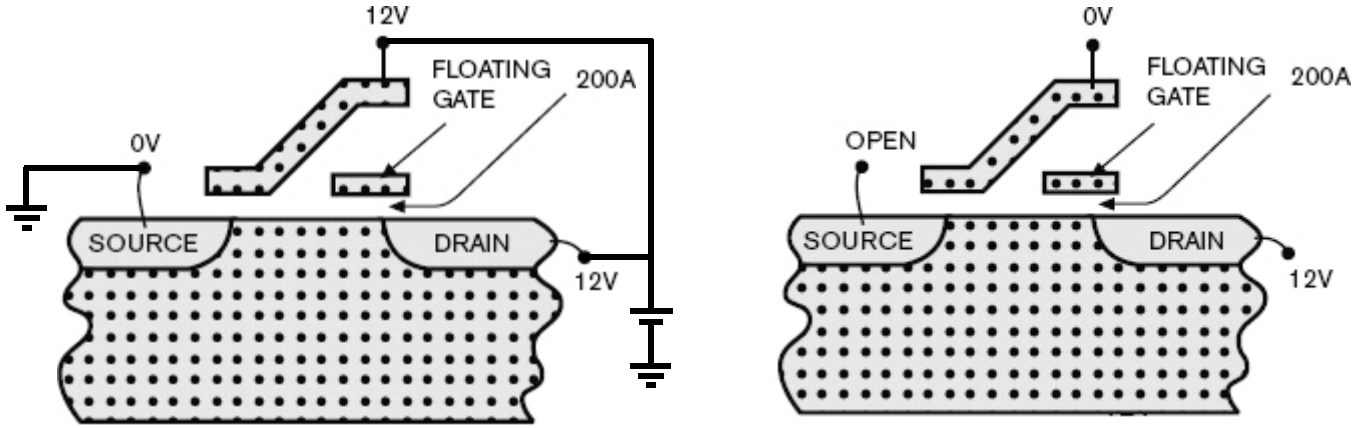

MEMORIAS
Volátiles
RAM
(Random Access Memory)
No volátiles
ROM
(Read Only Memory)
DRAM
(Dynamic RAM)
SRAM
(Static RAM)
Mask ROM
OTP ROM
(One Time Programmable ROM)
UV EPROM
(UV Erasable Programmable ROM)
E2PROM
(Electrically Erasable PROM)

E²ROM
(Electrically Erasable ROM)



EEPROM ó EEROM ó E²ROM:
¿Es posible modificar la estructura de las UV-PROM para que no sea necesario el borrado mediante luz UV?
Programables eléctricamente en programador especial (Vpp ≈ 12 V)
Se pueden borrar mediante el mismo programador
Reprogramables

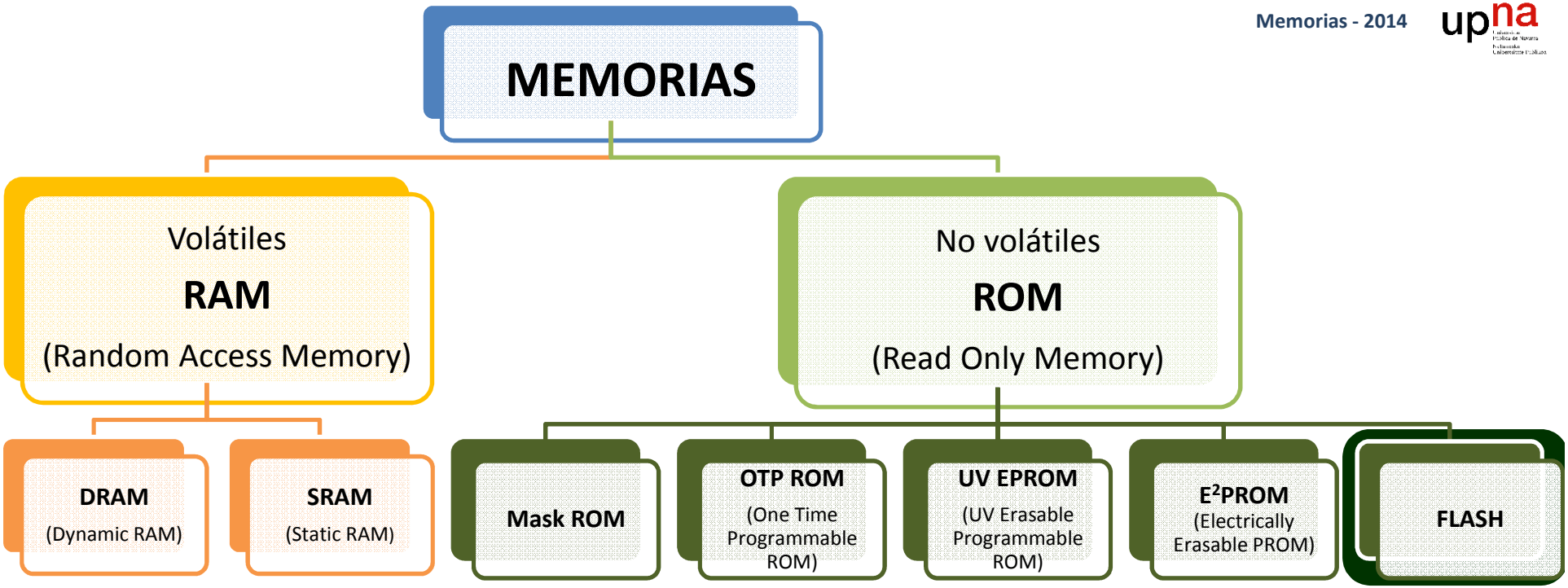
E²ROM
(Electrically Erasable ROM)



Fuente: "Analog floating-gate technology comes into its own" by Paul Rako -- EDN Europe, 01 Feb 2010

- **La programación de una E²ROM se produce mediante al fenómeno de "hot carrier Injection"**
- **El borrado de una E2PROM se produce mediante el fenómeno de "field electron emission" (más conocido como "Fowler–Nordheim tunneling")**

EEPROM ó EEROM ó E²ROM:
Programables eléctricamente en programador especial (Vpp ≈ 12 V)
Suele ser necesario sacarlas de su placa para insertarlas en su programador
Se pueden borrar mediante el mismo programador
Reprogramables
Versiones modernas incorporan circuitos elevadores de tension "charge pumps" para obtener las tensiones de programación "on chip"



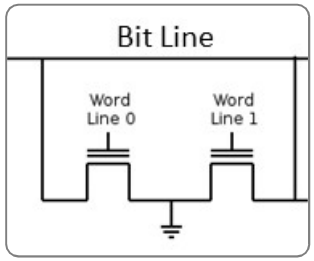
FLASH:

Técnicamente muy similares a las E^2ROM (se programan y se borran eléctricamente), aunque dependiendo de su configuración NOR Flash o NAND Flash, gestionan la memoria de forma diferente y ello repercute en la eficacia de la lectura y de la escritura.

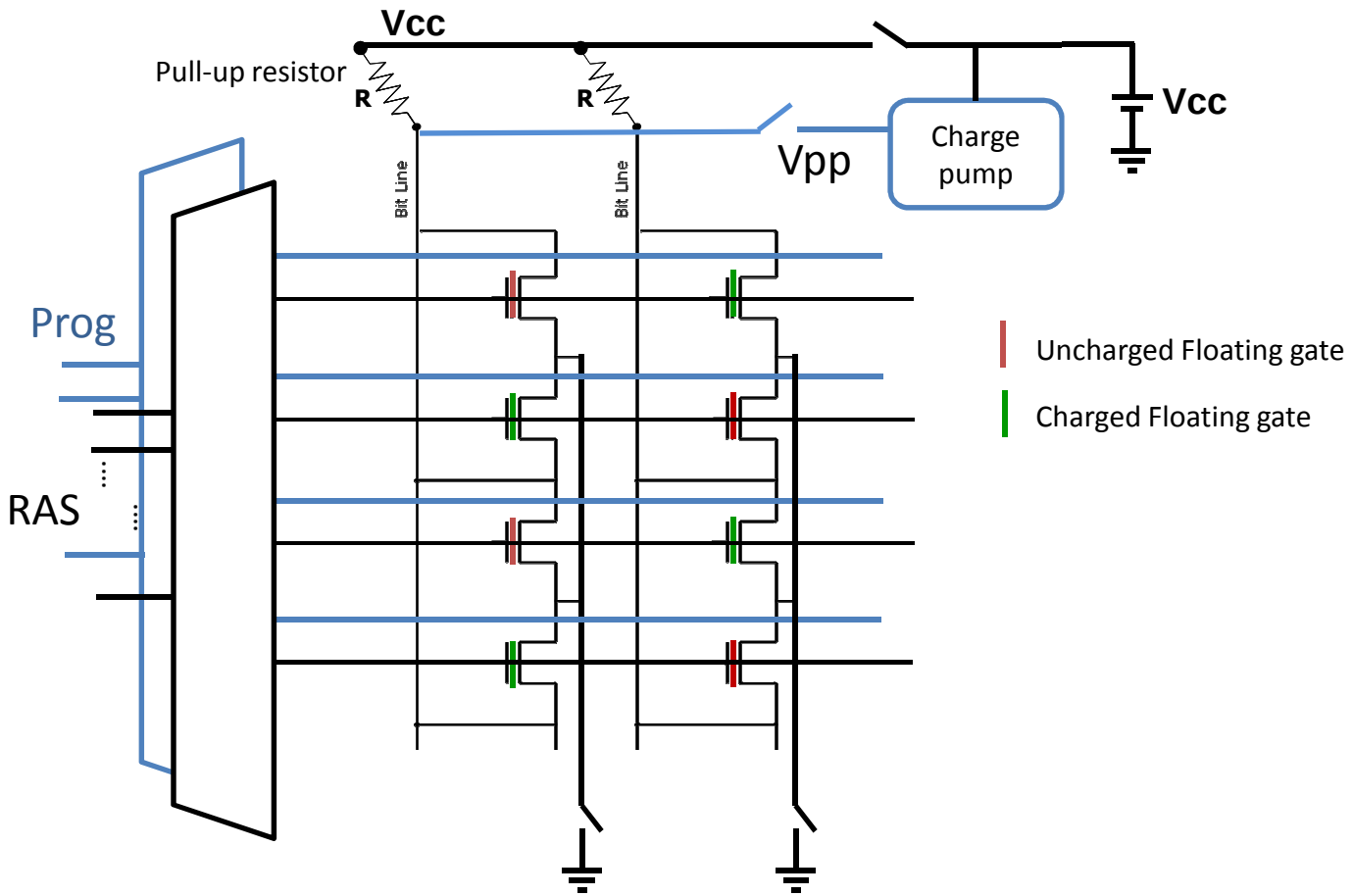
Se pueden programar en circuito sin necesidad de programador especial (Vpp ≈ 5V)

Dominantes actuales del mercado de memorias no volátiles (Ej. memorias USB)

NOR Flash



A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

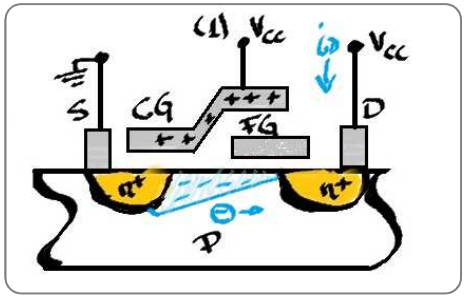


NOR FLASH:

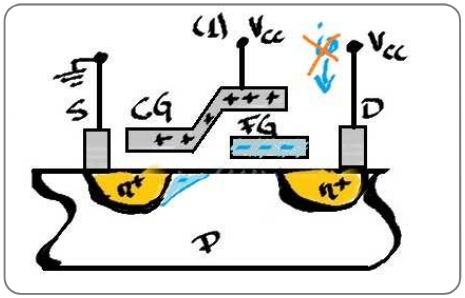
- Número limitado de Lecturas/Escrituras (Wear out)
- Rápidas. Muy parecidas al esquema tradicional de las ROMs. Random Access.
- Menor capacidad de integración. Precio bastante más elevado que las NAND
- Pueden ser borradas a nivel de palabra aunque es normal que estén divididas en bloques.
- Algunas pueden realizar operaciones de lectura mientras escriben (Read While Write)

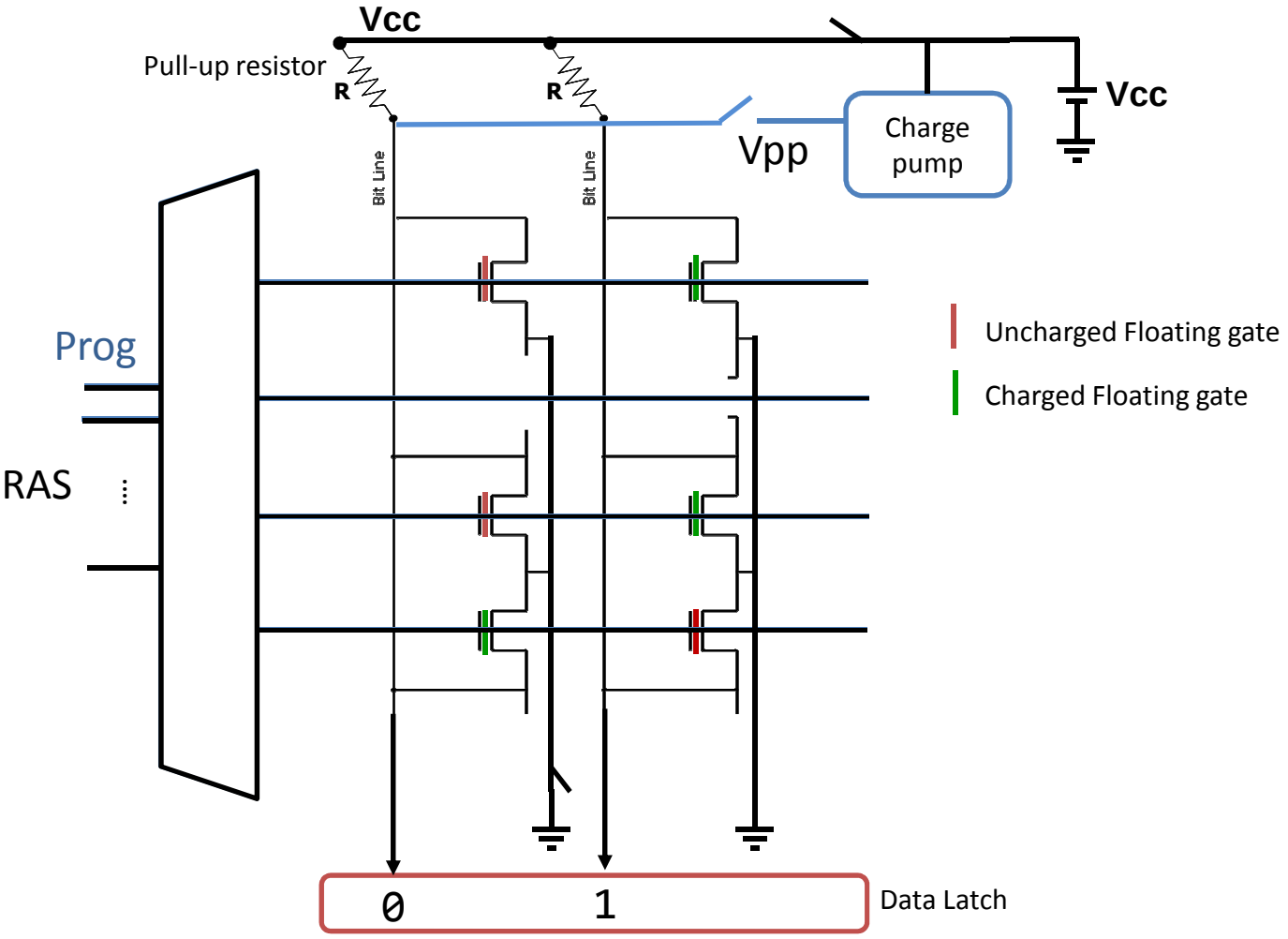
NOR Flash

Uncharged Floating gate



Charged Floating gate

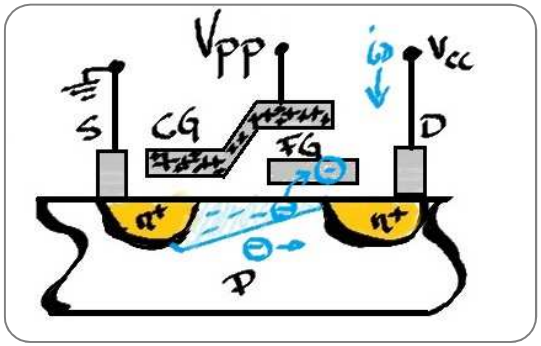


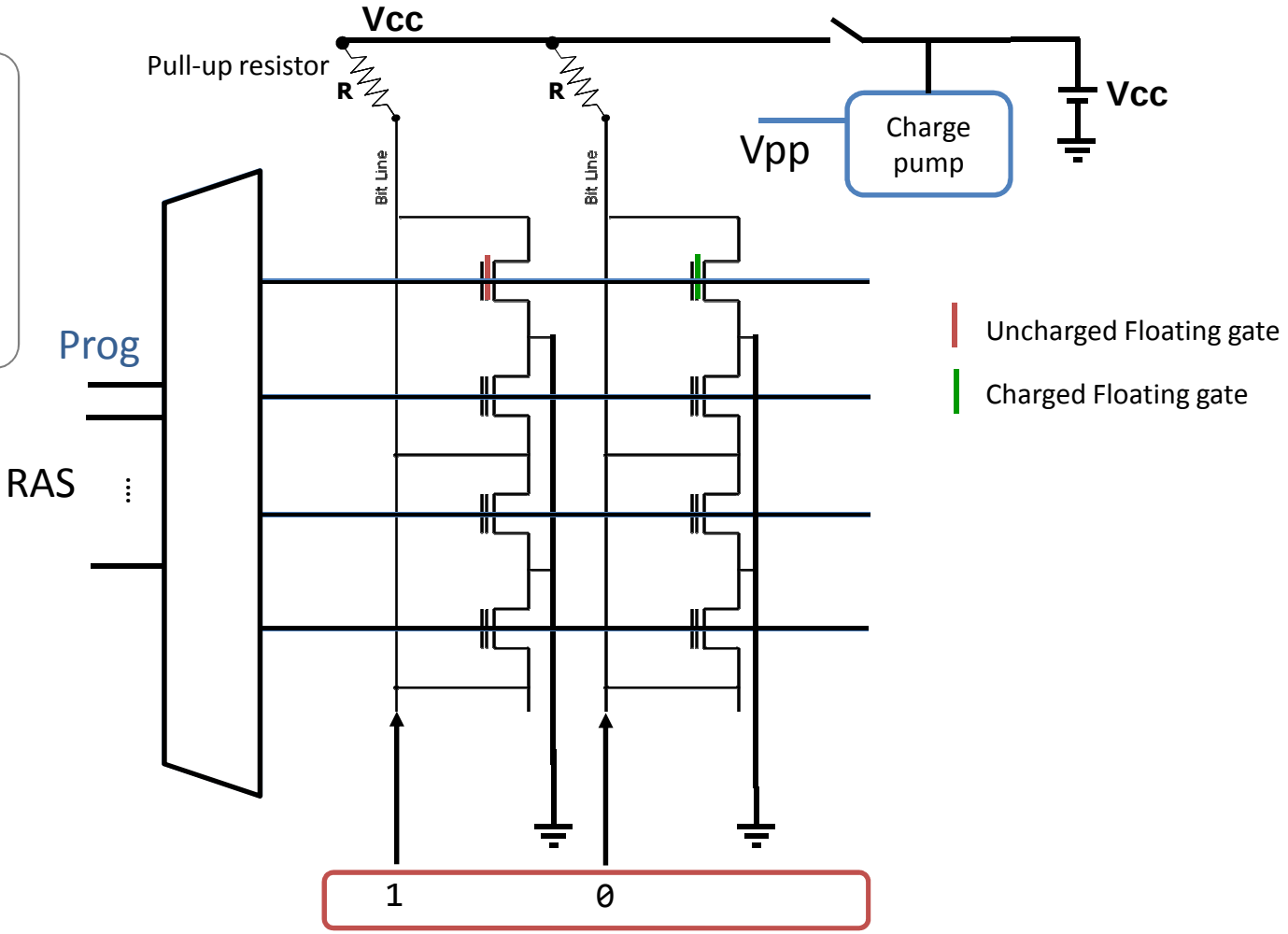


Lectura:

- Se activa la respectiva línea de palabra (RAS) a una tensión normal Vcc
- Se conectan todas las resistencias “pull up”
- Todas las fuentes se conectan a tierra
- Se leen las líneas de bit

NOR Flash

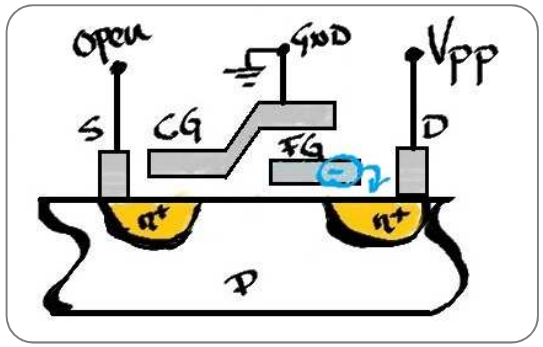


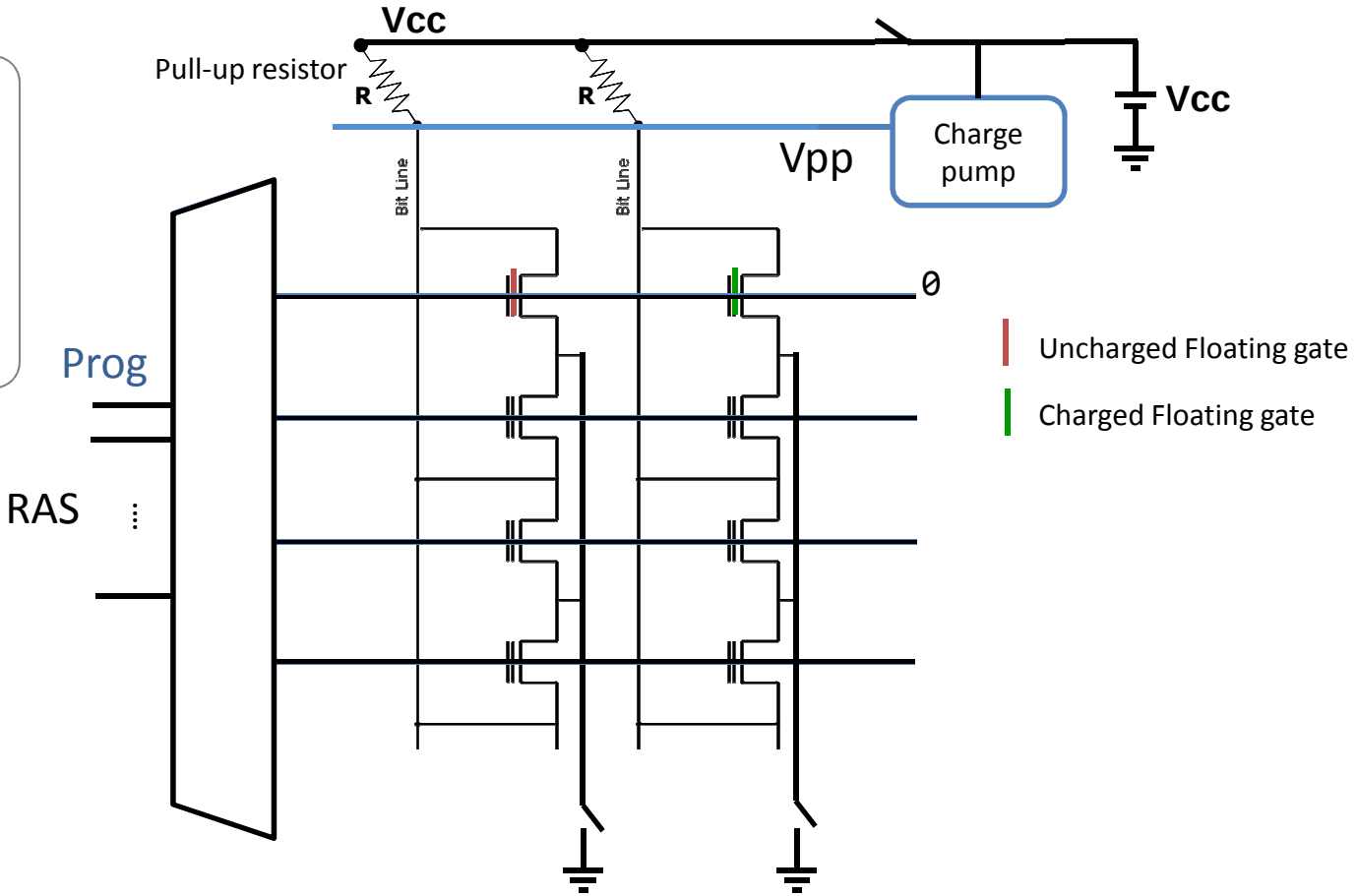


Escritura:

- Modo de programación de la palabra deseada (Activación RAS) (tensión alta Vpp)
- Se mantienen las fuentes de los transistores a tierra
- Se desconectan las resistencias Pull Up
- Se conectan las líneas de bit al registro de datos

NOR Flash

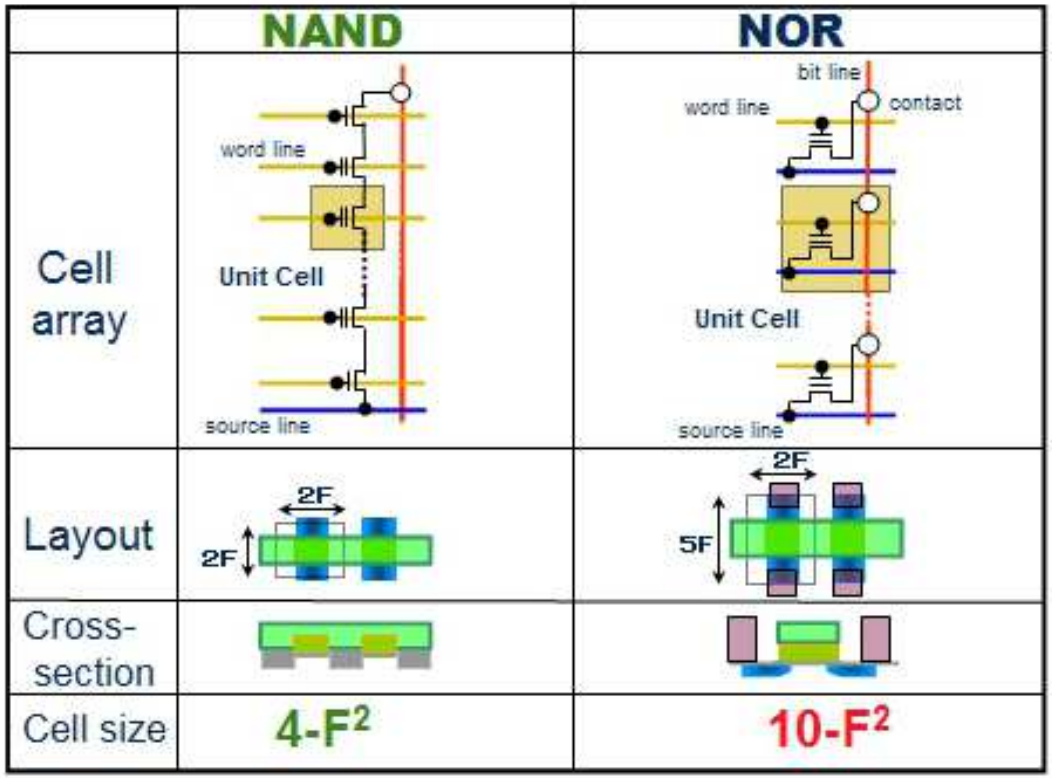




Borrado:

- Fuentes de los transistores abiertas (modo alta impedancia)
- Se pone a 0 (línea de palabra) la puerta de control de la fila que se desea borrar
- Se desconectan las resistencias Pull Up
- Se conectan las líneas de bit a la tensión de programación (tensión alta Vpp)

NAND Flash



Fuente: Digi-Key corp. *http://dkc1.digikey.com/ie/en/tod/Micron/NANDFlash_noaudio/NANDFlash_noaudio.html*

NAND FLASH:

Número limitado de Lecturas/Escrituras (wear out)

Se pueden programar a nivel de palabra, pero no pueden borrar un único byte sino en bloques (pages)

Mayor capacidad de integración, Precio mucho más reducido

Bastante más lentas que las NOR Flash

Dominantes actuales del mercado de memorias no volátiles (Ej. memorias USB)

NAND Flash

Basic NAND/NOR Comparison

NAND

- Advantages:
  - Fast writes
  - Fast erases
- Disadvantages:
  - Slow random access
  - Byte writes difficult
- Applications:
  - File (disk) applications
  - Voice, data, video recorder
  - Any large sequential data

NOR

- Advantages:
  - Random access
  - Byte writes possible
- Disadvantages:
  - Slow writes
  - Slow erases
- Applications:
  - Replacement of EPROM
  - Execute directly from nonvolatile memory

Characteristic	NAND Flash MT29F2G08	NOR (Q-Flash) MT28F128J3
Random access read	25µs (first byte) 0.03µs each for remaining 2111 bytes	0.12µs
Sustained read speed (sector basis)	23 MB/s (x8) or 37 MB/s (x16)	20.5 MB/s (x8) or 41 MB/s (x16)
Random write speed	~300µs/2,112 bytes	180µs/32 bytes
Sustained write speed (sector basis)	5 MB/s	0.178 MB/s
Erase block size	128KB	128KB
Erase time per block (typ)	2ms	750ms

Fuente: Digi-Key corp. *http://dkc1.digikey.com/ie/en/tod/Micron/NANDFlash_noaudio/NANDFlash_noaudio.html*

¿Qué tipo de sistema de almacenamiento es más rápido?

TIPO DE ALMACENAMIENTO	RANKING POR RAPIDEZ DE LECTURA	Tiempo de acceso equivalente
Disco duro HDD		
Blu Ray		
DRAM		
FLASH		
SRAM		

¿Qué tipo de sistema de almacenamiento es más rápido?

TIPO DE ALMACENAMIENTO	RANKING POR RAPIDEZ DE LECTURA	Tiempo de acceso equivalente
Disco duro HDD	4º	< 10 ms
Blu Ray	5º	180 ms
DRAM	2º	> 20 ns
FLASH	3º	≈25 ns
SRAM	1º	< 10 ns
SRAM L2 Cache		7ns
SRAM L1 Cache		0,5ns

EJEMPLOS DE MEMORIAS

M27C512

512 Kbit (64Kb x8) UV EPROM and OTP EPROM

- 5V ± 10% SUPPLY VOLTAGE in READ OPERATION
- ACCESS TIME: 45ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V ± 0.25V
- PROGRAMMING TIMES of AROUND 6sec.
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code: 3Dh

DESCRIPTION

The M27C512 is a 512 Kbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for applications where fast turn-around and pattern experimentation are important requirements and is organized as 65,536 by 8 bits.

The FDIP28W (window ceramic frit-seal package) has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C512 is offered in PDIP28, PLCC32 and TSOP28 (8 x 13.4 mm) packages.

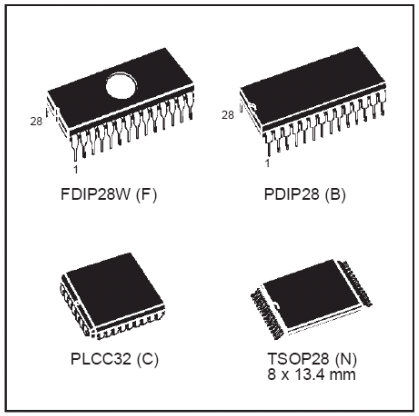
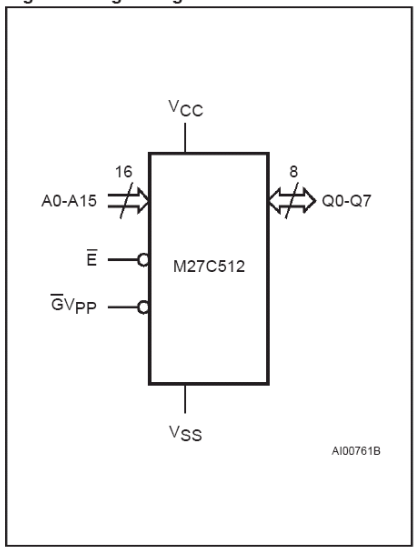


Figure 1. Logic Diagram



M27C322

32 Mbit (2Mb x16) UV EPROM and OTP EPROM

- 5V ± 10% SUPPLY VOLTAGE in READ OPERATION
- ACCESS TIME: 80ns
- WORD-WIDE CONFIGURABLE
- 32 Mbit MASK ROM REPLACEMENT
- LOW POWER CONSUMPTION
  - Active Current 50mA at 5MHz
  - Stand-by Current 100µA
- PROGRAMMING VOLTAGE: 12V ± 0.25V
- PROGRAMMING TIME: 50µs/word
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Device Code: 0034h

DESCRIPTION

The M27C322 is a 32 Mbit EPROM offered in the UV range (ultra violet erase). It is ideally suited for microprocessor systems requiring large data or program storage. It is organised as 2 MWords of 16 bit. The pin-out is compatible with a 32 Mbit Mask ROM.

The FDIP42W (window ceramic frit-seal package) has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written rapidly to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C322 is offered in PDIP42 and SDIP42 packages.

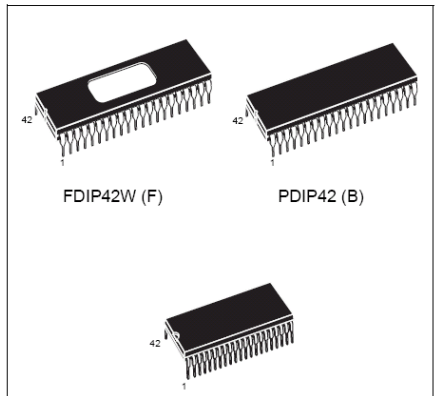
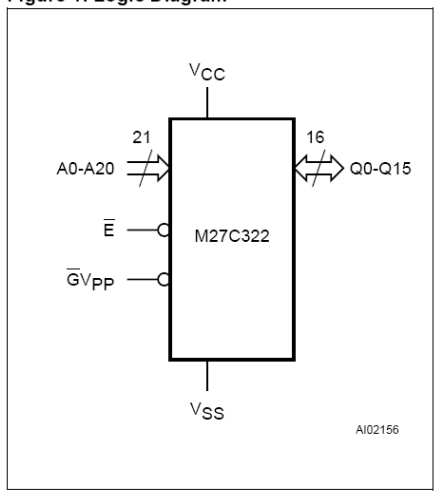


Figure 1. Logic Diagram

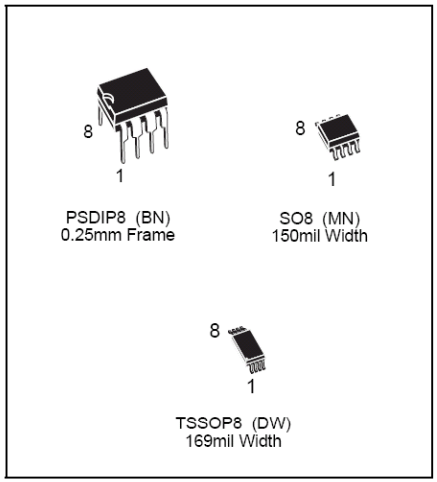


EJEMPLOS DE MEMORIAS

M93C86, M93C76, M93C66
M93C56, M93C46, M93C06

16K/8K/4K/2K/1K/256 (x8/x16) Serial Microwire Bus EEPROM

- INDUSTRY STANDARD MICROWIRE BUS
- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- DUAL ORGANIZATION: by WORD (x16) or by BYTE (x8)
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for M93Cx6 version
  - 2.5V to 5.5V for M93Cx6-W version
  - 1.8V to 3.6V for M93Cx6-R version
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ENHANCED ESD/LATCH-UP PERFORMANCES



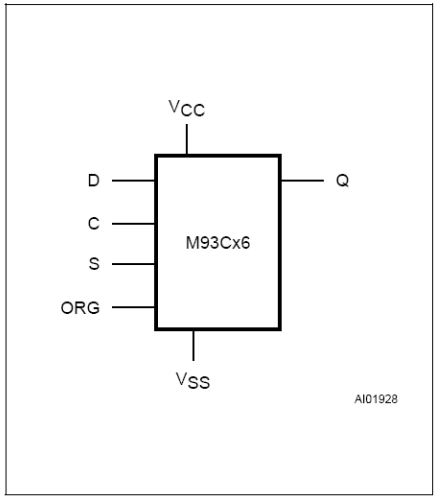
DESCRIPTION

This M93C86/C76/C66/C56/C46/C06 specification covers a range of 16K/8K/4K/2K/1K/256 bit serial EEPROM products respectively. In this text, products are referred to as M93Cx6. The M93Cx6 is an Electrically Erasable Programmable Memory (EEPROM) fabricated with STMicroelectronics's High Endurance Single Polysilicon CMOS technology. The M93Cx6 memory is accessed through a serial input (D) and output (Q) using the MICROWIRE bus protocol.

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



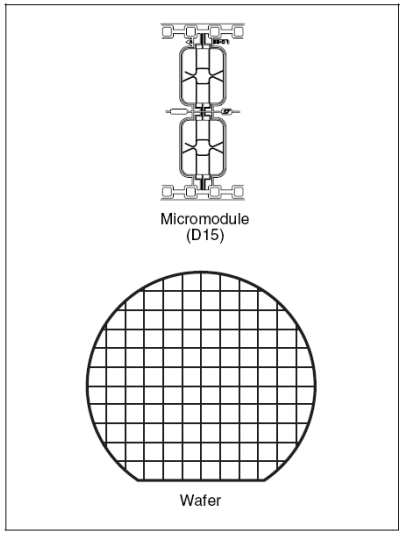
EJEMPLOS DE MEMORIAS

ST1335D, ST1336D ST1355D

5-Contact Memory Card IC 272-bit EEPROM With Advanced Security Mechanisms and Inlock System

DATA BRIEFING

- 5 V Single Supply Voltage
- Counting Capability (two options)
  - up to 32767 (8^5 -1)
  - 8 times reloadable, up to 4095 (8^4-1)
- Active Authentication Function (ST1335D/55D)
- Cipher Block Chaining Function (ST1355D)
- Memory Divided into :
  - 16 bits of Circuit Identification
  - 48 bits of Card Identification
  - 40 bits of Count Data
  - 16 bits for Validation Certificate
  - 24 bits of Transport Code
  - 64 bits of Issuer Data (ST1336D) or Authentication Secret Key (ST1335D/55D)
  - 32 bits of Anti-tearing Flags (optional)
  - 56 bits of User data (optionally not erasable)
- More than 500,000 Erase/Write Cycles
- More than 10 Years Data Retention
- 3.5 ms Programming Time at 5 V (typical)
- 500 µA Supply Current at 5 V (typical)
- 250 µA Stand-by Current at 5 V (typical)



DESCRIPTION

The members of the ST1335D/36D/55D family are principally designed for use in prepaid Phonecard applications. Each is a 272-bit EEPROM device, with associated security logic and special fuses to control memory access. The memory is arranged as a matrix of 34 x 8 cells, accessed in a serial bit-wise fashion for reading and programming, and in a byte-wise fashion for internal erasing. An on-chip address counter provides an internal address space of up to 512 bits.

Each member of the ST1335D/36D/55D family has an identification data area, unit-counters (with an anti-tearing mechanism for reliable usage in open readers), a post validation certificate, an issuer area (ST1336D) or an authentication secret key area (ST1335D/55D), and a user area. This is summarized in Figure 3.

The validation certificate allows the recognition of the device by the appropriate security module. When the 8 times reloadable option is activated, the certificate and the reload counter (address 64d to 71d) can be used to allow the recognition of the circuit by the appropriate security module. This will allow the development of a reloadable card as the certificate value is refreshed each time the reload counter is incremented.

Figure 1. Logic Diagram

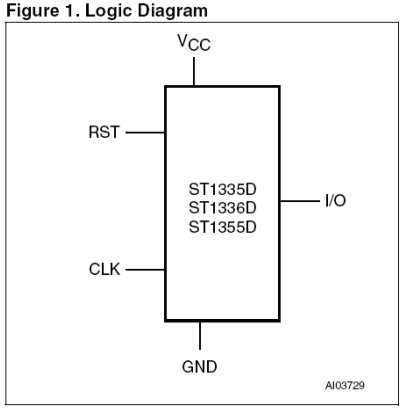
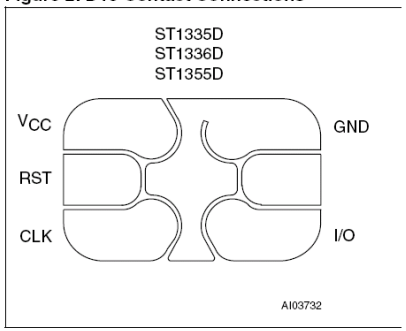


Table 1. Signal Names

CLK	Clock
RST	Reset
I/O	Serial Data Input / Output
V_{CC}	Supply Voltage
GND	Ground

Complete data available under NDA.

Figure 2. D15 Contact Connections



The anti-tearing mechanism guards against mis-counts occurring when the card is prematurely extracted, while an operation is underway, in an open reader.

MODES

The device works in two distinct modes of operation:

- Issuer Mode: for the card manufacturer. allowing custom data to be written to the device, to initialize it before release to the end user.
- User Mode: for the end user of the card, with restricted, and controlled access to the device.

Before delivery, from ST to the card issuer, the device is placed in the Issuer Mode. This operation is performed by blowing the "test fuse".

OPTIONS

Three options are available when ordering the device:

- The anti-tearing mechanism can be disconnected. In this case, the anti-tearing flag area from bit 288d to bit 319d is unused (Figure 3).
- The user area, from bit 320d to bit 375d, can be defined as "not erasable" in the User Mode.
- The reload mechanism can be activated. In this case, erasing a bit in the reload counter refreshes the certificate (CER). At this time, the certificate can be programmed with a new value.

ORDERING INFORMATION

The notation used for the device number is as shown in Table 2. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

Table 2. Ordering Information Scheme

Example: ST1335 D W4 / XX YY

Product

35 Active Authentication Function

36 Issuer Area

55 Cipher Block Chaining Authentication Function

Revision

D 5 V supply voltage, fuse blow and Inlock system

Transport Code

Given by ST

Customer Code

Given by the Issuer

Delivery Form

D15 Micromodule on reel

W4 Wafer (180 µm thickness)

Note: 1. Please contact your nearest ST Sales Office to check on availability

EJEMPLOS DE MEMORIAS

PRELIMINARY

DALLAS SEMICONDUCTOR

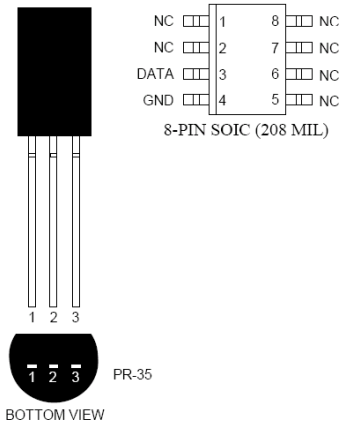
DS2433
4k-Bit 1-Wire™ EEPROM

www.dalsemi.com

FEATURES

- 4096 bits Electrically Erasable Programmable Read Only Memory (EEPROM)
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute identity because no two parts are alike
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- Memory partitioned into sixteen 256-bit pages for packetizing data
- 256-bit scratchpad with strict read/write protocols ensures integrity of data transfer
- Reduces control, address, data and power to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3k bits per second
- Overdrive mode boosts communication speed to 142k bits per second
- 8-bit family code specifies DS2433 communication requirements to reader
- Presence detector acknowledges when reader first applies voltage
- Low cost PR-35 or 8-pin SOIC surface mount package
- Reads and writes over a wide voltage range of 2.8V to 6.0V from -40°C to +85°C

PIN ASSIGNMENT



PIN DESCRIPTION

	PR-35	SOIC
Pin 1	Ground	NC
Pin 2	Data	NC
Pin 3	NC	Data
Pin 4	--	Ground
Pin 5-8	--	NC

ORDERING INFORMATION

DS2433	PR-35 package
DS2433S	8-pin SOIC package
DS2433T	Tape & Reel version of DS2433
DS2433Y	Tape & Reel version of DS2433S
DS2433X	Chip Scale Pkg., Tape & Reel

DALLAS SEMICONDUCTOR

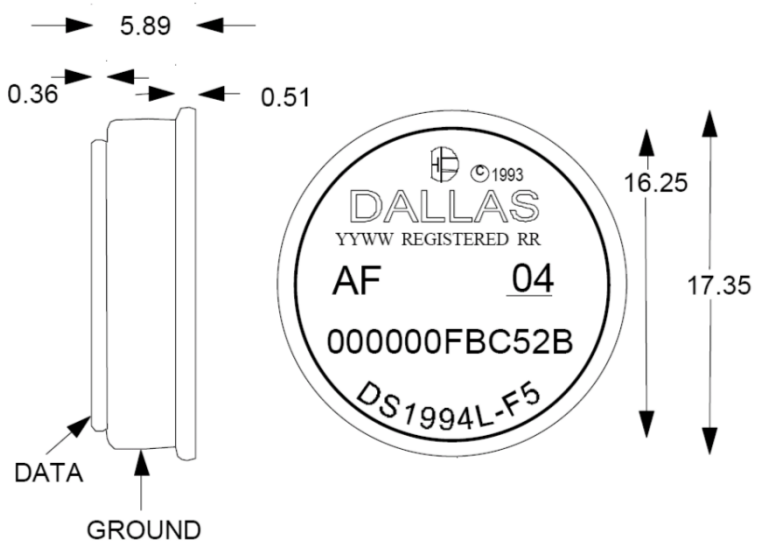
DS1992/DS1993
1kbit/4kbit Memory iButton™
DS1994
4-kbit Plus Time Memory iButton™

www.dalsemi.com

SPECIAL FEATURES

- 4096 bits of read/write nonvolatile memory (DS1993 and DS1994)
- 1024 bits of read/write nonvolatile memory (DS1992)
- 256-bit scratchpad ensures integrity of data transfer
- Memory partitioned into 256-bit pages for packetizing data
- Data integrity assured with strict read/write protocols
- Contains real time clock/calendar in binary format (DS1994)
- Interval timer can automatically accumulate time when power is applied (DS1994)
- Data can be accessed while affixed to object
- Economically communicates to bus master with a single digital signal at 16.3k bits per second
- Standard 16 mm diameter and 1-Wire protocol ensure compatibility with iButton family
- Button shape is self-aligning with cup-shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self-stick adhesive backing, latched by its flange, or locked with

F5 MICROCAN™



EJEMPLOS DE MEMORIAS

Somewhere in North Africa, Canada's Jen Crake clocks in at the TimePilot Extreme mounted on a race support vehicle.

EJEMPLOS DE MEMORIAS

M35101

13.56 MHz, ISO 14443, Contactless Memory Chip
2048-bit EEPROM

DATA BRIEFING

- ISO 14443-2 Type-B Standard Compliant
- 13.56 MHz Carrier Frequency
- 847 kHz Subcarrier Frequency
- 106 Kbit/second Data Transfer
- Internal Tuning Capacitor
- Data Transfer:
  - ASK Modulation from Reader to M35101
  - BPSK Coding from M35101 to Reader
- 2048-bit EEPROM with Write Protect Feature
- BYTE and PAGE READ (up to 16 Bytes)
- BYTE and PAGE WRITE (up to 16 Bytes)
- Self-Timed Programming Cycle with Auto-Erase
- 5 ms Programming Time (typical)
- More than 100,000 Erase/Write Cycles
- More than 40 Year Data Retention

DESCRIPTION

The M35101 is a contactless memory, powered by the received carrier electromagnetic wave. It is a 2048-bit EEPROM, organised as 16 pages of 16 x 8 bits.

The M35101 conforms to the ISO 14443-2 Type-B recommendation for the transfer of power and signals via radio transmission. The card reader circuitry amplitude modulates (10% modulation) the data on the carrier using amplitude shift keying (ASK). The card replies by load modulating the data on the carrier using bit phase shift keying (BPSK) of the subcarrier. The data transfer rate in each direction is 106 Kbit/second.

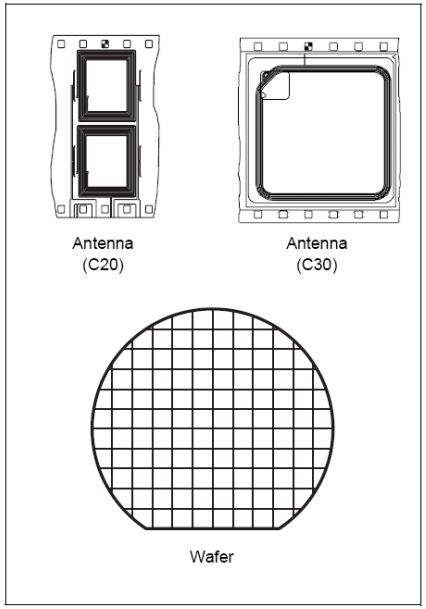


Figure 1. Logic Diagram

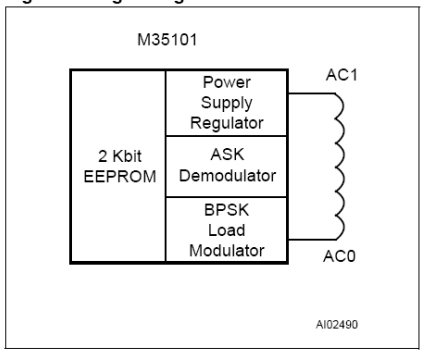


Table 1. Signal Names

AC1	Antenna Coil
AC0	Antenna Coil

Contactless Memory Solutions

Tags and RFID

www.st.com/contactless

Track and trace

Access control