CONVERSIÓN ANALÓGICO-DIGITAL

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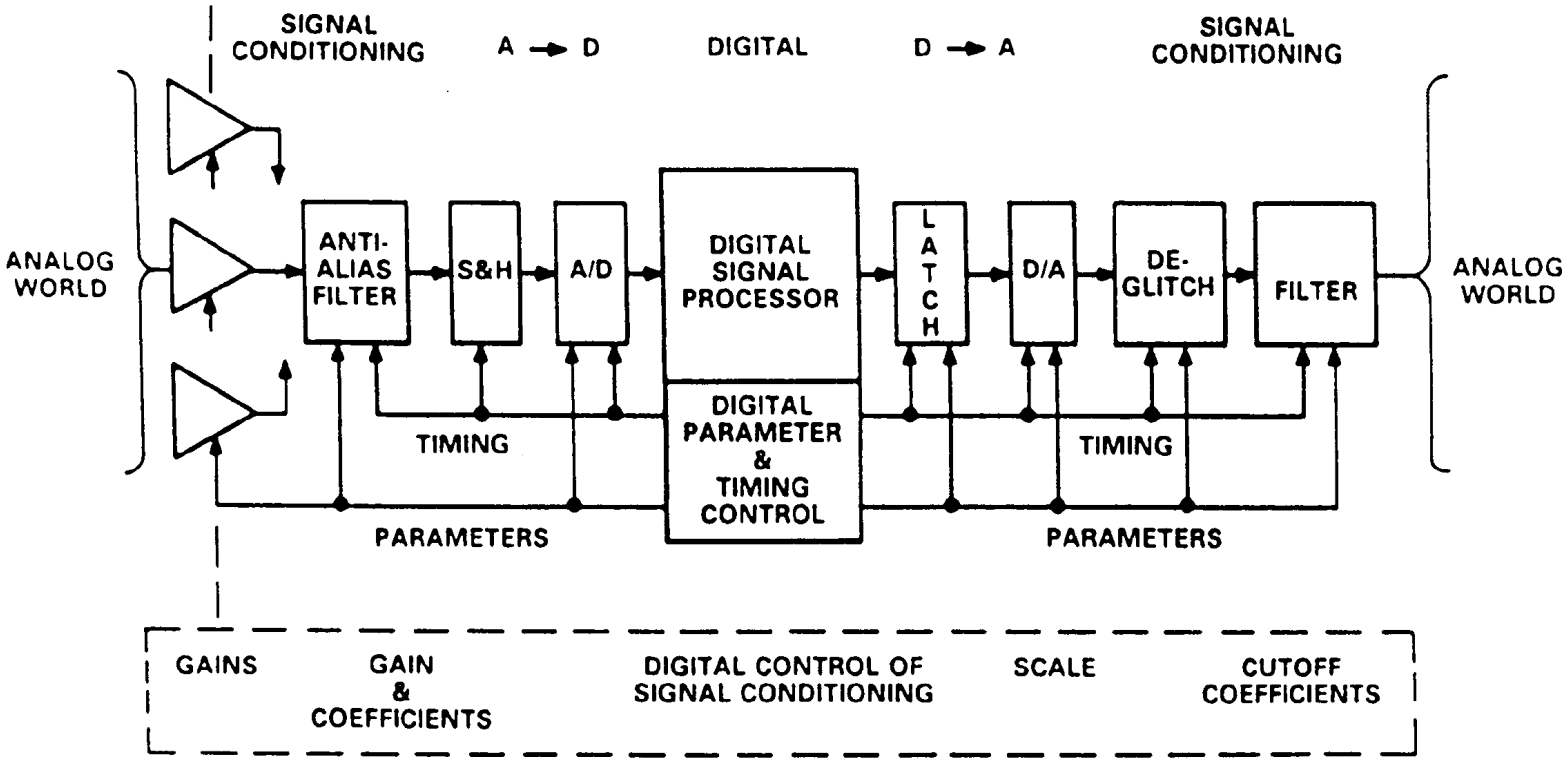
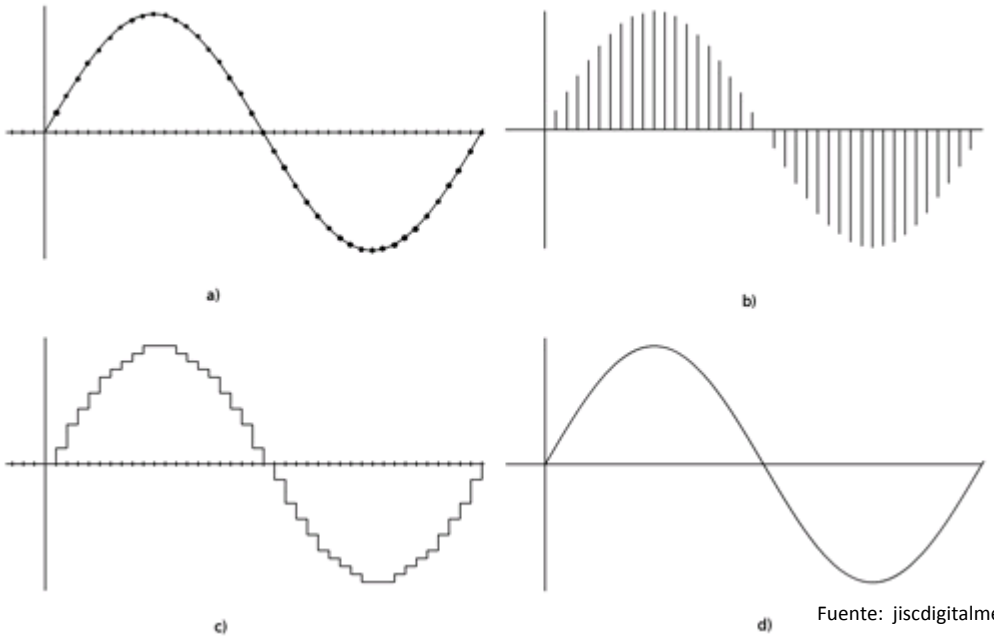
ELEMENTOS EN UN SISTEMA MUESTREADO DE DATOS



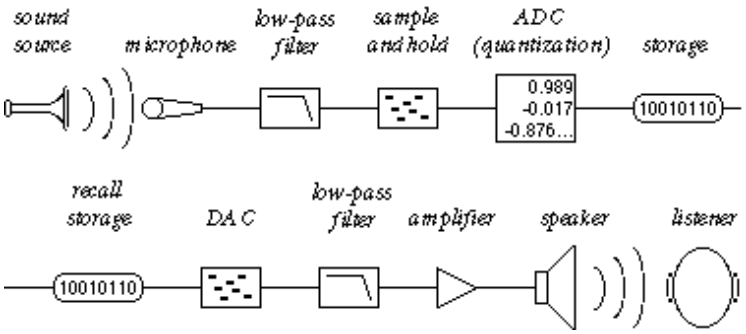
Fuente: Application Note AN-282 Analogue Devices.

SEÑALES ANALÓGICAS Y SEÑALES DISCRETAS

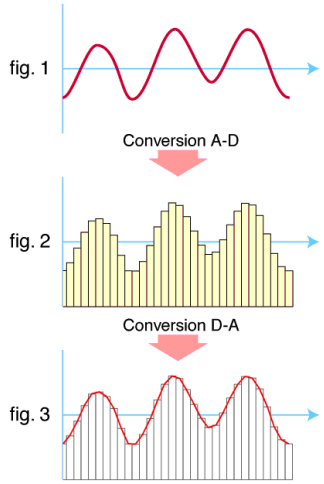


Fuente: jiscdigitalmedia "An introduction to digital audio"

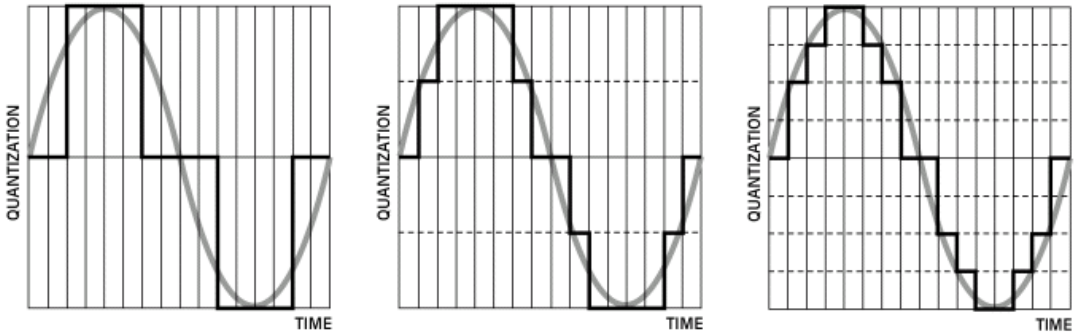
(a) Onda acústica original (función seno) con los puntos de muestreo en intervalos de tiempo regulares (eje X); **(b)** valores muestreados; **(c)** representación digital de la onda según los valores de la figura b; **(d)** reconstrucción de la señal analógica mediante la utilización de un filtro pasa-bajo para suavizar los cambios escalonados (altas frecuencias) de la señal c.

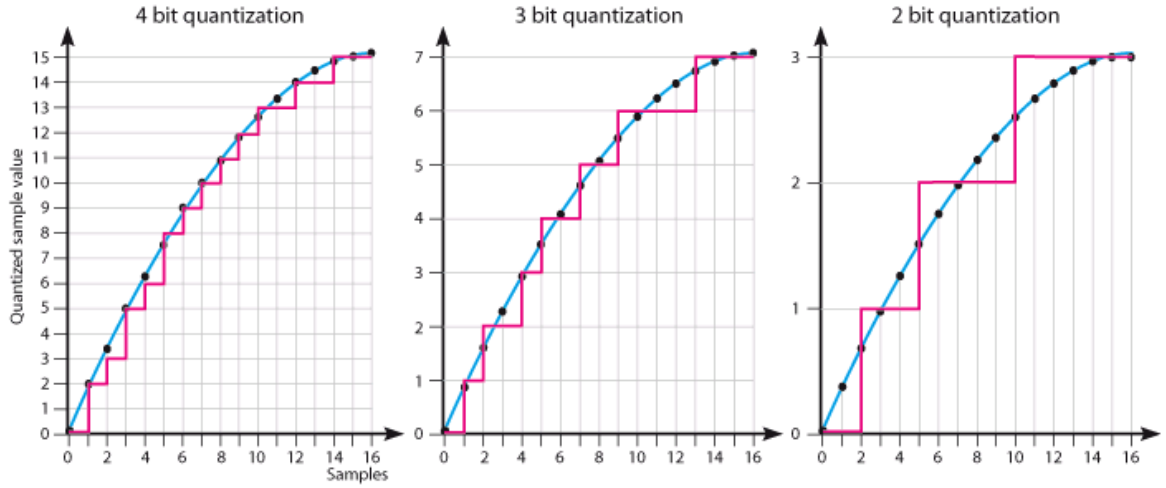


Fuente: Digital Audio by Christopher Dobrian

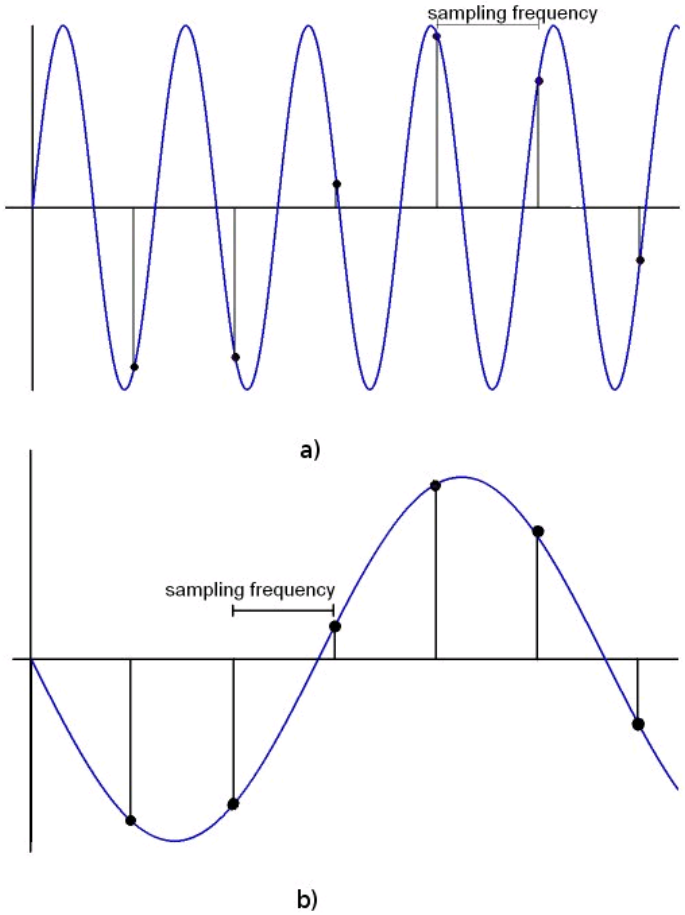


EFECTO DE LA CUANTIFICACIÓN

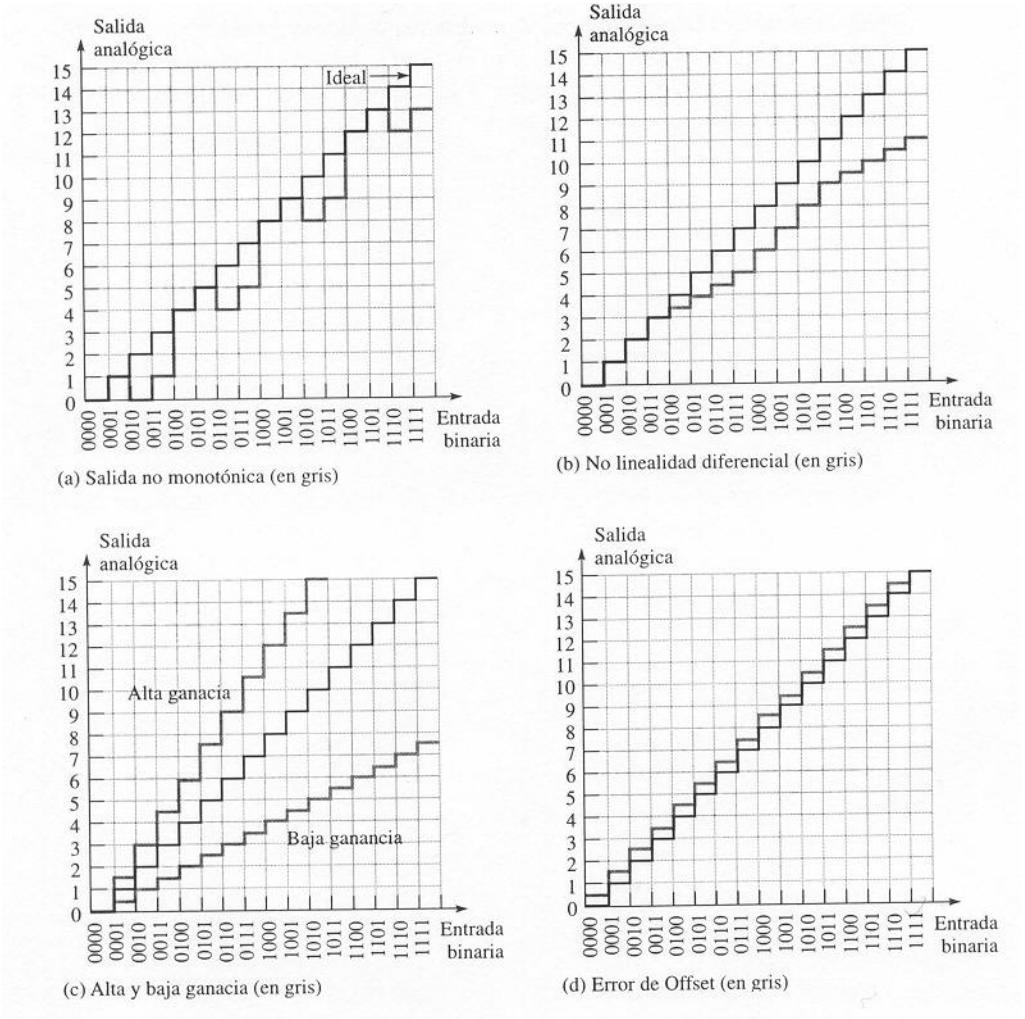




EFECTO DE LA FRECUENCIA DE MUESTREO (aliasing)

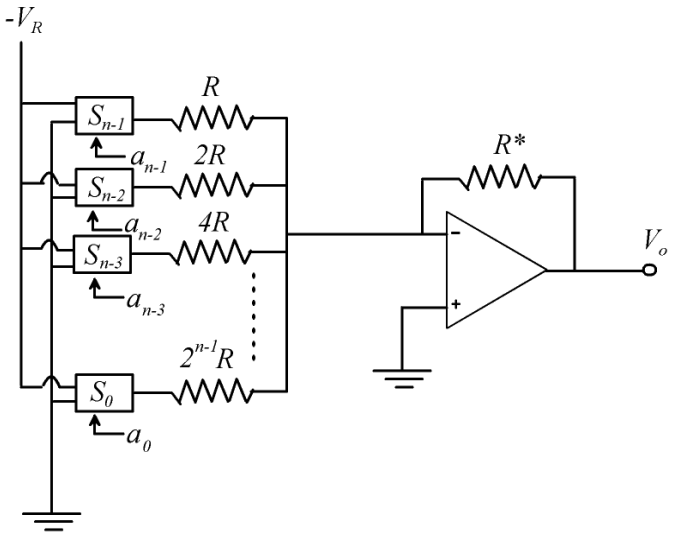


CONVERTIDORES DAC

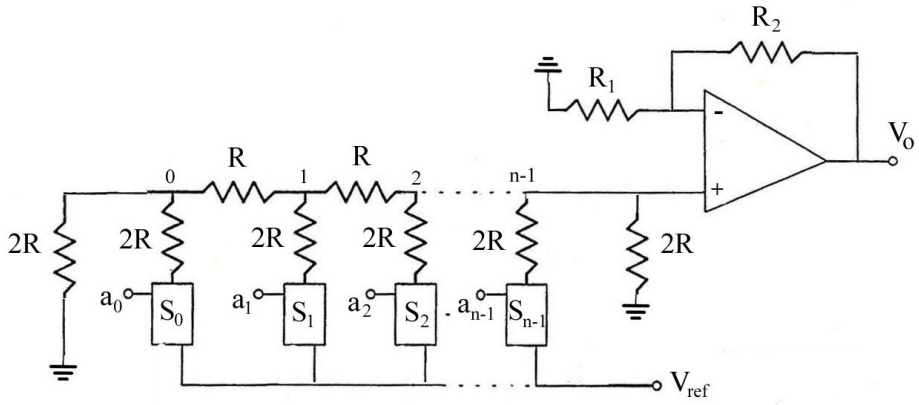


ERRORES EN CONVERSORES DAC

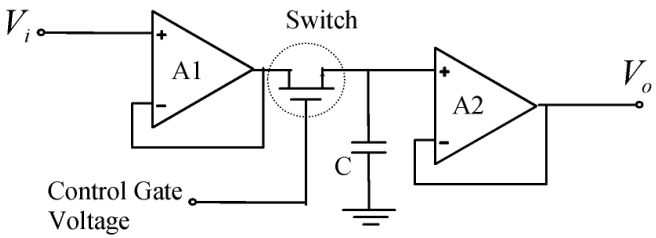
CONVERTIDORES DAC



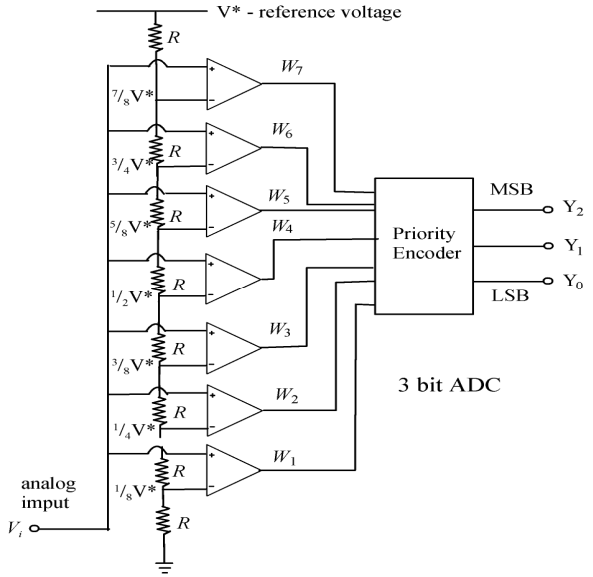
CONVERTIDOR DAC CON RESISTENCIAS PONDERADAS



CONVERTIDOR DAC CON ESTRUCTURA R-2R



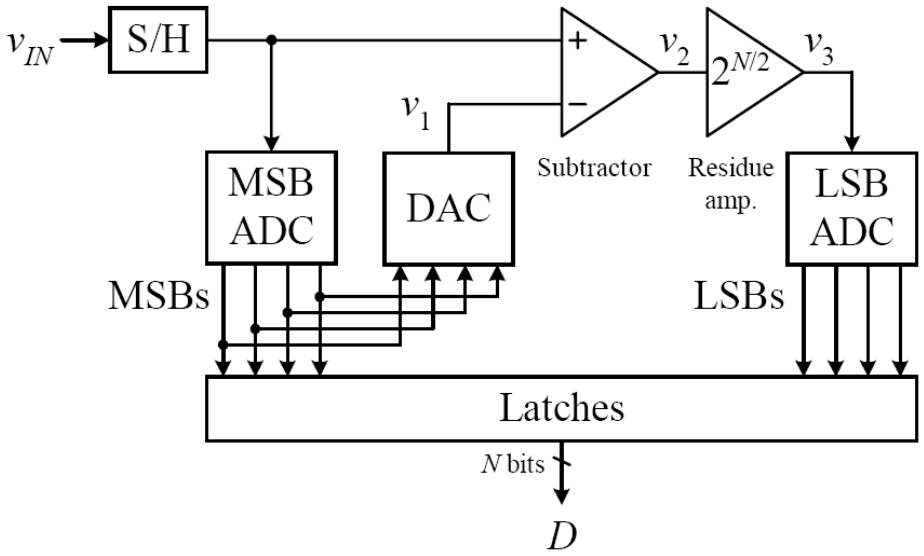
MUESTREO Y RETENCIÓN



CONVERTIDOR ADC DE TIPO FLASH

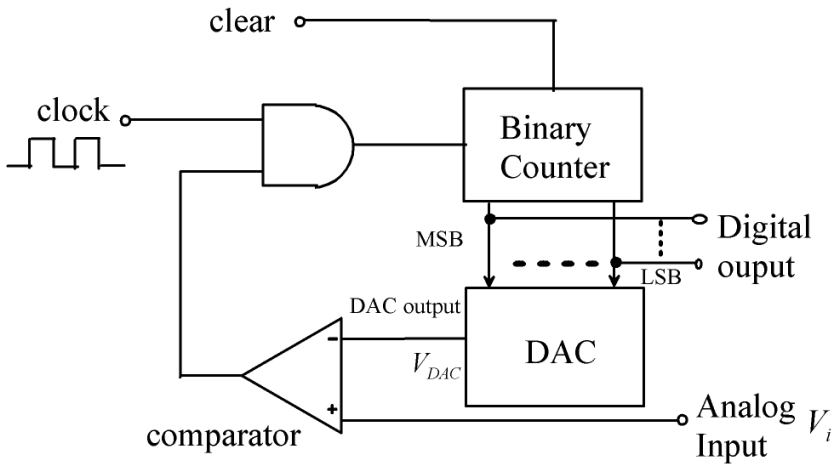
Two-step flash ADC

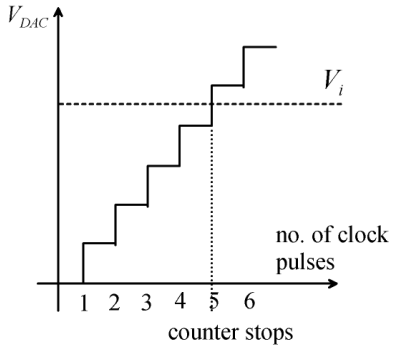
- Greatly reduce the number of comparators
  - Ex: for an 8-bit ADC, comparator no. 255 ⇒ 30

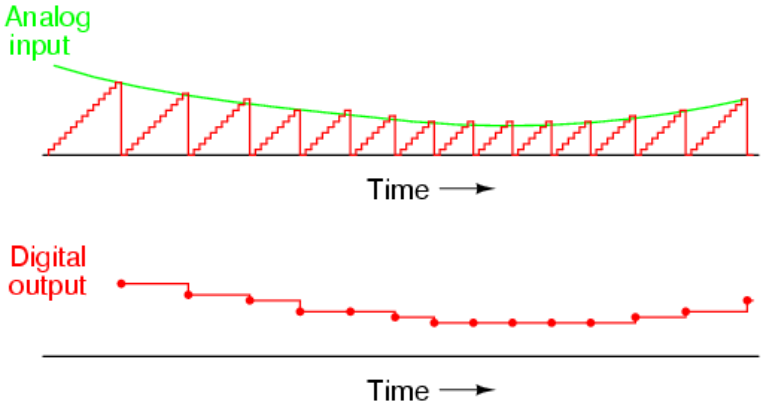


CONVERTIDOR ADC DE TIPO HALF-FLASH

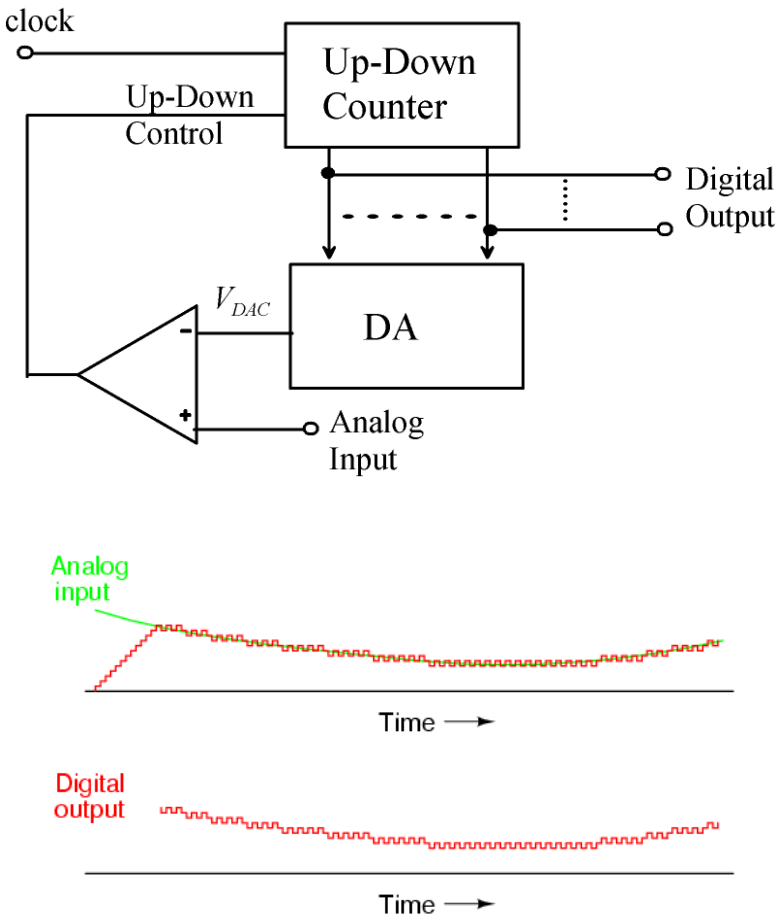
CONVERTIDORES ADC







CONVERTIDOR ADC DE RAMPA EN ESCALERA (contador ascendente)



CONVERTIDOR ADC DE SEGUIMIENTO (contador de cuenta reversible)

CONVERTIDORES ADC

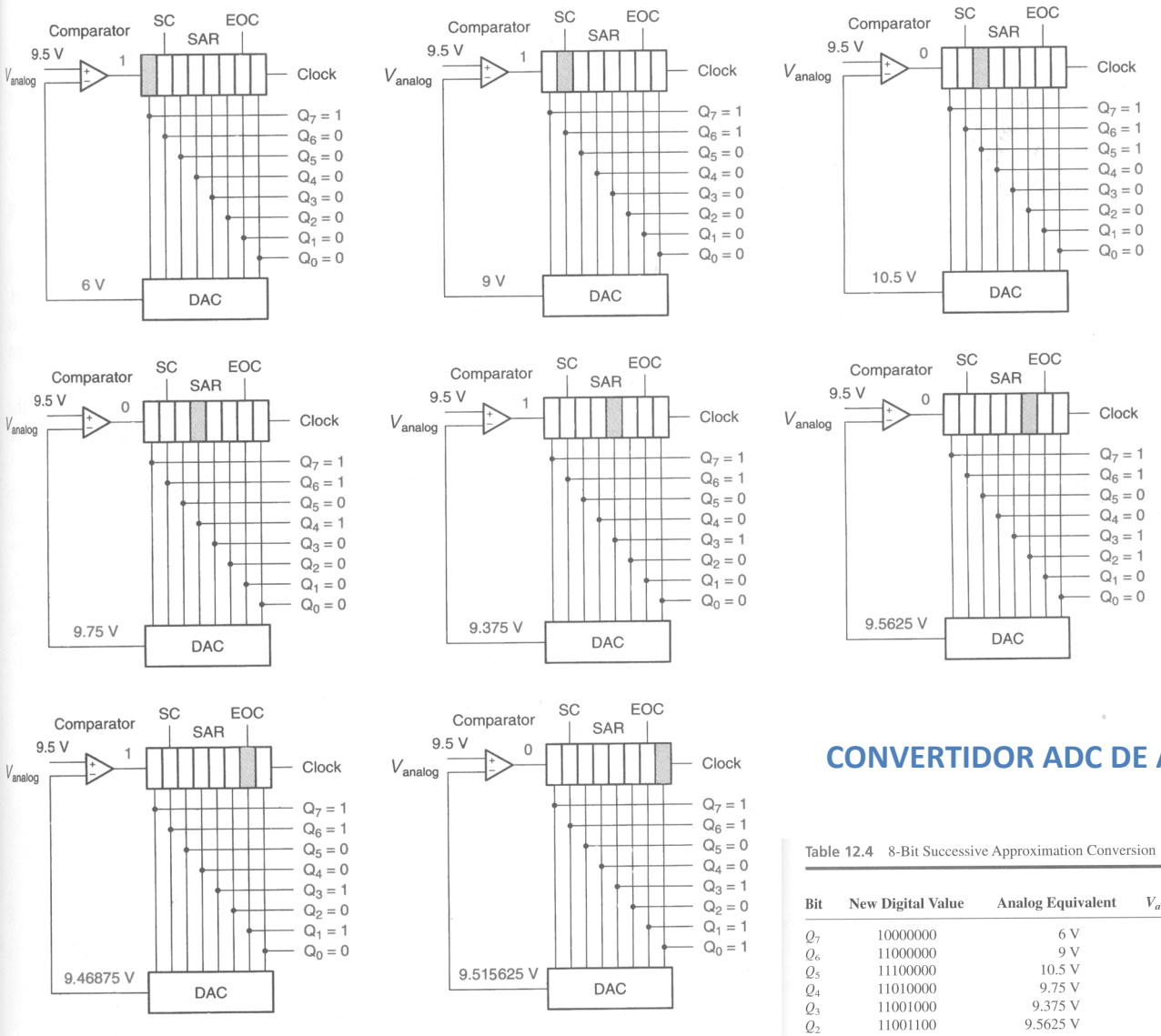


FIGURE 12.24
Example 12.11
Successive Approximation A/D Conversion

SC= START CONVERSION
EOC= END OF CONVERSION

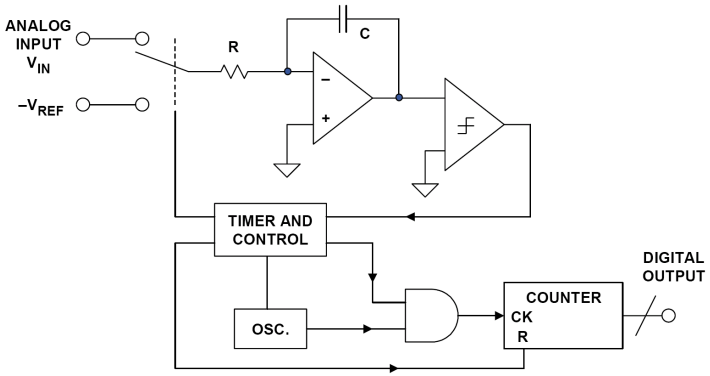
CONVERTIDOR ADC DE APROXIMACIONES SUCESIVAS

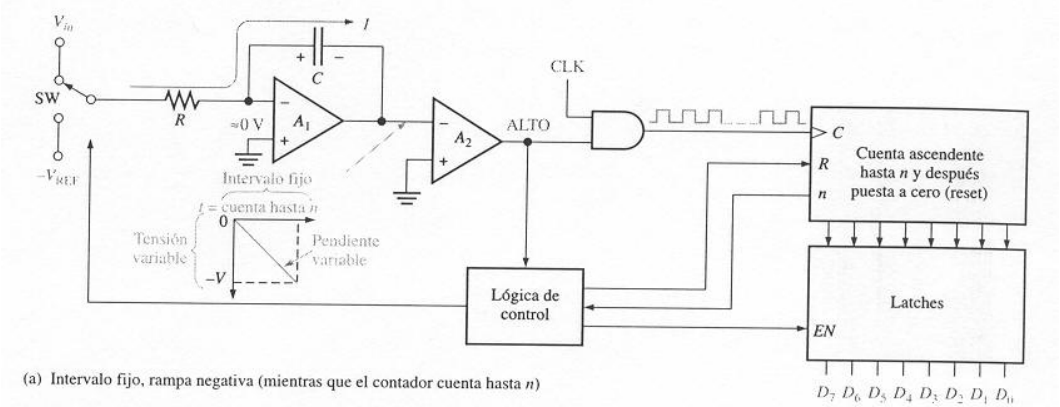
Table 12.4 8-Bit Successive Approximation Conversion

Bit	New Digital Value	Analog Equivalent	$V_{analog} \geq V_{DAC}$?	Comparator Output	Accumulated Digital Value
Q_7	10000000	6 V	Yes	1	10000000
Q_6	11000000	9 V	Yes	1	11000000
Q_5	11100000	10.5 V	No	0	11000000
Q_4	11010000	9.75 V	No	0	11000000
Q_3	11001000	9.375 V	Yes	1	11001000
Q_2	11001100	9.5625 V	No	0	11001000
Q_1	11001010	9.46875 V	Yes	1	11001010
Q_0	11001011	9.515625 V	No	0	11001010

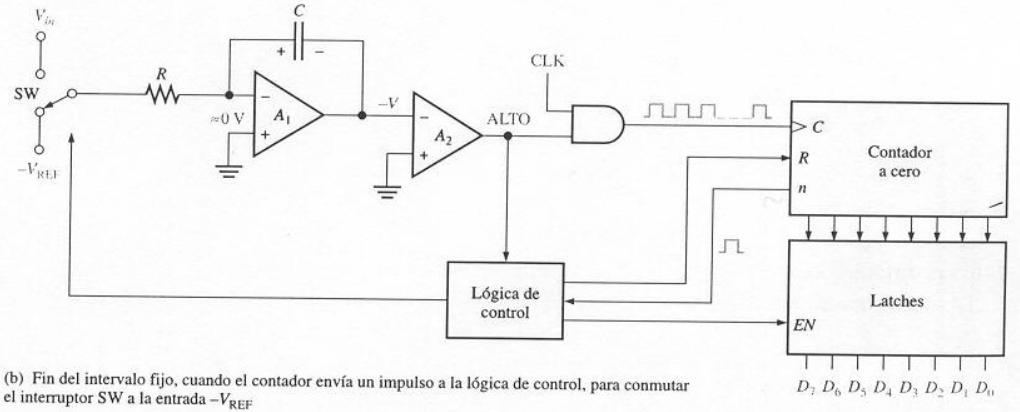
CONVERTIDORES ADC

CONVERTIDOR ADC DE DOBLE RAMPA

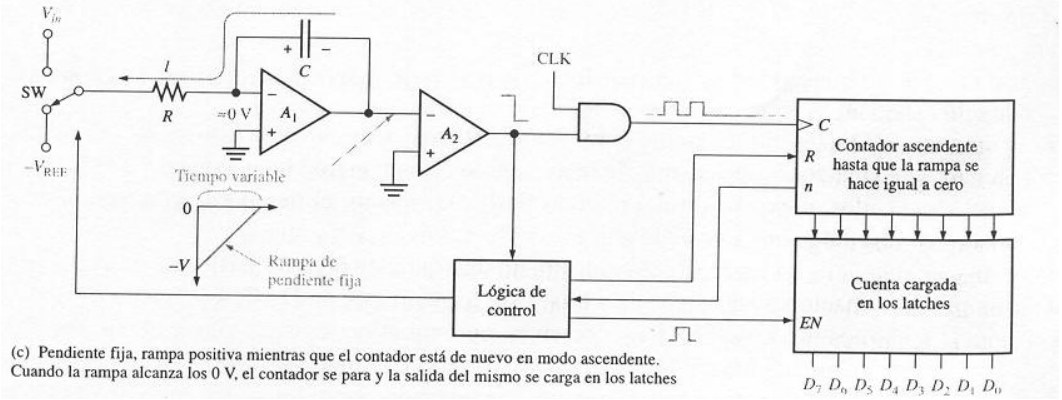




(a) Intervalo fijo, rampa negativa (mientras que el contador cuenta hasta n)

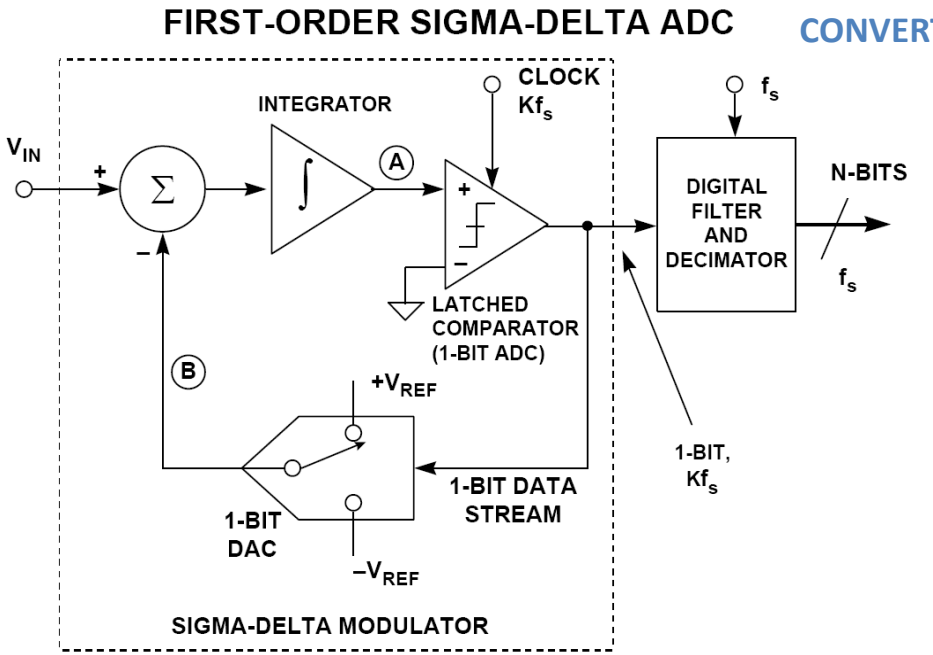


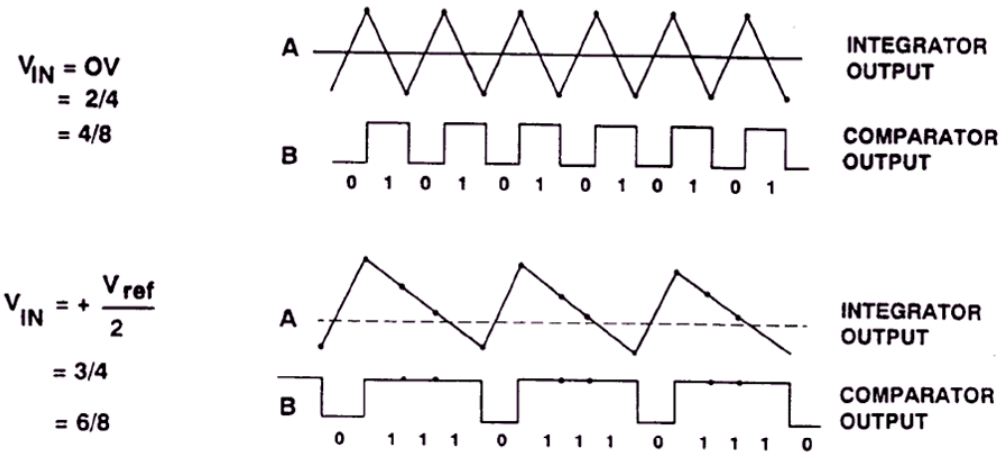
(b) Fin del intervalo fijo, cuando el contador envía un impulso a la lógica de control, para conmutar el interruptor SW a la entrada $-V_{REF}$



(c) Pendiente fija, rampa positiva mientras que el contador está de nuevo en modo ascendente. Cuando la rampa alcanza los 0 V, el contador se para y la salida del mismo se carga en los latches

CONVERTIDOR ADC SIGMA-DELTA (Σ-Δ)





CONVERTIDORES ADC

SYSTEM ARCHITECTURE	RESOLUTION	SPEED	MAXIM ADCs	ADVANTAGES/DRAWBACKS
Flash	8 bits	250Msps–1Gsps	MAX100 MAX101A MAX104*	+ Extremely fast + High input bandwidth - Highest power consumption - Large die size - High input capacitance - Expensive - Sparkle codes**
SAR	10 bits–16 bits	76ksps–250ksps	MAX195 MAX144/MAX145 MAX115* MAX157/MAX159 MAX186/MAX188	+ High resolution and accuracy + Low power consumption + Few external components - Low input bandwidth - Limited sampling rate - V_{IN} must remain constant during conversion
Integrating	> 18 bits	< 50ksps	MAX132 MAX135	+ High resolution + Low supply current + Excellent noise rejection - Low speed
Sigma-Delta (Σ-Δ)	> 16 bits	> 200ksps	MAX1400 MAX1401* MAX1402* MAX1403*	+ High resolution + High input bandwidth + Digital on-chip filtering - External T/H - Limited sampling rate
Pipeline	12 bits–16 bits	1Msps–80Msps	MAX1200 MAX1201 MAX1205	+ High throughput rate + Low power consumption + Digital error correction and on-chip self-calibration - Requires 50% duty cycle typical - Requires minimum clock frequency

**Future product—contact factory for availability.*

***Sparkle codes are erratic errors caused by meta-stable comparators or out-of-sequence output codes (thermometer bubbles), which in turn are*