INVITED PAPER

Graphene Transistors: Status, Prospects, and Problems

In this paper, the author provides an overview of the status and challenges in graphene-based transistors, including types of graphene-based transistors reported to date and a comparison of their performance metrics to those of transistors made from other materials systems.

By Frank Schwierz, *Senior Member IEEE*

ABSTRACT | Graphene is a relatively new material with unique properties that holds promise for electronic applications. Since 2004, when the first graphene samples were intentionally fabricated, the worldwide research activities on graphene have literally exploded. Apart from physicists, also device engineers became interested in the new material and soon the prospects of graphene in electronics have been considered. For the most part, the early discussions on the potential of graphene had a prevailing positive mood, mainly based on the high carrier mobilities observed in this material. This has repeatedly led to very optimistic assessments of the potential of graphene transistors and to an underestimation of their problems. In this paper, we discuss the properties of graphene relevant for electronic applications, examine its advantages and problems, and summarize the state of the art of graphene transistors.

KEYWORDS | Bilayer graphene; Field-effect transistor (FET); graphene; graphene nanoribbon; logic circuit; radio frequency (RF)

I. INTRODUCTION

Following Moore's law [1], semiconductor mainstream electronics (processors, memories, etc.) enjoyed a very dynamic evolution over decades, leading to a steady reduction of the cost per transistor by 25% per year and to an annual market growth of about 17%. Key to this success was the continuous scaling of the silicon metal–oxide–semiconductor field-effect transistor (Si MOSFET). Today, Si MOSFETs with 20-nm gates are in mass production, and, for the year 2020, the International Technology Roadmap for Semiconductors (ITRS) requires 10-nm MOSFETs [2].

Unfortunately, it becomes more and more difficult to further scale the Si MOSFET and simultaneously achieve the needed device performance. Major problems are parameter fluctuations of nominally identical transistors due to the discreteness of matter, short-channel effects, and the deteriorating effects of parasitics. To alleviate these problems, considerable efforts are spent on the development of nonclassical MOSFET architectures and, recently, the advanced trigate MOSFET has been introduced to mass production [3]. While these measures help for the moment, they will only delay the moment when further MOSFET scaling becomes impractical. The problems in scaling have already led to a slowdown of long lasting and desirable exponential trends in semiconductor electronics in the more recent years. Therefore, to extend the lifetime of Moore's law and to ensure a healthy evolution of semiconductor electronics in the future, researchers and chipmakers are intensively working on new material and device concepts.

In radio-frequency (RF) electronics, another important and dynamic area of semiconductor electronics, device engineers are also looking for new materials, in particular those with high mobilities. The aim is to develop transistors with high-mobility channels for operation in the terahertz gap (0.3–3 THz) that so far has not yet been tapped for applications.

Recently, graphene, a 2-D carbon-based material, has attracted a lot of attention. In 2004, groups from Manchester University (Manchester, U.K.) and from Georgia Institute of Technology (Atlanta, GA, USA) published two pioneering papers on the preparation of graphene and the occurrence of the field effect in their samples [4], [5]. Moreover, high carrier mobilities have been observed in graphene [4]. These two papers not only ignited a revolution in solid-state physics but also fueled

Manuscript received June 15, 2012; revised December 31, 2012 and March 7, 2013; accepted March 25, 2013. Date of publication May 22, 2013; date of current version June 14, 2013. This work was supported by the Excellence Research Grant and the Intra-Faculty Research Grant of the Technische Universität Ilmenau.
The author is with the Institut für Mikro- und Nanotechnologien, Technische Universität Ilmenau, Ilmenau 98684, Germany (e-mail: frank.schwierz@tu-ilmenau.de).
Digital Object Identifier: 10.1109/JPROC.2013.2257633

speculations that graphene could be used for transistors with scaling limits and operating speeds beyond those of conventional transistors. Already in 2007, graphene found its place in the Emerging Research Devices chapter of the ITRS, research programs to develop graphene transistors were established worldwide, and soon the first operating graphene transistors were demonstrated.

The aim of this paper is to examine the state of the art of graphene transistors and to analyze their merits and drawbacks. A large part of the discussion is devoted to graphene MOSFETs and issues related to FETs since so far most work on graphene devices has been focused on MOSFETs. Section II provides a short overview of the history of graphene, and Section III introduces important transistor figures of merit (FOMs). In Section IV, those properties of graphene relevant for transistors are reviewed, and Section V provides an in-depth discussion of the current status and of the prospects and problems of graphene transistors. Finally, Section VI provides an outlook and concludes the paper.

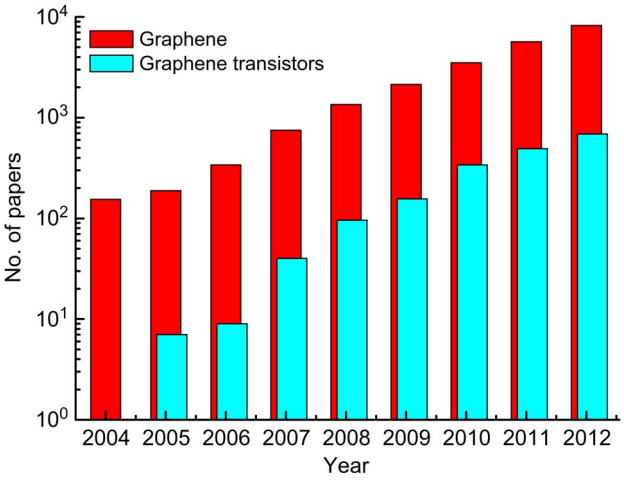

Fig. 2. *Number of papers published per year and listed in Web of Science [21] under the search terms "graphene" and "graphene transistor."*

II. THE HISTORY OF GRAPHENE

Graphene began to attract much attention in the scientific community in late 2004 after the publication of the two seminal papers on graphene [4], [5]. Insofar, 2004 was the magic year for graphene, but the history of this material goes back much further, as shown in Fig. 1. As early as 1947, at a time when the name graphene did not yet exist, Wallace calculated the band structure of a single layer of carbon atoms arranged in a hexagonal 2-D lattice, i.e., graphene, and predicted its gapless nature [6]. In 1962, Boehm *et al.* produced single graphene layers by the reduction of graphite oxide [7]; in 1969, single-layer graphene on platinum has been observed [8]; and in 1975, graphene has been produced by the thermal decomposition of SiC [9]. Initially, however, these results found only limited attention in the community. In 1994, the name graphene has been introduced for single carbon layers of the graphitic structure [10]. After another ten years, eventually, the interest in graphene exploded and the number of papers on graphene published per year grew at an enormous pace, as shown in Fig. 2.

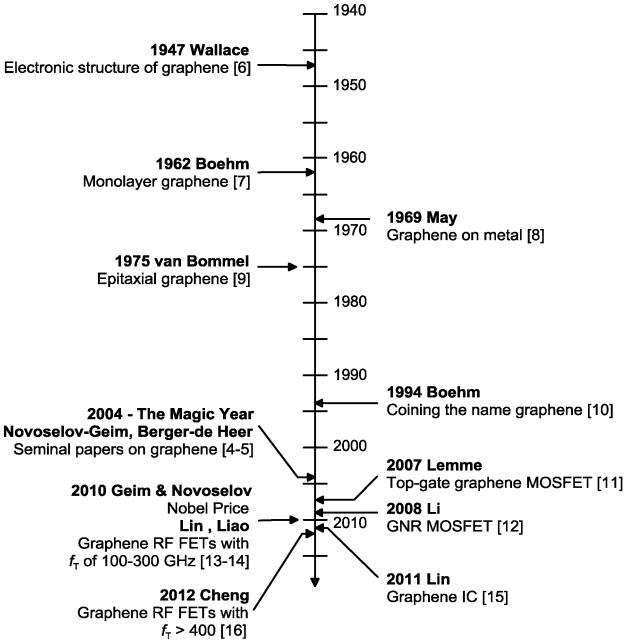

Fig. 1. *Important milestones of the evolution of graphene electronics.*

Physicists discovered remarkable effects in graphene [17], [18], and soon device engineers became interested in the new fascinating material [19], [20]. The first graphene MOSFET has been reported in 2007 [11], and since then a continuously increasing number of groups successfully fabricated graphene transistors. In 2010, graphene MOSFETs with cutoff frequencies in the 100–300-GHz range have been reported [13], [14]; in 2011, the first graphene integrated circuit has been presented [15]; and in 2012, a graphene MOSFET with a cutoff frequency exceeding 400 GHz has been demonstrated [16].

Early discussions on the prospects of graphene in electronics focused almost exclusively on the carrier mobility. Already in their 2004 paper, Novoselov and Geim reported high room-temperature mobilities of 10 000–15 000 cm^2/Vs in graphene [4], and meanwhile the measured record mobilities in graphene exceed 100 000 cm^2/Vs at room temperature and 1 000 000 cm^2/Vs at 4 K [22], [23]. High mobilities almost magically attract the attention of device engineers since a high mobility is one of the preconditions for fast transistors. On the other hand, other properties of graphene relevant for electronic devices received much less attention in the discussion. The reduction

of graphene to its high mobility, in particular in the media and in popular science publications, pushed the discussion on the prospects of graphene into an unfortunate direction and led to misleading assessments. Graphene has rashly been acclaimed as the perfect material for ultrafast high-performance transistors and designated as the successor of Si in mainstream electronics and of the III–V compounds in the RF field. Unfortunately, these high expectations graphene cannot meet, at least not in the short and medium term.

Such kind of euphoria is not really a new phenomenon. In the 1970s and early 1980s, GaAs has been considered as the semiconductor material of the future, and the discussions on carbon nanotubes in the 1990s had a similar optimistic tenor. Furthermore, a glance at the history of semiconductor electronics shows that a radical transition from one semiconductor material to another is not impossible in general and indeed has happened. Decades ago, Ge was the only semiconductor used, while later it has entirely been replaced by Si. We should recognize, however, that the current situation is hardly comparable to the one when the transition from Ge to Si happened. Today, the chip industry is focused on Si complementary MOS (CMOS) to such an extent that it will be extremely difficult for a new material or device concept to compete and to make inroads into the Si CMOS world unless the new concept offers a really significant edge.

Meanwhile the tenor of the discussion on graphene has changed, and its future in electronics is assessed still cautiously optimistic but much less enthusiastic. A series of recent competent commentaries has dealt with graphene's role in electronics [24]–[29]. The concurrent opinion is that graphene will not replace Si or the III–V compounds soon or in the midterm future. A key issue here is the bandgap. While all conventional semiconductors possess a sizeable bandgap (e.g., Si 1.1 eV, Ge 0.7 eV, GaAs 1.4 eV), natural graphene is a zero-gap material and the missing gap has consequences for the operation of graphene transistors. The most obvious effect discussed already in the early days of graphene transistors is that FETs with gapless channels do not switch off and, therefore, are not suited for complex logic circuits. Recently, the effect of the missing gap on the operation of graphene RF transistors has also received increasing attention.

A promising direction currently pursued in graphene research is directed to complement the conventional semiconductors instead of trying to replace them and to use graphene in applications where other materials fail or perform poor. Indeed, intensive work is underway on graphene transparent electrodes [30] and on graphene devices for flexible and printable electronics [31], [32].

III. IMPORTANT TRANSISTOR FIGURES OF MERIT

In the following, FOMs commonly used to assess the performance of transistors are introduced. The discussion is limited to FOMs that have already been reported for experimental graphene transistors and that are needed for the subsequent considerations. The essential feature of FETs is their ability to switch and to amplify. Switching on and off constitutes the basis of digital logic and the ability to amplify signals and provide gain is crucial for analog/RF applications.

We start our discussion with switching. Depending on the gate–source voltage V_{GS}, a FET is either in the ON-state (a large ON-current I_{on} can flow) or in the OFF-state (only a very low OFF-current I_{off} flows). The V_{GS} at which the FET is just at the verge of turning on is the threshold voltage V_{Th}, n-channel FETs (for short n-FET) are on for $V_{GS} > V_{Th}$, and p-FETs are on if V_{GS} is more negative than V_{Th}.

Logic integrated circuits (ICs) consist of cascaded logic gates (e.g., NAND and NOR), where the output signal of one gate serves as input for the next gate. The cascaded structure requires the restoration of the signal levels to ensure that a logic gate can reliably identify whether it receives a logic "1" or "0" at its input.

As shown in Fig. 3 for the example of a NAND gate, CMOS logic gates consist of an n-branch connected to ground and a p-branch connected to the positive supply voltage V_{DD}. The beauty of Si CMOS is that it provides ideal signal restoration, combined with the feature that in steady state, regardless of the input signals, always one of the branches is off and no current except the small I_{off} flows from V_{DD} to ground. Therefore, Si CMOS offers ultimately low static power dissipation. This is extremely important since power dissipation and the resulting self-heating are major problems of complex logic ICs. Si CMOS has superseded all competing logic technologies due to its low static power dissipation. Thus, a FET-based successor for Si CMOS logic will need transistors able to switch off.

A transistor FOM related to switching is the ON-off ratio I_{on}/I_{off}. I_{on} is the ON-current flowing when both V_{GS}

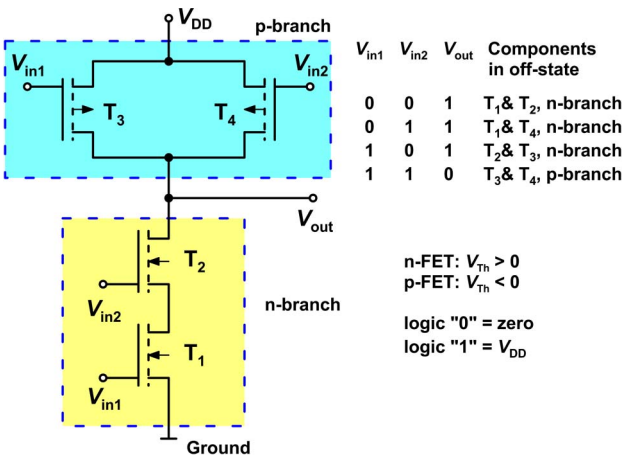

Fig. 3. *CMOS NAND gate.*

and the drain–source voltage V_{DS} are equal to V_{DD} and I_{off} is current in the OFF-state ($V_{GS} = 0$ and $V_{DS} = V_{DD}$). For CMOS logic, Si MOSFETs with ON–OFF ratios between 10^4 and 10^7 are required and competing devices should at least come close to this target. It is important to recognize that such ON–OFF ratios can only be achieved if the FET channel is semiconducting and has a wide enough bandgap. Another FOM for FET switching is the subthreshold swing S. It is related to FET operation in the subthreshold region (i.e., $V_{GS} < V_{Th}$ for n-FETs), given in units of mV/dec, and indicates by how many mV the gate–source voltage has to be varied to cause a change of the drain current a factor of 10. S should be as small as possible and its lower limit is 60 mV/dec for conventional Si MOSFETs.

A FOM describing the electrostatic integrity of a FET and its immunity against short-channel effects is the scale length λ. The scale length concept has originally been developed for Si MOSFETs and later been extended to graphene transistors [33], [34]. If a FET design has a certain scale length λ, it can be considered to be sufficiently immune against short-channel effects provided the condition $L > 1.5\pi\lambda$ (L is the gate length) is fulfilled. Obviously, a small λ is desirable and, in essence, this is achieved by transistors with both a thin gate dielectric and a thin channel. Note that the scale length concept applies only to FETs with a channel having a sizeable bandgap.

Let us now turn to analog/RF transistor FOMs. By applying direct current (dc) voltages to the terminals of a FET, it is driven to the dc operating point in the ON-state. Now the dc gate–source voltage V_{GS} is superimposed by a small RF signal that is to be amplified. By the small gate voltage variation $\pm\Delta V_{GS}$, the amount of carriers in the channel, and, consequently, the drain current, is changed. In this operating regime, the FET does not need to switch off.

The amplification characteristics of transistors are described in terms of the intrinsic gain G_{int}, the current gain h_{21}, and the unilateral power gain U. As shown in Fig. 4, both h_{21} and U are frequency dependent and roll off with increasing frequency at a slope of −20 dB/dec.

Closely related to the current and power gains are the two most widely used FOMs of RF transistors, namely the cutoff frequency f_T and the maximum frequency of oscillation f_{max}. The cutoff frequency is the frequency at which the magnitude of h_{21} has dropped to unity (0 dB) and at f_{max} the unilateral power gain equals unity. Thus, f_T and f_{max} mark upper frequency limits since beyond these frequencies the transistor looses its ability to amplify. It is important to recognize that for the vast majority of RF applications simultaneously high f_T and f_{max} are needed, although occasionally only current gain and f_T are considered, in particular in papers on graphene transistors and circuits [14], [36]. In many applications, power

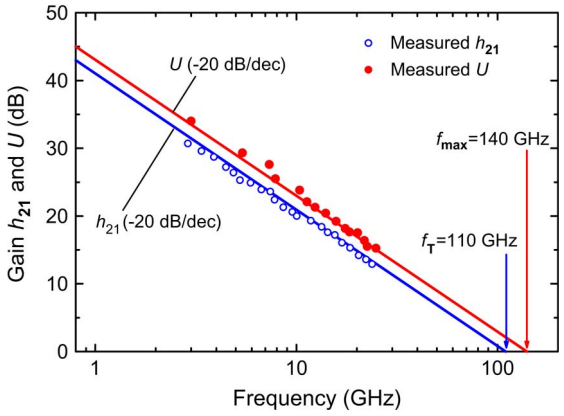

Fig. 4. *Small-signal current gain h_{21} and unilateral power gain U of an RF FET versus frequency; after [35].*

gain and f_{max} are even more important than current gain and f_T.

The frequency performance of transistors can be conveniently discussed with their small-signal equivalent circuit. Fig. 5 shows a frequently used equivalent circuit of analog/RF FETs. The elements within the shaded rectangle constitute the intrinsic transistor, i.e., the gate stack of the transistor and the channel underneath. It consists of the gate–source capacitance C_{gs} and the gate–drain capacitance C_{gd}, the transconductance g_m, the differential drain resistance r_{ds} (the inverse of the drain conductance g_{ds}), and the resistance R_i, while the external part of the transistor comprises the gate resistance R_G and the source/drain series resistances R_S and R_D. From the equivalent circuit, the gains of the transistor can be deduced. The intrinsic gain is defined as $G_{int} = g_m/g_{ds}$. Applying Kirchhoff's laws and the rules of two-port theory, expressions for the y parameters of the intrinsic and the extrinsic transistor $y_{11-int} \ldots y_{22-int}$ and $y_{11} \ldots y_{22}$ can be deduced, from which expressions for the current and power gains and finally for f_T and f_{max} are obtained.

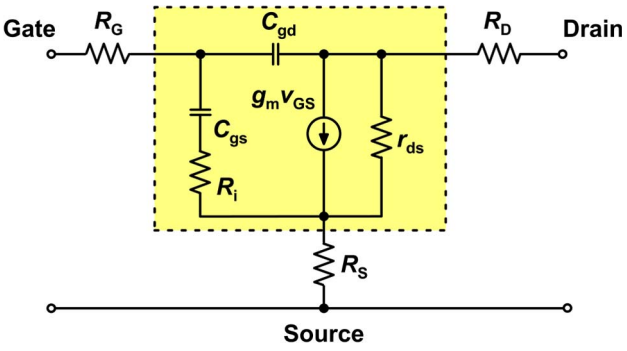

Fig. 5. *Small-signal equivalent circuit of a FET.*

The characteristic frequencies of the intrinsic transistor, $f_{T-\mathrm{int}}$ and $f_{\max-\mathrm{int}}$, read as

$$f_{T-\mathrm{int}} = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{1}$$

$$f_{\max-\mathrm{int}} = \frac{g_m}{4\pi C_{gs}} \times \frac{1}{\sqrt{g_{ds}R_i}} \tag{2}$$

and useful approximations for the corresponding extrinsic frequencies of the whole FET are [35], [37], [38]

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \frac{1}{1+g_{ds}(R_S+R_D)+\frac{C_{gd}g_m(R_S+R_D)}{C_{gs}+C_{gd}}} \tag{3}$$

$$f_{\max} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\left(g_{ds}(R_i+R_S+R_G)+g_m R_G \frac{C_{gd}}{C_{gs}}\right)^{\frac{1}{2}}}. \tag{4}$$

Simply speaking, to achieve high f_T and $f_{\max}$, the transistor's transconductance should be high and all other elements of the equivalent circuit should be as small as possible.

The elements of the intrinsic transistor as well as the gains f_T and $f_{\max}$ are sensitive to the dc bias conditions. We focus here on the drain bias dependence since it is particularly crucial for graphene transistors. Fig. 6(a) shows the dc output characteristics (drain current I_D as a function of V_{DS}) together with f_T and $f_{\max}$ for a typical RF FET.

The characteristics indicate the linear regime at low V_{DS} and the saturated regime at higher drain–source voltages. It becomes clear from the plot that at low V_{DS} (i.e., in the linear regime) f_T and $f_{\max}$ are very low and that the transistor has to be driven into saturation to achieve good RF performance. The reason for this behavior becomes clear by considering (3) and (4) together with Fig. 6(b). The small g_m and the large g_{ds} ($g_{ds} = dI_D/dV_{DS}$ is the slope of the output characteristics) at low V_{DS} automatically lead to small gains and thus to low f_T and $f_{\max}$. The fact that to arrive at the peak $f_{\max}$ the transistor has to be operated even deeper in saturation than to achieve the peak f_T already provides an indication for the important role current saturation and g_{ds} play for the power gain and $f_{\max}$ of analog/RF FETs. The main message of this discussion is that a FET inevitably must show saturation to fully exploit its speed potential.

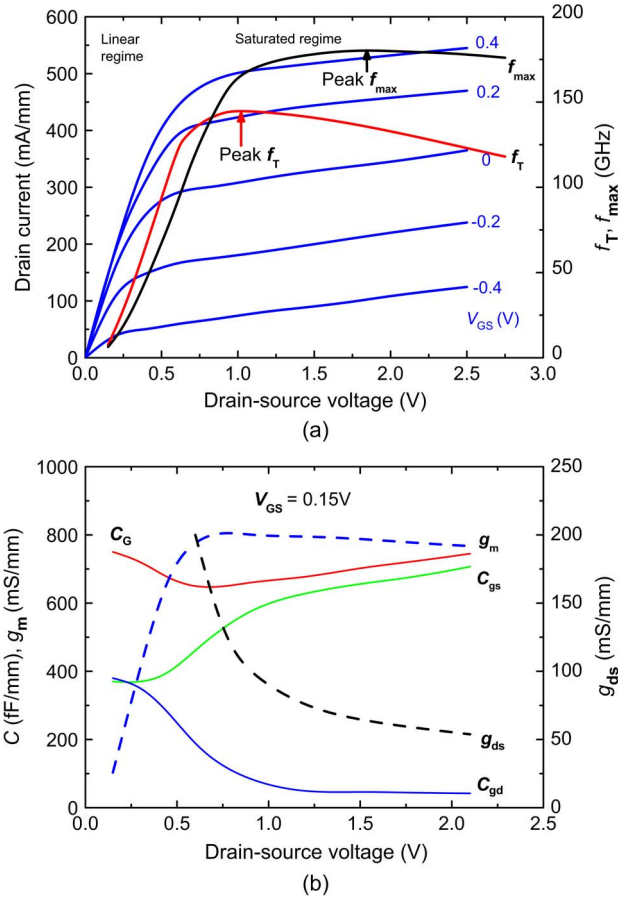

Fig. 6. *(a) Output characteristics of a GaAs pseudomorphic high electron mobility transistor (pHEMT), together with its f_T and $f_{\max}$ versus V_{DS} for the optimum gate bias (V_{GS} = 0.15 V). (b) Elements of the equivalent circuit as a function of V_{DS}, C_G is the sum of C_{gs} and C_{gd}. Data taken from [39] and [40].*

IV. RELEVANT GRAPHENE PROPERTIES

A wish list for the ideal semiconductor would include the following features: 1) sufficiently wide bandgap, combined with excellent carrier transport properties and a high thermal conductivity; 2) producible on large-diameter substrates, process friendly, and compatible with Si CMOS technology; 3) interfaces to dielectrics with good long-term stability and low defect density not affecting carrier transport in the semiconductor close to the interface; and 4) low contact resistance. Unfortunately, such a material does not exist and device engineers must always live with tradeoffs. How does graphene meet these requirements?

Natural large-area graphene is gapless and behaves like a semimetal; thus, already the first requirement is not fulfilled. Graphene's bandstructure features cone-shaped valence and conduction bands that touch each other at the K points of the Brillouin zone, as shown schematically in Fig. 7(a).

In contrast, the bands of conventional semiconductors are parabolic and separated from each other by a gap with size E_G; see Fig. 7(b). Due to the missing gap, graphene MOSFETs do not switch off, as shown in Fig. 7(c). A positive voltage V_{GS1} applied to the gate of the graphene MOSFET leads to the Fermi level position E_{F1} in the conduction band and to a pronounced n-type conduction in the graphene channel that corresponds to the drain

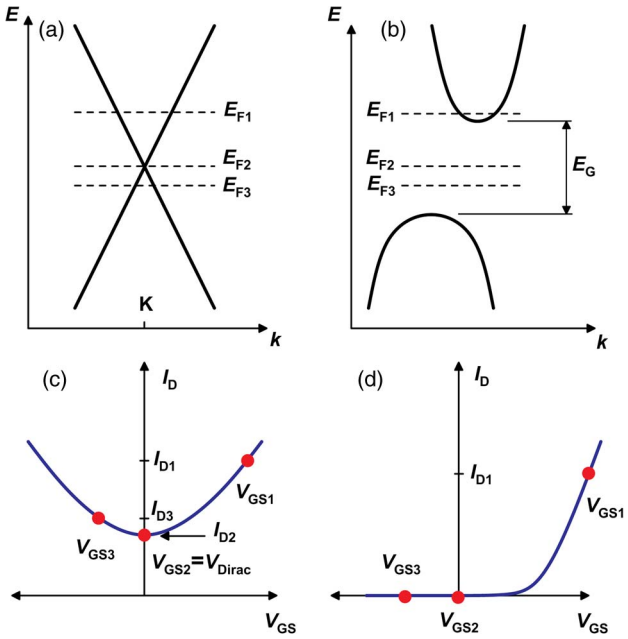

Fig. 7. *(a) Schematic band diagram of gapless large-area graphene. (b) Band diagram of an indirect semiconductor, e.g., Si. (c) Transfer characteristics of a graphene MOSFET. (d) Transfer characteristics of an n-channel Si MOSFET.*

current I_{D1}. When lowering the gate voltage, the Fermi level is shifted downward causing a decreasing electron concentration and a reduction of the drain current. At a certain gate voltage V_{GS2}, the Fermi level arrives at the energy where the valence and conduction bands meet, the so-called Dirac point. Here, carrier density and drain current show a minimum—not zero as one would expect since due to inevitable disorder electron and hole puddles occur in graphene causing a residual conductivity at the Dirac point [41]. At the Dirac point, the conductivity type changes from n to p. For negative gate voltages, such as V_{GS3}, the channel is p-type conducting and the drain current rises again. This phenomenon is called ambipolar conduction and has first been explained in [42]. The situation is fundamentally different in conventional semiconductors such as Si; see Fig. 7(b) and (d). At V_{GS1}, we have an n-type channel as in the graphene transistor. Decreasing the gate voltage shifts the Fermi level into the gap, the carrier density in the channel decreases continuously and rapidly, and the transistor switches off.

Sometimes the question arises if a graphene channel only one atomic layer thick can provide enough carries for appropriate FET operation. The answer is definitely yes. Carrier sheet densities in excess of 10^{12} cm^{-2}, i.e., similar to those in conventional FETs, are easily obtained in graphene. When modeling the gate capacitance C_G and the dependence of the sheet density on the gate voltage in graphene MOSFETs, the effect of the quantum capacitance needs to be taken into account [43]. It is not sufficient to approximate C_G by the oxide capacitance per unit area given as $C_{ox} = \varepsilon_{ox}/t_{ox}$, where ε_{ox} and t_{ox} are the dielectric constant and the thickness of the gate dielectric. Instead, for graphene MOSFETs (in particular, those with thin dielectrics) the quantum capacitance C_q connected in series with C_{ox} has to be taken into account leading to an overall gate capacitance $C_G = C_{ox} \times C_q/(C_{ox} + C_q)$ that can be significantly smaller than C_{ox}, particularly close to the Dirac point. In mathematical terms, the quantum capacitance is the derivative of the channel charge with respect to the channel potential, i.e., $C_q = dQ_{ch}/dV_{ch}$, where dV_{ch} is caused by a small variation of the gate voltage dV_{GS}. In a more phenomenological sense, C_q takes the finite density of states (DOS) of the graphene channel into account and is proportional to the DOS. The overall gate capacitance C_G would approach C_{ox} only for an infinite DOS while the DOS in graphene is not infinite but rather small.

We now come back to the bandgap issue. Although natural graphene is gapless, there are different approaches to open a gap. The first option is to form narrow graphene nanoribbons (GNRs). It has been predicted that, in GNRs, a gap with a size inversely proportional to the ribbon width can be opened and that GNRs with a width below 2 nm should show a gap in excess of 1 eV [44]. It should be noted that the origin of the bandgap in GNRs is still under debate. In addition to pure lateral confinement [44], it has been suggested that other effects, most notably Coulomb blockade [45], [46], are responsible for the formation of a gap.

Experiments revealed gaps around 300–400 meV in GNRs less than 15 nm wide [12], [47], [48]. So far it is not exactly known how wide the bandgap of the channel of a good FET should be, but rough estimations consistently suggest that a minimum gap of 360–500 meV is needed for digital logic [20], [49], [50]. While narrow GNRs would meet this target, it is extremely difficult to prepare GNRs with a defined width of a few nanometers. Narrow GNRs suffer from edge roughness affecting the gap of the ribbons along their lengths and carrier transport. The second option to open a gap is to use bilayer graphene and to apply an electric field perpendicular to the bilayer. Theoretical considerations and experiments have shown that for high fields (a few 10^4 kV/cm) gaps of up to 250 meV can be opened [51], [52]. This would at least come close to the lower limit needed for good transistors. Recently, two further options to form a gap in large-area graphene have been suggested, namely: 1) graphene growth on MgO [53]; and 2) irradiation of graphene with an ion beam [54].

Let us next discuss the carrier transport properties in graphene under diffusive conditions. If a low electric field $\mathcal{E}$ acts on a carrier, the carrier is set into motion and achieves a velocity v given by $v = \mu \times \mathcal{E}$, where μ is the mobility. For FETs with long gates, the mobility is an appropriate measure for the speed of carrier transport. In scaled FETs with nanometer gates, however, the situation is more complex. Here, the field in the channel can be very

high and much beyond the range where the concept of constant mobility is valid. At high fields, the steady-state carrier velocity saturates, and the saturation velocity becomes another important measure for carrier transport. Moreover, in short-channel FETs, nonstationary transport effects such as velocity overshoot and quasi-ballistic transport occur. Nevertheless, the mobility is not meaningless for nanometer-gate FETs, and a high mobility is still desirable [55].

Gapless large-area graphene shows high mobilities ranging from 10 000 cm^2/Vs up to more than 100 000 cm^2/Vs. The mobility depends on the carrier density n and decreases with increasing n following the relation $\mu(n) \sim n^{-b}$ where b is a fitting parameter [56], [57].

The mobility of semiconductors is inseparably connected to the bandstructure and thus to the bandgap. As a general trend, the mobility decreases with increasing bandgap. This is illustrated in Fig. 8 showing the room-temperature electron mobility for conventional semiconductors (Si, Ge, III–V compounds), carbon nanotubes, and graphene. The plot makes clear that neither GNRs nor bilayer graphene can escape from this trend. The high mobility of gapless large-area graphene declines rapidly when opening a gap in GNRs and bilayer graphene, interestingly even at a faster rate compared to conventional semiconductors. The mobility data for GNRs and bilayer graphene in Fig. 8 are simulated, and experimental mobilities are even a bit lower. For example, the highest measured GNR mobility is about 2000 cm^2/Vs at room temperature for a 20-nm ribbon with a gap around 100 meV [58]. We come to the conclusion that, in terms of electron mobility and for a given bandgap, graphene does not offer a distinct advantage over conventional semiconductors.

For holes the picture is less cloudy since in conventional semiconductors the hole mobility μ_p is significantly lower than the electron mobility μ_n. The ratio μ_p/μ_n is around 0.3 for Si, 0.05 for GaAs, and approaches 0.01 for the narrow bandgap compounds InAs and InSb, while in graphene the difference is by far not that large and the observed hole mobility may even exceed the electron mobility [22]. Moreover, bandstructure calculations for GNRs and bilayer graphene reveal a high degree of symmetry of the conduction and valence bands pointing to similar effective electron and hole masses [51], [59].

Early top-gated graphene MOS structures suffered from a degradation of the mobility after depositing the top-gate dielectric [11]. Recent reports on mobilities in top-gated graphene MOS structures of up to 24 000 cm^2/Vs show, however, that graphene MOSFETs with very high mobility can be realized [61], [62].

It is worthwhile to extend the discussion on the mobility to a comparison graphene versus the less common organic semiconductors. The traditional semiconductors mentioned in Fig. 8 are rigid materials and not useful for the emerging fields of flexible and printable electronics. In this area, commonly organic semiconductors, of which pentacene is the most popular one, are applied. Organic materials are bendable and printable, but this comes at the expense of a low mobility. Here, graphene definitely has an edge, as shown in Fig. 9.

Large-area graphene is bendable, and, recently, the deposition of graphene on flexible substrates and the use of

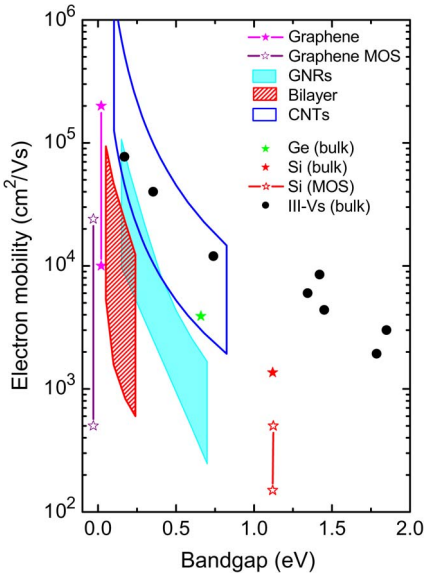

Fig. 8. *Mobility versus bandgap for different materials including pristine large-area graphene (experiment [4], [22], [60]), large-area graphene MOS channels (experiment [11], [61], [62]), graphene nanoribbons [63], [64], bilayer graphene [65], and carbon nanotubes (simulation [66], [67]). The III–V compounds, from left to right, are InSb, InAs, $In_{0.53}Ga_{0.47}As$, InP, GaAs, $In_{0.52}Al_{0.48}As$, $Al_{0.3}Ga_{0.7}As$, and $In_{0.49}Ga_{0.51}P$. The mobility for the conventional bulk semiconductors relates to undoped material.*

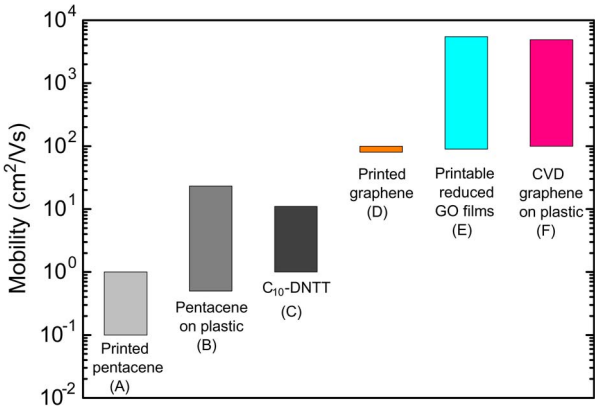

Fig. 9. *Mobility of printable and flexible graphene compared to the best reported mobilities of organic semiconductors. C_{10}-DNTT: 2,9-didecyldinaphtol [2,3-b:2′,3′-f]thieno[3,1-b]thiophene. GO: graphene oxide. Data taken from: A [68], B and C [69], D [70], E [32], F [71]–[73], and references therein.*

graphene ink for printed electronics have become fields on intensive research. While the gapless nature of graphene may be problematic for the digital part of flexible and printed circuits, due to its significantly higher mobility compared to organic semiconductors, graphene opens the door to high-frequency low-voltage flexible and printable electronic applications.

Carrier transport at high fields can be assessed in detail by evaluating the $v - \mathcal{E}$ (velocity field) characteristics [20]. For graphene, several groups have calculated $v - \mathcal{E}$ characteristics and a few reports on experimental $v - \mathcal{E}$ characteristics are available. Two key figures of high-field transport are the peak velocity (the maximum carrier velocity in semiconductors showing a negative differential mobility region in the $v - \mathcal{E}$ characteristics) and the saturation velocity carriers attain at very high fields. Experiments and theoretical studies consistently revealed saturation velocities of $3–6\times10^7$ cm/s for gapless large-area graphene [65], [74]–[76], GNRs [76], [77], and bilayer graphene [65], [76]. For comparison, III–V semiconductors show electron peak velocities between 2×10^7 cm/s (GaAs) and 4×10^7 cm/s (InAs) and the electron saturation velocity in conventional semiconductors (III–Vs, Ge, Si) is around $0.6–1\times10^7$ cm/s. This brings us to the conclusion that, regarding high-field transport, graphene in its different configurations shows an advantage over the conventional materials. It should be noted, however, that the high velocities predicted for ideal GNRs are expected to degrade seriously in the presence of rough edges [76].

The resistance between metal contacts and an underlying graphene layer is crucial for the operation of transistors and should be as low as possible. It is usually given in a normalized form in units of $\Omega \times \mu$m, i.e., resistance times contact width. By late 2009, the lowest reported metal–graphene contact resistances were in the range 400–1000 $\Omega\mu$m [78], about ten times the contact resistance in Si and III–V FETs. Since then, significant progress could be made, and, meanwhile, contact resistances in the 100–200-$\Omega\mu$m range have been demonstrated [79], [80].

Graphene is an excellent heat conductor showing a superior thermal conductivity around 30–50 W/(cmK) [81], compared to 4 W/(cmK) for copper. For circuit applications, a high thermal conductivity of the channel material is certainly desirable, although the heat transfer through the underlying substrate is more important. Graphene can be realized on different substrates, such as SiC (epitaxial graphene), oxidized Si wafers (exfoliated and transferred CVD graphene), or flexible materials. The heat generated in a graphene channel has to cross the graphene–substrate interface, thereby experiencing the interfacial thermal resistance (frequently called Kapitza resistance). Graphene–substrate interfaces show significant Kapitza resistances [82], [83]. For example, for graphene–SiC interfaces, it is more than a factor of ten larger than the Kapitza resistance of Si–SiO_2 interfaces as used in modern silicon-on-insulator structures (36×10^{-9} m^2K/W, compared to 0.5×10^{-9} m^2K/W [84]).

V. GRAPHENE TRANSISTORS

A. Classification and Basic Transistor Structures

A variety of different graphene transistor configurations has been presented during the past five years that can be categorized in different ways, as shown in Fig. 10. In the following, we review the current status of graphene transistors and start with MOSFETs having large-area gapless channels, examine their potential for analog/RF applications as well as for flexible and printable electronics, and introduce the side-gate architecture. Next, bilayer and GNR MOSFETs operating like conventional MOSFETs (i.e., no tunneling involved) are considered, followed by a short discourse on tunneling MOSFETs. Finally, vertical

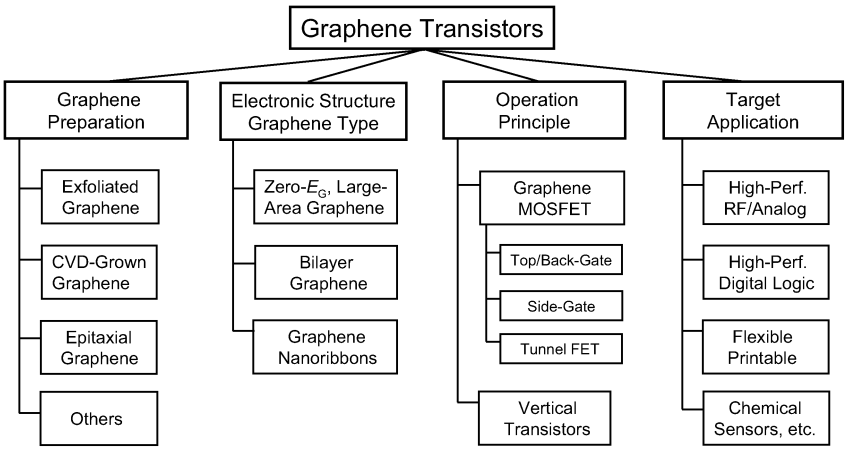

Fig. 10. *Classification schemes for graphene transistors.*

graphene transistor concepts exploiting tunneling mechanisms are briefly considered.

B. Conventional Graphene Transistors

Conventional graphene MOSFETs with large-area gapless graphene channels show ON–OFF ratios of only 2–10, much too less for complex logic circuits. Since, on the other hand, analog/RF FETs do not need to switch off, intensive work on such transistors is under way. The first graphene MOSFET with a cutoff frequency f_T in the gigahertz range has been reported in late 2008 [85]. In 2009, graphene MOSFETs with 350-nm gates and a cutoff frequency of 50 GHz have been presented [86]; in early 2010, a graphene MOSFET with a 240-nm gate showing an f_T of 100 GHz has been reported [13], soon followed by a 144-nm gate graphene MOSFET with $f_T = 300$ GHz later that year [14]. Finally, in 2012, a graphene MOSFET with a 40-nm-long gate showing 350-GHz f_T [87] and a 67-nm gate graphene MOSFET with an f_T of 427 GHz have been reported [16]. Graphene RF MOSFETs have successfully been realized using exfoliated (e.g., [14] and [86]), epitaxial (e.g., [13] and [88]), and CVD (e.g., [89] and [90]) graphene.

Fig. 11 shows the cutoff frequency of the best graphene MOSFETs reported so far, together with the f_T performance of competing RF FET types. The record f_T data of the competing FETs are 688 GHz for a 40-nm GaAs mHEMT [91] and 644 GHz for a 30-nm InP HEMT [92], 485 GHz for a 29-nm Si MOSFET [93], 152 GHz for a 100-nm GaAs pHEMT [94], and 153 GHz for a 100-nm carbon nanotube (CNT) MOSFET [95]. For the sake of clarity, we noted that in terms of InP HEMT, GaAs mHEMT, and GaAs pHEMT, the material, i.e., InP or GaAs, refers to the substrate and not to the channel. The channels of InP HEMTs and GaAs mHEMTs consist of InAs or $In_xGa_{1-x}As$ with high In content x, while GaAs pHEMTs have $In_xGa_{1-x}As$ channel with lower In content (typically $x < 0.25$).

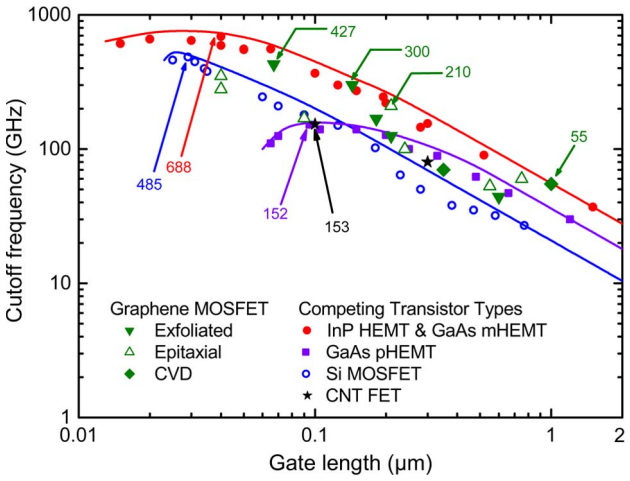

Fig. 11. *Cutoff frequency of graphene MOSFETs versus gate length L. Also shown is the f_T performance of the best CNT FET and that of three classes of conventional RF FETs: 1) InP HEMTs and GaAs mHEMTs (metamorphic HEMT); 2) GaAs pHEMTs; and 3) Si MOSFETs. The numbers indicate f_T in gigahertz. Updated from [20].*

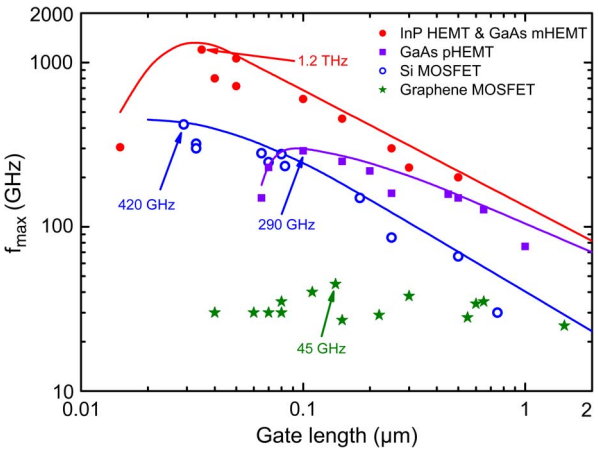

Fig. 12. *Maximum frequency of oscillation of graphene MOSFETs versus gate length. Also shown is the f_{max} performance of three classes of competing RF FETs: InP HEMTs and GaAs mHEMTs, GaAs pHEMTs, and Si MOSFETs.*

Several conclusions can be drawn from Fig. 11.

1) For long gate lengths (above 0.2 μm), the f_T data for all transistor types show a $1/L$ dependence.
2) For conventional RF FETs and $L > 0.2$ μm, the cutoff frequency increases with increasing channel mobility [96]. Si MOSFETs show channel mobilities of a few 100 cm^2/Vs compared to about 6000 cm^2/Vs for GaAs pHEMTs and above 10 000 cm^2/Vs for InP HEMTs and GaAs mHEMTs with their high-In-content channels.
3) Down to about 100-nm gate length, graphene MOSFETs compete extremely well with InP HEMTs and GaAs mHEMTs (note that these HEMTs are the fastest RF FETs at all) and this is the case for graphene transistors using exfoliated [14], epitaxial [97], and CVD-grown [89] graphene.

In contrast to their impressing f_T performance, graphene MOSFETs behave rather poor in terms of the maximum frequency of oscillation f_{max}, as shown in Fig. 12. The highest f_{max} data reported so far for graphene MOSFETs is in the range of 30–45 GHz only [87], [98], [99], compared to several hundreds of gigahertz for the competing FET types and a record f_{max} above 1 THz for an InP HEMT with 35-nm gate length [100]. Another remarkable feature of Fig. 12 is the fact that, in contrast to the competing transistor types, f_{max} of graphene MOSFETs does not show a distinct gate-length dependence.

We note that the f_T and f_{max} data of all transistors, shown in Figs. 11 and 12, are de-embedded data.

De-embedding is common practice in RF device characterization and means that the measured results are corrected to exclude parasitics of the measurement setup and probe pads from the RF transistor parameters. Specific of RF graphene MOSFETs, in particular those based on exfoliated graphene, is that their channel widths are small compared to RF Si MOSFETs and III–V HEMTs. This is why the as-measured and the de-embedded RF parameters of graphene MOSFETs frequently differ significantly, much more than for conventional RF FETs. This makes the de-embedding procedure for graphene MOSFETs with small channel width very delicate.

The contradiction of very competitive f_T and poor $f_{\max}$ reminds the situation of RF Si MOSFETs before the year 2000 [35]. At that time, RF Si MOSFETs suffered from unacceptably high gate resistances that deteriorate $f_{\max}$ [see (4)] but have no effect on f_T [see (3)]. For graphene MOSFETs, however, the gate resistance is *not* the dominant effect causing the poor $f_{\max}$. Instead, the large drain conductance g_{ds} caused by the weak and unsatisfying saturation of the drain current, possibly combined with too high source–drain series resistances, deteriorate seriously their power gain and $f_{\max}$ [101].

An inspection of (3) and (4) shows that both f_T and $f_{\max}$ are affected by g_{ds}. Thus, the question arises why graphene MOSFETs show very high f_T values while the $f_{\max}$ values are so low. We get a first hint from (1) and (2) for $f_{T-\mathrm{int}}$ and $f_{\max-\mathrm{int}}$ of the intrinsic transistor. Clearly, the cutoff frequency of the intrinsic transistor is not affected by g_{ds} at all and a high $f_{T-\mathrm{int}}$ is possible even in the presence of a large g_{ds}, while the maximum frequency of oscillation of the intrinsic transistor is proportional to $1/\sqrt{g_{ds}}$ and can become very small for large g_{ds}.

The interaction of g_{ds} and the source–drain series resistances affects the cutoff frequency of the extrinsic transistor by the term $g_{ds} \times (R_S + R_D)$ in the denominator of (3), but this is only a second-order effect compared to the strong effect of g_{ds} on both $f_{\max-\mathrm{int}}$ and $f_{\max}$ [102]. Thus, good current saturation and a small g_{ds} are much more important for power gain and $f_{\max}$ than for current gain and f_T. Even without considering the whole equivalent circuit, the g_{ds} problem of graphene FETs for analog applications becomes obvious by considering the intrinsic gain $G_{\mathrm{int}} = g_m/g_{ds}$. Due to the large g_{ds}, the intrinsic gain of graphene MOSFETs is significantly lower than that of Si MOSFETs and III–V HEMTs.

Since a small g_{ds} can only be achieved if the transistor operates in saturation, it is important to understand that the physics of current saturation in graphene FETs is different from that in conventional FETs. This was first discussed descriptively by Meric *et al.* [42]. Later, several groups have investigated this effect in more detail by either extending the Meric model [103], [104] or by modifying models originally developed for Si MOSFETs [105] or HEMTs [106]. In a conventional FET operated in saturation, the carrier density in the channel continuously decreases toward the drain leading to a high-field, high-resistance pinch-off region in the drain-sided portion of the channel. In a graphene FET, the carrier density decreases and the field increases initially when moving in the channel from source toward the drain as well. At some point in the channel, the potential conditions correspond to those of the Dirac point. Here, the field becomes maximal and the conductivity type changes (from *n* to *p* or *vice versa*). Further toward the drain, however, the carrier density increases again and the field goes down. This is schematically shown in Fig. 13(a), and the resulting output characteristics with the peculiar saturation behavior of graphene FETs are depicted in Fig. 13(b). It should be noted that the reason for this behavior is the missing bandgap of the graphene channel. The series resistances R_S and R_D have an effect on the saturation behavior as well.

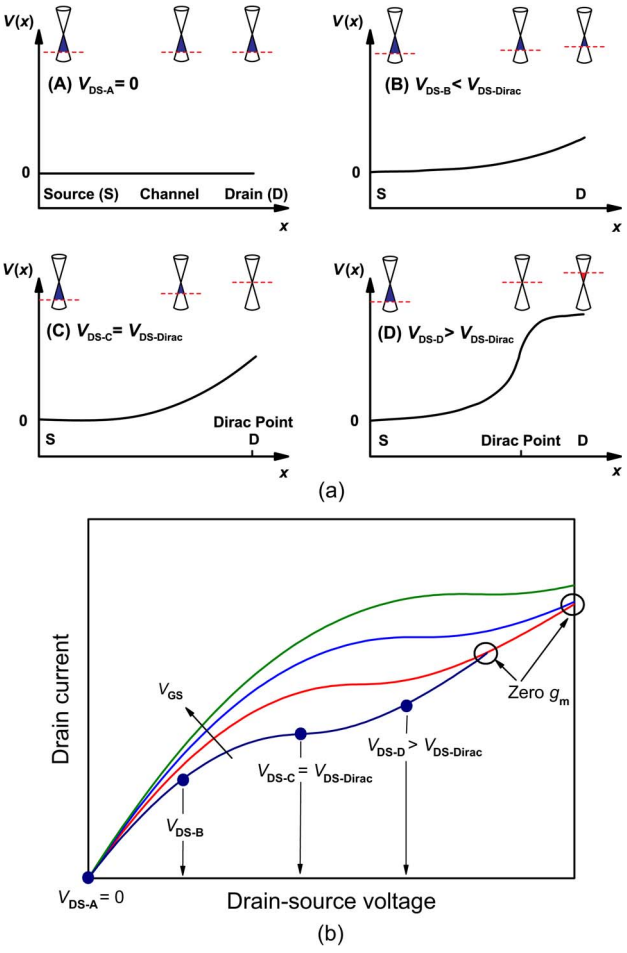

Fig. 13. *(a) Conditions in the channel of an n-channel graphene MOSFET. Shown are the potential distribution along the channel and the Fermi energy (red dashed line) at three positions in the channel. The drain–source voltage is (A) zero, (B) positive but still below $V_{DS\text{-Dirac}}$ (the voltage to reach the Dirac condition), (C) equal to $V_{DS\text{-Dirac}}$, and (D) beyond $V_{DS\text{-Dirac}}$. (b) Schematic output characteristics of the transistor indicating the four operating points shown in (a); after [20].*

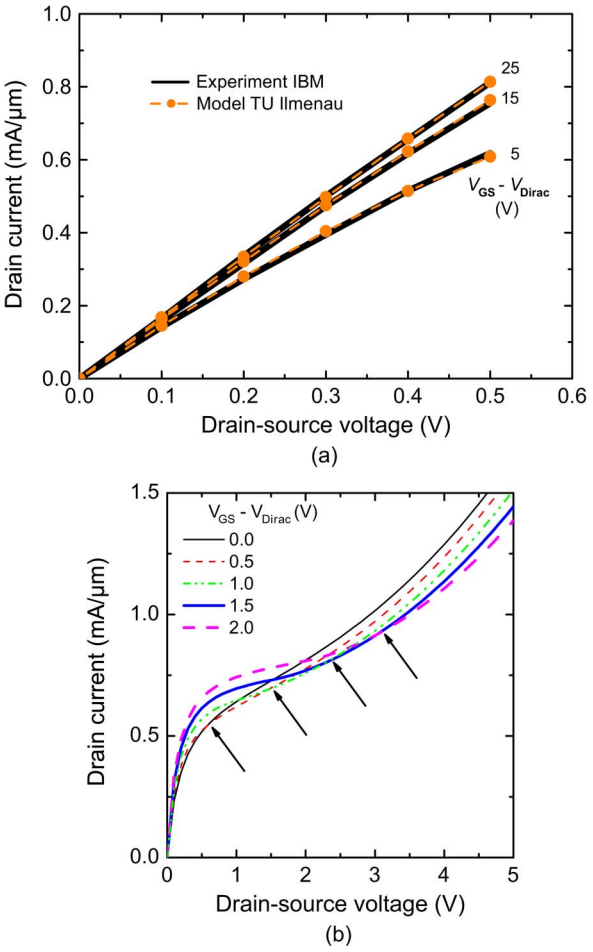

Fig. 14. *(a) Measured and simulated output characteristics of a 70-nm back-gate graphene MOSFET with source–drain contact resistances of 285 $\Omega\mu$m. (b) Simulated output characteristics of the same transistor assuming zero contact resistance.*

Series resistances always deteriorate transistor performance, and this can become dramatic in short-channel FETs [107]. It can go so far that the series resistances fully overshadow the operation of the intrinsic transistor, degrade gain to an unacceptable extent [108], and fully obscure current saturation [109].

We now consider the saturation in more detail and follow the approach presented in [109]. To this end, we take the structure and contact resistance of the 70-nm transistor from [109], use our own transistor model [103], and simulate the output characteristics of the device. Fig. 14(a) shows excellent agreement with the measured data from [109]. The characteristics indicate no saturation but an almost linear shape since the large contact resistance dominates transistor operation. Next, we model the transistor assuming zero contact resistance. As shown in Fig. 14(b), now the transistor shows saturation. However, the saturation behavior differs from that of Si MOSFETs or III–V HEMTs and follows the peculiar behavior qualitatively sketched in Fig. 13(b). After the onset of current saturation, the slope of the I–V curves increases again and an effect sometimes called second linear regime occurs. This leads to the situation that the curves for different gate–source voltages cross each other at certain drain–source voltages. At the intersections [marked by arrows in Fig. 14(b)], the transconductance g_m is zero, and beyond the intersection it becomes negative. This is a dramatic feature since a zero g_m means that the gain of the transistor is zero. Such intersecting current-voltage characteristics are not modeling artifacts but are observed frequently in experiments [110], [111].

The preceding discussions lead us to the conclusion that, to achieve competitive power gain and $f_{\max}$ performance of graphene transistors, first, current saturation is needed and a channel having a bandgap is desirable, even if this comes at the expense of a degraded mobility.

We note that a recent simulation study suggested that graphene MOSFETs, in spite of the saturation problem, should be able to achieve high $f_{\max}$. Assuming small but reasonable source/drain series and gate resistances, the study predicted 400–600 GHz $f_{\max}$ for 50-nm gate graphene MOSFETs [112]. Moreover, recently, a region of negative differential resistance, i.e., negative output conductance, in the output characteristics of graphene MOSFETs has been observed experimentally and modeled [113], [114]. More work in this direction is desirable since it could lead to deeper insights in the saturation mechanisms in graphene transistors and to the definition of appropriate bias conditions and design rules to improve the saturation behavior.

In contrast to the large amount of f_T and $f_{\max}$ data available, so far, no data on the RF noise figure and output power have been reported for graphene transistors. Furthermore, no experimental RF data for bilayer and GNR MOSFETs are available yet, while it would certainly be worth to evaluate the RF potential of these transistors.

Recently, graphene RF circuits have been successfully fabricated. In [15], the first integrated graphene RF circuit, a frequency mixer operating at frequencies up to 10 GHz where all components (a graphene transistor, inductors, interconnects) are integrated on a SiC wafer, has been reported. Another promising route recently pursued is to exploit the gapless nature of graphene and the resulting ambipolarity instead of trying to circumvent it [115], [116]. RF mixers [117], [118] and frequency multipliers [72], [119] based on the ambipolar conduction occurring in gapless graphene channels have been realized. These circuits are simpler and need fewer components than mixers and multipliers based on conventional transistors.

Impressing results have been obtained with graphene transistors on flexible substrates. In particular, the RF performance of such transistors with f_T and $f_{\max}$ beyond 1 GHz is remarkable [71], [72], [120]. A recent highlight is a 500-nm gate graphene MOSFET on polyethylene naphthalate substrate with an f_T of 10.7 GHz and an $f_{\max}$

of 3.7 GHz [120]. These transistors are much faster than competing organic transistors on flexible substrate and hold the potential for gigahertz operation on plastic. Another promising application for graphene is printable electronics. Printed graphene transistors have been reported [32], [70] that could pave the way for graphene to the emerging field of low-cost printed circuits that can be fabricated without lithography.

All transistors discussed so far in this section are graphene MOSFETs with a top gate. If oxidized doped Si wafers are used as substrate, the wafer can act as a second gate called back gate and the SiO_2 between the wafer and the graphene channel acts as back-gate dielectric. Recently, an alternative gate arrangement where the gate is not located above (top gate) or underneath (back gate) the graphene channel, but in the same plane as the channel (side by side to the channel), has been proposed [121], [122]. The compelling feature of this side-gate design is that it does not require the deposition of a top-gate dielectric. Although the lateral separation between the side gate and the channel is large compared to the vertical distance between the gate and the channel, i.e., the gate oxide thickness, in a top-gate MOSFET, the side-gate control of the channel can be very effective, in particular if the device is located on a substrate with a high dielectric constant, such as SiC. In [122], an epitaxial graphene side-gate FET with a transconductance exceeding 500 mS/mm has been reported.

C. Graphene Bilayer and Nanoribbon MOSFETs

A limited number of publications on experimental bilayer graphene MOSFETs can be found in the literature [123]–[126]. For graphene bilayer FETs, large-area graphene can be used to get semiconducting channels, and narrow ribbons are not needed. To achieve a field-induced gap opening, a specific stacking of the two layers of bilayer graphene called Bernal stacking is required. Here, half of the atoms of one layer are located above the atoms of the second layer, while the other half of the atoms lie precisely above the empty center of the hexagons of the other layer [127]. So far, Bernal-stacked bilayer graphene for FET channels has been prepared exclusively by mechanical exfoliation. While it is not clear if bilayer graphene showing field-induced gap opening can be produced by other methods, recent experiments provide indications that Bernal-stacked bilayer graphene can be obtained by CVD growth [128], [129].

According to theoretical considerations, the gap in bilayer graphene FETs is limited to about 150 meV [130], much less than 0.4 eV needed for good switch-off. Indeed, the gap observed in experimental bilayer FETs is in the range of 40–130 meV and the ON–OFF ratios are only about 100 [123], [124]. This seriously limits the prospects of bilayer graphene FETs for logic applications. So far, no experimental RF performance data for bilayer graphene MOSFETs has been published. Recent dc results for bilayer MOSFETs indicate a significantly improved current saturation and an intrinsic gain of 35 [126].

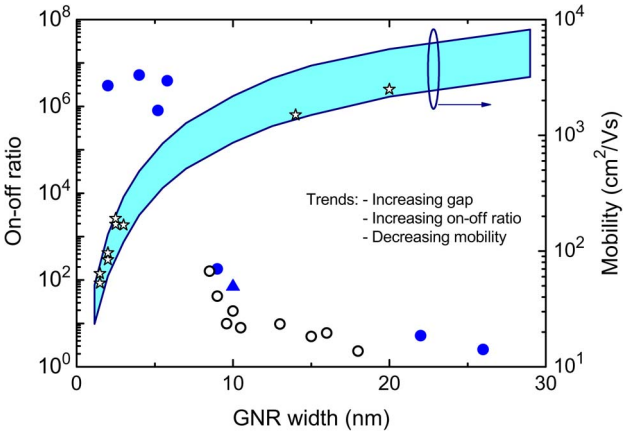

Fig. 15. *ON–OFF ratio and mobility of experimental GNR MOSFETs versus ribbon width. ON–OFF ratio: data taken from [131] (triangle), [12], [132] (full circles), and [133] (open circles). Mobility: experimental data (stars) taken from [58], [132], and [137], and simulated data (shaded area) taken from [76].*

Regarding switching behavior, GNR MOSFETs are more promising. GNR MOSFETs with top-gate [131] and back-gate control [12], [132], [133] and ribbon widths down to 2 nm have been fabricated. These devices show, depending on the width, ON–OFF ratios in excess of 10^6, as indicated in Fig. 15. It has been discussed in qualitative terms already in 2007 that GNR MOSFETs are expected to show excellent electrostatics and much better immunity against short-channel effects than Si MOSFETs [134]. A quantitative estimation of the scale length λ of SOI MOSFETs (λ_{SOI}) and GNR MOSFETs (λ_{GNR}) with thin gate dielectrics revealed a ratio $\lambda_{GNR}/\lambda_{SOI}$ of 0.3 to 0.4 showing that GNR MOSFETs are much less vulnerable to short-channel effects and should be scalable to shorter gate lengths than Si MOSFETs [34]. Thus, the advantage of GNR MOSFETs compared to conventional FETs is not the mobility but rather the better electrostatic integrity due to the ultimately thin graphene channel.

As shown in Fig. 15, narrow ribbons with widths below 5 nm are needed to achieve ON–OFF ratios of 10^4–10^7, as required for logic. Given the current status of semiconductor processing technology, this represents a serious challenge, and a high-volume fabrication of logic ICs with such narrow-width GNR MOSFETs is rather unlikely in the near future. Moreover, the mobility in such narrow ribbons is much smaller than in large-area graphene. Finally, simulations have shown that edge effects lead to huge differences in the characteristics of GNR MOSFETs with identical design but slightly different edge configurations, significantly reduced I_{on}, increased I_{off}, and consequently seriously degraded ON–OFF ratios [130], [135], [136]. Thus, currently neither GNR nor bilayer graphene

MOSFETs are a satisfying choice to replace the Si MOSFET in high-performance logic.

An interesting option for graphene logic transistors is the concept of the tunnel MOSFET. In tunnel FETs, the gate voltage controls the band-to-band tunneling across the source-channel junction instead of the carrier concentration in the channel as in conventional MOSFETs. This operating principle allows subthreshold swings much below the 60-mV/dec limit of conventional MOSFETs leading to steeper subthreshold characteristics and better switch-off. Si and III–V tunnel MOSFETs are currently intensively investigated, and experimental devices have been presented [138]. Since a precondition for proper tunnel MOSFET operation is a semiconducting channel, either GNRs or bilayer graphene must be used for graphene tunnel FETs. Experimental graphene tunnel FETs have not been realized yet, but their potential has been investigated by device simulations [130], [139], [140]. While GNR tunnel MOSFETs suffer from the same problems as conventional GNR MOSFET (narrow ribbons needed, edge roughness effects), the bilayer graphene tunnel MOSFET shows promise since narrow ribbons are not needed, the limited gap opening should be sufficient to enable safe switch-off, and high ON–OFF ratios may be possible thanks to the subthreshold swing below 60 mV/dec [130].

D. Vertical Graphene Transistors

The graphene transistors discussed so far are essentially planar device structures where the current flows along the graphene sheet parallel to the substrate surface. Recently, alternative graphene transistor concepts with vertical structure have been proposed where the current, strictly speaking a tunnel current, flows normal to the substrate surface. In the following, three of these concepts are introduced.

In 2009, the bilayer pseudospin field-effect transistor (BiSFET) has been proposed [141]. As shown in Fig. 16, it consists of two graphene monolayers, one *p*-type and the other *n*-type conducting, separated from each other by a thin tunnel dielectric. In the active device region, both graphene layers are electrostatically coupled to a gate (e.g., *p*-type graphene to a top gate and *n*-type graphene to a bottom gate) through a thicker gate dielectric, and outside the active region both graphene layers have a metallic contact.

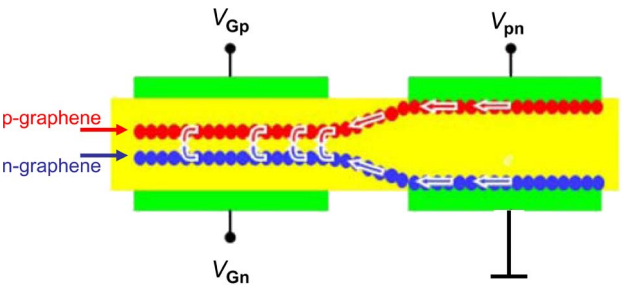

Fig. 16. *Schematic of a BiSFET, from [143].*

Under certain conditions (gate biases V_{Gp} and V_{Gn}, tunnel dielectric design, applied voltage V_{pn}), the holes of the upper graphene layer pair with the electrons of the lower graphene and form a condensate. If this happens, the originally large tunnel resistance between the graphene layers reduces dramatically to such an extent that the layers are effectively shorted and a pronounced tunnel current can flow. With increasing V_{pn}, the tunnel current first increases and reaches a maximum, while at higher V_{pn}, the condensate is destroyed and the current decreases. It should be noted that this tunneling mechanism differs from conventional tunneling through a barrier where the tunnel current increases continuously for increasing voltage. The power consumption of BiSFET logic gates is expected to be much lower compared to Si CMOS logic [142]. So far, however, and in spite of numerous attempts, an experimental manifestation of BiSFETs is still missing. Nevertheless, the concept has gained enough attention to be mentioned already in the 2009 ITRS edition.

Another graphene-based vertical tunnel transistor has been proposed by Britnell *et al.* recently [144]. It consists of two graphene layers (source and drain) separated by a thin (only a few atomic layers thick) boron nitride (BN) tunneling barrier. This graphene–BN–graphene layer sequence is sandwiched between two further BN layers, and the entire structure is located on an oxidized doped Si wafer that acts as the gate. Applying a voltage between the two graphene layers causes a tunnel current through the BN tunnel barrier, and by the gate voltage applied to the Si wafer, the amount of the tunnel current can be controlled. Experimental devices of this type with ON–OFF ratios around 50 have been realized, and by optimizing the device structure, ON–OFF ratios exceeding 10^4 should be possible.

Finally, a graphene transistor that shows parallels to metal-base hot-electron transistors has been proposed [145]. The heart of this device is a graphene layer serving as the transistor's base (in [145], the contact terminology of bipolar transistors is used) and sandwiched between an emitter-base and a base-collector insulator. Depending on the base-emitter voltage, the transistor is either off (no emitter-collector current flows) or a Fowler–Nordheim tunnel current flows through the emitter-base insulator and through the atomically thin graphene base to the collector. While experimental devices of this type have not been reported yet, simulations predict saturated output characteristics and very high cutoff frequencies [145]. Thus, this type of device shows promise for analog/RF applications.

Currently, the potential of the three vertical transistor structures discussed above cannot be assessed reliably. Nevertheless, they represent alternatives to the graphene MOSFET, indicate that the graphene MOSFET is by far not

the only option for graphene-based transistors, and show that research toward novel graphene devices beyond the MOSFET is underway.

VI. CONCLUSION AND OUTLOOK

Graphene transistors comprise a quite young class of devices compared to Si MOSFETs and III–V FETs that have been investigated for decades. Given the short history of graphene transistors, their current performance is impressing, regardless of the different problems still to be solved, and further progress is expected. It is always difficult to make serious predictions on the future progress in dynamic fields such as graphene and of applications that may arise from them. Nevertheless, we venture a precautious prognosis here.

Currently, we see many activities focused on using graphene for the well-established areas of RF amplifiers and CMOS-like digital logic. Here, graphene must compete with the conventional semiconductors and the missing gap is a serious problem. Moreover, future graphene MOSFETs and high-performance logic ICs will suffer from the same fundamental problems as Si MOSFETs and CMOS ICs, i.e., gate and source-to-drain tunneling, variability, parasitic resistances and capacitances, and power consumption. The best channel material does not help if the external parasitics dominate FET operation. In [146], the effect of the parasitics on graphene MOSFETs has been investigated. It has been shown that the performance of a 210-nm gate transistor is seriously affected by the parasitics and that the intrinsic device contributes with only 20% to the overall delay time $\tau = 1/(2\pi f_T)$. While [146] focused on an RF FOM, a similar tendency can be assumed for logic transistors. A successor of the Si MOSFET for future high-performance logic will most likely be an entirely new device based on an alternative operating principle. Presumably, it will be not sufficient to stay with the MOSFET as the basic building block for logic circuits and only change the channel material.

Therefore, we do not expect to see graphene MOSFETs in commercial high-performance logic and ultrafast RF circuits in the near- and medium-term future. A key issue for graphene is to open a gap of defined size with a reliable approach compatible to standard semiconductor processing. For logic applications, a gap of 0.4 eV or larger will be needed, while for RF transistors, a smaller gap that improves current saturation would already help.

A promising route for graphene, on the other hand, is research in directions where the unique properties of graphene can be exploited. Three areas in this respect are devices for a beyond-CMOS logic, device and circuit concepts taking advantage of the ambipolar conduction in graphene (e.g., for nonlinear analog/RF circuits), and the application of graphene transistors on flexible substrates and for printable electronics.

Graphene is undoubtedly the best-known 2-D material, but by far not the only one [147], [148]. Already in 2005, the Novoselov–Geim group reported the preparation of single-layer materials other than graphene [149]. It has been shown that semiconducting single layers of different transition metal dichalcogenides, e.g., MoS_2, $MoSe_2$, $MoTe_2$, and WS_2, can be produced by mechanical [150] and/or liquid [151] exfoliation. Recently, the first experimental MoS_2 MOSFETs have been demonstrated, e.g., [152] and [153]. These devices show reasonable mobilities and excellent switch-off. Theoretical studies qualitatively confirm the experimental results and predict very high ON–OFF ratios and excellent immunity to short-channel effects for MOSFETs with monolayer dichalcogenide channels [154], [155].

We expect that 2-D materials, most notably graphene but others like dichalcogenides as well, will remain a hot topic and that these materials will find their place in future electronics. ■

Acknowledgment

The author would like to thank J. Pezoldt for processing graphene and MoS_2 devices, T. Palacios for fruitful discussions on the prospects of graphene, and D. Akinwande for helpful comments and providing data before publication.

REFERENCES

[1] G. E. Moore, "No exponential is forever: But 'Forever' can be delayed," in *Dig. Tech Papers Int. Solid-State Circuits Conf.*, 2003, pp. 20–23.

[2] ITRS—The International Technology Roadmap for Semiconductors. [Online]. Available: http://www.itrs.net

[3] S. Damaraju, V. George, S. Jahagirdar, T. Khondker, R. Milstrey, S. Sarkar, S. Siers, I. Stolero, and A. Subbiah, "A 22 nm IA multi-CPU and GPU system-on-chip," in *Dig. Tech Papers Int. Solid-State Circuits Conf.*, 2012, pp. 56–57.

[4] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, pp. 666–669, 2004.

[5] C. Berger, Z. Song, T. Li, X. Li, A. Y. Ogbazghi, R. Feng, Z. Dai, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, "Ultrathin epitaxial graphite: 2D electron gas properties and a route toward graphene-based nanoelectronics," *J. Phys. Chem. B*, vol. 108, pp. 19912–19916, 2004.

[6] P. R. Wallace, "The band theory of graphite," *Phys. Rev.*, vol. 71, pp. 622–634, 1947.

[7] H. P. Boehm, A. Clauss, G. O. Fischer, and U. Hofmann, "Dünnste Kohlenstoff-Folien," *Z. Naturforschg.*, vol. 17b, pp. 150–153, 1962.

[8] J. W. May, "Platinum surface LEED rings," *Surf. Sci.*, vol. 17, pp. 267–270, 1969.

[9] A. J. van Bommel, J. E. Crombeen, and A. van Tooren, "LEED and Auger electron observations of the SiC(0001) surface," *Surf. Sci.*, vol. 48, pp. 463–472, 1975.

[10] H.-P. Boehm, R. Setton, and E. Stumpp, "Nomenclature and terminology of graphitic intercalation compounds," *Pure Appl. Chem.*, vol. 66, pp. 1893–1901, 1994.

[11] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A graphene field-effect device," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 282–284, Apr. 2007.

[12] X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, "Chemically derived, ultrasmooth graphene nanoribbon semiconductors," *Science*, vol. 319, pp. 1229–1232, 2008.

[13] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, "100-GHz transistors from wafer-scale epitaxial grapheme," *Science*, vol. 327, p. 662, 2010.

[14] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, and X. Duan, "High-speed graphene transistors

with a self-aligned nanowire gate," *Nature*, vol. 467, pp. 305–308, 2010.

[15] Y.-M. Lin, A. Valdes-Garcia, S.-J. Han, D. B. Farmer, I. Meric, Y. Sun, Y. Wu, C. Dimitrakopoulos, A. Grill, P. Avouris, and K. A. Jenkins, "Wafer-scale graphene integrated circuit," *Science*, vol. 332, pp. 1294–1297, 2011.

[16] R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y.-C. Lin, S. Jiang, Y. Huang, and X. Duan, "High-frequency self-aligned graphene transistors with transferred gate stacks," *Proc. Nat. Acad. Sci.*, vol. 109, pp. 11588–11592, 2012.

[17] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nature Mater.*, vol. 6, pp. 183–191, 2007.

[18] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev. Mod. Phys.*, vol. 81, pp. 109–162, 2009.

[19] P. Avouris, "Graphene: Electronic and photonic properties and devices," *Nano Lett.*, vol. 10, pp. 4285–4294, 2010.

[20] F. Schwierz, "Graphene transistors," *Nature Nanotechnol.*, vol. 5, pp. 487–496, 2010.

[21] Web of Knowledge. [Online]. Available: http://apps.webofknowledge.com/

[22] A. S. Mayorov, R. V. Gorbachev, S. V. Morozov, L. Britnell, R. Jalil, L. A. Ponomarenko, P. Blake, K. S. Novoselov, K. Watanabe, T. Taniguchi, and A. K. Geim, "Micrometer-scale ballistic transport in encapsulated graphene at room temperature," *Nano Lett.*, vol. 11, pp. 2396–2399, 2011.

[23] E. V. Castro, H. Ochoa, M. I. Katsnelson, R. V. Gorbachev, D. C. Elias, K. S. Novoselov, A. K. Geim, and F. Guinea, "Limits on charge carrier mobility in suspended graphene due to flexural phonons," *Phys. Rev. Lett.*, vol. 105, 2010, 266601.

[24] N. Savage, "Super carbon," *Nature*, vol. 483, pp. S30–S31, 2012.

[25] R. Van Noorden, "Beyond sticky tape," *Nature*, vol. 483, pp. S32–S33, 2012.

[26] K. Bourzac, "Back to analogue," *Nature*, vol. 483, pp. S34–S36, 2012.

[27] N. Savage, "Come into the light," *Nature*, vol. 483, pp. S38–S39, 2012.

[28] P. Gwynne and T. Palacios, "Taking charge," *Nature*, vol. 483, pp. S40–S41, 2012.

[29] M. Segal, "Learning from silicon," *Nature*, vol. 483, pp. S43–S44, 2012.

[30] G. Jo, M. Choe, S. Lee, W. Park, Y. H. Kahng, and T. Lee, "The application of graphene as electrodes in electrical and optical devices," *Nanotechnology*, vol. 23, 2012, 112001.

[31] B. J. Kim, H. Jang, S.-K. Lee, B. H. Hong, J.-H. Ahn, and J. H. Cho, "High-performance flexible graphene field effect transistors with ion gel gate dielectrics," *Nano Lett.*, vol. 10, pp. 3464–3466, 2010.

[32] S. Wang, P. K. Ang, Z. Wang, A. L. L. Tang, J. T. L. Thong, and K. P. Loh, "High mobility, printable, solution-processed graphene electronics," *Nano Lett.*, vol. 10, pp. 92–98, 2010.

[33] Q. Zhang, Y. Lu, H. G. Xing, S. J. Koester, and S. O. Koswatta, "Scalability of atomic-thin-body (ATB) transistors based on graphene nanoribbons," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 531–533, Jun. 2010.

[34] Q. Zhang, Y. Lu, G. H. Xing, C. A. Richter, S. J. Koester, and S. O. Koswatta, "Graphene nanoribbon schottky-barrier FETs for end-of-roadmap CMOS: Challenges and opportunities," in *Proc. Device Res. Conf.*, 2010, pp. 75–76.

[35] F. Schwierz, H. Wong, and J. J. Liou, *Nanometer CMOS*. Singapore: Pan Stanford, 2010.

[36] D. Das and J. Appenzeller, "On the importance of bandgap formation in graphene for analog device applications," *IEEE Trans. Nanotechnol.*, vol. 10, no. 5, pp. 1093–1098, Sep. 2011.

[37] P. Wolf, "Microwave properties of a Schottky-barrier field-effect transistor," *IBM J. Res. Develop.*, vol. 14, pp. 125–141, 1970.

[38] P. J. Tasker and B. Hughes, "Importance of source and drain resistance to the maximum f_T of millimeter-wave MODFETs," *IEEE Electron Device Lett.*, vol. 10, no. 7, pp. 291–293, Jul. 1989.

[39] B. Hughes and P. J. Tasker, "Bias dependence of the MODFET intrinsic model elements values at microwave frequencies," *IEEE Trans. Electron Devices*, vol. 36, no. 10, pp. 2267–2273, Oct. 1989.

[40] L. D. Nguyen, P. J. Tasker, D. C. Radulescu, and L. F. Eastman, "Design, fabrication, characterization of ultra high speed AlGaAs/InGaAs MODFETs," in *Tech. Dig. Int. Electron Devices Meeting*, 1988, pp. 176–179.

[41] J. Martin, N. Akerman, G. Ulbricht, T. Lohmann, J. H. Smet, K. von Klitzing, and A. Yacoby, "Observation of electron-hole puddles in graphene using scanning single-electron transistor," *Nature Phys.*, vol. 4, pp. 144–148, 2007.

[42] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nature Nanotechnol.*, vol. 3, pp. 654–659, 2008.

[43] T. Fang, A. Konar, H. Xing, and D. Jena, "Carrier statistics and quantum capacitance of graphene sheets and ribbons," *Appl. Phys. Lett.*, vol. 91, 2007, 092109.

[44] L. Yang, C.-H. Park, Y.-W. Son, M. L. Cohen, and S. G. Louie, "Quasiparticle energies and band gaps in graphene nanoribbons," *Phys. Rev. Lett.*, vol. 99, 2007, 186801.

[45] F. Sols, F. Guinea, and A. H. Castro Neto, "Coulomb blockade in graphene nanoribbons," *Phys. Rev. Lett.*, vol. 99, 2007, 166803.

[46] M. Han, J. C. Brant, and P. Kim, "Electron transport in disordered graphene nanoribbons," *Phys. Rev. Lett.*, vol. 104, 2010, 056801.

[47] M. Y. Han B. Özyilmaz, Y. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," *Phys. Rev. Lett.*, vol. 98, 2007, 206805.

[48] P. Kim, M. Y. Han, A. F. Young, I. Meric, and K. L. Shepard, "Graphene nanoribbon devices and quantum heterojunction devices," in *Tech. Dig. Int. Electron Devices Meeting*, 2009, pp. 241–244.

[49] K. Kim, J.-Y. Choi, S.-H. Cho, and H.-J. Chung, "A role for graphene in silicon-based semiconductor devices," *Nature*, vol. 479, pp. 338–344, 2011.

[50] D. Reddy, L. F. Register, G. D. Carpenter, and S. K. Banerjee, "Graphene field-effect transistors," *J. Phys. D, Appl. Phys.*, vol. 44, 2011, 313001.

[51] E. V. Castro, K. S. Novoselov, S. V. Morozov, N. M. R. Peres, J. M. B. Lopes dos Santos, J. Nilsson, F. Guinea, A. K. Geim, and A. H. Castro Netro, "Biased bilayer graphene: Semiconductor with a gap tunable by the electric field effect," *Phys. Rev. Lett.*, vol. 99, 2007, 216802.

[52] P. Gava, M. Lazzeri, A. M. Saitta, and F. Mauri, "*Ab initio* study of gap opening and screening effects in gated bilayer graphene," *Phys. Rev. B*, vol. 79, 2009, 165431.

[53] J. A. Kelber, M. Zhou, S. Gaddam, F. L. Pasquale, L. M. Kong, and P. A. Dowben, "Direct graphene growth on oxides: Interfacial interactions and band gap formation," *ECS Trans.*, vol. 45, no. 4, pp. 49–61, 2012.

[54] S. Nakaharai, T. Iijima, S. Ogawa, S. Suzuki, K. Tsukagoshi, S. Sato, and N. Yokoyama, "Electrostatically-reversible polarity of dual-gated graphene transistors with He ion irradiated channel: Toward reconfigurable CMOS applications," in *Tech. Dig. Int. Electron Devices Meeting*, 2012, pp. 72–75.

[55] M. Lundstrom, "Device physics at the scaling limit: What matters?" in *Tech. Dig. Int. Electron Devices Meeting*, 2003, pp. 789–792.

[56] A. Lherbier, X. Blasé, Y.-M. Niquet, F. Triozon, and S. Roche, "Charge transport in chemically doped 2D graphene," *Phys. Rev. Lett.*, vol. 101, 2008, 036808.

[57] A. Konar, T. Fang, and D. Jena, "Effect of high-κ gate dielectrics on charge transport in graphene-based field-effect transistors," *Phys. Rev. B*, vol. 82, 2010, 115452.

[58] M.-W. Lin, C. Ling, L. A. Agapito, N. Kioussis, Y. Zhang, M. M.-C. Cheng, W. L. Wang, E. Kaxiras, and Z. Zhou, "Approaching the intrinsic band gap in suspended high-mobility graphene nanoribbons," *Phys. Rev. B*, vol. 84, 2011, 125411.

[59] H. Raza and E. Kan, "Armchair graphene nanoribbons: Electronic structure and electric-field modulation," *Phys. Rev. B*, vol. 77, 2008, 245434.

[60] J.-H. Chen, C. Jang, S. Xiao, M. Ishigami, and M. S. Fuhrer, "Intrinsic and extrinsic performance limits of graphene devices on SiO_2," *Nature Nanotechnol.*, vol. 3, pp. 206–209, 2008.

[61] L. Liao, J. Bai, Y. Qu, Y.-C. Lin, Y. Li, Y. Huang, and X. Duan, "High-κ oxide nanoribbons as gate dielectrics for high mobility top-gated graphene transistors," *Proc. Nat. Acad. Sci.*, vol. 107, pp. 6711–6715, 2010.

[62] Y. Wang, B.-C. Huang, M. Zhang, C. Miao, Y.-H. Xie, and J. C. S. Woo, "High performance graphene FETs with self-aligned buried gates fabricated on scalable patterned Ni-catalyzed graphene," in *Dig. Symp. Very Large Scale Integr. (VLSI) Technol.*, 2011, pp. 116–117.

[63] B. Obradovic, R. Kotlyar, F. Heinz, T. Rakshit, M. D. Giles, M. A. Stettler, and D. E. Nikonov, "Analysis of graphene nanoribbons as a channel material for field-effect transistors," *Appl. Phys. Lett.*, vol. 88, 2006, 142102.

[64] T. Fang, A. Konar, H. Xing, and D. Jena, "Mobility in semiconducting nanoribbons: Phonon, impurity edge roughness scattering," *Phys. Rev. B*, vol. 78, 2008, 205403.

[65] X. Li, K. M. Borysenko, M. B. Nardelli, and K. W. Kim, "Electron transport properties of bilayer graphene," *Phys. Rev. B*, vol. 84, 2011, 195453.

[66] X. Zhou, J.-Y. Park, S. Huang, J. Liu, and P. L. McEuen, "Band structure, phonon scattering, performance limit of single-walled carbon nanotube transistors," *Phys. Rev. Lett.*, vol. 95, 2005, 146805.

[67] V. Perebeinos, J. Tersoff, and P. Avouris, "Electron-phonon interaction and transport in semiconducting carbon nanotubes," *Phys. Rev. Lett.*, vol. 94, 2005, 0786802.

[68] V. Subramanian, J. M. J. Frechet, P. C. Chang, D. C. Huang, J. B. Lee, S. E. Molesa, A. R. Murphy, D. R. Redinger, and S. K. Volkman, "Progress toward development of all-printed RFID tags: Materials, processes, devices," *Proc. IEEE*, vol. 93, no. 7, pp. 1330–1338, Jul. 2005.

[69] Q. Meng, H. Dong, W. Hu, and D. Zhu, "Recent progress of high performance organic thin film field-effect transistors," *J. Mater. Chem.*, vol. 21, pp. 11708–11721, 2011.

[70] F. Torrisi, T. Hasan, W. Wu, Z. Sun, A. Lombardo, T. S. Kulmala, G.-W. Hshieh, S. J. Jung, F. Bonaccorso, P. J. Paul, D. P. Chu, and A. C. Ferrari, "Inkjet-printed graphene electronics," *ACS Nano*, vol. 6, pp. 2992–3006, 2012.

[71] C. Sire, F. Ardiaca, S. Lepilliet, J.-W. T. Seo, M. C. Hersam, G. Dambrine, H. Happy, and V. Derycke, "Flexible gigahertz transistors derived from solution-based single-layer graphene," *Nano Lett.*, vol. 12, pp. 1184–1188, 2012.

[72] J. Lee, K. N. Parrish, S. F. Chowdhury, T.-J. Ha, Y. Hao, L. Tao, A. Dodabalapur, R. S. Ruoff, and D. Akinwande, "State-of-the-art graphene transistors on hexagonal boron nitride, high-k, polymeric films for flexible analog nanoelectronics," in *Tech. Dig. Int. Electron Devices Meeting*, 2012, pp. 343–346.

[73] J. Lee, L. Tao, Y. Hao, R. S. Ruoff, and D. Akinwande, "Embedded-gate graphene transistors for high-mobility detachable flexible nanoelectronics," *Appl. Phys. Lett.*, vol. 100, 2012, 152104.

[74] V. E. Dorgan, M.-H. Bae, and E. Pop, "Mobility and saturation velocity in graphene on SiO_2," *Appl. Phys. Lett.*, vol. 97, 2010, 082112.

[75] R. S. Shishir and D. K. Ferry, "Velocity saturation in intrinsic graphene," *J. Phys., Condens. Matter*, vol. 21, 2009, 344201.

[76] M. Bresciani, A. Paussa, P. Palestri, D. Esseni, and L. Selmi, "Low-field mobility and high-field drift velocity in graphene nanoribbons and graphene bilayers," in *Tech. Dig. Int. Electron Devices Meeting*, 2010, pp. 724–727.

[77] A. Betti, G. Fiori, and G. Iannaccone, "Drift velocity peak and negative differential mobility in high field transport in graphene nanoribbons explained by numerical simulations," *Appl. Phys. Lett.*, vol. 99, 2011, 242108.

[78] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, "Metal/graphene contact as a performance killer of ultra-high mobility graphene—Analysis of intrinsic mobility and contact resistance," in *Tech. Dig. Int. Electron Devices Meeting*, 2009, pp. 565–568.

[79] F. Xia, V. Perebeinos, Y.-M. Lin, Y. Wu, and P. Avouris, "The origin and limits of metal-graphene junction resistance," *Nature Nanotechnol.*, vol. 6, pp. 179–184, 2011.

[80] H. Madan, M. J. Hollander, M. LaBella, R. Cavalero, D. Snyder, J. A. Robinson, and S. Datta, "Record high conversion gain ambipolar graphene mixer at 10 GHz using scaled gate oxide," in *Tech. Dig. Int. Electron Devices Meeting*, 2012, pp. 76–79.

[81] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, "Superior thermal conductivity of single-layer graphene," *Nano Lett.*, vol. 8, pp. 902–907, 2008.

[82] W. Cai, A. L. Moore, Y. Zhu, X. Li, S. Chen, L. Shi, and R. S. Ruoff, "Thermal transport in suspended and supported monolayer graphene grown by chemical vapor deposition," *Nano Lett.*, vol. 10, pp. 1645–1651, 2010.

[83] R. Mao, B. D. Kong, K. W. Kim, T. Jayasekera, A. Calzolari, and M. B. Nardelli, "Phonon engineering in nanostructures: Controlling interfacial thermal resistance in multilayer-graphene/dielectric heterojunctions," *Appl. Phys. Lett.*, vol. 101, 2012, 113111.

[84] S. S. Mahajan, G. Subbarayan, and B. G. Sammakia, "Estimating Kapitza resistance between Si–SiO_2 interface using molecular dynamics simulations," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, no. 8, pp. 1132–1139, Aug. 2011.

[85] I. Meric, N. Baklitskaya, P. Kim, and K. L. Shepard, "RF performance of top-gated, zero-bandgap graphene field-effect transistors," in *Tech. Dig. Int. Electron Devices Meeting*, 2008, DOI: 10.1109/IEDM.2008.4796738.

[86] Y.-M. Lin, K. Jenkins, D. Farmer, A. Valdes-Garcia, P. Avouris, C.-Y. Sung, H.-Y. Chiu, and B. Ek, "Development of graphene FETs for high frequency electronics," in *Tech. Dig. Int. Electron Devices Meeting*, 2009, pp. 237–240.

[87] Y. Wu, K. A. Jenkins, A. Valdes-Garcia, D. B. Farmer, Y. Zhu, A. A. Bol, C. Dimitrakopoulos, W. Zhu, F. Xia, P. Avouris, and Y.-M. Lin, "State-of-the-art graphene high-frequency electronics," *Nano Lett.*, vol. 12, pp. 3062–3067, 2012.

[88] J. S. Moon, D. Curtis, M. Hu, D. Wong, C. McGuire, P. M. Campbell, G. Jernigan, J. L. Tedesco, B. VanMil, R. Myers-Ward, C. Eddy, Jr., and D. K. Gaskill, "Epitaxial-graphene RF field-effect transistors on Si-face 6H-SiC substrates," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 650–652, Jun. 2009.

[89] J. Lee, H.-J. Chung, J. Lee, H. Shin, J. Heo, H. Yang, S.-H. Lee, S. Seo, J. Shin, U.-I. Chung, I. Yoo, and K. Kim, "RF performance of pre-patterned locally-embedded-back-gate graphene devices," in *Tech. Dig. Int. Electron Devices Meeting*, 2010, pp. 568–571.

[90] Y. Wu, Y.-M. Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farmer, Y. Zhu, and P. Avouris, "High-frequency, scaled graphene transistors on diamond-like carbon," *Nature*, vol. 472, pp. 74–78, 2011.

[91] D.-H. Kim, B. Brar, and J. A. del Alamo, "$f_T = 688$ GHz and $f_{max} = 800$ GHz in $L_g = 40$ nm $In_{0.7}Ga_{0.3}As$ MHEMTs with $g_{m\_max} > 2.7$ mS/μm," in *Tech. Dig. Int. Electron Devices Meeting*, 2011, pp. 319–322.

[92] D.-H. Kim and J. A. del Alamo, "30-nm InAs PHEMTs with $f_T = 644$ GHz and $f_{max} = 681$ GHz," *IEEE Electron Device Lett.*, vol. 31, no. 8, pp. 806–808, Aug. 2010.

[93] S. Lee, B. Jagannathan, S. Narasimha, A. Chou, N. Zamdmer, J. Johnson, R. Williams, L. Wagner, J. Kim, J.-O. Plouchart, J. Pekarik, S. Springer, and G. Freeman, "Record RF performance of 45-nm SOI CMOS technology," in *Tech. Dig. Int. Electron Devices Meeting*, 2007, pp. 255–258.

[94] L. D. Nguyen, P. J. Tasker, D. C. Radulescu, and L. F. Eastman, "Characterization of ultra-high-speed AlGaAs/InGaAs (on GaAs) MODFETs," *IEEE Trans. Electron Devices*, vol. 36, no. 10, pp. 2243–2248, Oct. 1989.

[95] M. Steiner, M. Engel, Y.-M. Lin, Y. Wu, K. Jenkins, D. B. Farmer, J. J. Humes, N. L. Yoder, J.-W. T. Seo, A. A. Green, M. C. Hersam, R. Krupke, and P. Avouris, "High-frequency performance of scaled carbon nanotube array field-effect transistors," *Appl. Phys. Lett.*, vol. 101, 2012, 053123.

[96] F. Schwierz and J. J. Liou, "RF transistors: Recent developments and roadmap toward terahertz applications," *Solid-State Electron.*, vol. 51, pp. 1079–1091, 2007.

[97] Y.-M. Lin, D. B. Farmer, K. A. Jenkins, Y. Wu, J. L. Tedesco, R. L. Myers-Ward, C. R. Eddy, Jr., D. K. Gaskill, C. Dimitrakopoulos, and P. Avouris, "Enhanced performance in epitaxial graphene FETs with optimized channel morphology," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1343–1345, Oct. 2011.

[98] I. Meric, C. R. Dean, S.-J. Han, L. Wang, K. A. Jenkins, J. Hone, and K. L. Shepard, "High performance of graphene field effect transistors with saturating IV-characteristics," in *Tech. Dig. Int. Electron Devices Meeting*, 2011, pp. 15–18.

[99] Y. Wu, D. B. Farmer, A. Valdes-Garcia, W. J. Zhu, K. A. Jenkins, C. Dimitrakopoulos, P. Avouris, and Y.-M. Lin, "Record high RF performance for epitaxial graphene transistors," in *Tech. Dig. Int. Electron Devices Meeting*, 2011, pp. 528–530.

[100] R. Lai, X. B. Mei, W. R. Deal, W. Yoshida, Y. M. Kim, P. H. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier, L. Samoska, and A. Fung, "Sub 50 nm InP HEMT device with f_{max} greater than 1 THz," in *Tech. Dig. Int. Electron Devices Meeting*, 2007, pp. 609–611.

[101] F. Schwierz, "Industry-compatible graphene transistors," *Nature*, vol. 472, pp. 41–42, 2011.

[102] F. Schwierz, "Graphene transistors 2011," in *Proc. Int. Symp. Very Large Scale Integr. Technol. Syst. Appl.*, 2011, pp. 16–17.

[103] S. Thiele, J. A. Schaefer, and F. Schwierz, "Modeling of graphene metal-oxide-semiconductor field-effect transistors with gapless large-area graphene channels," *J. Appl. Phys.*, vol. 107, 2010, 094505.

[104] D. Jimenez and O. Moldovan, "Explicit drain-current model of graphene field-effect transistors targeting analog and radio-frequency applications," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 4049–4052, Nov. 2011.

[105] H. Wang, A. Hsu, J. Kong, D. A. Antoniadis, and T. Palacios, "Compact virtual-source current-voltage model for top- and back-gated graphene field-effect transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1523–1533, May 2011.

[106] S. Thiele and F. Schwierz, "Modeling of the steady state characteristics of large-area graphene field-effect transistors," *J. Appl. Phys.*, vol. 110, 2011, 034506.

[107] S. E. Thompson, R. S. Chau, T. Ghani, K. Mistry, S. Tyagi, and M. T. Bohr, "In search of 'forever', continued transistor scaling one new material at a time," *IEEE Trans. Semicond. Manuf.*, vol. 18, no. 1, pp. 26–36, Feb. 2005.

[108] K. N. Parrish and D. Akinwande, "Impact of contact resistance on the transconductance and linearity of graphene transistors," *Appl. Phys. Lett.*, vol. 98, 2011, 183505.

[109] Y. Q. Wu, Y.-M. Lin, K. A. Jenkins, J. A. Ott, C. Dimitrakopoulos, D. B. Farmer, F. Xia, A. Grill, D. A. Antoniadis, and P. Avouris, "RF performance of short channel graphene field-effect transistor," in *Tech. Dig. Int. Electron Devices Meeting*, 2010, pp. 226–228.

[110] K. Tahy, S. Koswatta, T. Fang, Q. Zhang, H. G. Xing, and D. Jena, "High field transport properties of 2D and nanoribbon graphene FETs," in *Proc. Device Res. Conf.*, 2009, pp. 207–208.

[111] J. Kedzierski, P.-L. Hsu, A. Reina, J. Kong, P. Healey, P. Wyatt, and C. Keast, "Graphene-on-insulator transistors made using C on Ni chemical-vapor deposition," *IEEE Electron Device Lett.*, vol. 30, no. 7, pp. 745–747, Jul. 2009.

[112] S. O. Koswatta, A. Valdes-Garcia, M. B. Steiner, Y.-M. Lin, and P. Avouris, "Ultimate RF performance potential of carbon electronics," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 10, pt. 2, pp. 2739–2750, Oct. 2011.

[113] Y. Wu, D. B. Farmer, W. Zhu, S.-J. Han, C. D. Dimitrakopoulos, A. A. Bol, P. Avouris, and Y.-M. Lin, "Three-terminal graphene negative differential resistance devices," *ACS Nano*, vol. 6, pp. 2610–2616, 2012.

[114] K. Parrish and D. Akinwande, "An exactly solvable model for the graphene transistor in the quantum capacitance limit," *Appl. Phys. Lett.*, vol. 101, 2012, 053501.

[115] J. S. Moon, D. Curtis, D. Zehnder, S. Kim, D. K. Gaskill, G. G. Jernigan, R. L. Myers-Ward, C. R. Eddy, Jr., P. M. Campbell, K.-M. Lee, and P. Asbeck, "Low-phase-noise graphene FETs in ambipolar RF applications," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 270–272, Mar. 2011.

[116] H. Wang, A. L. Hsu, and T. Palacios, "Graphene electronics for RF applications," *IEEE Microw. Mag.*, vol. 13, no. 4, pp. 114–125, May–Jun. 2012.

[117] H. Wang, A. Hsu, J. Wu, J. Kong, and T. Palacios, "Graphene-based ambipolar RF mixers," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 906–908, Sep. 2010.

[118] O. Habibpour, S. Cherednichenko, J. Vukusic, K. Yhland, and J. Stake, "A subharmonic graphene FET mixer," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 71–73, Jan. 2012.

[119] H. Wang, A. Hsu, K. K. Kang, J. Kong, and T. Palacios, "Gigahertz ambiploar frequency multiplier based on CVD graphene," in *Tech. Dig. Int. Electron Devices Meeting*, 2010, pp. 572–575.

[120] N. Petrone, I. Meric, J. Hone, and K. L. Shepard, "Graphene field-effect transistors with gigahertz-frequency power gain on flexible substrates," *Nano Lett.*, vol. 13, pp. 121–125, 2013.

[121] C.-T. Chen, T. Low, H.-Y. Chiu, and W. Zhu, "Graphene-side-gate-engineering," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 330–332, Mar. 2012.

[122] B. Hähnlein, B. Händel, J. Pezoldt, H. Töpfer, R. Granzner, and F. Schwierz, "Side-gate graphene field-effect transistors with high transconductance," *Appl. Phys. Lett.*, vol. 101, 2012, 093504.

[123] F. Xia, D. B. Farmer, Y.-M. Lin, and P. Avouris, "Graphene field-effect transistors with high on/off ratio and large transport band gap at room temperature," *Nano Lett.*, vol. 10, pp. 715–718, 2010.

[124] B. N. Szafranek, D. Schall, M. Otto, D. Neumaier, and H. Kurz, "High on/off ratios in bilayer graphene field effect transistors realized by surface dopants," *Nano Lett.*, vol. 11, pp. 2640–2643, 2011.

[125] S.-L. Li, H. Miyazaki, H. Hiura, C. Liu, and K. Tsukagoshi, "Enhanced logic performance with semiconducting bilayer graphene channels," *ACS Nano*, vol. 5, pp. 500–506, 2011.

[126] B. N. Szafranek, G. Fiori, D. Schall, D. Neumaier, and H. Kurz, "Current saturation and voltage gain in bilayer graphene field effect transistors," *Nano Lett.*, vol. 12, pp. 1324–1328, 2012.

[127] E. McCann, "Interlayer asymmetry gap in the electronic band structure of bilayer graphene," *Phys. Stat. Sol. (b)*, vol. 244, pp. 4112–4117, 2007.

[128] G. G. Jernigan, T. J. Anderson, J. T. Robinson, J. D. Caldwell, J. C. Culbertson, R. Myers-Ward, A. L. Davidson, M. G. Ancona, V. D. Wheeler, L. O. Nyakiti, A. L. Friedman, P. M. Campbell, and D. K. Gaskill, "Bilayer graphene by bonding CVD graphene to epitaxial graphene," *J. Vac. Sci. Technol. B*, vol. 30, 2012, 03D110.

[129] L. Liu, H. Zhou, R. Cheng, W. J. Yu, Y. Liu, Y. Chen, J. Shaw, X. Zhong, Y. Huang, and X. Duan, "High-yield chemical vapor deposition growth of high-quality large-are AB-stacked bilayer graphene," *ACS Nano*, vol. 6, pp. 8241–8249, 2012.

[130] G. Iannaccone, G. Fiori, M. Macucci, P. Michetti, M. Cheli, A. Betti, and P. Marconcini, "Perspectives of graphene nanoelectronics: Probing technological options with modeling," in *Tech. Dig. Int. Electron Devices Meeting*, 2009, pp. 245–248.

[131] L. Liao, J. Bai, R. Cheng, Y.-C. Lin, S. Jiang, Y. Huang, and X. Duan, "Top-gated graphene nanoribbon transistors with ultrathin high-k dielectrics," *Nano Lett.*, vol. 10, pp. 1917–1921, 2010.

[132] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors," *Phys. Rev. Lett.*, vol. 100, 2008, 206803.

[133] J. Bai, X. Duan, and Y. Huang, "Rational fabrication of graphene nanoribbons using a nanowire etch mask," *Nano Lett.*, vol. 9, pp. 2083–2087, 2009.

[134] G. Liang, N. Neophytou, D. E. Nikonov, and M. S. Lundstrom, "Performance projection for ballistic graphene nanoribbon field-effect transistors," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 677–682, Apr. 2007.

[135] Y. Yoon and J. Guo, "Effects of edge roughness in graphene nanoribbon transistors," *Appl. Phys. Lett.*, vol. 91, 2007, 073103.

[136] D. Basu, M. J. Gilbert, L. F. Register, S. K. Banerjee, and A. H. MacDonald, "Effect of edge roughness on electronic transport in graphene nanoribbon channel metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 92, 2008, 042114.

[137] L. Jiao, X. Wang, G. Diankov, H. Wang, and H. Dai, "Facile synthesis of high-quality graphene nanoribbons," *Nature Nanotechnol.*, vol. 5, pp. 321–325, 2010.

[138] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, pp. 329–337, 2011.

[139] M. Luisier and G. Klimeck, "Performance analysis of statistical samples of graphene nanoribbon tunneling transistors with line edge roughness," *Appl. Phys. Lett.*, vol. 94, 2009, 223505.

[140] G. Fiori and G. Iannaccone, "Ultralow-voltage bilayer graphene tunnel FET," *IEEE Electron Device Lett.*, vol. 30, no. 10, pp. 1096–1098, Oct. 2009.

[141] S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer pseudospin field-effect transistor (BiSFET): A proposed new logic device," *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 158–160, Feb. 2009.

[142] D. Reddy, L. F. Register, E. Tutuc, and S. K. Banerjee, "Bilayer pseudospin field-effect transistor: Applications to Boolean logic," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 755–764, Apr. 2010.

[143] K. Bernstein, R. K. Cavin, III, W. Porod, A. Seabaugh, and J. Welser, "Device and architecture outlook for beyond CMOS switches," *Proc. IEEE*, vol. 98, no. 12, pp. 2169–2184, Dec. 2010.

[144] L. Britnell, R. V. Gorbatchev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko, "Field-effect tunneling transistor based on vertical graphene heterostructures," *Science*, vol. 335, pp. 947–950, 2011.

[145] W. Mehr, J. Dabrowski, J. C. Scheytt, G. Lippert, Y.-H. Xie, M. C. Lemme, M. Ostling, and G. Lupina, "Vertical graphene base transistor," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 691–693, May 2012.

[146] H. Wang, A. Hsu, D. S. Lee, K. K. Kim, J. Kong, and T. Palacios, "Delay analysis of graphene field-effect transistors," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 324–326, Mar. 2012.

[147] A. H. Castro Neto and K. Novoselov, "New directions in science and technology," *Rep. Progr. Phys.*, vol. 74, 2011, 082501.

[148] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, "Electronics and optoelectronics of two-dimensional transition metal dichalcogenides," *Nature Nanotechnol.*, vol. 7, pp. 699–712, 2012.

[149] K. S. Novoselov, D. Jiang, F. Schedin, T. J. Booth, V. V. Khotkevich, S. V. Morozov, and A. K. Geim, "Two-dimensional atomic crystals," *Proc. Nat. Acad. Sci.*, vol. 102, pp. 10451–10453, 2005.

[150] C. Lee, Q. Li, W. Kalb, X.-Z. Liu, H. Berger, R. W. Carpick, and J. Hone, "Frictional characteristics of atomically thin sheets," *Science*, vol. 328, pp. 76–80, 2010.

[151] J. N. Coleman, M. Lotya, A. O'Neill, S. D. Bergin, P. J. King, U. Khan, K. Young, A. Gaucher, S. De, R. J. Smith, I. V. Shvets, S. K. Arora, G. Stanton,

H.-Y. Kim, K. Lee, G. T. Kim, G. S. Duesberg, T. Hallam, J. J. Boland, J. J. Wang, J. F. Donegan, J. C. Grunlan, G. Moriarty, A. Shmeliov, R. J. Nicholls, J. M. Perkins, E. M. Grieveson, K. Theuwissen, D. W. McComb, P. D. Nellist, and V. Nicolosi, "Two-dimensional nanosheets produced by liquid exfoliation of layered materials," *Science*, vol. 331, pp. 568–571, 2011.

[152] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nature Nanotechnol.*, vol. 6, pp. 147–150, 2011.

[153] H. Liu and P. D. Ye, "MoS_2 dual-gate MOSFET with atomic-layer-deposited Al_2O_3 as top-gate dielectric," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 546–548, Apr. 2012.

[154] L. B. Kumar, Y. Ouyang, and J. Guo, "Performance limits of monolayer transition metal dichalcogenide transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 3042–3047, Sep. 2011.

[155] Y. Yoon, K. Ganapathi, and S. Salahuddin, "How good can monolayer MoS_2 transistors be?" *Nano Lett.*, vol. 11, pp. 3768–3773, 2011.

ABOUT THE AUTHOR

Frank Schwierz (Senior Member, IEEE) received the Diploma, Dr.-Ing., and Dr. habil. degrees from the Technische Universität (TU) Ilmenau, Ilmenau, Germany, in 1982, 1986, and 2003, respectively.

Currently, he serves as Privatdozent at TU Ilmenau and is Head of the RF & Nano Device Research Group. He conducts research projects funded by the European Community, German government agencies, and the industry. Together with partners from German universities and industry, he was involved in the development of the fastest Si-based transistors worldwide in the late 1990s and of Europe's smallest MOSFETs in the early 2000s. He has published 200 journal and conference papers, including 30 invited papers. He is the author of the books *Modern Microwave Transistors—Theory, Design, and Performance* (New York, NY, USA: Wiley, 2003) and *Nanometer CMOS* (Singapore: Pan Stanford, 2010). His research interests include semiconductor device modeling and simulation, ultrahigh-speed transistors, and novel device and material concepts for future transistor generations. Currently, he is particularly interested in 2-D electronic materials, such as graphene and transition metal dichalcogenides.