REVIEW

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A role for graphene in silicon-based semiconductor devices

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As silicon-based electronics approach the limit of improvements to performance and capacity through dimensional scaling, attention in the semiconductor field has turned to graphene, a single layer of carbon atoms arranged in a honeycomb lattice. Its high mobility of charge carriers (electrons and holes) could lead to its use in the next generation of high-performance devices. Graphene is unlikely to replace silicon completely, however, because of the poor on/off current ratio resulting from its zero bandgap. But it could be used to improve silicon-based devices, in particular in high-speed electronics and optical modulators.

Silicon-based microprocessors and memory chips with a linewidth as small as 20 nm can meet the demand for low-power multifunctional chips that can process and store massive amounts of heterogeneous data. But achieving physical dimensions near the 'deeper nanoscale' regime of 10 nm or beyond[1] is a challenge for existing technologies. It will require dimensional scaling using novel structures, materials and processes for complementary metal–oxide–semiconductor (CMOS) devices, such as three-dimensional architectures for memory and logic, high-κ/metal gate transistors, extreme ultraviolet lithography and new computing architectures. Materials such as graphene, which has an extremely high charge-carrier mobility, are expected to have an important role in the advancement of semiconductor technology[2–4].

Graphene is a monolayer of carbon atoms arranged in a two-dimensional honeycomb lattice and is a basic building block of well-known carbon materials such as graphite, carbon nanotubes and fullerene. Since graphene was isolated by mechanical exfoliation in 2004 (ref. 5), many extraordinary properties have been reported, such as extremely high electron mobility[3–5]. High mobility arises because electrons can propagate without scattering over large distances, perhaps micrometres, because of its reduced phonon scattering. A recent poll conducted by the semiconductor industry for the *International Technology Roadmap for Semiconductors* (ITRS) named graphene as the material likely to have the greatest impact on geometric scaling, thanks to its high mobility, which is desirable in metal–oxide–semiconductor field-effect transistor (MOSFET) channels[6]. Furthermore, graphene's strong interactions with photons[7–9] and electrochemical stability could add more functions to silicon-based CMOS devices, such as radio-frequency switches and photonic modulators.

Here we consider how graphene can be incorporated into these semiconductor devices, examine the requirements and challenges that must be met, and discuss possible solutions.

Radio-frequency transistors

The high mobility of charge carriers in graphene is ideal for obtaining fast switching and a high 'on' current (I_{ON}). Zero bandgap induces a large 'off' current, however, so the on/off current ratios for graphene transistors are about 100 (ref. 5), much lower than the 10^3–10^6 required for mainstream logic applications. But this relatively low on/off ratio is not a significant problem for high-frequency applications, such as radio-frequency switches.

In general, radio-frequency transistor performance is characterized by two parameters: the cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}), where f_T and f_{max} represent how fast channel current and power transmission, respectively, are modulated by the gate. As shown in following equation

$$f_T = \frac{g_m}{2\pi C_G} \quad (1)$$

f_T is determined by the gate capacitance (C_G) and the transconductance (g_m). Thus far, the highest measured f_T has been 300 GHz with Co_2Si-nanowire gates using exfoliated graphene[10]. At a wafer scale, 240 GHz has been reported using epitaxial graphene[11], compared with 200 GHz using chemical vapour deposition (CVD)[12]. As shown in Table 1, even with larger gate lengths, graphene has demonstrated superior performance to silicon[13] and III–V group compounds[14–16] as a result of its high drift velocity of 4×10^7 cm s^{-1} (ref. 17). This means that f_T for graphene transistors is approximately 1.42 THz for a 56-nm gate[17], although this value excludes parasitic capacitances, which would be halved in such cases.

Another important parameter for radio-frequency transistors is f_{max}:

$$f_{max} = \frac{f_T}{2\sqrt{(g_D(R_G + R_{SD}) + 2\pi f_T R_G C_G)}} \quad (2)$$

where g_D is the channel conductance, R_G is the gate resistance and R_{SD} is the source–drain resistance. Studies have shown large discrepancies in values between f_T and f_{max} for graphene radio-frequency transistors. Previous work initially attributed the discrepancy to the high contact resistance[18] and high R_G without considering issues inherent to the graphene film, in particular the low output resistance. We expect that the low output resistance is one of the key factors in increasing f_{max}. Because f_{max} measures transmitted power (I^2R), it can be increased by minimizing g_D attained at channel saturation; this is a pinch-off in most MOS transistors. In graphene, the pinch-off condition, effective for the drain saturation, can be produced if graphene has a bandgap. More research to improve f_{max} through improvements in saturation currents is needed[19,20]. As long as f_{max} remains at current levels, it will be difficult to use graphene transistors in radio-frequency amplifiers. At present, they will be valuable for radio-frequency switching applications only if f_T exceeds the performance of current silicon-based devices.

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Table 1 | Properties of radio-frequency transistors

Transistor	f_T (GHz)	f_{max} (GHz)	L_g (nm)	W_g (μm)	Fingers	g_m (mS μm^{-1})	Mobility (cm^2 V^{-1} s^{-1})	Specific contact resistance (Ω μm^2)
Graphene								
Estimated[17]*	1,420	–	56	2	1	2.3	>10,000	
Measured[12]*	300	–	144	10	1	1.27		7.5 (ref. 23)
CVD grown[18]	155	<10	40	30	2	0.02	500–600	
Epitaxial[21]	100	–	240	–	2	0.15	1,000–1,500	
Silicon								
Silicon[13]	485	–	29	30	30	1.3	1,400‡	0.1§
ITRS 2011	310	330	29	–	–	–		
ITRS 2014†	480	540	18	–	–	–		
III–V								
InP[14]	385	>1,100	<50	40	2	1.2	15,000	0.5 (ref. 16)
InAs[15]	628	331	30	100	2	1.62	13,200	

*Flake graphene; †Target specification; ‡Electron mobility; §100 nm × 100 nm NiSi/Si. L_g, gate length; W_g, gate width.

As shown in Table 1, the estimated f_T for graphene is significantly higher than that for silicon. However, the experimentally measured f_T for graphene is much lower than expected. To increase f_T, mobility has to be increased[11,12,21], for which three factors need to be considered: minimizing defects in graphene; minimizing impurities that cause scattering at the graphene channel–gate dielectric interface[22]; and reducing contact resistance[23,24].

Defects in graphene are highly dependent on the growth process. The highest reported mobility is 200,000 cm^2 V^{-1} s^{-1}, which has been obtained using mechanically exfoliated graphene flakes without a substrate at a temperature of 5 K (ref. 6). Mobility remains within the same order of magnitude at elevated temperatures because the scattering mechanism is mainly caused by electron or hole puddles within the two-dimensional graphene sheet[25]. In reality, graphene flakes cannot be used for silicon applications, so CVD or sublimation of SiC will be needed, even though these might reduce mobility.

The impurities that cause scattering at the graphene channel–gate dielectric interface have been attributed to interactions with the underlying substrate, such as surface charge traps[26,27], interfacial phonons[28] and nanometre-scale deformation or ripples[29–31]. To minimize these impurities, we propose a new structure containing air gaps, a 'nothing-on-graphene' architecture that provides a free-standing condition for graphene. On the other side of graphene is a gate oxide that does not reduce the mobility, such as hexagonal boron nitride (hBN), which allows a reasonable charge transport in graphene (up to 40,000 cm^2 V^{-1} s^{-1} at room temperature) because it is atomically flat and free of dangling bonds and charge traps[32,33].

Figure 1 shows the formation of the 'nothing-on-graphene' architecture. Copper gates are formed through a 'damascene' process, along with the first metal line (M1), which here is copper (Fig. 1a). The next step is the transfer of hBN and graphene (Fig. 1b). The critical step in producing 'nothing-on-graphene' is the formation of air gaps between the source and drain metal electrodes; this is achieved by depositing a sacrificial film on the electrodes (Fig. 1c), which is then etched back to expose the electrodes (Fig. 1d). A porous film is then deposited (Fig. 1d) over the electrodes, and the sacrificial film is removed, creating the air gaps (Fig. 1e). The porous film must then be patterned (Fig. 1f). This 'nothing-on-graphene' architecture minimizes interfacial scattering interactions and thus maximizes mobility.

The contact resistance of graphene is more than 70 times higher than that of silicon (see Table 1). However, reducing the contact resistance poses significant challenges because of the interactions between graphene and different metals. Graphene shows weak binding with metals such as copper, gold and platinum on their (111) surfaces, where

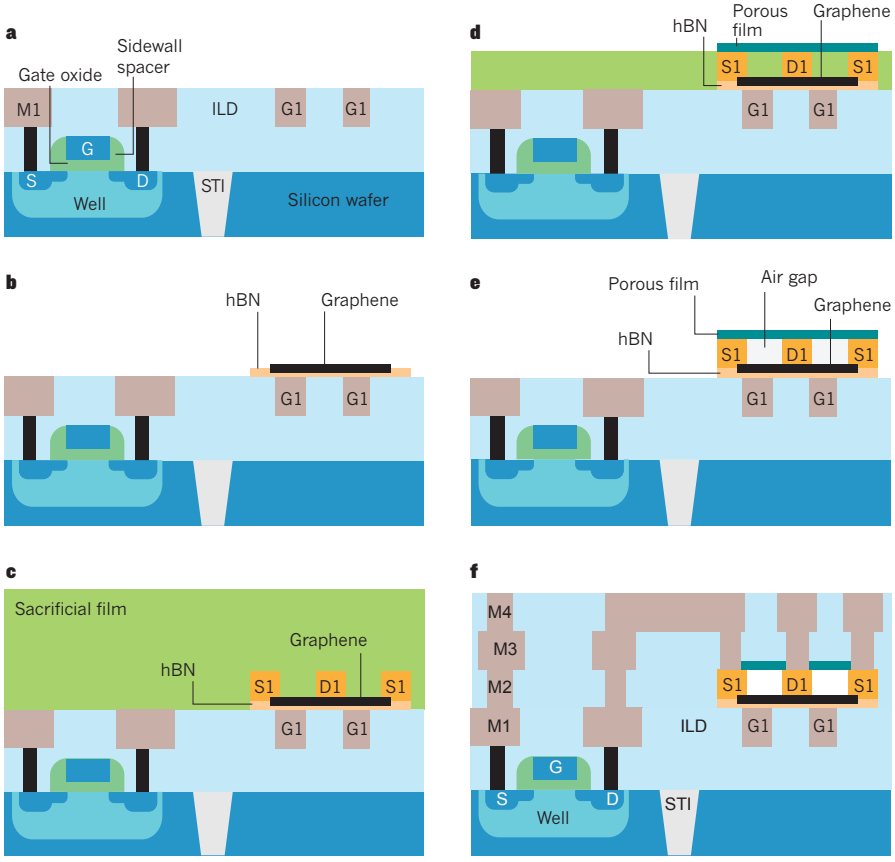

Figure 1 | Formation of 'nothing-on-graphene' architecture, which minimizes the scattering of electrons. **a**, A 'damascene' process is used to create a layer of copper metal (M1) that functions as the gate electrode (G1) for the graphene transistor. G, S and D indicate the gate, the source and the drain of the silicon transistor, respectively, and STI indicates the shallow trench isolation. The well is for the separation of the p–n doping regions. **b**, A layer of hexagonal boron nitride (hBN) is introduced to act as a gate oxide. This is atomically flat and lacks dangling bonds and charge traps, so it allows fast charge transport. A layer of graphene is placed over the hBN. **c**, The source (S1) and drain (D1) metal electrodes are patterned, and a sacrificial film is placed over the top. **d**, The sacrificial film is then etched back to reveal the electrodes, and a porous film is then deposited. **e**, The remainder of the sacrificial film is removed through pores of the porous film, leaving air gaps between the electrodes. **f**, Once the 'nothing-on-graphene' architecture is established, CMOS 'back end of the line' processes, including the addition of further metal layers, can complete the circuit. ILD, interlayer dielectric.

Table 2 | On/Offcurrent ratios for a 20-nm Si logic process

Property	Type 1*	Type 2†	Type 3‡	Type 4§
On/Off ratio	~2×10^6	~2×10^5	~4×10^4	~5×10^3
I_{ON} (μA μm^{-1})	~800	~1,000	~1,100	~1,300

All transistor types are needed for 20-nm silicon CMOS logic circuits. *Low on current, highest on/off ratio; †Medium on current, high on/off ratio; ‡Medium on current, medium on/off ratio; §High on current, low on/off ratio.

graphene preserves its band structure[34,35]. By contrast, graphene binds strongly to nickel, cobalt and palladium as their electronic structures are strongly intermixed[36,37]. Although contact resistance is expected to be lower in strongly binding metals, binding strength has been shown not to affect resistance, as experimental values for gold, nickel and palladium are quite similar[24,36–39]. This suggests that even for strong metal–graphene contacts, electron transmission from the graphene region in contact with the metal to the pristine graphene channel becomes difficult. Careful studies are required to determine whether contact resistances have intrinsic limitations.

Even if f_T is maximized, the task of improving f_{max} still remains. To accomplish this, saturation (a pinch-off condition with a bandgap) should be created in graphene for a high output resistance.

When a bandgap is effectively formed, graphene can be used in high-speed logic applications. So far, there have been no specific guidelines on how wide the bandgap should be, but this could be inferred from the minimum I_{ON}/I_{OFF} ratio requirement. For a noticeable bandgap to be engineered at the graphene–metal junction, I_{OFF} must be governed by the thermionic emission of carriers through the metal–graphene Schottky barrier. Thus I_{OFF} would be proportional to $\exp(-q\varphi_{barrier}/kT)$, where q is the electron charge, $\varphi_{barrier}$ is the Schottky barrier height, k is the Boltzmann constant and T is the temperature. In addition, assuming that the work functions of graphene and the metal are the same, the resultant Schottky barrier height would be $E_g/2$, where E_g is the bandgap energy. Hence the I_{ON}/I_{OFF} ratio would be proportional to $\exp(E_g/2kT)$. Among various transistor technologies of 20-nm CMOS logic products, a high-speed transistor requires the I_{ON}/I_{OFF} ratio to be three to four orders of magnitude, which is the lowest acceptable value for high-performance logic applications (K. Kim, unpublished data; see Table 2). Because the I_{ON}/I_{OFF} ratio is proportional to $\exp(E_g/2kT)$, the minimum required bandgap would be 360 meV for high-speed CMOS applications.

There is considerable research to improve the I_{ON}/I_{OFF} ratios of current graphene transistors: nanoribbon[40–42], bilayer[43] and perforated graphene[44–46]. So far, such studies have been unable to achieve this value. It might take years for graphene transistors to be used for high-speed logic, but they could still find use embedded in radio-frequency applications such as low-noise amplifiers, mixers, frequency multipliers and resonators[47–49].

Once a graphene radio-frequency transistor can be integrated into a silicon CMOS, and assuming it has a very high f_T and linear gain, which are usually observed in graphene radio-frequency transistors, it will enhance the performance of low-noise and low-distortion circuits. Furthermore, if f_{max} can also be improved, its usage will extend to all circuitry, including all power-sensitive blocks.

Optical devices for silicon photonics

As well as the radio-frequency field, graphene could find another promising market in photonics because it can facilitate ultrawide bandwidths for exa-scale (10^{18}) computing systems. The explosive data growth on the Internet drives the need for exa-scale systems for large data centres. Peta-scale (10^{15}) systems consumed about 2.5 MW in 2008; a simple estimate shows that exa-scale systems will consume about 2.5 GW, which is unacceptably high[50]. Energy efficiency is therefore the next challenge for the silicon industry. Silicon photonics can provide ultrawide bandwidths through the multiplexing of numerous wavelengths[51,52] and reduced power consumption.

Graphene can find a use here because of its optical properties. It absorbs about 2.3% of normal incident light, despite only being one atom thick[53–55]. Transparency is almost independent of wavelength over spectra ranging from visible light to infrared because there are two-dimensional gases of free electrons in the gapless electronic structure of graphene[53,56]. These optical characteristics, allied with its high electron mobility, make graphene a prime candidate for ultrawide-bandwidth optical modulators and photo-detectors.

An optical modulator is one of the key components for altering the properties of light, such as its phase, amplitude or polarization, by electro-refraction or electro-absorption[57]. Optical modulators, such as Mach–Zehnder interferometers[57,58], ring or disk resonators[59,60] and germanium- or III–V-based electro-absorption modulators[61,62], are based on interference, resonance and bandgap absorption, respectively. Their operating spectra are usually narrow[59–63]. A single sheet of graphene on a silicon waveguide has recently been reported to provide an ultrafast response time[7].

The interband transitions of photo-generated electrons are modulated over broad spectral ranges by a drive voltage, so a broadband and high-speed optical modulator can be implemented with graphene. This CMOS-compatible graphene optical modulator can provide excellent performance over broad operating spectra ranging from 1.35 μm to 1.60 μm, with an operating speed of 1.2 GHz, a modulation efficiency of ~0.1 dB μm^{-1} and a small footprint of 25 μm^2 (ref. 7).

Optical modulators can be further improved by increasing both modulation depth and operating speed using a novel modulator structure, as shown in Fig. 2, in which graphene is placed at the location of maximum light intensity of the ridge region in the waveguide,

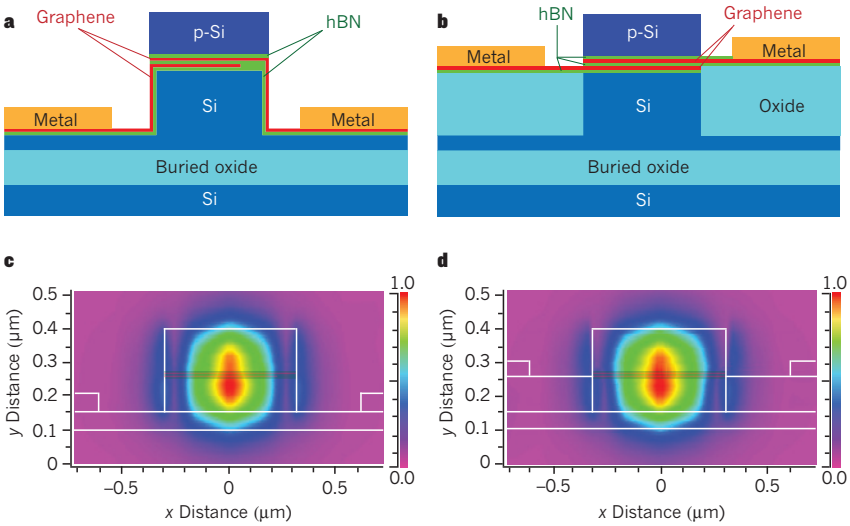

Figure 2 | Structure of a graphene-gated optical modulator. **a**, A ridge-type modulator. **b**, A buried-type modulator. In each case, two monolayer graphene sheets and an hBN spacer 7 nm thick are used to separate the waveguides, which are made of two different sections of silicon substrate and polycrystalline silicon (p-Si). The ridge is 600 nm wide, 250 nm high and 35 μm long. The metal electrode is located 300 nm from the waveguide. **c**, **d**, Transverse electric mode profiles at a wavelength of 1.55 μm are shown for the ridge type (**c**) and the buried type (**d**) modulator. The multilayer structure of graphene and hBN is overlaid with the mode profiles.

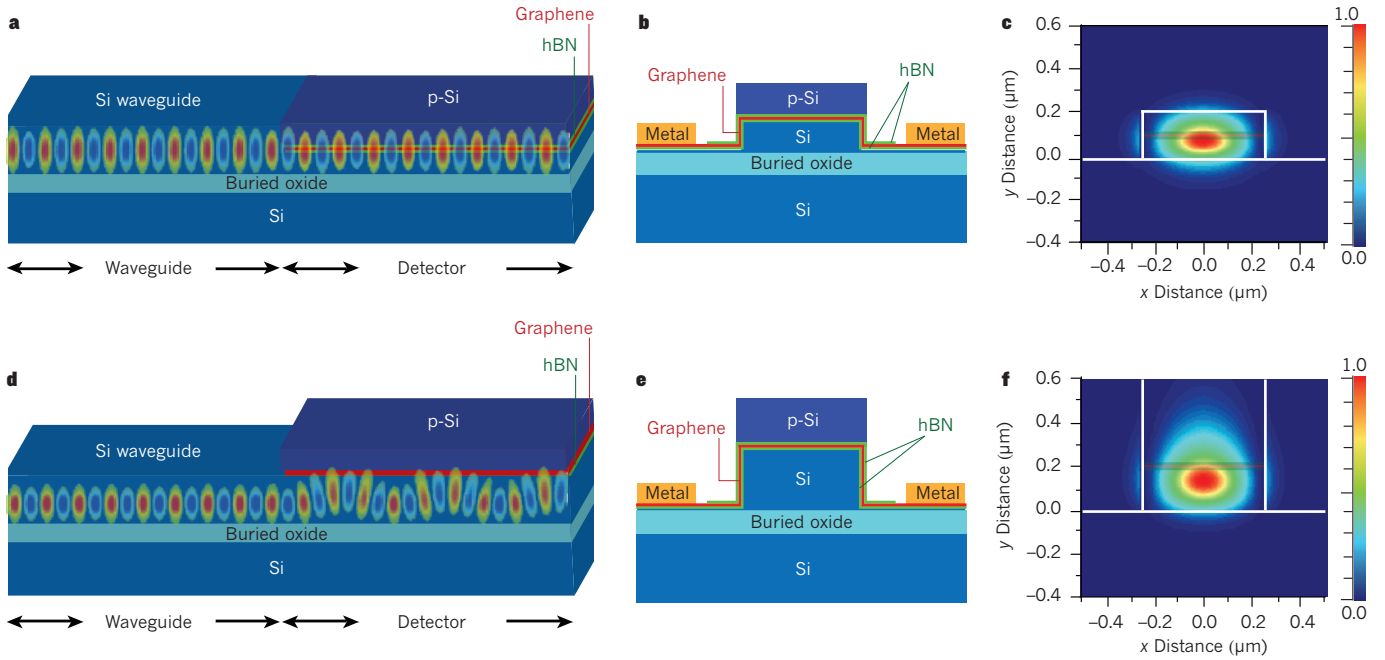

Figure 3 | The structure of graphene photo-detectors with integrated waveguides. **a–c**, Butt-coupled photo-detectors. **a**, A longitudinal schematic is shown with an overlaid longitudinal electric field (E-field) that shows the light transport from the waveguide to the detector. The layer of graphene is surrounded by hBN to maximize mobility. **b**, A cross-section of the photo-detector shown in **a**. Graphene is placed between the half-etched Si waveguide and the p-Si to minimize optical losses at the waveguide–detector interface. **c**, A cross-sectional E-field profile showing a good overlap with the graphene. **d–f**, Evanescent-coupled photo-detectors. **d**, A longitudinal schematic is shown with an overlaid longitudinal E-field profile. The E-field extends into the p-Si, enhancing the interaction with graphene. **e**, A cross-section of the photo-detector shown in **d**. Unlike **b**, graphene is placed above the Si waveguide. **f**, A cross-sectional profile showing the E-field tailing upwards to increase the overlap with the graphene. For simplicity, longitudinal views omit the metal grids. The silicon waveguide is 500 nm wide and 200 nm high. The E-field amplitudes are calculated at a wavelength of 1.3 μm. Graphene's thickness of 0.335 nm and absorption coefficient of 301,655 cm^{-1} (ref. 56) are used to calculate the normalized detector lengths. The multilayer structure of graphene and hBN is overlaid on the cross-sectional E-field profiles.

maximizing the modulation depth. To this end, the ridge is composed of two different regions, for example polycrystalline silicon on the top and single-crystalline silicon on the bottom. New modulator structures where dual graphene layers are separated by a thin hBN spacer are shown in Fig. 2a, b. Their propagating mode profiles, which confirm a good spatial overlap between the light mode and the graphene layers, are shown in Fig. 2c,d. Oxide deteriorates carrier mobility in graphene, so hBN is used as an insulator because it allows graphene to maintain its high mobility. The capacitance-resistance (RC) time constant can be reduced by replacing high-resistance bulk silicon with low-resistance graphene, and by replacing the gating spacer with low-dielectric-constant hBN. With two single sheets of graphene 600 nm wide on the waveguide, which is 300 nm from the metal contact and 35 μm long (Fig. 2b), the total resistance, including the metal contact, is reduced from 600 Ω to 26 Ω, where the sheet resistance is 15 Ω and the contact resistance is 11 Ω, using unit sheet and unit contact resistances for single-sheet graphene of 300 Ω per square (Ω □$^{-1}$) (ref. 64) and 200 Ω μm (ref. 36), respectively. In addition, the capacitance is reduced from 220 fF to 100 fF. The predicted bandwidth of this high-speed modulator, $f_{3B} = 1/2\pi RC$, is intrinsically suitable for 55-GHz modulation, which is comparable to the best reported optical modulator bandwidth[63]. In the near future, it is likely that both inter-chip and intra-chip interconnects for ultrawide-bandwidth data networks will be possible using graphene.

Another prime optical application for graphene is as a photo-detector. Extremely high bandwidth is possible because the high carrier mobility allows the ultrafast extraction of light-generated carriers. The transit time-limited bandwidth is calculated to be 1.5 THz[4] at the reported saturation carrier velocity[65]. In comparison, the best results using germanium photo-detectors are around 30 GHz[66,67], and the maximum bandwidth is expected to be 80 GHz[68].

The feasibility of graphene as a photo-detector has been demonstrated in photo-generated current imaging studies[69,70]. A 10-GHz bandwidth stand-alone graphene photo-detector for optical communication has recently been reported[71]. However, its maximum responsivity is low (6.1 mA W^{-1}) because the detector is designed to absorb only a small percentage of normal incident light. The responsivity can be improved by integrating the waveguide with the photo-detector because the light–graphene interaction length increases as light propagates along graphene's plane.

In a photo-detector with an integrated waveguide, optical signals from a waveguide can be transferred to a detector by either butt-coupled or evanescent-coupled schemes[72]. In the butt-coupled scheme, the detector and the waveguide are directly connected to each other on the same plane, whereas in the evanescent scheme the detector is on top of the waveguide. Our proposed approaches for both schemes are shown in Fig. 3 with their longitudinal and cross-sectional electric-field profiles. For the butt-coupling approach (Fig. 3a–c), graphene is sandwiched between half-etched silicon and polycrystalline silicon to minimize light reflection at the interface. In the evanescent-coupling approach (Fig. 3d–f), graphene is too thin to shift the light mode coming from the silicon waveguide and hardly absorbs any light. The polycrystalline silicon layer in Fig. 3b enables graphene to absorb light by changing the refractive index such that the mode shifts upwards.

To determine whether these detectors could adequately absorb light despite their extreme thinness, normalized detector lengths for the same absorption have been compared based on detector volume and electric-field intensity profiles. To achieve the same absorption as that of the widely used evanescent-coupled germanium detector, the evanescent-coupled graphene detector needs to be 3.5 times longer. In the butt-coupled case, however, the graphene detector only needs to be 12% longer because the graphene overlaps with the highest electric field. A further decrease in detector length can be achieved by using multilayer graphene because the absorption increases linearly with thickness for up to six layers[73].

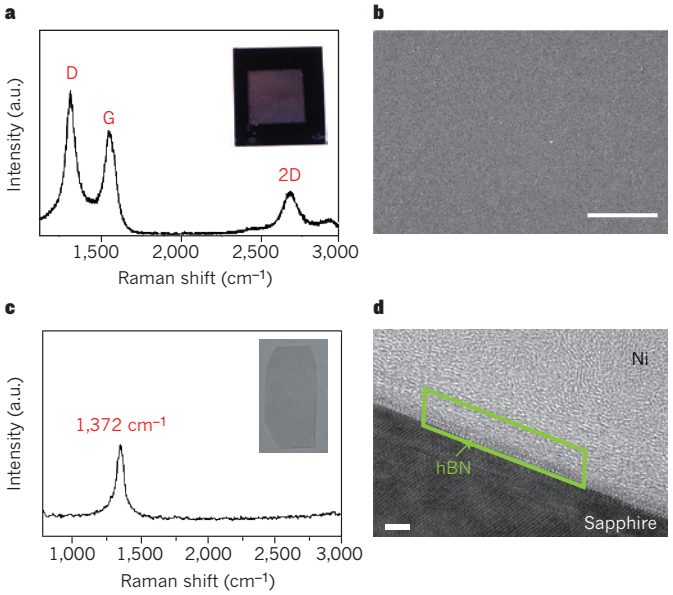

Figure 4 | Direct growth of graphene and hBN. **a**, **b**, The growth of graphene on hBN film showing the Raman spectrum (**a**) and a scanning electron microscopy image (**b**). Scale bar, 1 μm. The hBN film was grown on copper foil and transferred to a SiO_2/Si wafer. The inset in **a** shows a graphene sample grown on a 1 cm × 1 cm hBN film on a 2 cm × 2 cm SiO_2/Si wafer. Graphene shows typical Raman peaks of D (1,346 cm^{-1}), G (1,582 cm^{-1}) and 2D (2,700 cm^{-1}) and a homogeneous film structure with no particulate impurities. The G peak originates from the doubly degenerated vibrational mode of hexagonally structured graphene. The D peak is a disorder-induced band observed in a defective graphene structure. The 2D peak is the second order of the D band. **c**, **d**, The growth of hBN film on Al_2O_3 (0001) substrate showing the Raman spectrum (**c**) and a transmission electron microscopy image (**d**). Scale bar, 2 nm. The inset in **c** shows an hBN sample grown on the Al_2O_3 (0001) substrate measuring 1 cm × 2 cm. The hBN film shows a typical Raman peak at 1,372 cm^{-1}. a.u., arbitrary units.

To increase responsivity, effective extraction of photo-generated carriers should also be considered. Because doping control is difficult, graphene requires different carrier-extraction structures from semiconductor photo-detectors. A novel system for using metal-induced, built-in potential has been studied[35,69,70,74] and the device demonstrated[8,71]. Assuming light absorption of 2.3%, about 21% carrier extraction is estimated from 6.1 mA W^{-1} responsivity[71], and up to 60% carrier extraction can be anticipated[69]. Further structural optimization and graphene doping studies[75,76] are expected to increase the extraction efficiency.

Integration in semiconductor processes

Incorporating graphene into silicon devices is challenging, and careful selection of the right growth methods for the application is important. For graphene-based hybrid silicon-CMOS applications, graphene films should be deposited on topological surfaces as determined by the device architecture. There are generally two methods of graphene deposition: epitaxial growth on SiC(0001) by the sublimation of silicon atoms[77,78], and growth on catalytic metal films with subsequent transfer onto target substrates (CVD transfer)[79–81].

CVD transfer processes have already been demonstrated at wafer scales[82]. This method allows graphene to be transferred onto any type of material as long as it is flat, and there are no limitations on process temperatures. However, it is difficult to avoid defects such as holes, cracks and folds during the transfer[79–81]. Such defects would be minimized if graphene could be grown directly on underlying materials with topological surfaces at reasonable process temperatures.

The structures and process requirements of devices discussed in this Review are summarized in Fig. 5. For the radio-frequency transistor shown in Fig. 5a, for example, graphene will be deposited on hBN. However, growing hBN presents a challenge because growth could take place on two or more different materials such as metals (usually copper) and low-κ dielectrics. The problem is the high processing temperature for graphene and hBN, which exceeds the back-end-of-line processing temperatures of less than 500 °C. The most sensible way of preparing graphene and hBN is therefore by CVD on metal catalysts and film transfer.

An optical modulator with a buried architecture (Fig. 5b) requires multiple stacking of graphene and hBN (hBN/graphene/hBN/graphene/hBN) on Si and SiO_2. Because multiple transfers could increase the number of transfer-related defects, the entire film stack could be divided into two different stacks, which would require only a two-step transfer. The first stack would consist of graphene/hBN, and the second would be hBN/graphene/hBN. In this case, these stacks could be grown on catalytic metal film by CVD.

For the ridge structures shown in Fig. 5b, c, conformal stacking of graphene and hBN is needed on a topological silicon surface: hBN/graphene/hBN/graphene/hBN for optical modulators (Fig. 5b) and hBN/graphene/hBN for the photo-detector (Fig. 5c). Because the transfer method is limited to flat surfaces, transfer-free deposition on non-catalytic surfaces such as in silicon, graphene and hBN is required. Moreover, graphene and hBN depositions on non-catalytic surfaces must be prepared below 1,000 °C to avoid structural changes in CMOS devices, such as in doping profiles. There are two approaches for the transfer-free deposition of graphene on non-catalytic surfaces: on a catalytic metal film/substrate followed by eliminating the underlying metal[83–85], and directly on non-catalytic substrates by CVD[86,87]. Both approaches pose challenges. In the first approach, graphene can be torn during the elimination of the underlying metal. The second approach is not applicable to CMOS structures because of the high growth temperatures required (above 1,400 °C). Moreover, this latter process produces graphene flakes and dots, rather than continuous films. Therefore, direct growth of defect-free graphene at low temperatures on non-catalytic surfaces is required for CMOS integration. We have demonstrated that graphene film can be formed on a large-area hBN film by flow control of the precursor gas. Figure 4a shows the experimental results demonstrating that few-layered graphene can be directly grown on hBN at 1,000 °C using the CVD method. Graphene growth on the non-catalytic hBN film is enabled by enhancing the interactions of the precursor gas (C_2H_2) with the hBN film and by optimizing the flow direction as well as the pressure. This indicates that CVD has the potential to grow graphene on hBN directly; however, defects need to be minimized, and control of the number of layers should be improved.

For hBN growth, most studies have focused on catalytic metal substrates[88–90]. To realize the suggested modulator and detector structures, however, hBN on non-catalytic surfaces is required. We have attempted to deposit hBN directly on non-catalytic surfaces such as Si (001) and Al_2O_3 (0001) by thermal CVD. The hBN on Si could not be grown at all. However, a crystalline hBN has been successfully grown on Al_2O_3. Figure 4d shows a four-layered hBN on Al_2O_3 at 1,000 °C, achieved by controlling the flow kinetics where a large amount of precursor gas flows vertically relative to the substrate. These preliminary results suggest that the kinetic interactions of precursors with the substrate, as well as the chemical reactivity of surface atoms on the substrate, are important control parameters. Therefore, hBN could be deposited on Si if the Si surface is modified by adsorption of Al atoms, enhancing precursor reactivity with the surface.

To integrate graphene in silicon CMOS devices, direct growth of graphene on three-dimensional structures, simultaneous deposition on various underlying materials, and low processing temperatures are required. It will also be important to pursue further work on hBN film growth that could be used as dielectrics in radio-frequency transistors and as insulating materials in optical modulators and detectors. In-depth study of nucleation and growth mechanisms on non-catalytic surfaces will also accelerate the full realization of graphene-based hybrid silicon-CMOS applications.

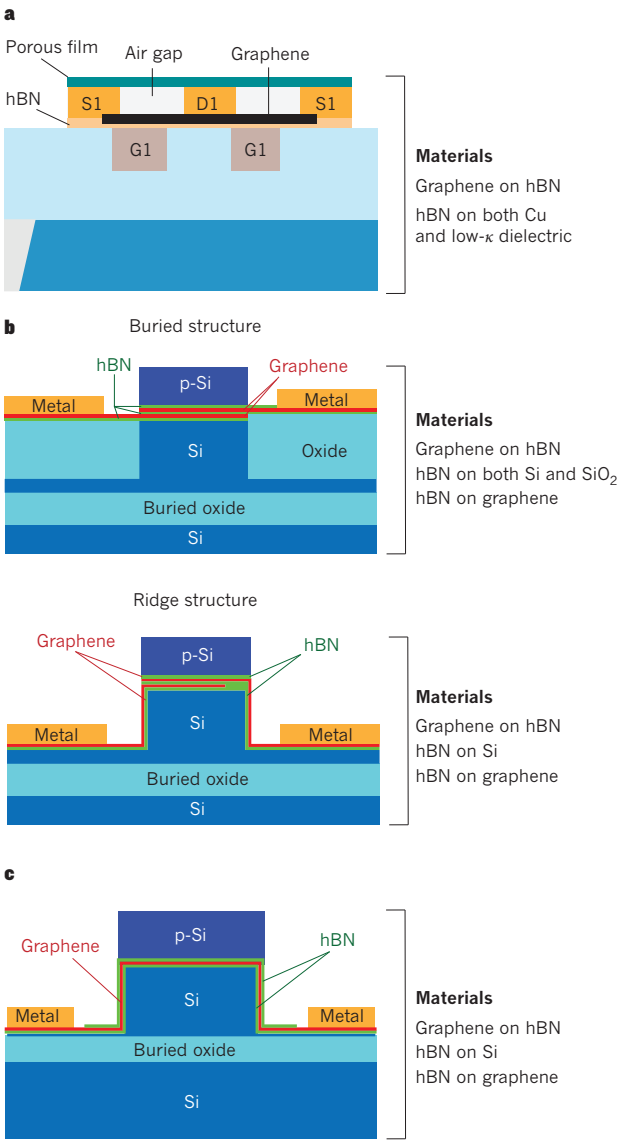

Figure 5 | Proposed device structures and process requirements for graphene and hBN films. **a**, Radio-frequency transistors have flat surface coverage. Film growth temperatures should not exceed the back-end-of-line processing temperatures around 500 °C. **b**, Optical modulators with buried structures also have flat surface coverage, whereas those with ridge structures have topological surface coverage. Both types have structural stability even at high fabrication temperatures of up to 1,000 °C. **c**, Photo-detectors have a ridge structure, giving them topological surface coverage. Like optical modulators, they have structural stability and are able to withstand fabrication temperatures of up to 1,000 °C.

Outlook

We have reviewed graphene devices for possible applications of current CMOS technology, focusing on radio-frequency transistors, optical devices and the deposition processes. By taking advantage of graphene's high carrier mobility and ultra-wideband optical absorption, we have proposed new architectures that are most likely to provide the earliest applications: the 'nothing-on-graphene' architecture for maximizing f_T, the graphene-gating optical modulator and the waveguide-integrated graphene photo-detector. We have also considered the limitations of graphene, such as the lack of bandgap through which f_{max} can be improved and its high contact resistance.

Graphene-based memory chips and microprocessors are unlikely to appear in the next few decades. In the meantime, graphene will have an important role in enhancing the performance of, and adding analogue functions to, silicon-based CMOS devices. However, for use in commercial graphene device applications, fabrication must be simple, reproducible and compatible with existing semiconductor processes. This implies that many of the current practices of graphene production will have to be changed drastically. Direct growth of high-quality graphene onto commonly used materials in semiconductor processes, such as Si and SiO_2, would be desirable. Advances confined to graphene alone are probably insufficient; new underlying materials, such as hBN, and processes to obtain such materials must be developed to fully maximize graphene's potential.

As interest in graphene continues to increase, we are optimistic that these technical issues will be resolved. The first application for graphene will probably be the radio-frequency switch, which has already shown a potential for improved performance, followed by optical modulators and photo-detectors. The next breakthrough, when the bandgap energy can be increased and controlled, is likely to expand the versatility of hybrid silicon-CMOS applications, making it a vital part of silicon CMOS evolution. ■

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