Phase Engineered Atomically thin high-K Dielectrics for 2D Electronics

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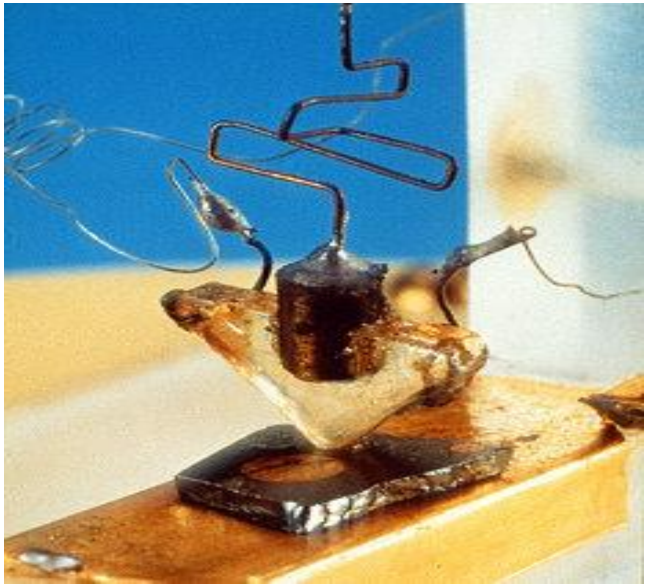
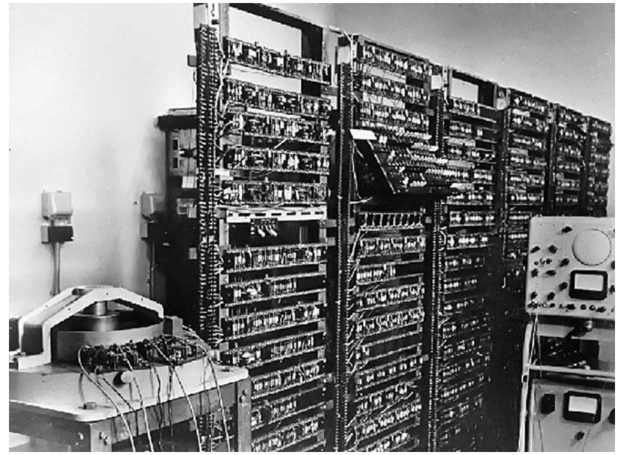
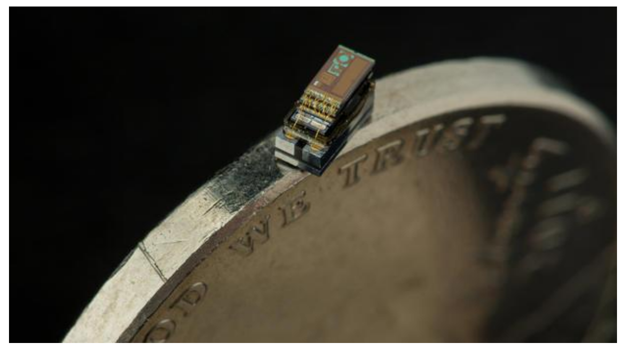
Introduction:



First Transistor 1947



First Transistor used computer 1953



Michigan Micro Mote (M^3) 2015

- Size of transistor decreased from 10 μm in 1970's to submicron le
- Development of Silicon based devices took the central focus
- Two dimensional materials like Graphene attracted lot of interest

Graphene

- Strong in-plane bond and weak inter-layer force
- Uniform surface
- Free from Dangling bonds
- Stable at room temp
- High Mobility

  10^6 $cm^2 v^{-1} s^{-1}$ at **2K**

  10^5 $cm^2 v^{-1} s^{-1}$ **room temp**

  Elac D.C.(2011)
- Zero band gap

Graphene Like 2D material : Transitional Metal Dichalcogenides (TMD)

- Graphene like material with finite band gap
- Thermally stable
- Compatible
- Excellent on-off ratio **> 10^6**

MoS2 FET

- Field effect mobility of MoS2 (8-40 nm) is found in tens of cm^2 /Vs and on-off ratio higher than 10^5 .

  Anthony Ayari et al., (2007)

- The mobility for the single layer MoS_2 FET on SiO_2 is found in the range 0.1 – 10 cm^2/Vs.

  B. Radisavljevic et. al.,(2011)

- The mobility of bi-layer MoS_2 FET were extracted 10-15 cm^2/Vs.

  Han Wang et. al., (2012)

- Room temperature mobility 50-200 cm^2/Vs for bulk MoS_2.

  R. Fivaz et.al., (1967)

Challenges of MoS2 FET

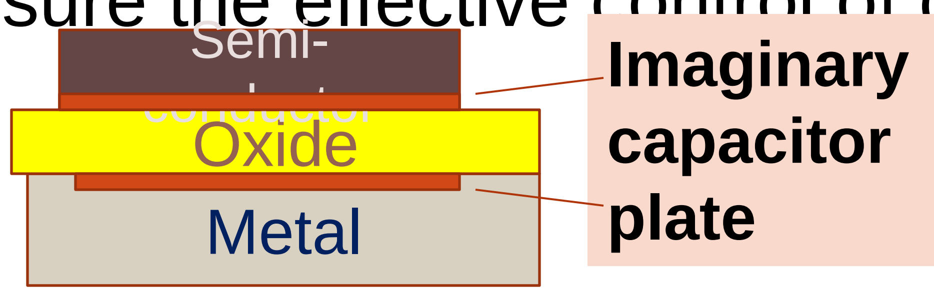
- Contact
- Interface
- High K dielectric integration

In our study, we will be focusing on High K dielectric integration of

Why High K dielectric ?

Electrostatic control of channel is achieved through the capacitive coupling between the gate and the channel region

Scaling requires reduction in the source and drain depth by the same scaling factor as gate length, to ensure the effective control of channel.



$$C = \frac{A\varepsilon_r \varepsilon_0}{t_{ox}}$$

Decreasing the thickness of gate oxide provides same

But ,

Decreasing the gate oxide thickness gives rise to short channel effects:

- Increase in leakage current
- Reduction In On-off ratio
- Break down of gate oxide

Another Way,

Replacing SiO_2 by dielectric having high dielectric constant increases the capacitive coupling

Finding new dielectrics having high dielectric constant !!

Criteria Required

- Good thermal stability
- Low density of intrinsic defects
- Sufficient gate dielectric lifetime
- Sufficient energy band-gap

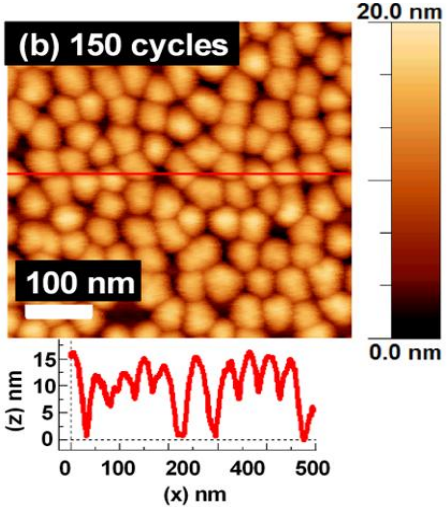
Possible Candidates

Table 1 Some physical parameters of high-κ dielectrics and heterostructures with Si and Ge

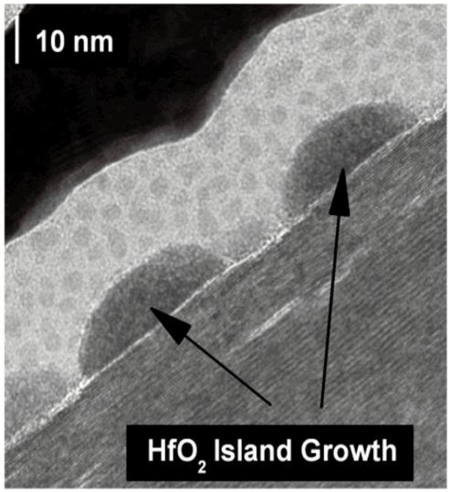
Material	Dielectric constant (k)	Band gap E_G (eV)	Band offset ΔE_C (eV) to Si	Band offset ΔE_C (eV) to Ge	Crystal structure
SiO_2	3.9	8.9	3.2		Amorphous
Al_2O_3	9	8.7	2.8	2.6 [24]	Amorphous
Si_3N_4					Amorphous
TiO_2	80–100	3.5	1.2		Tetragonal
Ta_2O_5	26	4.5	1–1.5		Orthorhombic
HfO_2	25	5.7	1.4	2.0 ± 0.1 [25]	Monoclinic, tetragonal, cubic
ZrO_2	25	7.8	1.5		Monoclinic, tetragonal, cubic
La_2O_3	30	4.3	2.3	2.56 [24]	Hexagonal, cubic
Y_2O_3	15	5.6	2.3	2.56 [24]	Cubic
Gd_2O_3	24 ± 2 [6]			2.44 [24]	
MgO	9.8 [7]	7.3 [7]			Cubic
Er_2O_3	14.4 [8]	7.5 [8]	3.5 [8]		
Nd_2O_3		5.8 [9]	2.2 [9]		
PrO_2	25 [10]	3–4 [10]	>1 [10]		Cubic
CeO_2	52 [11], 26 [12]	4.5 [12]			
$LaAlO_3$	26 [13]	6.0 [10]		2.2 [24]	
$ZrSiO_4$					Amorphous
$HfSiO_4$				2.2 [24]	Amorphous
(Dy_2O_3)	14	4.8			

Source :Wu, M. et. Al., 2008

Problem in High K dielectric integration of TMD

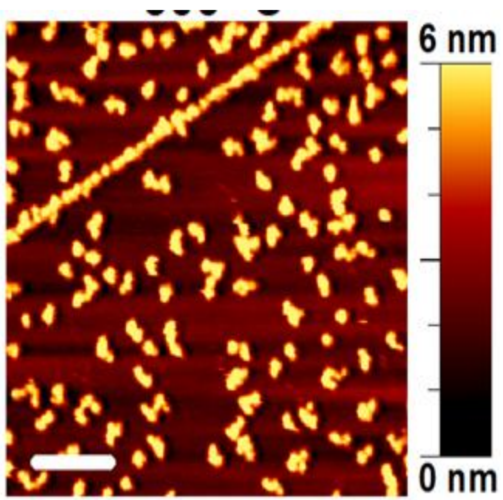


AFM image of HfO2 on MoS2 surface by ALD



XPS image showing island type of growth

Source : Stephen M. et. al., (2013)



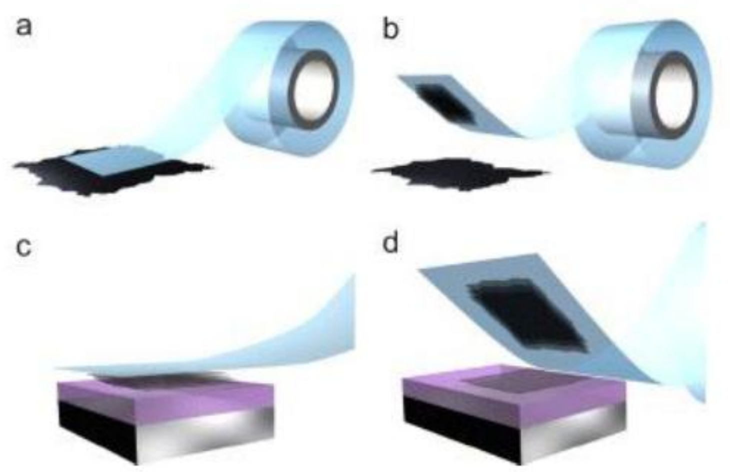
AFM image of Al2O3 deposited by 30 ALD cycles on MoS2 .

Source: Azcati A et.al., 2014

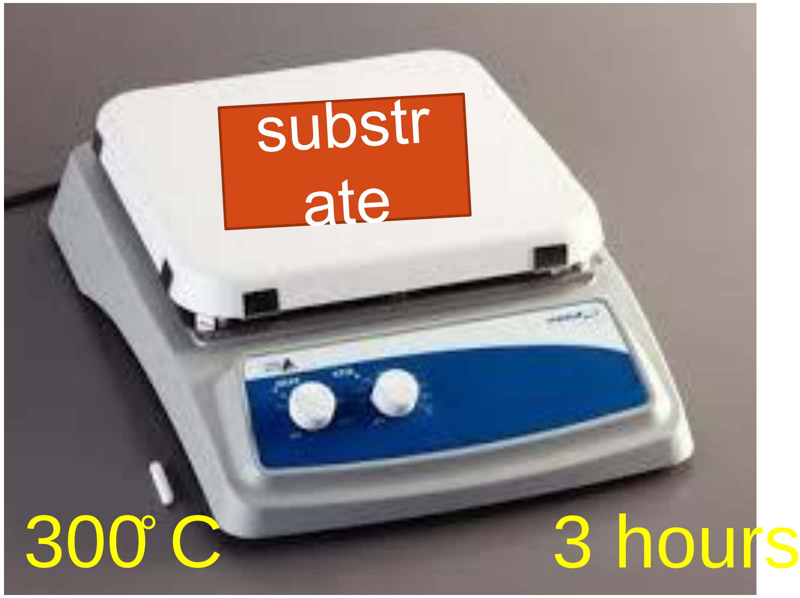
- ➢They require complex growth process
- ➢Non-uniform deposition
- ➢ Needs Surface treatme
- ➢Surface contamination

Solution

Two dimensional atomically flat high K dielectric obtained through mechanical exfoliation

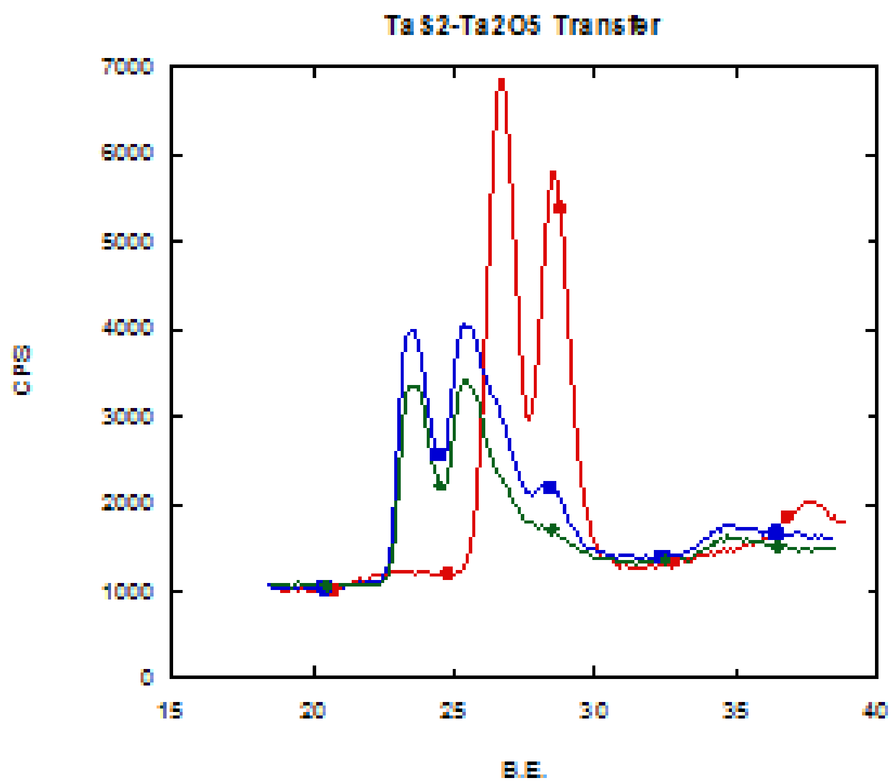


Exfoliation of TaS_2



Thermal Oxidation

XPS Study of Oxidized TaS2 :

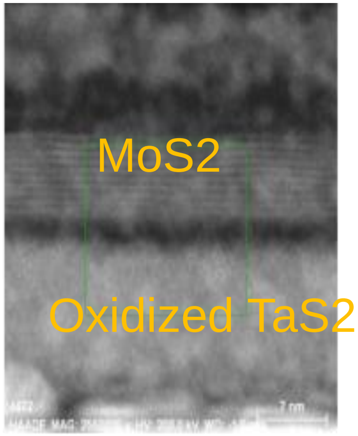


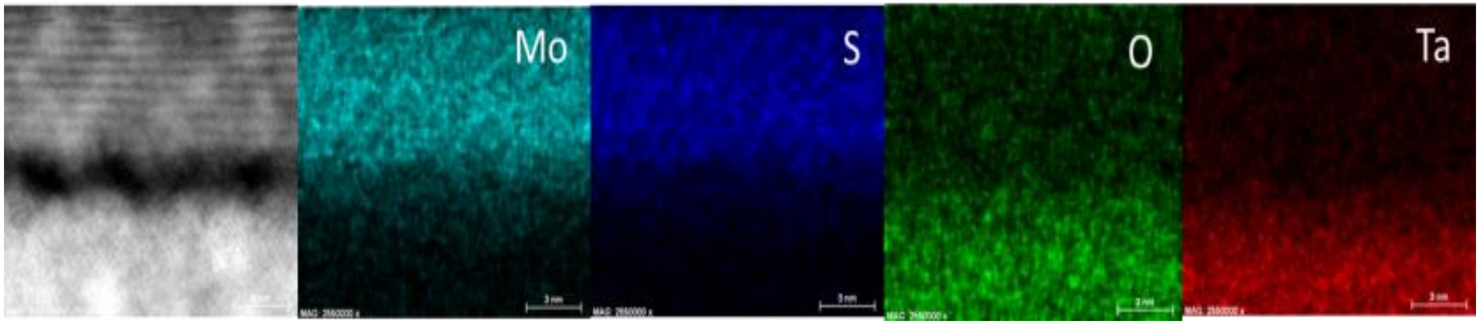
Kuo Y.,

Th in

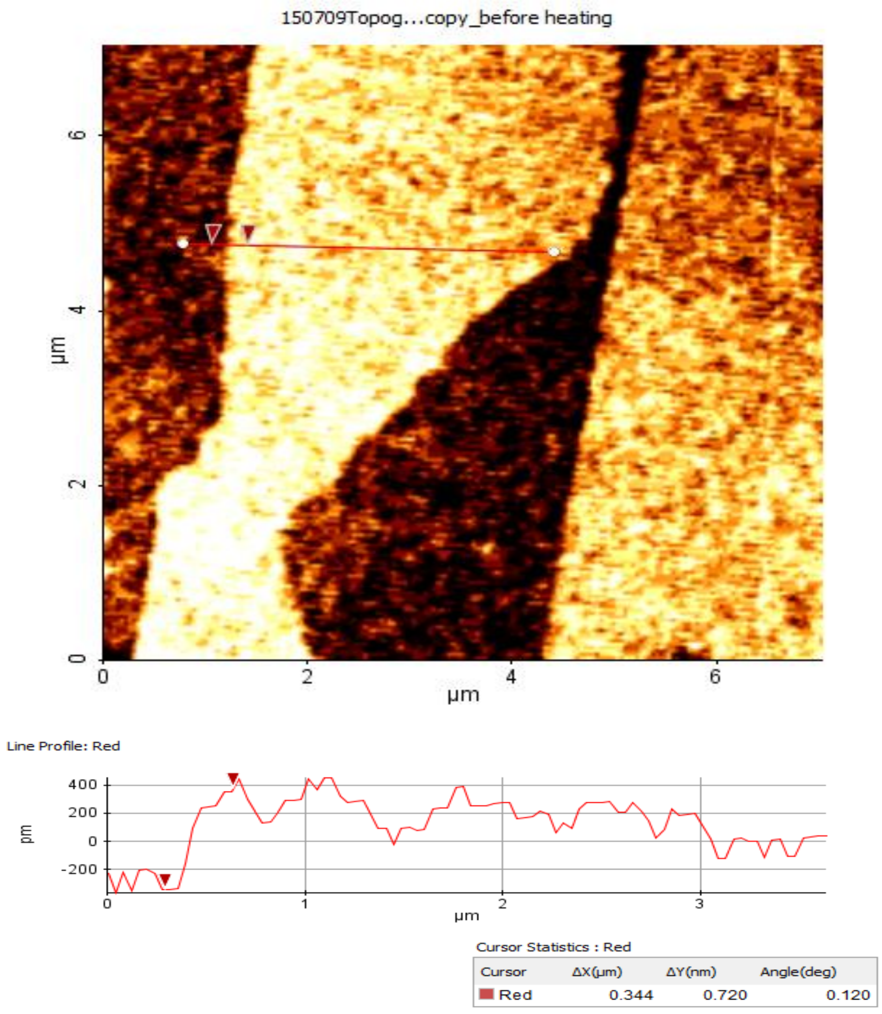
st Ta_2O_5.

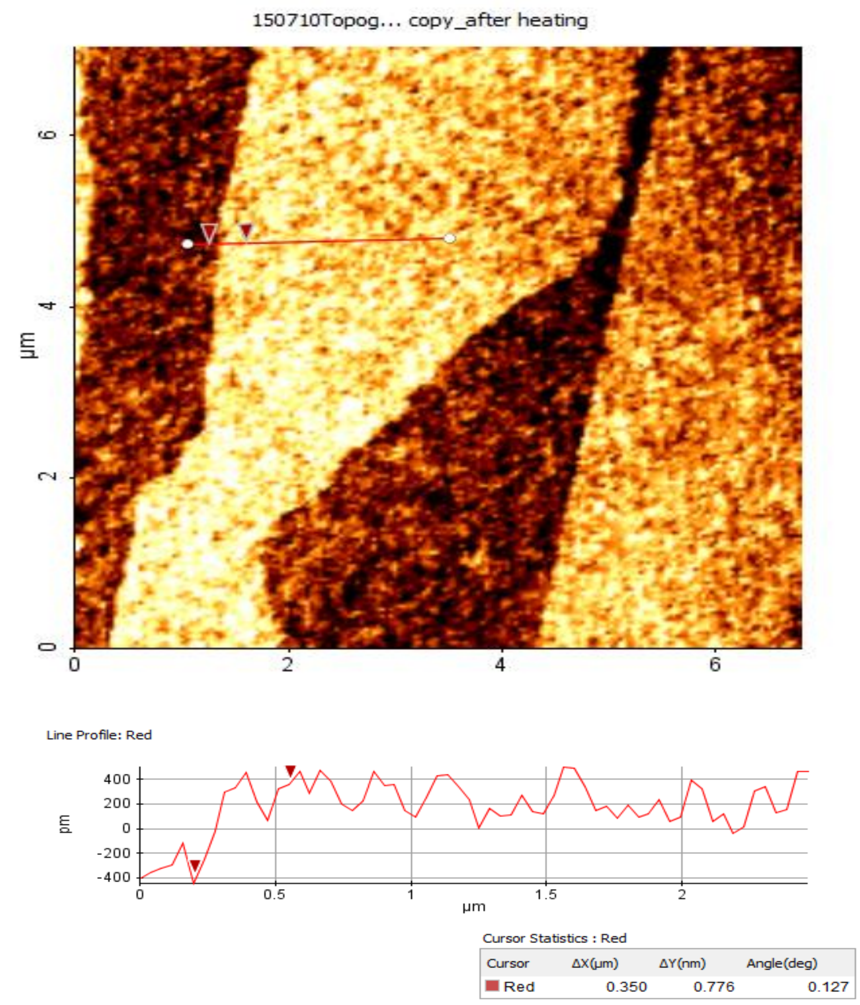
TEM Study





AFM Study :

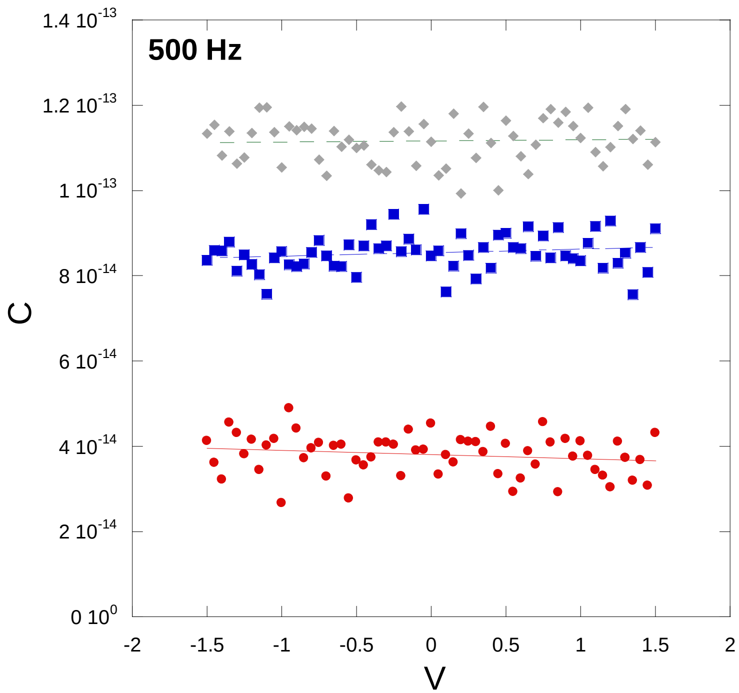


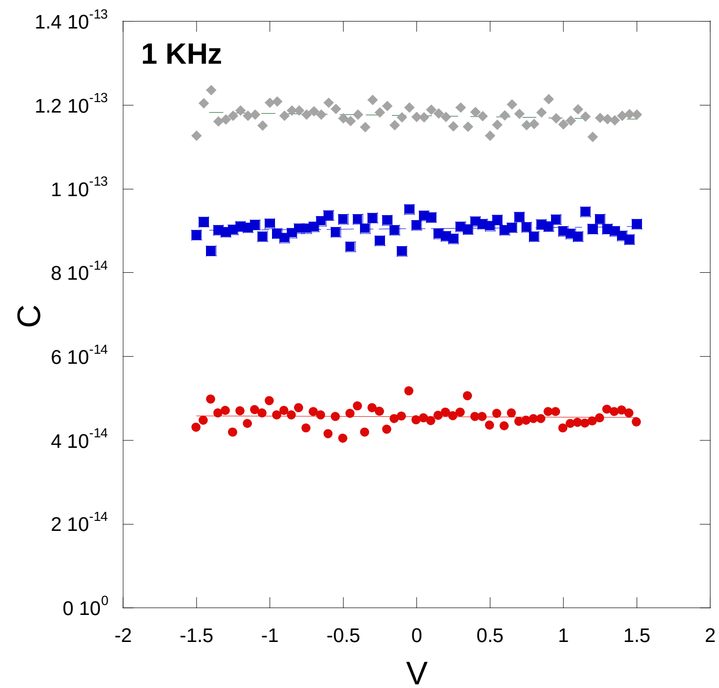


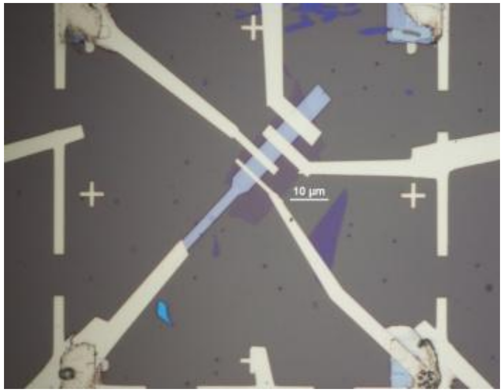
Before heating

After heating

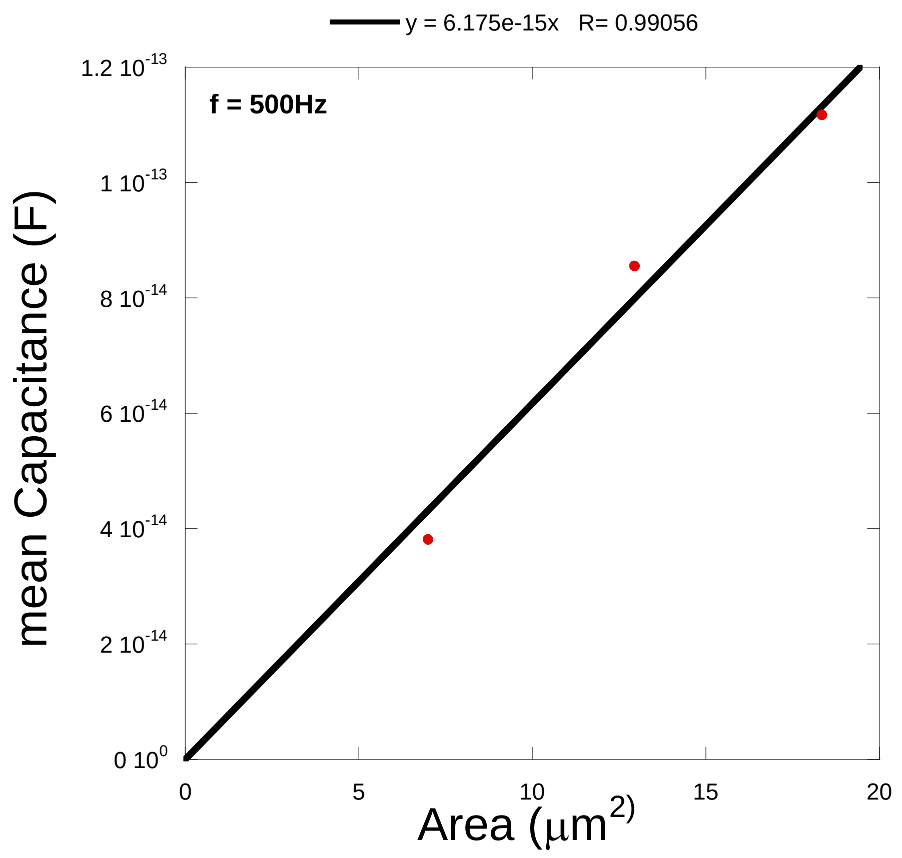
C-V Measurement :







C-V Measurement (cont.) :

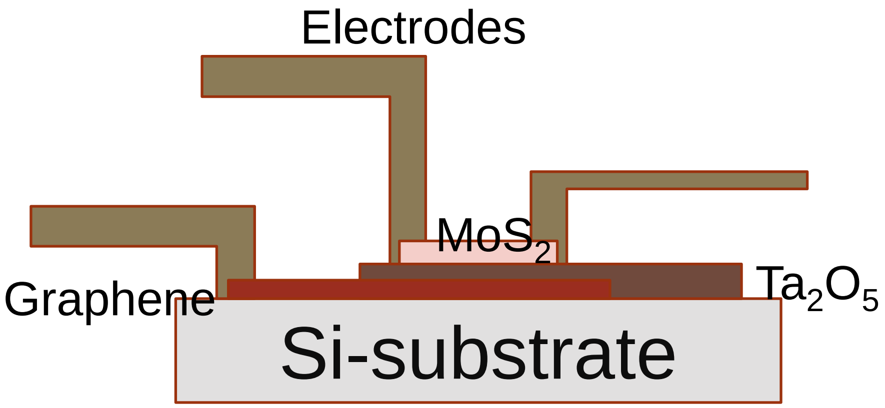


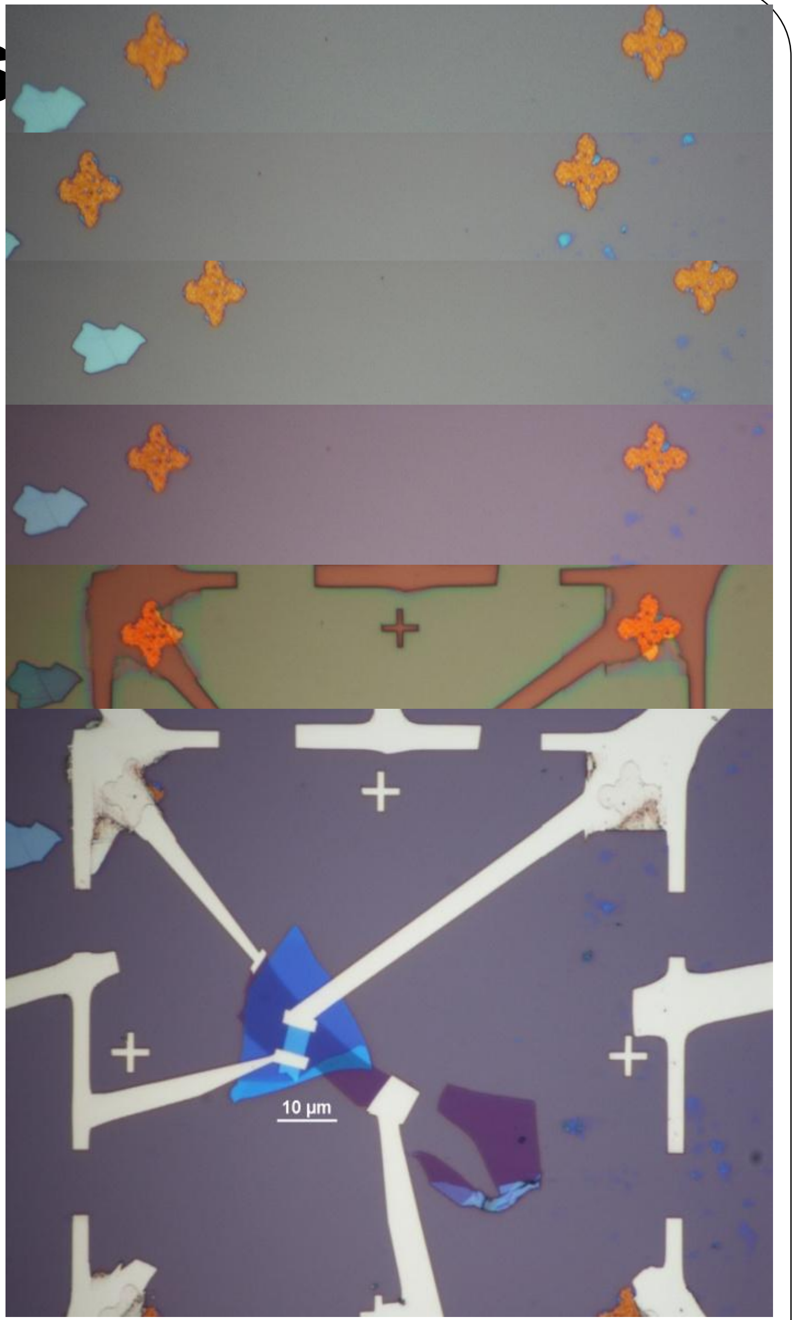
Using $$C = \frac{A\varepsilon_r\varepsilon_0}{t_{ox}}$$

We found: **K = 12.6**

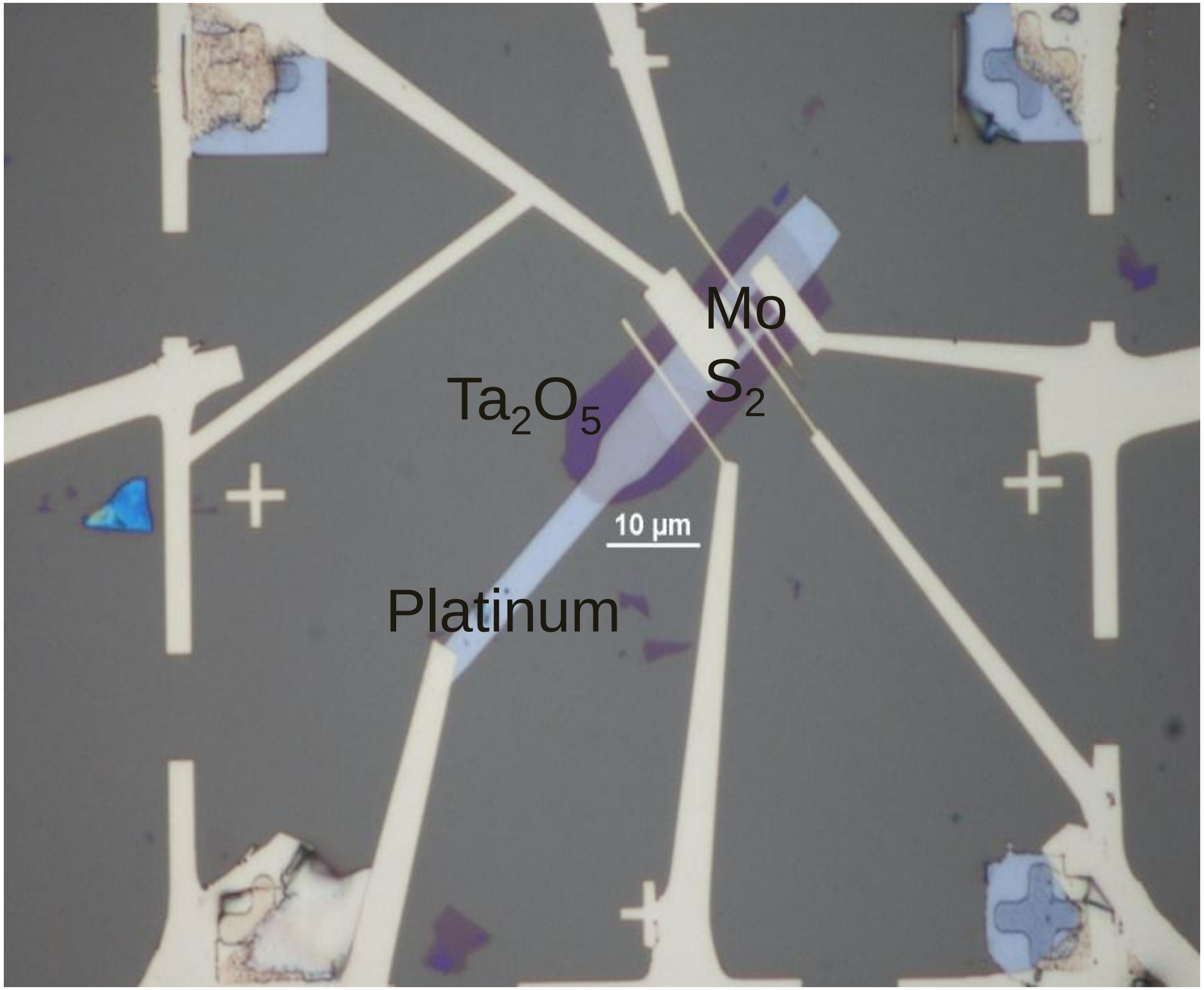
Experimental Details

1. Graphene Transfer
2. TaS_2 Transfer
3. Oxidation
4. MoS2 Transfer
5. E-beam Lithography
6. Gold Deposition



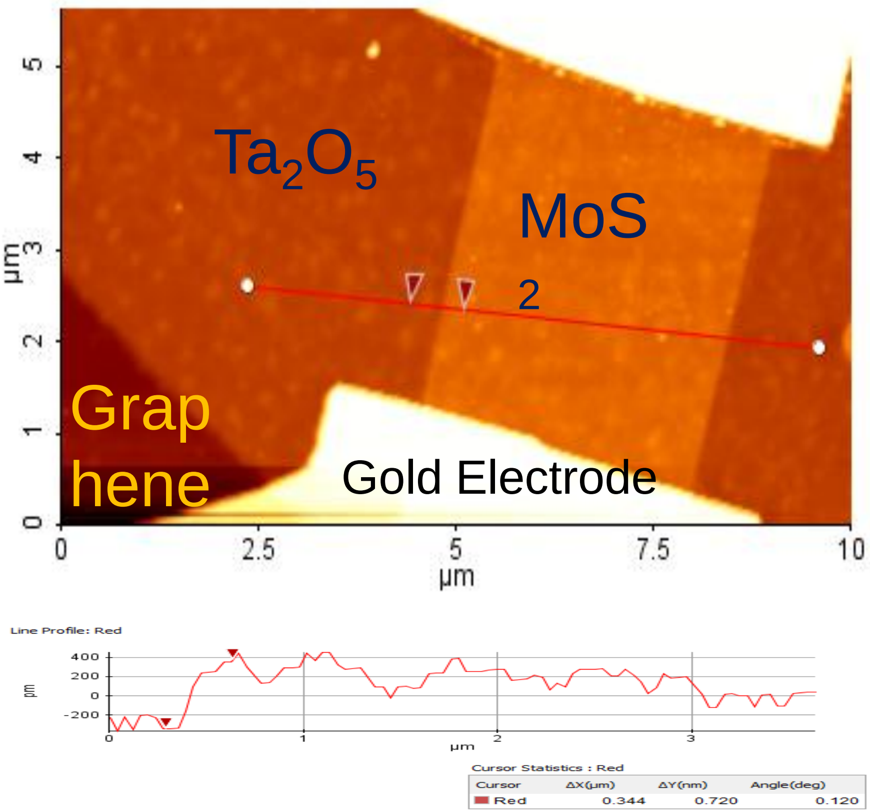


Platinum back-gate device :

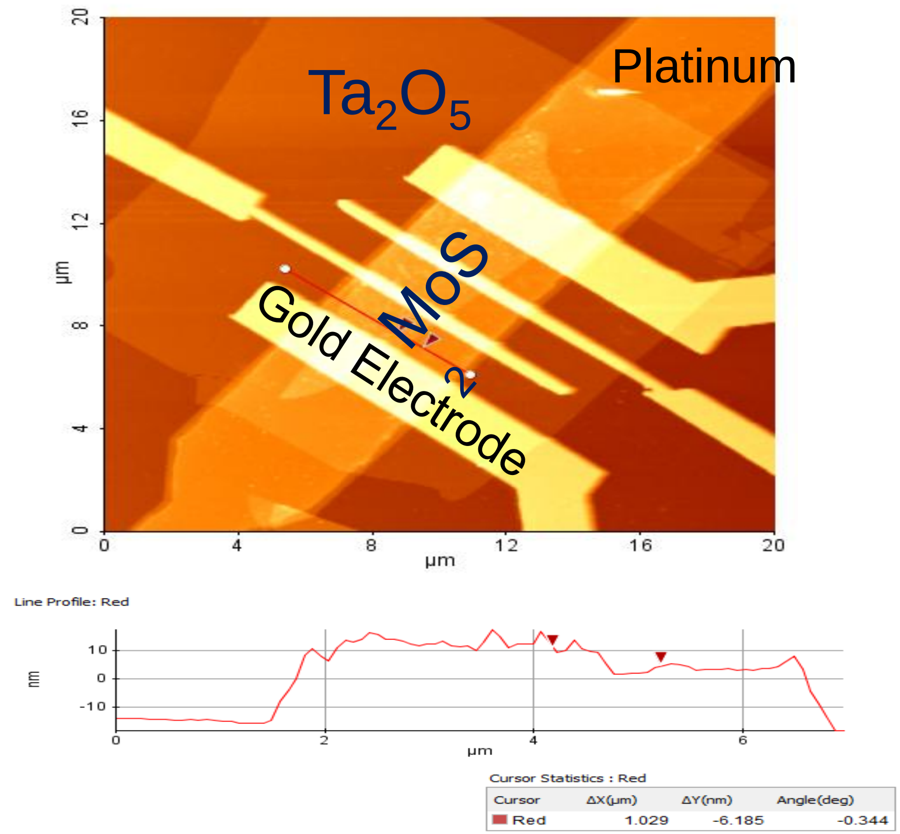


AFM Characterization :

Graphene back gate device



Platinum back gate device



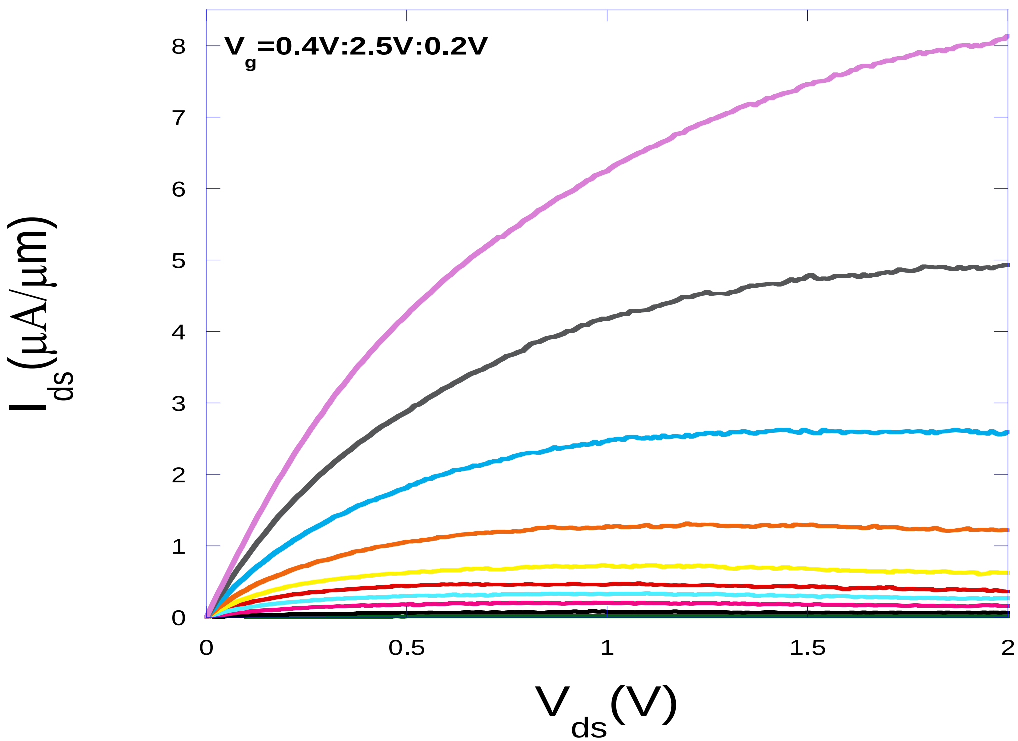
Gr : 8 nm
Ta_2O_5 : 18 nm
MoS2 : 7 nm

Pt = 22 nm
Ta2O5 = 12 nm
MoS2 = 6 nm

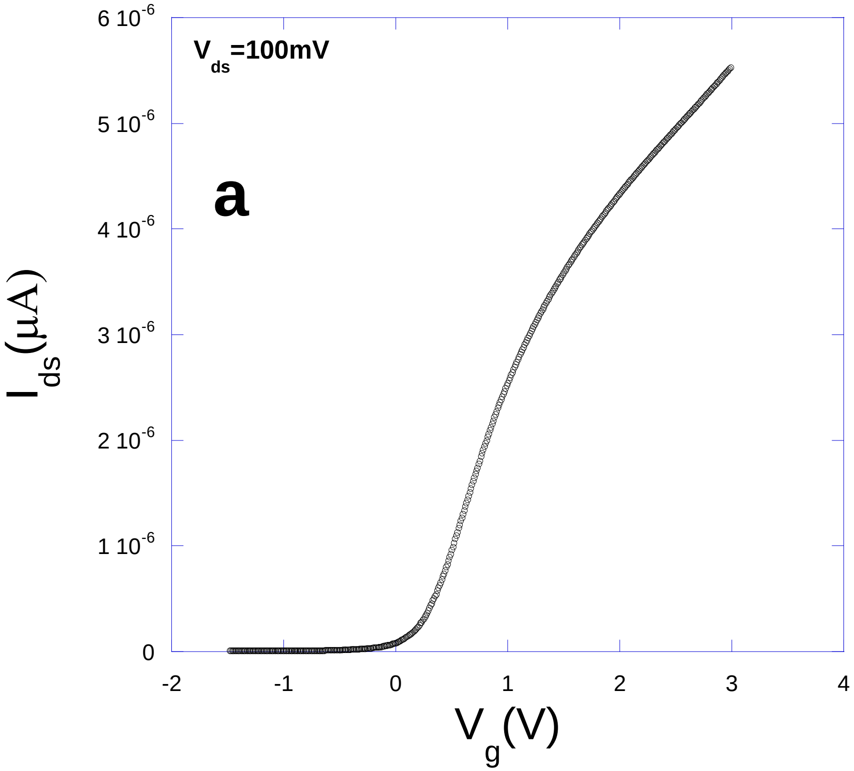
Electrical Characterization

Graphene Back gate Device

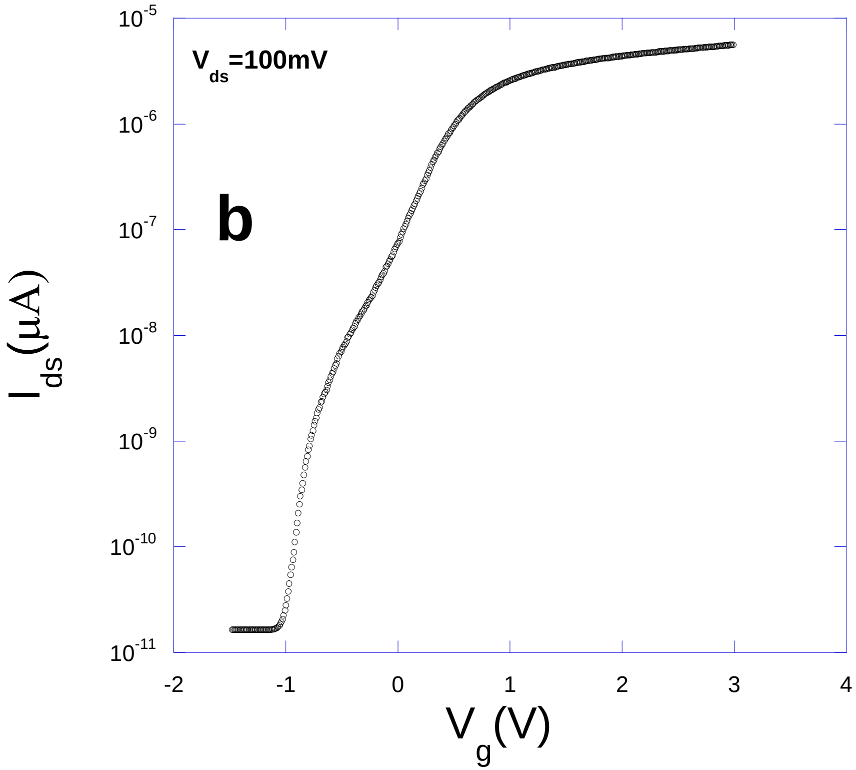
Output Characteristics



Transfer Characteristic

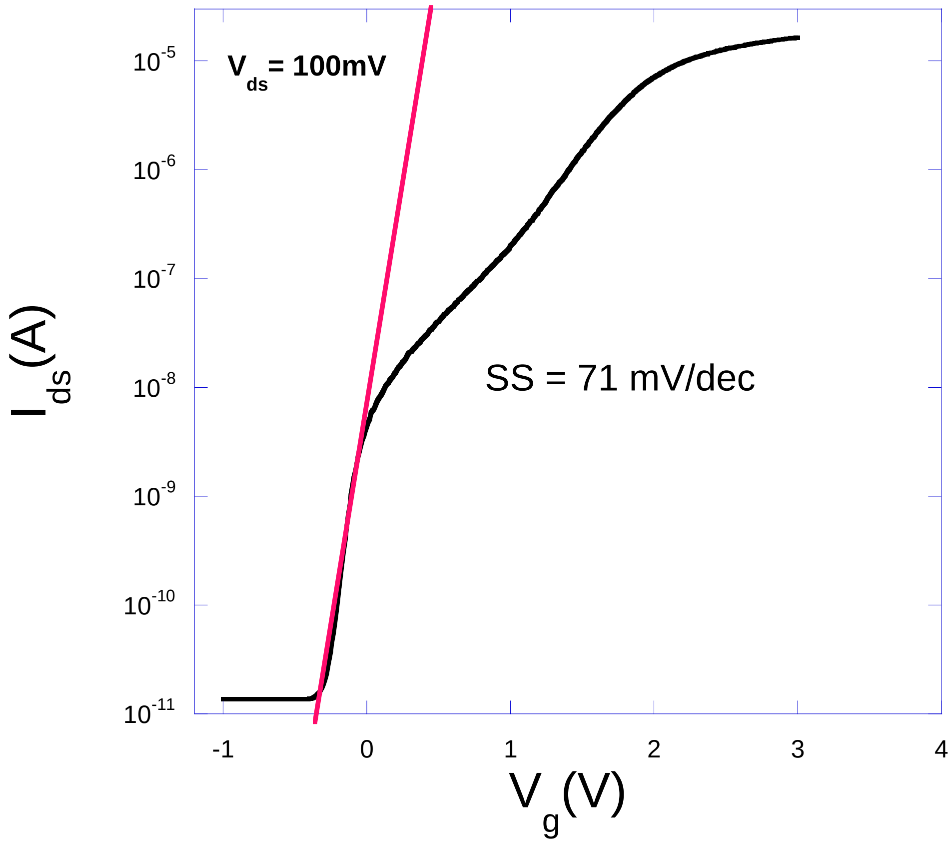


Linear plot



Semi-log plot

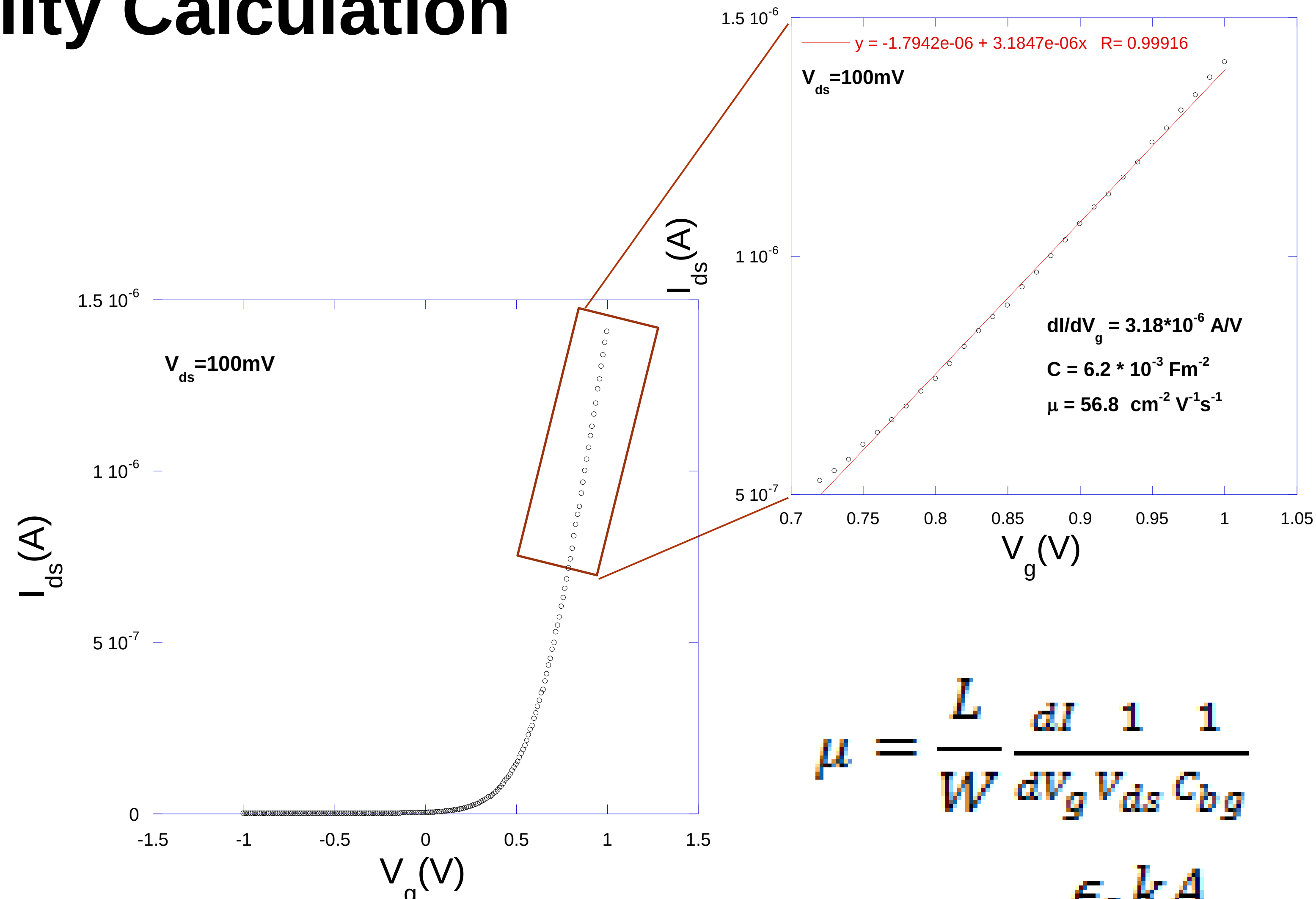
Sub-threshold Swing



Sub-threshold swing = Δx / (Order of Δy)

70 mV/decade ~ SS

Mobility Calculation

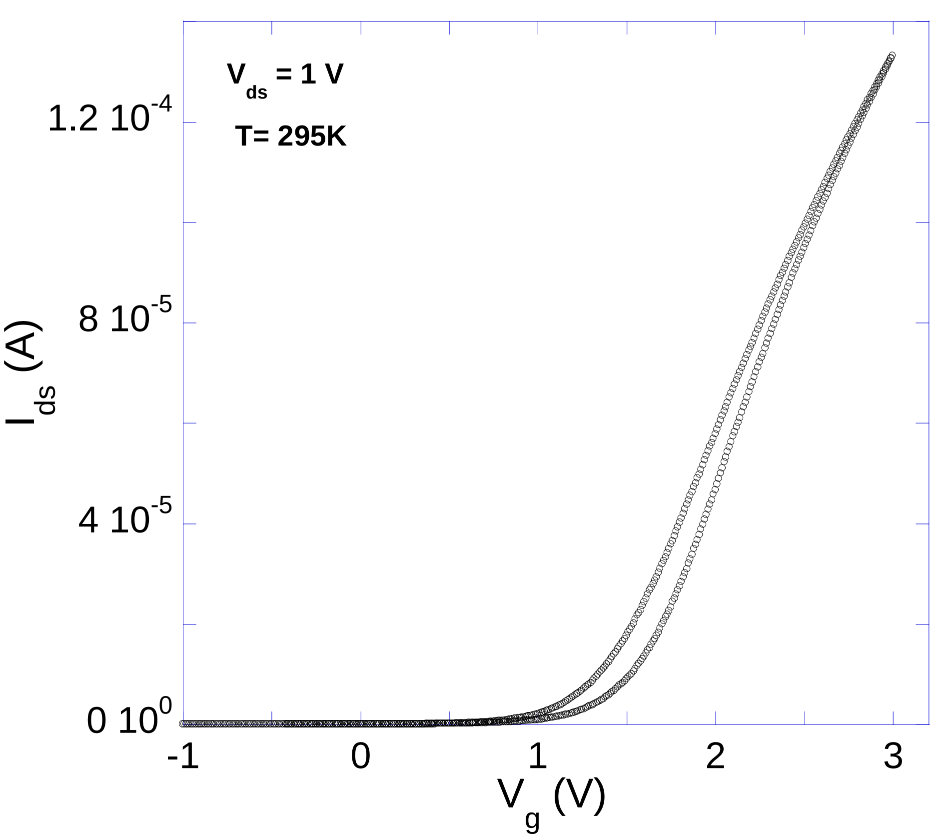


$$\mu = \frac{L}{W}\frac{dI}{dV_g}\frac{1}{V_{ds}}\frac{1}{C_{bg}}$$

$$C_{bg} = \frac{\epsilon_0 k A}{d}$$

$\mu \sim 55\ cm^2V^{-1}s^{-1}$

Hysteresis Behavior



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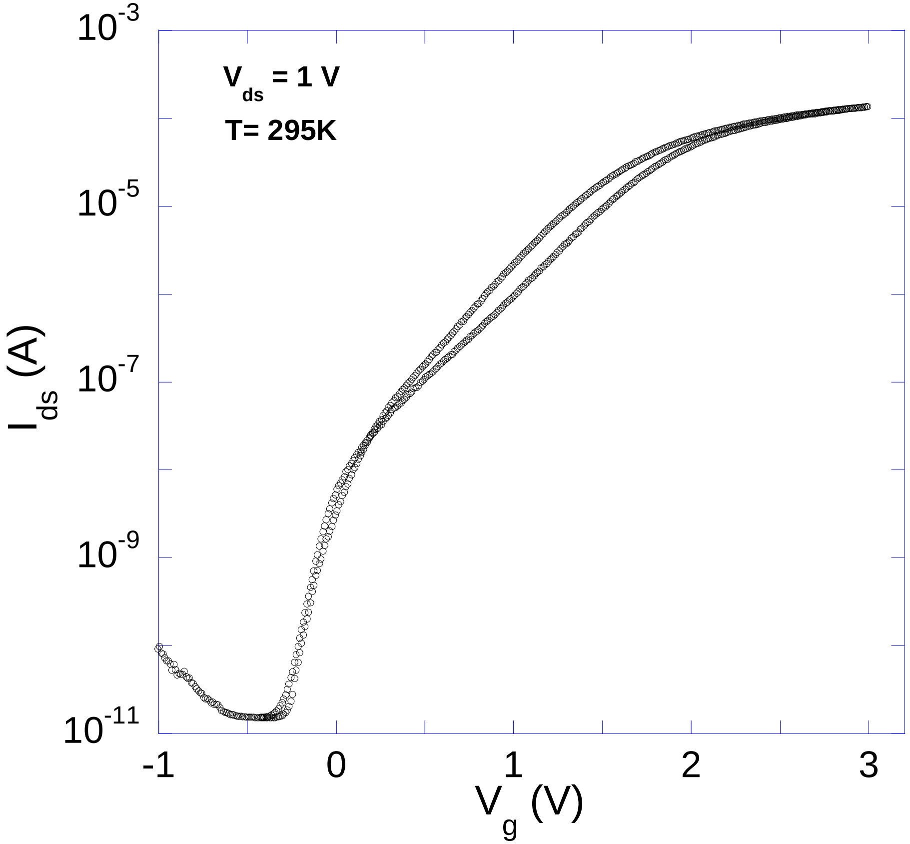

Semi-log plot

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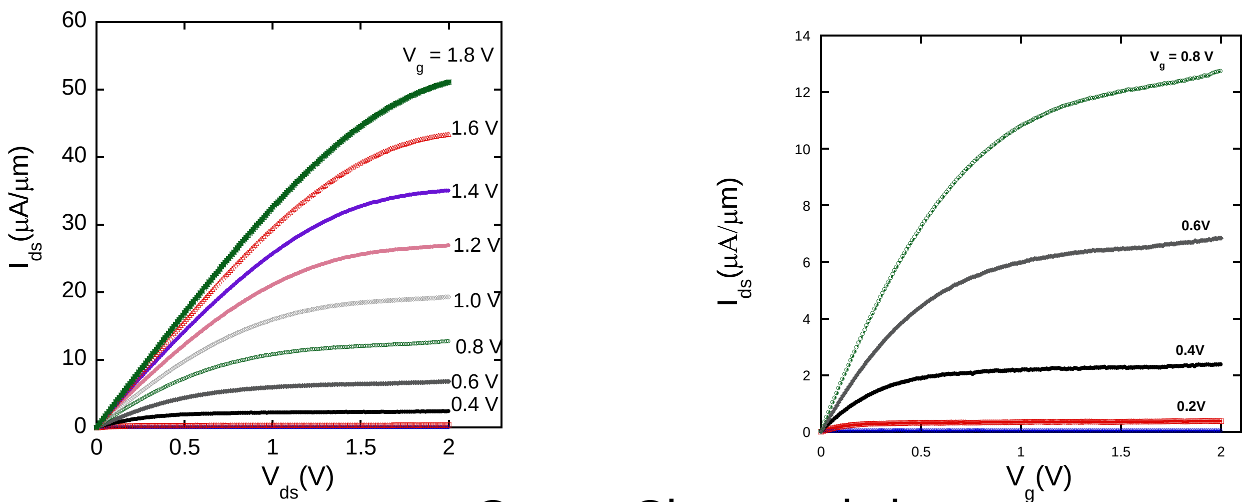
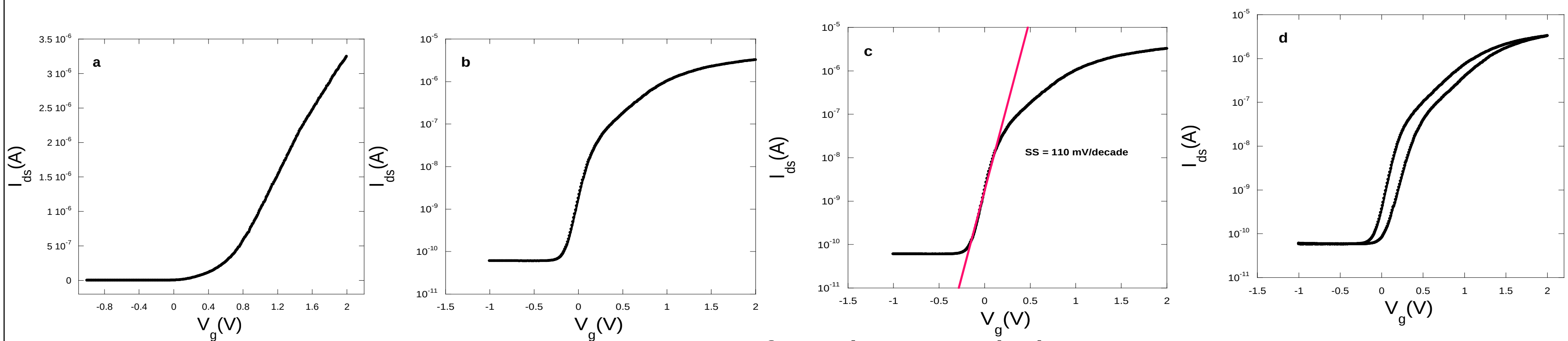


Output Characteristic



Transfer Characteristic

100 mV/decade < SS

$\mu \sim 50\ cm^2V^{-1}s^{-1}$

Future Works

- Ta_2O_5 as Top Gate dielectric
- Optimizing the Contacts with Graphene electr
- Optimizing the thermal oxidation Process
- Scaling of Dielectric thickness
- Scaling of Channel length

Acknowledgements

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Meeghage Perera.
Upendra, Kraig, Arthur, Prakash.


THANK YOU

High K Dielectrics

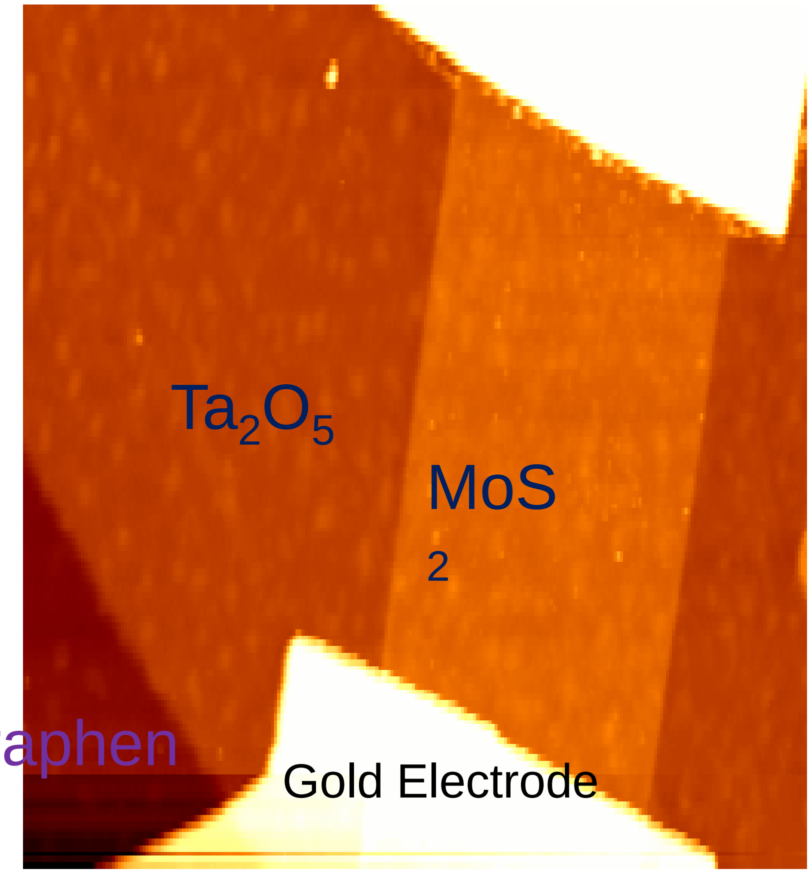
$$\frac{t_{eq}}{\varepsilon_{r,SiO2}} = \frac{t_{high\ k}}{\varepsilon_{r,high\ k}}$$

$t_{high\ K} = 10$ nm
$\varepsilon_{r,\ SiO2} = 3.9$
$\varepsilon_{r,\ Ta2O5} = 20$

$\Rightarrow$

$t_{eq} = 1.95$ nm

AFM Characterization :



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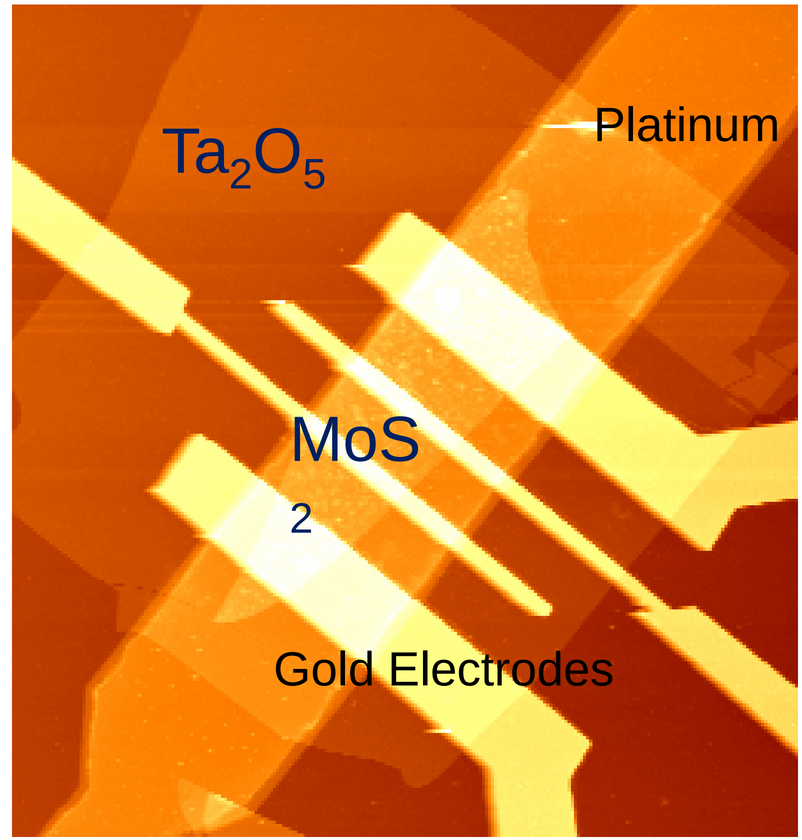

Platinum Back gate device

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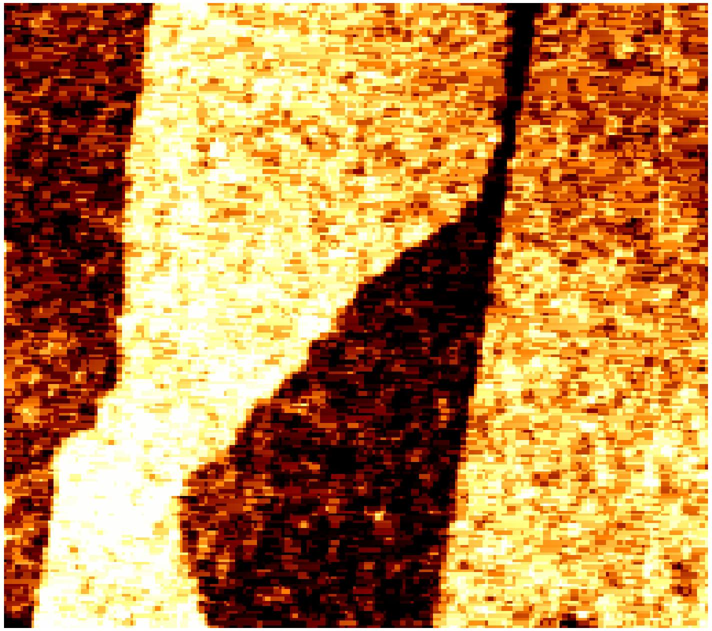
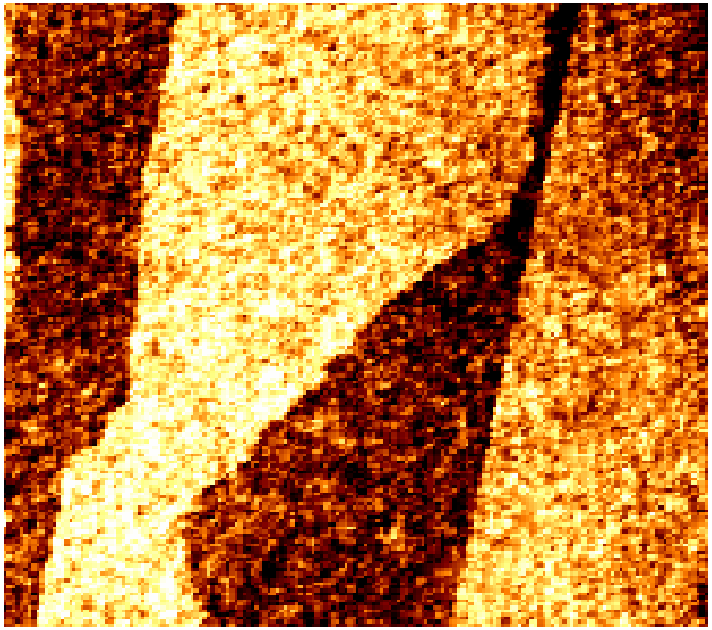


Before heating



After heating