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ABSTRACT

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Chapter 1

Introduction

1.1 Birth of Integrated Circuits

The development of microelectronics revolutionized the world in the latter half of the twentieth century. The term semiconductor, in the sense it is known today, first appears in literature in 1911 [1]. Initially, work on the subject was rather pessimistic. However, in the years following Word War II breakthroughs began shed light on the possible applications and the underlying physics involved, such as the ideas of *intrinsic* and *extrinsic* semiconductors [2, 3, 4, 5].

The history of semiconductors and transistors is a well documented subject. The first transistor was constructed at Bell Labs in 1947 using polycrystalline germanium. Shortly thereafter one was developed using silicon. Throughout the following years, these devices were improved on by replacing polycrystalline with single crystals [6]. Then Jack Kilby demonstrated the first integrated circuit (IC) in 1958, for which he would win the Nobel Prize in physics [7, 8]. The scale of ICs grew rapidly in the subsequent years. Initially only a few transistors could fit on a chip (small-scale integration), in stark contrast to moder-day chips that contains billions of transistors [9, 10]. Growth continued at a rapid pace, but eventually it was realized that some limits, material and integration based, existed in silicon and other commonly used materials [11, 12]. In part, these limitations increased the interest in alternative materials. As a result widespread and renewed interest has led to a breadth information and results on a wide range of materials and their applications.

1.2 Graphene as a New Two-dimensional Material

Layered materials have existed for billions of years, and have been studied over the last few centuries [13, 14]. In recent decades the scientific study of graphite (3D) has led to new forms materials, such as carbon nanotubes (1D) and fullerenes (0D) [15, 16, 17]. However, only more recently have scientists began to understand the potential of such layered materials and their potential technological applications. After attempting unsuccessfully to synthesize few-layer graphite during the 1960s (only around 10-50 layers were able to be synthesized) a breakthrough was finally achieved [16]. This most notably began with the synthesis of monolayer graphene [18].

1.2.1 Properties of Graphene

To date, graphene's properties have been the focus of much research, both theoretical and experimental. It has been one of the primary driving forces in study of 'relativistic' condensed matter physics due to its low dimensionality and its band structure that allows electrons to mimic relativistic particles confirming the appearance of several relativistic phenomena [19, 20, 21, 22]. In its most basic sense, graphene is

composed of a single layer of carbon atoms arranged in two-dimensional honeycomb lattice (see fig. 1.1). It has a Young's modulus of 100 GPa (several times more than steel) with a breaking force that is 13% of its Young's modulus [23, 24]. Its strength is due, in part, to its strong in-plane carbon (C) bonds. In addition, graphene can sustain elastic deformations of 20% due to its two-dimensional nature and it has high pliability [16]. These mechanical properties are of interest because graphene lies in the extreme ranges of many metrics considering its size and dimensionality.

Aside from its mechanical properties, graphene's transport properties were another reason why the material was so appealing. Graphene's mobility is several times that of silicon's. Experimental results have shown graphene mobility around $15,000 \text{ cm}^{-2}\text{V}^{-1}\text{s}^{-1}$ with a potential theoretical limit of $200,000 \text{ cm}^{-2}\text{V}^{-1}\text{s}^{-1}$ [25, 24]. The upper theoretical limit imposed on mobility is due to scattering, however, these high mobilities are achieved mainly because electrons in graphene act very much like photons in their mobility due to their lack of mass. This enables them to travel sub-micron distances without scattering [26]. In reality, there are other limiting factors that need to be considered such as the quality of graphene and scattering with the substrate, for example.

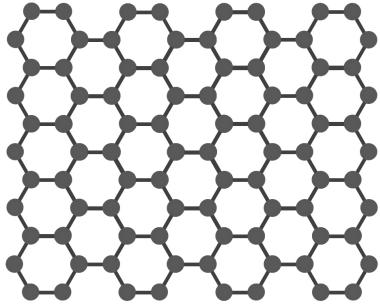


Figure 1.1: Graphene: a layer of carbon atoms in a honeycomb lattice.

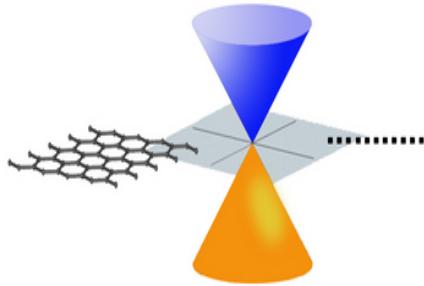


Figure 1.2: One of the most unusual features of graphene is that its conduction and valence bands meet at a point, meaning that in single-layer graphene there is no band gap (figure obtained from [27])

1.2.2 Band Structure of Graphene

Despite its impressive properties, the main drawback of graphene is its lack of bandgap. As this became known, the prospect of using graphene for the fabrication to ICs became unlikely. In graphene the conduction and valence bands touch at a single point as shown in fig. 1.2 [28]. Ultimately, the lack of a bandgap means that the current on/off ratio is low and is unappealing for logical circuit applications [29]. However, graphene exhibits some interesting properties as a result of having no bandgap, particularly as it pertains to its optical properties. The material's band structure allows for absorption of light over a large range of the electromagnetic spectrum, ranging from infrared ($< 1.65 \text{ eV}$) to ultraviolet ($> 3.2 \text{ eV}$), offering potential electronic-photonic device applications [30, 31, 32]. Since a direct use in logical circuits is not practical researchers have moved on to look for 'two-dimensional materials beyond graphene.' Several attempts at some derivatives of graphene-like materials have been studied, but for the most part they do not seem promising for use in logical circuits [33, 34]. As of late, research has been concentrated on two-dimensional materials, namely transition metal dichalcogenides, as a candidate for applications in ICs.

1.3 Two-dimensional Materials: Transition Metal Dichalcogenides

Commonly referred to two-dimensional materials beyond graphene, TMD have garnered much interest. TMDs were studied previously, however, they have gained renewed interest due to their properties [35, 36, 37, 38]. TMDs consist of hexagonal layers of metal (M) atoms in between two layers chalcogen (X) atoms (see fig. 1.4, such that the stoichiometry of the material is MX_2 [29]. The material is dependent on the type of transition metal, typically one of: molybdenum (Mo), tungsten (W), niobium (Nb), rhenium (Re), nickel (Ni), or vanadium (V), and two chalcogen atoms, typically one of: sulfur (S), selenium (Se), or tellurium (Te) [38, 39]. The most commonly studied variations of TMDs are molybdenum disulfide (MoS_2), tungsten diselenide (WSe_2), and tungsten disulfide (WS_2). These materials are commonly stacked together involving van der Waals interactions between adjacent sheets and covalent bonding within each individual sheet (see fig. 1.3) [29]. TMDs exhibit a wide variety of properties, including either being a

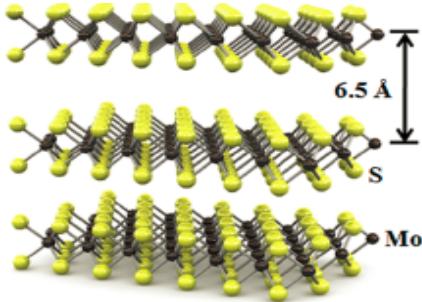


Figure 1.3: The atomic structure of a layered TMD, depicting MoS_2 . Each sheet is composed of three atoms with Mo sandwiched in between two S atoms, S-Mo-S. (Figure obtained from [40])

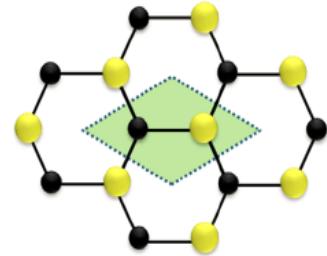


Figure 1.4: Top view of a TMD (MoS_2) lattice. (Figure obtained from [40])

metal or insulator, and displaying the topological insulator effect, superconductivity, and thermoelectricity [41, 42, 43, 44].

1.3.1 Properties of Commonly Used TMDs

As stated in sec. 1.2.2, one important property as it pertains to applications for logical circuits is the material's band structure. One of the main reasons TMDs have been so extensively studied lately is due to the fact that, unlike graphene, they do exhibit a band gap. The band gaps in some commonly used TMDs is interesting because of the transition from an indirect to a direct band gap as the layered thickness decreases. Fig. 1.5 illustrates this, for bulk and few-layer MoS_2 there is an indirect band gap while for monolayer MoS_2 there is a direct band gap. This unusual structure results in some unique optical and properties.

1.3.2 Current State of TMDs

1.4 Hall Effect

Give a brief overview of the history



Figure 1.5: Calculated band structures of (a) bulk MoS₂, (b) four-layer MoS₂, (c) bilayer MoS₂, and (d) monolayer MoS₂. Here the solid arrows indicate the lowest energy transitions. (Taken from [45], originally appeared in [46])

2D material	theoretical E_g (eV)	experimental E_g (eV)
graphene	0	0
bilayer graphene	0	0
bulk <i>h</i> -BN	-	5.97 [47]
monolayer <i>h</i> -BN	-	6.07 [48]
few layer (2-5) <i>h</i> -BN	-	5.92 [49]
bulk MoS ₂	1.2 ^{a,b} [50, 51]	1.0-1.29 ^b [50, 51]
monolayer MoS ₂	~ 1.90 ^{a,c} [52]	~ 1.90 ^b [52]
bulk WS ₂	~ 1.30 ^{a,b} [50, 53]	~ 1.35 ^c [50, 53]
monolayer WS ₂	~ 2.10 ^{a,c} [54]	-

^a Theoretical calculations based on first-principles calculations using density functional theory (DFT).

^b Indirect band gap semiconductor.

^c Direct band gap semiconductor.

Table 1.1: Summary of the band gaps of typical monolayer, bilayer, and bulk TMDs and *h*-BN materials. Table adapted from ref. [29].

1.4.1 Overview

1.4.2 Theoretical Background

Some useful references for this section [55, 56, 57, 58, 59, 60]

Chapter 2

Experimental Details

2.1 Substrate Preparation

Using degenerately doped silicon dioxide (SiO_2) wafers that are 270 nm thick as pictured in fig. 2.1 and the subsequent substrate's schematic in fig. 2.2, there are several preliminary steps needed prior to device fabrication. For easy identification of locations on the substrate alignment marks are placed on the wafer using photolithography. There is a main alignment mark pictured in fig. 2.4 (REALLY ONLY WANT TO REF A,B) which allows for quicker identification during electron beam lithography, for example. The alignment marks are in a grid pattern with the coordinate (0,0) at the center, stretching to $(\pm 6, \pm 6)$ in both the right and left directions. In each of these coordinate locations there smaller alignment marks evenly spaced within them as shown in fig. 2.4 (FIGURE OUT HOW TO REF SUBFIGS, HERE WE WANT TO REF (c,d)). Next, gold (Au) is deposited on the surface of the wafer, a process that will be explained in more detail in sec. 2.5.



Figure 2.1: Plain, polished uncut Si/SiO_2 wafer.

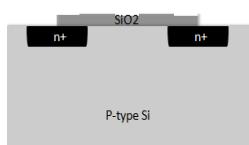


Figure 2.2: Schematic of Si/SiO_2 substrate.

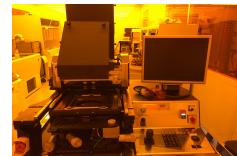


Figure 2.3: Photolithography system for creating alignment marks on substrates.

2.1.1 Substrate Cleaning

Beginning with a cut SiO_2 substrate with a deposited Au layer. To remove the Au layer, the substrate is first soaked in acetone for approximately 5-10 minutes then washed using isopropanol (IPA) and dried with nitrogen (N_2) gas. Next, the substrate is placed in acetone and sonicated for 15 minutes. Then sonicated once more but in IPA this time with a repetition of washing and drying step using IPA and N_2 as described above in between each sonication. In order to remove remaining organic matter on the surface of the substrate, the substrate is annealed under vacuum at 600°C for 10 minutes and passing forming gas for 2 of the 10 minutes. Forming gas is a mixture of H_2 and an inert gas, usually N_2 [61]. In addition to annealing the substrate for cleanliness, in certain cases when a higher degree of cleanliness is desired the substrate can be treated with oxygen plasma cleaning.

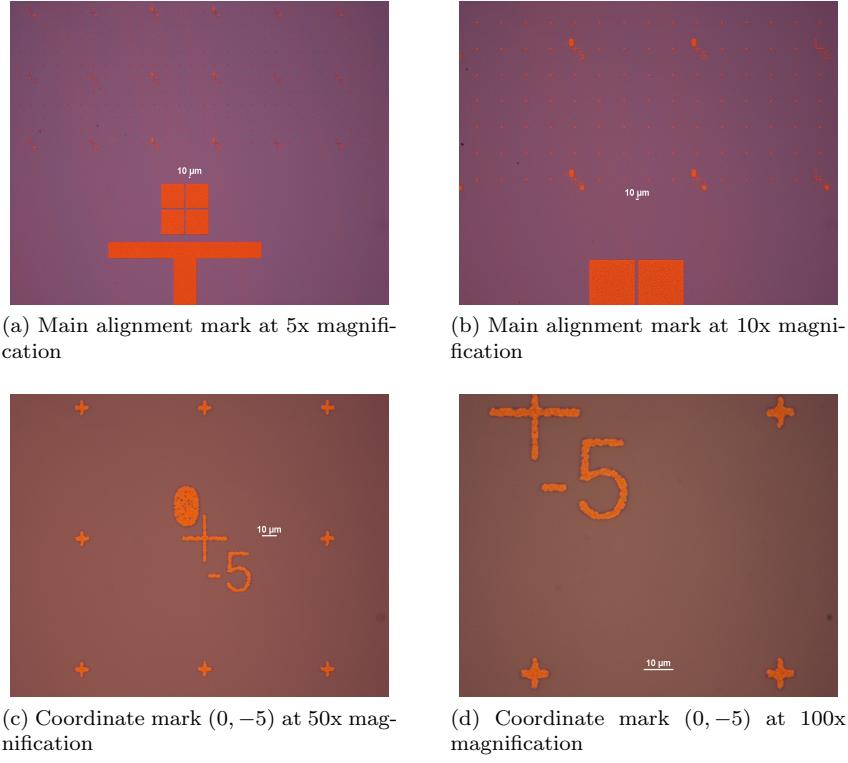


Figure 2.4: Main alignment mark and a coordinate point on a substrate at various magnifications

2.2 Exfoliation

To synthesize samples the most common and often most effective method used is mechanical exfoliation, a technique made famous by the 2004 Novoselov et al. paper. The process involves using Scotch tape to repeatedly cleave layers of MoS₂ or some other TMD. Starting with a crystal of a particular TMD, placing it on a piece of Scotch tape. Then taking another piece of tape and pressing in on the crystal that is on the first piece of tape, being sure to press hard and firm on the crystal. The tape is then lifted up and this process is repeated until the whole piece of tape is filled with small samples of the TMD. At the end of this process it is expected that there are a wide range of mixture of sample sizes in terms of area and in term of thickness as well, where thicknesses of < 3 nm are not uncommon. To better characterize the samples the optical microscope can be used to do so.

The main challenge that exists with this method is the ability to synthesize a high yield of monolayer samples. This does not seem to be much of a challenge when it comes to graphene and some other TMDs, but with regard to MoS₂ this is not so simple. Based on recently published literature in an effort to increase the yield of monolayer MoS₂ various methods and techniques were tested and modified accordingly [62]. In this modified method an additional step to cleaning the substrate is added in which it undergoes oxygen plasma cleaning for 10 minutes to ensure the cleanliness of the substrate's surface. To promote more bonding between the substrate and the samples, the substrate is first heated at 300 °C for 10 minutes without any samples on it. During this process the normal cleaving of sample on tape from crystal taking place. Once the substrate is done heating the tape containing sample is immediately placed on the substrate and pressed firmly for several minutes. Then the substrate (with the tape still on it) is placed on a glass slide (microscope slide) and is heated at around 85 °C for five minutes. Next, the substrate (with tape) is removed from heat and the tape slowly peeled back from the substrate. The result should be a much higher yield of < 3 nm samples of larger surface area, and several trilayer, bilayer, and a few

monolayer samples. (ADD PICTURES OF EACH STEP)

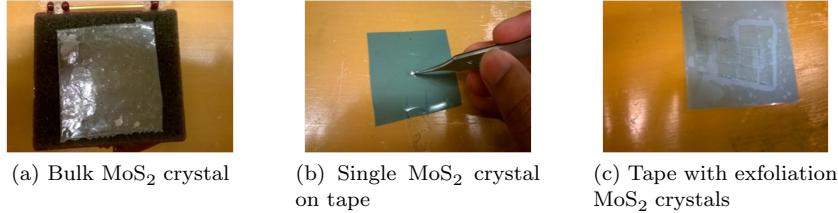


Figure 2.5: Steps of exfoliation of MoS₂.

Most commonly SiO₂ substrates are the main items that are exfoliated onto. However, depending on the material being synthesized, this may not always be the case. In cases where samples of hBN or in the event that the thickness of the synthesized sample is not of great importance and can be tolerated up to 20 – 30 nm, polydimethylsiloxane (PDMS) is exfoliated onto instead of SiO₂ substrates. The resulting samples are of varying thickness, on average around 20 nm. Thin samples (usually trilayer and above) can be made using this method of PDMS, however, these samples tend to have small surface area and lack uniformity which poses problems as to their usability. As such, this remains an effective method for obtaining samples in which thickness is not the main concern. Once the samples have been optically characterized, the sample(s) on PDMS must be transferred to a SiO₂ substrate.

2.3 Device Synthesis

Once the sample or samples have been synthesized and characterized for their specific purpose these samples can begin to be synthesized into a device for measurement. Generally, this involves the technique of transfer. Transfer is usually done using the aforementioned PDMS or using polycarbonate (PC) known as the PC pickup method. Each method has its advantages and disadvantages depending on the type of sample, type of device, or any number of the factors.

2.3.1 PDMS Transfer

PDMS transfer is most useful for samples that were originally exfoliated onto PDMS, for example hBN. To manufacture PDMS a 10:1 ratio of silicone base and curing agent is mixed together and placed in vacuum for 30 minutes to ensure the removal of any remaining air bubbles. After this time the mixture is then spin coated on a plain SiO₂ wafer and heated at 80 °C for 30 minutes then allowed to cool for 30 minutes. Once cooled, the surface of the wafer can be cut using a razor into small stamps that can be used for exfoliation and for transfer.

Once the samples that are to be transferred are on the PDMS stamp, then it is placed on a glass slide. Using the optical microscope to locate the sample on the stamp and using a razor to cut small excess pieces from the portions of the stamp where the desired sample is not located. This process is repeated until the size of the cut stamp is now reasonably small. The cut stamp is then placed at the edge of a new glass slide with sample area of the stamp as close to the edge as can be and the other side of the stamp is taped down using Scotch tape.

Next a substrate is placed and secured using glue (usually PMMA) to the stage of the transfer setup. The transfer stage setup is pictured in fig. 2.6. It consists of a microscope that has the capability of 10x or 20x magnification and a micro-manipulator. The micro-manipulator is where the glass slide with the PDMS stamp is placed. Using the manipulator the substrate on the stage is approached and the position of the stamp is checked and re-checked multiple times using the microscope to ensure correct overlap of

the desired portion of the sample(s). Upon reaching the desired position, the glass slide is lowered but this time there should be a contrast seen which is the overlapping of the glass slide and the substrate. Once the contrast has enveloped the entire sample that was to be transferred then the manipulator can be used to lift up the glass slide. Once the transfer is complete then the substrate should be annealed at 250 °C for 30 minutes in order to remove any residue or organic matter that may have remained during the transfer process.



Figure 2.6: Transfer stage setup

2.3.2 Polycarbonate Pickup Method

The PC pickup method is used for samples that have been exfoliated onto a SiO₂ substrate. Generally these are thinner samples with larger surface area that are not as easily obtained by using the PDMS exfoliation method as described in sec. 2.2. To manufacture the PC, 3.0 g of chloroform and 0.18 g of polycarbonate resin are put on a plate shaker for about 60 minutes or until the polycarbonate resin have dissolved into the solution.

Next, the substrate that has the sample that is going to be transferred is taped using double-sided tape to a glass slide facing up. Then using a syringe the PC solution is placed in the substrate and evenly spread across it. Being sure to locate the area(s) on the substrate where the sample(s) are located, small pre-cut pieces of PDMS are placed over top of these areas. An outline of the PDMS stamps is cut using a razor and any excess PDMS is carefully torn away. Once only the PDMS strips are remaining on the substrate deionized water (DI) is put under the strips in order to create a hydrophobic surface and to ensure that the strip and PC that is trapped underneath it come off the substrate with relative ease. Each strip is placed on its own glass slide and is gently blown with N₂ gas to remove any excess DI from the surface.

Moving to the transfer stage setup and following the steps described in sec. 2.3.1 with regard to using the transfer stage setup. The only difference at this point to using this method as opposed to PDMS transfer is in the final step of the transfer. Instead of only lowering until the contrast change is shown between the region that is desired to be transferred, with PC transfer the entire PC must be lowered down. This is because since the PC will be heated before being lifted up. Lowering all the way ensures that all the PC will be melted. Once lowered all the way, the heating device, which is connected to the stage, should be turned up to 130 °C. Once this temperature is reached, it should be maintained for approximately two minutes to fully melt the PC film. After heating the substrate and lifting up using micro-manipulator the substrate is placed in chloroform and covered for 30-60 minutes. The purpose of this is to remove any residue left over by the PC film or any other items that may have been introduced at any point in the transfer process. In practice the chloroform soaking generally needs to be repeated

several times over a few hours in order to ensure the least amount of remaining residue possible. To confirm the reduction of residue and also characterize the transferred samples an AFM is used.

2.4 Characterization

There are many ways used in modern academia and industry to characterize samples and devices. Some of these methods include scanning tunneling microscopy (STM), transmission electron microscopy (TEM), atomic force microscopy (AFM), and magnetic force microscopy (MFM) [57]. The primary characterization techniques used in this project are AFM and optical characterization.

2.4.1 Optical Characterization

The majority of the optical characterization is carried out using the optical microscope as shown in figs. 2.7 and 2.8. The microscope can magnify 5x, 10x, 20x, 50x, and 100x, in addition, it can show dark field images.

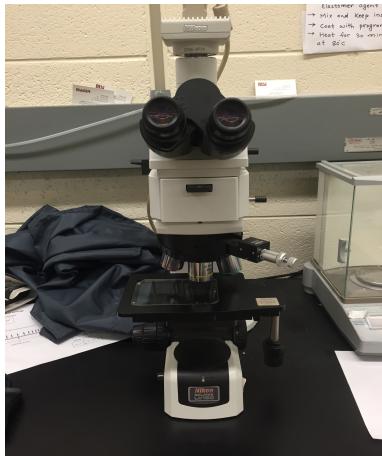


Figure 2.7: Optical microscope front view

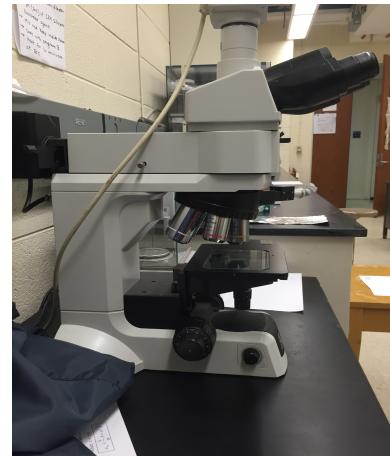


Figure 2.8: Optical microscope side view

2.4.2 AFM Characterization

In addition to the characterizing samples optically, AFM characterization is another important aspect of the device design and fabrication process. AFM characterization occurs several times throughout the process, after each transfer of a sample onto another, for example. This occurs for two reasons; to verify the thickness of the sample(s) that have been transferred, and also to verify the cleanliness of the surface of the sample (to ensure that any residue has been removed, especially during the course of PC transfer). Additionally, once the electrodes of the device have been fabricated a final AFM characterization is needed to determine the width of the device's channel which is needed to calculate various important electrical properties.

Fig. 2.9 shows a front view of the AFM used to characterize. For these purposes, the AFM is operating in “tapping” mode which is less invasive than “contact” mode [57]. In basic terms, an AFM works by measuring the force between the tip of a cantilever (see fig. 2.10) and the sample being imaged.



Figure 2.9: AFM front view

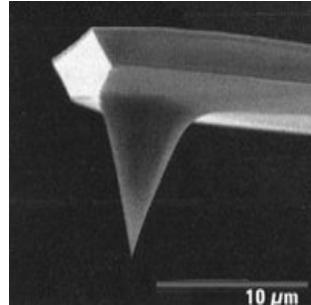


Figure 2.10: AFM cantilever [63]

2.5 Device Fabrication

In order to perform electrical measurements of devices one must fabricate devices. The devices are fabricated according to a specific process, though it is worth noting that under certain circumstances some steps of the process may be omitted or altered, however, the main idea remains the same regardless of the device type being fabricated. Once all transfer steps and samples have been placed in their correct locations the fabrication process begins. This process has three main steps: device design (sec. 2.5.1), electron beam lithography (EBL) (sec. 2.5.2), and metal deposition (sec. 2.5.3).

2.5.1 Device Design

The specifics of device electrode design depends largely on the type of measurement that is desired. For example, fig. 2.12(b) demonstrates a Hall bar device pattern. Despite the varying possibilities of patterns, the method for which the designs are generated remains largely the same. In order to generate these patterns a design software, Nanometer Pattern Generation System (NPGS), is used to draw the electrodes which in turn communicates the designed pattern to the SEM [64].

In preparation for EBL the substrate is spin-coated with two layers of polymethyl methacrylate (PMMA). The first layer of PMMA is 495-A4 is added then the substrate is baked on a hot plate for 5 minutes at 180° C. The first layer is followed by another layer of PMMA, 950-A2 (same polymer of different molecular weight). Again, the substrate is spin-coated with this PMMA layer and baked at the same temperature for 5 minutes.

2.5.2 Electron Beam Lithography

To generate the patterns described in sec. 2.5.1 a SEM is used to complete EBL. Fig. 2.11 shows the control panel and electron beam writer of the SEM. The SEM is optimized by adjusting the beam current to the saturation point. Using the alignment marks mentioned in sec. 2.1 the electron beam is aligned to correct position on the substrate. The NPGS system allows for adjustments in the concentration of the electron beam current at certain areas. For example, whether a line does or an area dose is necessary. In general, these values are adjusted as needed depending on the device design but are usually around $300 \mu\text{C cm}^{-2}$ for area doses and $15 \mu\text{C cm}^{-1}$ for line doses. Ultimately, the EBL process creates three separate patterns that are joined together. The first pattern is written at 1000x magnification on the SEM (see fig. 2.12(b)). The second and third patterns (written at 300x and 100x, respectively, see fig. 2.12(a)) are connected to the inner 1000x pattern and they connect this inner pattern to the “electrode pads” where the electrodes will eventually be connected for device measurement. After completing the device pattern, the substrate is developed in a solution of methyl isobutyl ketone (MIBK) and methyl ethyl ketone (MEK) for 70 seconds. The MIBK is the main developer while the MEK acts to enhance the developing process, both fig. 2.12(a) and fig. 2.12(b) have undergone this development process.



Figure 2.11: Control panel and electron beam writer of scanning electron microscope.

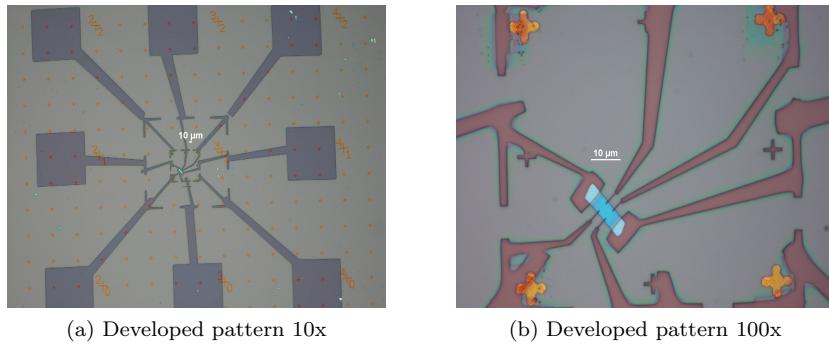


Figure 2.12: 10x and 100x electron beam lithography patterns developed using MIBK and MEK.

2.5.3 Metal Deposition

In order to make proper electrical contacts metal must be deposited on the pattern made by EBL. This process of metal deposition is done using a Bell Jar deposition (BJD) system (fig.) which evaporates 10 nm of titanium (Ti) followed by 40 nm of Au on the substrate's surface at ultrahigh vacuum ($\sim 10^{-7}$ torr) at a rate of 1 \AA s^{-1} . After the metal deposition process is complete, a process called "lift-off" is performed. In this process the substrate is placed in acetone for approximately 5-10 minutes, until the Au has "lifted-off." Once this process is complete all that remains on the substrate is Au where the EBL was performed. Fig. 2.14 illustrates a substrate that has undergone the lift-off process, all that remains is the portion of the pattern that is necessary to perform electrical measurements on the device.

2.6 Electrical Measurements and Characterization

Upon completion of the fabrication process and physical characterization processes, the remaining process is electrical characterization. Many of the options available in electrical characterization are put to use, at least in some capacity regardless of the device. Then, depending on the device's quality, further measurements can be made in which a more comprehensive electrical data profile can be obtained.

2.6.1 Measurement Devices

Pictured in fig. 2.15(a) is a measurement device that allows for automated electrical data collection through pre-made programs. The user adjusts parameters and the desired device properties to be measured. Initially, the device is usually measured in non-vacuum conditions at room temperature in order to determine the device's quality. If it is determined that the device's quality is worth continuing with low temperature measurements then the substrate is placed in the vacuum measurement chamber pic-

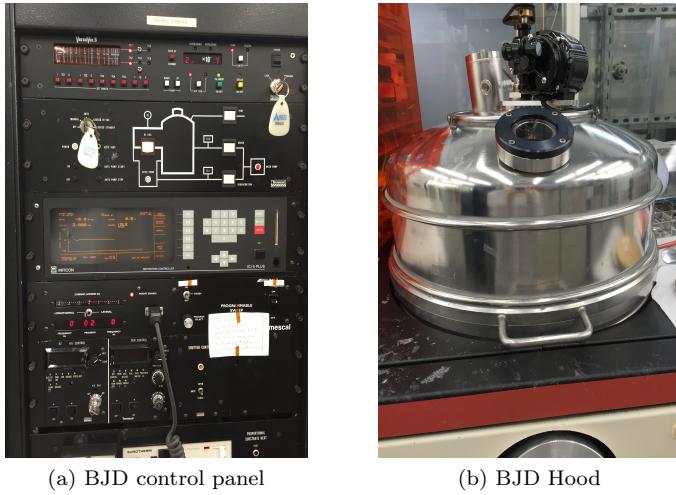


Figure 2.13: BJD evaporation system in cleanroom environment

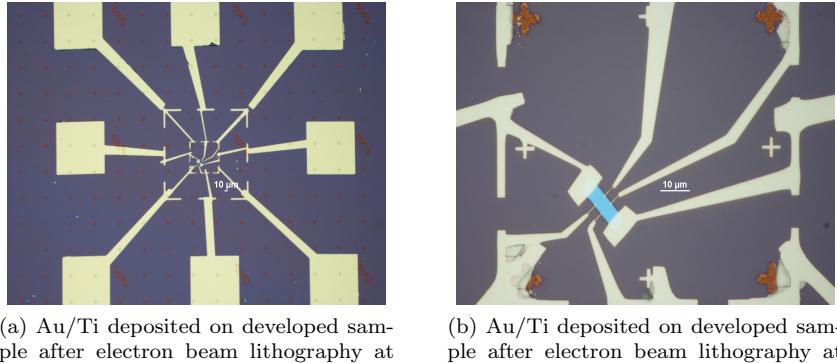


Figure 2.14: Metal deposition on a device pattern.

tured in fig. 2.15(b). This apparatus is used in conjunction with the measurement setup in fig. 2.15(a) to continue measurements. However, in this configuration the measurements take place under ultrahigh vacuum ($\sim 10^{-6}$ to 10^{-7} torr) and temperature control via liquid nitrogen (with the ability to cool to 70 K). In addition, there is another measurement device that allows for both temperature control and the application of a magnetic field. This device, known as a physical property measurement system (PPMS), is shown in fig. 2.15(c) and is used in situations when it is necessary to apply a magnetic field such as measuring a Hall device.

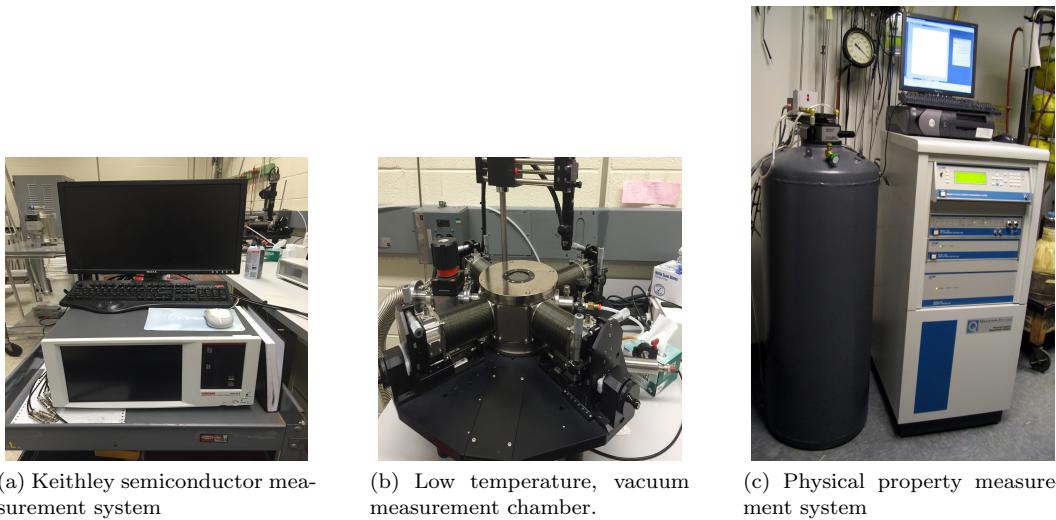


Figure 2.15: Electrical measurement devices used for electrical characterization of samples including vacuum and low temperature environments.

Chapter 3

Studying Intrinsic Channel Properties, Scattering Mechanisms, and Quantum Transport

Developing low resistance two-dimensional/two-dimensional (2D/2D) ohmic contacts opens up possibility to study the intrinsic properties of TMDs and quantum physics. In particular, quantum phenomena inherent to two-dimensional electron gass (2DEGs) and two-dimensional hole gass (2DHGs) such as the integers and fractional quantum Hall effects and Shubnikov-de Haas (SdH) oscillations can be explored in high mobility monolayer and few-layer TMDs [65]. In addition to quantum transport properties and quantum effects in monolayer and few-layer TMDs the study of mobility and its corresponding temperature dependence can be used to understand the multiple scattering mechanisms present [66]. These study of both electron and hole transport mechanisms is important due to the fact that high-performance *p*-type and *n*-type transistors are necessary for complimentary digital applications.

3.1 *p*-type MoS₂ Semiconductor Doping

One of the major challenges that still remains in fabricating devices to study quantum transport and scattering mechanisms is developing high quality *p*-type MoS₂ devices. This is due to the fact that the metal/MoS₂ interface is obstructed by a large Schottky barrier (SB) formed by Fermi level pinning close to the conduction band of the MoS₂ [67, 68].

3.1.1 *p*-type MoS₂ and WSe₂ Semiconductor Contact Resistance

To study the effects of doping and how it affects the Schottky barrier height (SBH) several MoS₂ device geometries were designed. In particular, the purpose is to find how doping MoS₂ and WSe₂ can help improve the 2D/2D contacts in devices and, in addition, how doping the channel affects the intrinsic properties of the device. To address the the issue of contact resistance, transmission lines were designed in which electrodes are spaced at varying lengths from the source electrode. Resistance is given by

$$R = \frac{\rho}{A} l, \quad (3.1)$$

where, in this case, it is assumed that the resistivity ρ and the area A are constant throughout [56]. Thus the resistance R is then proportional to the length l . By determining the resistance as a function of length one can determine the inherent contact resistance of the device. This is done by using what is known as the transmission line model (TLM). In this approach the total resistance is given by

$$R = R_c + R_{ch}, \quad (3.2)$$

where R_c and R_{ch} are the contact and channel resistances, respectively [56]. Thus by finding the resistance from the gradient of an $I - V$ characteristic curve one can apply the logic from eq. 3.1 to find the overall contact resistance. Fig. 3.1(a), fig. 3.1(c), and fig. 3.1(e) illustrate the design of several 0.05% WSe₂ doped WSe₂ transmission lines with varying lengths of electrodes. Ultimately, the contact resistance from using the TLM is illustrated in fig. 3.1(b), fig. 3.1(d), and fig. 3.1(f). The corresponding contact resistances for each device are: 4.70 kΩ m, 25.8 kΩ m, and 19.3 kΩ m for the devices shown in fig. 3.1(a), fig. 3.1(c), and fig. 3.1(e), respectively.

3.1.2 *p*-type MoS₂ and WSe₂ Semiconductor Intrinsic Channel Properties

To further study the intrinsic channel properties of TMDs Hall bar devices were fabricated. The devices are encapsulated in hBN, meaning the TMD lies sandwiched between two hBN layers. The bottom hBN acts as a substrate while the top hBN covers the center part of the TMD flake. Fig. 3.2(a) and fig. 3.2(b) illustrate the design of the Hall bar devices used in this study. In addition, these figures further show the doping scheme used here. In order to form better 2D/2D contacts the drain/source contacts are degenerately doped Nb and the semiconductor channel is fabricated using 0.05% Nb doped WSe₂.

The Hall effect measurement is widely used for device characterization because it gives the resistivity ρ , carrier density n , and mobility μ . Using the PPMS a magnetic field is applied perpendicular to the current flow direction producing an electric field that is perpendicular to the magnetic field and the current. For example, consider the case shown in fig. 3.6 where current is flowing in the $+x$ -direction with a magnetic field applied in the $+z$ -direction. The result is that the Lorentz force will accelerate the holes (*p*-type material) in the $-y$ -direction. For holes the electric field points in the $+y$ -direction. The force felt by holes is given by

$$\vec{F} = q \left(\vec{E} + \vec{v} \times \vec{B} \right), \quad (3.3)$$

where \vec{E} , \vec{v} , and \vec{B} are the electric field, velocity, and magnetic field, respectively. In addition, the current is given by

$$I = qtdpv_x, \quad (3.4)$$

where q is the charge of an electron, t is the thickness of the sample, d is the width of the sample, p is the hole density, and v_x is the velocity of holes in the x -direction. Combining eqs. 3.3 and 3.4 gives the electric field,

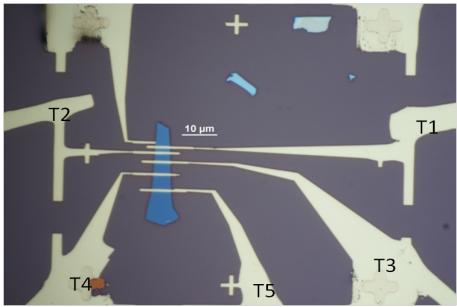
$$E_y = Bv_x = \frac{BI}{qwt}. \quad (3.5)$$

The electric field in the y -direction produces the Hall voltage V_H . Integrating the electric field one arrives at the Hall coefficient R_H which is defined as

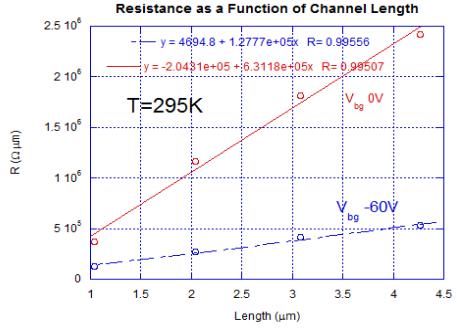
$$R_H = \frac{1}{pq} = \frac{V_H t}{IB}. \quad (3.6)$$

Furthermore, the Hall mobility μ_H is defined by

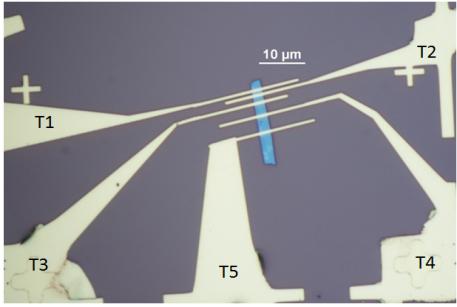
$$\mu_H = \dots \quad (3.7)$$



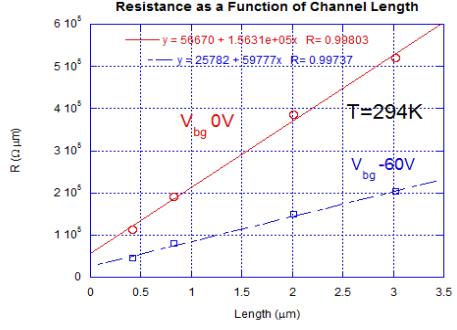
(a) 0.05% Nb doped WSe₂ channel transmission lines with corresponding channel lengths and widths of $L_{12} = 1.04 \mu\text{m}$, $W_{12} = 4.42 \mu\text{m}$, $L_{23} = 2.04 \mu\text{m}$, $W_{23} = 4.47 \mu\text{m}$, $L_{34} = 3.09 \mu\text{m}$, $W_{34} = 4.90 \mu\text{m}$, $W_{45} = 5.15 \mu\text{m}$, and $L_{45} = 4.27 \mu\text{m}$.



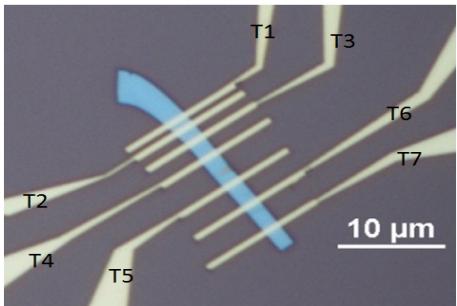
(b) Caption here



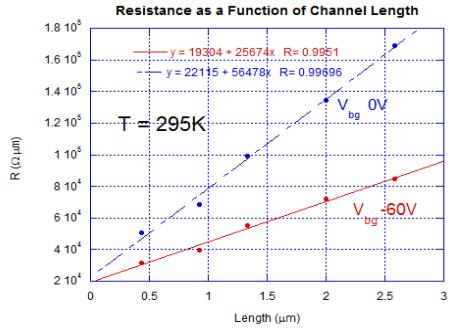
(c) 0.05% Nb doped WSe₂ channel transmission lines with corresponding channel lengths and widths of $L_{12} = 0.42 \mu\text{m}$, $W_{12} = 2.27 \mu\text{m}$, $L_{23} = 0.83 \mu\text{m}$, $W_{23} = 2.30 \mu\text{m}$, $L_{34} = 2.01 \mu\text{m}$, $W_{34} = 2.27 \mu\text{m}$, $W_{45} = 2.45 \mu\text{m}$, and $L_{45} = 3.02 \mu\text{m}$.



(d) Caption here

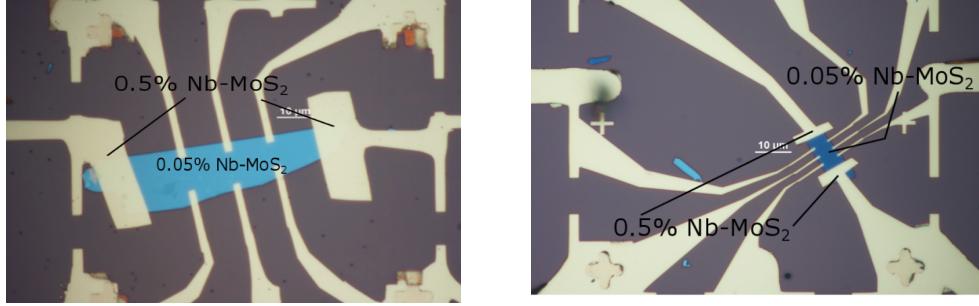


(e) 0.05% Nb doped WSe₂ channel transmission lines with corresponding channel lengths and widths of $L_{12} = 0.43 \mu\text{m}$, $W_{12} = 2.10 \mu\text{m}$, $L_{23} = 0.93 \mu\text{m}$, $W_{23} = 1.90 \mu\text{m}$, $L_{34} = 1.34 \mu\text{m}$, $W_{34} = 1.98 \mu\text{m}$, $L_{56} = 2.00 \mu\text{m}$, $W_{56} = 1.89 \mu\text{m}$, $W_{67} = 1.80 \mu\text{m}$, and $L_{67} = 2.58 \mu\text{m}$.



(f) Caption here

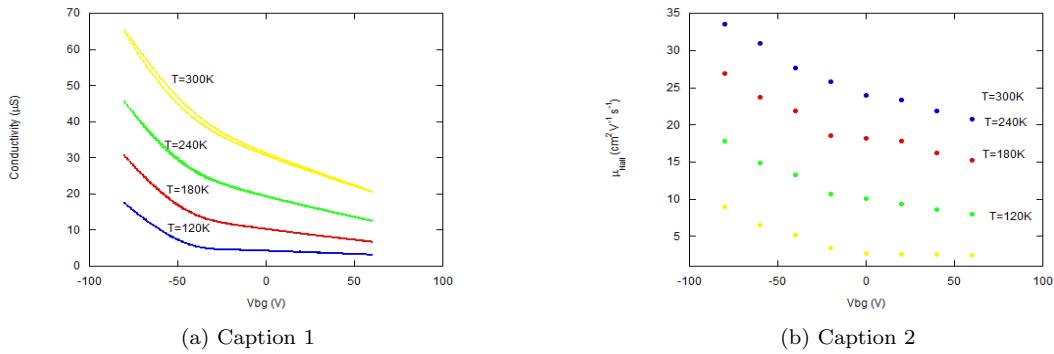
Figure 3.1: Several 0.05% Nb doped WSe₂ transmission lines with varying lengths and widths.



(a) Hall bar device with a 0.05% Nb doped WSe_2 channel. Device thickness is 18.6 nm with an average width of $W_{\text{avg}} = 14 \mu\text{m}$.

(b) Hall bar device with a 0.05% Nb doped WSe_2 channel. Device thickness is 7.74 nm with an average width of $W_{\text{avg}} = 5.74 \mu\text{m}$.

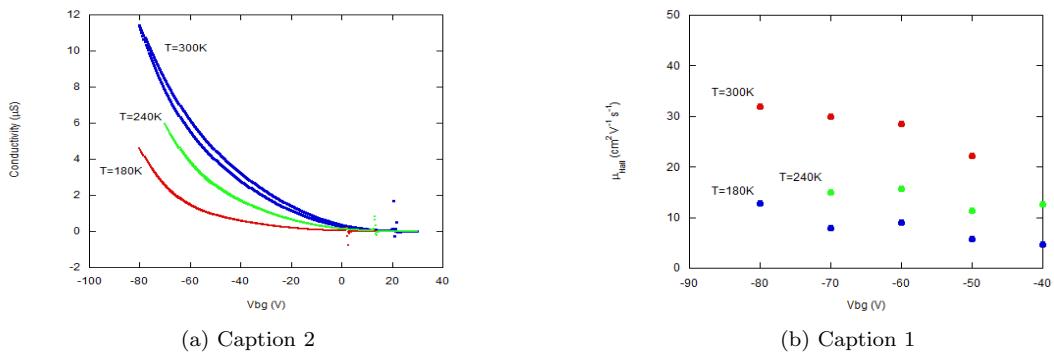
Figure 3.2: Degenerately doped contact and lightly doped channel WSe_2 Hall bar devices.



(a) Caption 1

(b) Caption 2

Figure 3.3: caption



(a) Caption 2

(b) Caption 1

Figure 3.4: caption

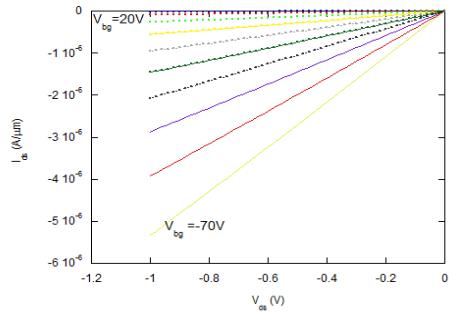


Figure 3.5: $T = 300\text{ K}$ add more here

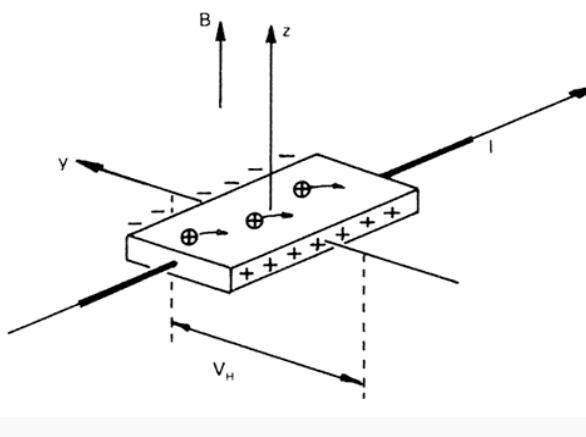


Figure 3.6: The current I flows in the $+x$ -direction and the magnetic field B is applied in the $+z$ -direction deflects positive charge carriers (holes) in the $-y$ -direction generating a Hall voltage V_H [69, 70].

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Appendices

2DEG two-dimensional electron gas

2DHG two-dimensional hole gas

AFM atomic force microscopy

Au gold

BJD Bell Jar deposition

DI deionized water

DFT density functional theory

EBL electron beam lithography

IC integrated circuit

IPA isopropanol

MEK methyl ethyl ketone

MFM magnetic force microscopy

MIBK methyl isobutyl ketone

Mo molybdenum

MoS₂ molybdenum disulfide

N₂ nitrogen

Nb niobium

Ni nickel

NPGS Nanometer Pattern Generation System

PC polycarbonate

PDMS polydimethylsiloxane

PMMA polymethyl methacrylate

PPMS physical property measurement system

Re rhenium

S sulfur

SB Schottky barrier

SBH Schottky barrier height

Se selenium

SEM scanning electron microscope

SdH Shubnikov-de Haas

SiO₂ silicon dioxide

STM scanning tunneling microscopy

Te tellurium

TEM transmission electron microscopy

TLM transmission line model

Ti titanium

TMD transition metal dichalcogenides

V vanadium

W tungsten

WS₂ tungsten disulfide

WSe₂ tungsten diselenide