

**Quantum Transport Properties and Scattering Mechanisms in Transition Metal
Dichalcogenides**

by

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ABSTRACT

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Two-dimensional materials have garnered much interest since the isolation of graphene. Since then layered materials, such as transition metal dichalcogenides (TMDs) have been studied extensively. However, several key problems have yet to be solved. In this study we propose using methods developed to decrease and minimize contact resistance through a novel approach of 2D/2D contacts and hBN encapsulation to study how the mobility and intrinsic properties are affect by *p*-doping WSe₂ device channels. Preliminary results show contact resistance as low as $0.185 \text{ k}\Omega \cdot \mu\text{m}$ using degenerately doped contacts and field-effect mobilities of $\sim 200 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $\sim 650 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at $T = 300 \text{ K}$ and $T = 5 \text{ K}$, respectively using this 2D/2D contact hBN encapsulation method. In addition, this method is intended to improve mobility at both room temperature for device applications and at low temperatures ($\sim 4 \text{ K}$) to study the integer quantum hall effect (IQHE) and the corresponding related Shubnikov-de Haas oscillations (SdH) to determine information related to quantum scattering times, effective cyclotron mass, and the geometry of the Fermi surface.

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Chapter 1

Introduction

1.1 Early Semiconductors

The development of microelectronics revolutionized the world in the latter half of the twentieth century. The term semiconductor, in the sense it is known today, first appears in literature in 1911 [1]. Initially, work on the subject was rather pessimistic. However, in the years following Word War II breakthroughs began shed light on the possible applications and the underlying physics involved, such as the ideas of *intrinsic* and *extrinsic* semiconductors [2, 3, 4, 5].

The history of semiconductors and transistors is a well documented subject. The first transistor was constructed at Bell Labs in 1947 using polycrystalline germanium. Shortly thereafter one was developed using silicon. Throughout the following years, these devices were improved on by replacing polycrystalline with single crystals [6]. Then Jack Kilby demonstrated the first integrated circuit (IC) in 1958, for which he would win the Nobel Prize in physics [7, 8]. The scale of ICs grew rapidly in the subsequent years. Initially only a few transistors could fit on a chip (small-scale integration), in stark contrast to modern-day chips that contains billions of transistors [9, 10]. Growth continued at a rapid pace, but eventually it was realized that some limits, material and integration based, existed in silicon and other commonly used materials [11, 12]. In part, these limitations increased the interest in alternative materials. As a result widespread and renewed interest has led to a breadth information and results on a wide range of materials and their applications.

1.2 Graphene as a New Two-dimensional Material

Layered materials have existed for a long time, and have been studied over the last few centuries [13, 14]. In recent decades the scientific study of graphite (3D) has led to new forms of materials, such as carbon nanotubes (1D) and fullerenes (0D) [15, 16, 17]. However, only more recently have scientists began to understand the potential of such layered materials and their potential technological applications. After attempting unsuccessfully to synthesize few-layer graphite during the 1960s, only around 10-50 layers were able to be synthesized, a breakthrough was finally achieved [16]. This most notably began with the synthesis of monolayer graphene [18].

1.2.1 Properties of Graphene

To date, graphene's properties have been the focus of much research, both theoretical and experimental. It has been one of the primary driving forces in study of 'relativistic' condensed matter physics due to its low dimensionality and its band structure that allows electrons to mimic relativistic particles confirming

the appearance of several relativistic phenomena [19, 20, 21, 22]. In its most basic sense, graphene is composed of a single layer of carbon atoms arranged in two-dimensional honeycomb lattice (see fig. 1.1(a)) It has a Young's modulus of 100 GPa (several times more than steel) with a breaking force that is 13% of its Young's modulus [23, 24]. Its strength is due, in part, to its strong in-plane carbon (C) bonds. In addition, graphene can sustain elastic deformations of 20% due to its two-dimensional nature and it has high pliability [16]. These mechanical properties are of interest because graphene lies in the extreme ranges of many metrics considering its size and dimensionality.

Aside from its mechanical properties, graphene's transport properties were another reason why the material was so appealing. Graphene's mobility is several times that of silicon's (electron mobility $\mu \sim 1400 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, hole mobility $\mu \sim 450 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ at room temperature). Experimental results have shown graphene mobility around $15,000 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ with a potential theoretical limit of $200,000 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ [25, 24, 26]. The upper theoretical limit imposed on mobility is due to scattering, however, these high mobilities are achieved mainly because electrons in graphene act very much like photons in their mobility due to their lack of mass. This enables them to travel sub-micron distances without scattering [27]. In reality, there are other limiting factors that need to be considered such as the quality of graphene and scattering with the substrate, for example.

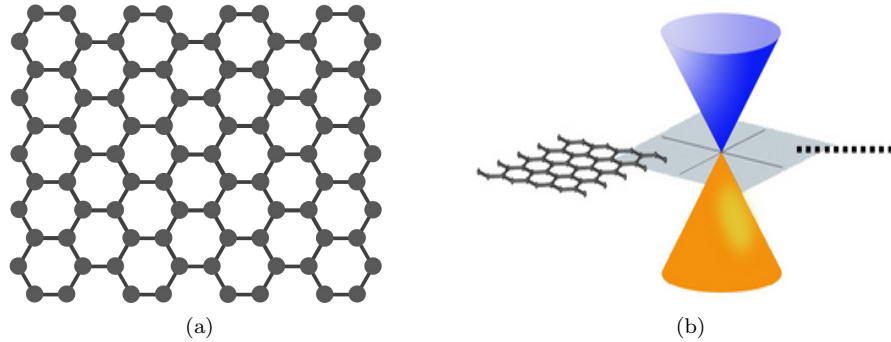


Figure 1.1: (a) Graphene: a layer of carbon atoms in a honeycomb lattice. (b) One of the most unusual features of graphene is that its conduction and valence bands meet at a point, meaning that in single-layer graphene there is no bandgap (Figures obtained from [28]).

1.2.2 Band Structure of Graphene

Despite its impressive properties, the main drawback of graphene is its lack of bandgap. As this became known, the prospect of using graphene for the fabrication to ICs became unlikely. In graphene the conduction and valence bands touch at a single point as shown in fig. 1.1(b) [29]. Ultimately, the lack of a bandgap means that the current on/off ratio is low and is unappealing for logical circuit applications [30]. However, graphene exhibits some interesting properties as a result of having no bandgap, particularly as it pertains to its optical properties. The material's band structure allows for absorption of light over a large range of the electromagnetic spectrum, ranging from infrared ($< 1.65 \text{ eV}$) to ultraviolet ($> 3.2 \text{ eV}$), offering potential electronic-photonic device applications [31, 32, 33]. Since a direct use in logical circuits is not practical researchers have moved on to look for 'two-dimensional materials beyond graphene.' Several attempts at some derivatives of graphene-like materials have been studied, but for the most part they do not seem promising for use in logical circuits [34, 35]. As of late, research has been concentrated on two-dimensional materials, namely transition metal dichalcogenides, as a candidate in ICs and other potential device applications.

1.3 Two-dimensional Materials: Transition Metal Dichalcogenides

Commonly referred to two-dimensional materials beyond graphene, transition metal dichalcogenides (TMDs) have garnered much interest in recent years. TMDs were studied previously, however, they have gained renewed interest due to their properties [36, 37, 38, 39]. TMDs consist of hexagonal layers of metal (M) atoms in between two layers of chalcogen (X) atoms (see fig. 1.2(b)), such that the stoichiometry of the material is MX_2 [30]. The material is dependent on the type of transition metal, typically one of: molybdenum (Mo), tungsten (W), niobium (Nb), rhenium (Re), nickel (Ni), or vanadium (V), and two chalcogen atoms, typically one of: sulfur (S), selenium (Se), or tellurium (Te) [39, 40]. The most commonly studied variations of TMDs are molybdenum disulfide (MoS_2), tungsten diselenide (WSe_2), and tungsten disulfide (WS_2). These materials are commonly stacked together involving van der Waals interactions between adjacent sheets and covalent bonding within each individual sheet (see fig. 1.2(a)) [30]. TMDs have been

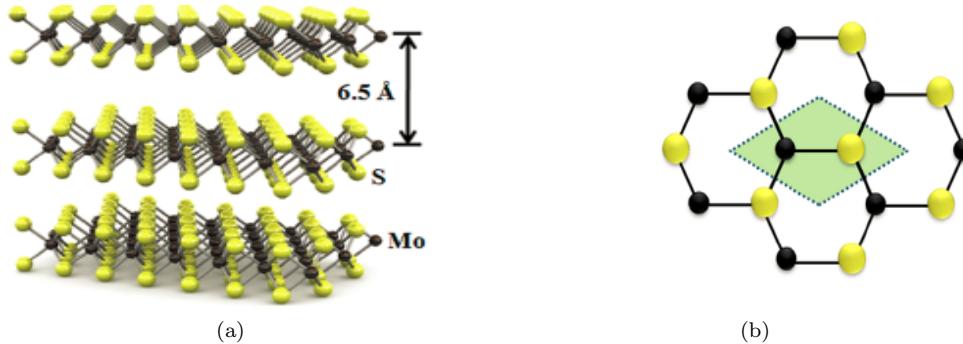


Figure 1.2: (a) The atomic structure of a layered TMD, depicting MoS_2 . Each sheet is composed of three atoms with Mo sandwiched in between two S atoms, S-Mo-S. (b) Top view of a TMD (MoS_2) lattice. (Figures obtained from [41])

found to exhibit a wide variety of interesting properties, including either being a metal or insulator, and displaying the topological insulator effect, superconductivity, and thermoelectricity [42, 43, 44, 45].

1.3.1 Band Structures of TMDs

As stated in sec. 1.2.2, one important property as it pertains to applications for logical circuits is the material's band structure. One of the main reasons TMDs have been so extensively studied lately is due to the fact that, unlike graphene, they do exhibit a bandgap. The bandgaps in some commonly used TMDs is interesting because of the transition from an indirect to a direct bandgap as the layered thickness decreases. Fig. 1.3 illustrates this, for bulk and few-layer MoS_2 there is an indirect band gap while for monolayer MoS_2 there is a direct bandgap. This unusual structure results in some unique optical properties making monolayer TMD promising candidates for optoelectronic devices [46, 47]. Table 1.1 summarizes some TMD bandgap energies that are of considerable interest to the device fabrication process.

1.4 Current Challenges in TMDs and Beyond

There are several challenges facing the advancement of study of TMDs. One of these is the development of low contact resistance devices. The formation of a Schottky barrier (SB) occurs when making electrical contacts [59, 60]. This problem affects many aspects of the growth of TMDs, low contact resistance devices are essential for the study of intrinsic transport properties and performance limits of devices. Two main approaches exist for achieving low-resistance metal-semiconductor contacts. The first of these is lowering the Schottky barrier height (SBH) by choosing metals with proper work functions. Finding metals with the proper work function to minimize the SBH while still maintaining a high conductivity has proven to be



Figure 1.3: Calculated band structures of (a) bulk MoS₂, (b) four-layer MoS₂, (c) bilayer MoS₂, and (d) monolayer MoS₂. Here the solid arrows indicate the lowest energy transitions. (Taken from [48], originally appeared in [49])

difficult [61, 62]. If a proper work function metal were to be found that met the requirements for current TMD performance the effect of lowering the SBH may still be diminished due to Fermi level pinning [63]. Therefore, another method to achieve low-resistance contacts is desirable. The second approach used to achieve low-resistance contacts is to degenerately dope the contact regions. Heavily doping the contact region effectively decreases the SB width [64]. However, this too, has its own challenges associated with it. One possible way to overcome the problems and tune the SB is to use a buffer layer and covering with a material such as hBN or graphene [65, 66, 67, 68]. This second approach has shown promise in reducing the contact resistance and lowering the SB while still maintaining high carrier mobility (see ch. 3).

Aside from the commonly used two-dimensional materials like MoS₂ and WSe₂, black phosphorus (BP) has begun to show promise. Bulk BP has a direct bandgap of $\sim 0.3\text{ eV}$, which is expected to increase to $\sim 2.0\text{ eV}$ as the thickness approaches monolayer [69, 70, 71]. In the past few years, few-layer black phosphorus has been shown to have desireable room temperature field-effect mobility ($\sim 1,000\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for ~ 10 layer BP and $\sim 200\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for 5 nm BP) [72, 73, 74]. BP has shown potential for applications to thin-film electronics and infrared optoelectronics due to its bandgap energy range [75, 74]. In addition, the high mobility measurements have recently allowed for measurements of novel quantum physics, opening the door to further study of intrinsic channel properties of TMDs.

2D material	theoretical E_g (eV)	experimental E_g (eV)
graphene	0	0
bilayer graphene	0	0
bulk <i>h</i> -BN	-	5.97 [50]
monolayer <i>h</i> -BN	-	6.07 [51]
few layer (2-5) <i>h</i> -BN	-	5.92 [52]
bulk MoS ₂	1.2 ^{a,b} [53, 54]	1.0-1.29 ^b [53, 54]
monolayer MoS ₂	~ 1.90 ^{a,c} [55]	~ 1.90 ^b [55]
bulk WS ₂	~ 1.30 ^{a,b} [53, 56]	~ 1.35 ^c [53, 56]
monolayer WS ₂	~ 2.10 ^{a,c} [57]	-
bulk WSe ₂	-	~ 1.20 ^b [58]
monolayer WSe ₂	-	~ 1.7 ^c [58]

^a Theoretical calculations based on first-principles calculations using density functional theory (DFT).

^b Indirect bandgap semiconductor.

^c Direct bandgap semiconductor.

Table 1.1: Summary of the bandgaps of typical monolayer, bilayer, and bulk TMDs and *h*-BN materials. Table adapted from ref. [30].

Chapter 2

Experimental Details

2.1 Substrate Preparation

Using degenerately doped silicon dioxide (SiO_2) wafers that are 270 nm thick as pictured in fig. 2.1 and the subsequent substrate's schematic in fig. 2.2, there are several preliminary steps needed prior to device fabrication. For easy identification of locations on the substrate alignment marks are placed on the wafer using photolithography (see setup in fig. 2.3). There is a main alignment mark pictured in figs. 2.4(a) and 2.4(b) which allows for quicker identification during electron beam lithography, for example. The alignment marks are in a grid pattern with the coordinate $(0, 0)$ at the center, stretching to $(\pm 6, \pm 6)$ in both the right and left directions. In each of these coordinate locations there smaller alignment marks evenly spaced within them as shown in figs. 2.4(c) and 2.4(d). Next, gold (Au) is deposited on the surface of the wafer, a process that will be explained in more detail in sec. 2.5.



Figure 2.1: Plain, polished uncut Si/SiO_2 wafer.



Figure 2.2: Schematic of Si/SiO_2 substrate.

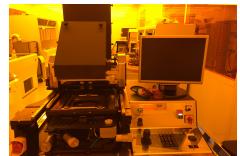


Figure 2.3: Photolithography system for creating alignment marks on substrates.

2.1.1 Substrate Cleaning

First, a SiO_2 wafer is cut to the appropriate size with its preexisting Au layer. To remove the Au layer, the substrate is first soaked in acetone for approximately 5-10 minutes then washed using isopropanol (IPA) and dried with nitrogen (N_2) gas. Next, the substrate is placed in acetone and sonicated for 15 minutes. Then sonicated once more but in IPA this time with a repetition of washing and drying step using IPA and N_2 as described above in between each sonication. In order to remove any remaining organic matter on the surface of the substrate, the substrate is annealed under vacuum at 600°C for 10 minutes and passing forming gas for 2 of the 10 minutes. Forming gas is a mixture of H_2 and an inert gas, usually N_2 [76]. In addition to annealing the substrate for cleanliness, in certain cases when a higher degree of cleanliness is desired the substrate can be treated with oxygen plasma cleaning.

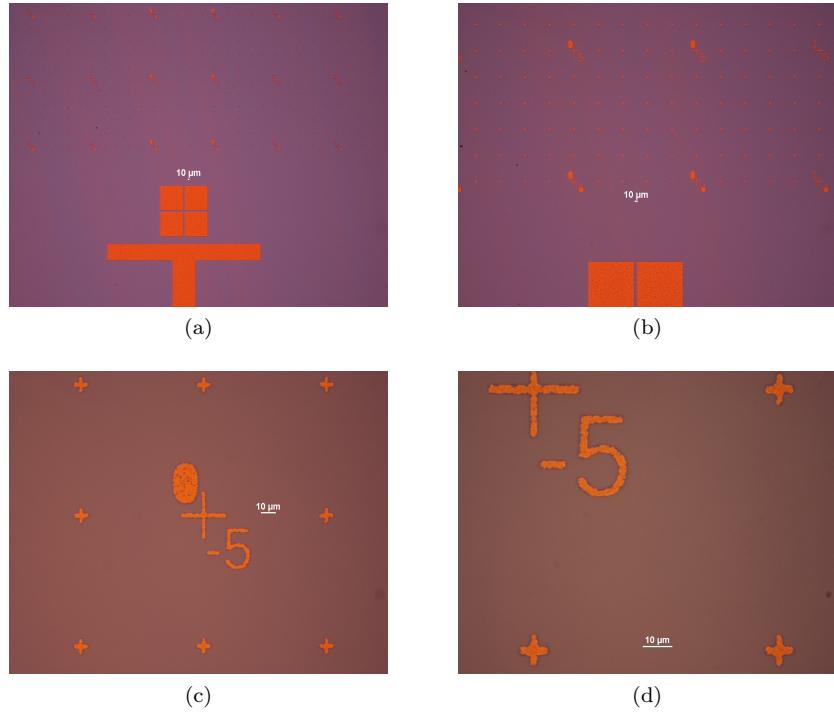


Figure 2.4: (a) Main alignment mark at 5x magnification. (b) Main alignment mark at 10x magnification. (c) Coordinate mark $(0, -5)$ at 50x magnification. (d) Coordinate mark $(0, -5)$ at 100x magnification.

2.2 Exfoliation

To synthesize samples the most common and often most effective method used is mechanical exfoliation, a technique made famous by Novoselov *et al.* [18]. The process involves using Scotch tape to repeatedly cleave layers of MoS₂ or some other TMD. Initially a crystal of a particular TMD (see fig. 2.5(a)) is placed on a piece of Scotch tape (see fig. 2.5(b)). Then taking another piece of tape and pressing in on the crystal that is on the first piece of tape, being sure to press hard and firm on the crystal. The tape is then lifted up and this process is repeated until the whole piece of tape is filled with small samples of the TMD (see fig. 2.5(c)). At the end of this process it is expected that there are a wide range of mixture of sample sizes in terms of area and in term of thickness as well, where thicknesses of < 3 nm are not uncommon. To better characterize the samples the optical microscope is used.

The main challenge that exists with this method is the ability to synthesize a high yield of monolayer samples. This does not seem to be much of a challenge when it comes to graphene and some other TMDs, but with regard to MoS₂ this is not the case. Based on recently published literature in an effort to increase the yield of monolayer MoS₂ various methods and techniques were tested and modified accordingly [77]. In this modified method an additional step to cleaning the substrate is added in which it undergoes oxygen plasma cleaning for 10 minutes to ensure the cleanliness of the substrate's surface. To promote more bonding between the substrate and the samples, the substrate is first heated at 300° C for 10 minutes without any samples on it. During this process the normal cleaving of sample on tape from crystal takes place. Once the substrate is done heating the tape containing the samples is immediately placed on the substrate and pressed firmly for several minutes. Then the substrate (with the tape still on it) is placed on a glass slide (microscope slide) and is heated at around 85° C for five minutes. Next, the substrate (with tape) is removed from heat and the tape slowly peeled back from the substrate. The result should be a much higher yield of < 3 nm samples of larger surface area, and several trilayer, bilayer, and a few

monolayer samples.

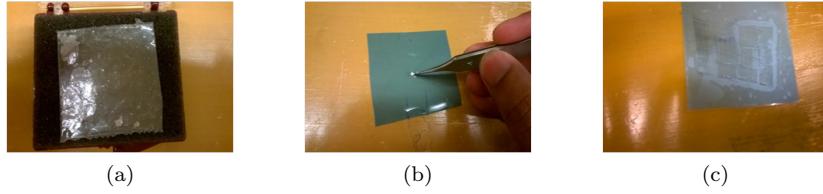


Figure 2.5: (a) Bulk MoS₂ crystal. (b) Single MoS₂ crystal on tape. (c) Tape with exfoliation MoS₂ crystals.

Most commonly SiO₂ substrates are the main items that are exfoliated onto. However, depending on the material being synthesized, this may not always be the case. In cases where samples of hBN or in the event that the thickness of the synthesized sample is not of great importance and can be tolerated up to 20 – 30 nm, polydimethylsiloxane (PDMS) is exfoliated onto instead of SiO₂ substrates. The resulting samples are of varying thickness, on average around 20 nm. Thin samples (usually trilayer and above) can be made using this method of PDMS, however, these samples tend to have small surface area and lack uniformity which poses problems as to their usability. As such, this remains an effective method for obtaining samples in which thickness is not the main concern. Once the samples have been optically characterized, the sample(s) on PDMS must be transferred to a SiO₂ substrate.

2.3 Device Synthesis

Once the sample or samples have been synthesized and characterized for their specific purpose these samples can begin to be synthesized into a device for measurement. Generally, this involves the technique of transfer. Transfer is usually done using the aforementioned PDMS or using polycarbonate (PC) known as the PC pickup method.

2.3.1 PDMS Transfer

PDMS transfer is most useful for samples that were originally exfoliated onto PDMS, for example hBN. To manufacture PDMS a 10:1 ratio of silicone base and curing agent is mixed together and placed in vacuum for 30 minutes to ensure the removal of any remaining air bubbles. After this time the mixture is then spin coated on a plain SiO₂ wafer and heated at 80 °C for 30 minutes then allowed to cool for 30 minutes. Once cooled, the surface of the wafer can be cut using a razor into small stamps that can be used for exfoliation and for transfer.

Once the samples that are to be transferred are on the PDMS stamp, it is placed on a glass slide. The optical microscope is used to locate the sample on the stamp and using a razor to cut small excess pieces from the portions of the stamp where the desired sample is not located. This process is repeated until the size of the cut stamp is now reasonably small. The cut stamp is then placed at the edge of a new glass slide with sample area of the stamp as close to the edge as can be and the other side of the stamp is taped down using Scotch tape.

Next a substrate is placed and secured using glue (usually PMMA) to the stage of the transfer setup. The transfer stage setup is pictured in fig. 2.6. It consists of a microscope that has the capability of 10x or 20x magnification and a micro-manipulator. The micro-manipulator is where the glass slide with the PDMS stamp is placed. Using the manipulator the substrate on the stage is approached and the position

of the stamp is checked and re-checked multiple times using the microscope to ensure correct overlap of the desired portion of the sample(s). Upon reaching the desired position, the glass slide is lowered, but this time there should be a contrast seen which is the overlapping of the glass slide and the substrate. Once the contrast has enveloped the entire sample that was to be transferred then the manipulator can be used to lift up the glass slide. Once the transfer is complete then the substrate should be annealed at 250°C for 30 minutes in order to remove any residue or organic matter that may have remained during the transfer process.



Figure 2.6: Transfer stage setup

2.3.2 Polycarbonate Pickup Method

The PC pickup method is used for samples that have been exfoliated onto a SiO₂ substrate. Generally these are thinner samples with larger surface area that are not as easily obtained by using the PDMS exfoliation method as described in sec. 2.2. To manufacture the PC 3.0 g of chloroform and 0.18 g of polycarbonate resin are put on a plate shaker for about 60 minutes or until the polycarbonate resin have dissolved into the solution.

Next, the substrate that has the sample that is going to be transferred is taped using double-sided tape to a glass slide facing up. Then using a syringe the PC solution is placed in the substrate and evenly spread across it, being sure to locate the area(s) on the substrate where the sample(s) are located, small pre-cut pieces of PDMS are placed over top of these areas. An outline of the PDMS stamps is cut using a razor and any excess PDMS is carefully torn away. Once only the PDMS strips are remaining on the substrate deionized water (DI) is put under the strips in order to create a hydrophobic surface and to ensure that the strip and PC that is trapped underneath it come off the substrate with relative ease. Each strip is placed on its own glass slide and is gently blown with N₂ gas to remove any excess DI from the surface.

Moving to the transfer stage setup and following the steps described in sec. 2.3.1 with regard to using the transfer stage setup. The only difference at this point to using this method as opposed to PDMS transfer is in the final step of the transfer. Instead of only lowering until the contrast change is shown between the region that is desired to be transferred, with PC transfer the entire PC must be lowered down. This is because the PC will be heated before being lifted up. Lowering all the way ensures that all the PC will be melted. Once lowered all the way, the heating device, which is connected to the stage, should be turned up to 130°C. Once this temperature is reached, it should be maintained for approximately two minutes to fully melt the PC film. After heating the substrate and lifting up using micro-manipulator the substrate is placed in chloroform and covered for 30-60 minutes. The purpose of this is to remove any

residue left over by the PC film or any other items that may have been introduced at any point in the transfer process. In practice the chloroform soaking generally needs to be repeated several times over a few hours in order to ensure the least amount of remaining residue possible. To confirm the reduction of residue and also characterize the transferred samples an AFM is used.

2.4 Characterization

There are many ways used in modern academia and industry to characterize samples and devices. Some of these methods include scanning tunneling microscopy (STM), transmission electron microscopy (TEM), atomic force microscopy (AFM), and magnetic force microscopy (MFM) [78]. The primary characterization techniques used in this project are AFM and optical characterization.

2.4.1 Optical Characterization

The majority of the optical characterization is carried out using the optical microscope as shown in figs. 2.7(a) and 2.7(b). The microscope can magnify 5x, 10x, 20x, 50x, and 100x, in addition, it can show dark field images.

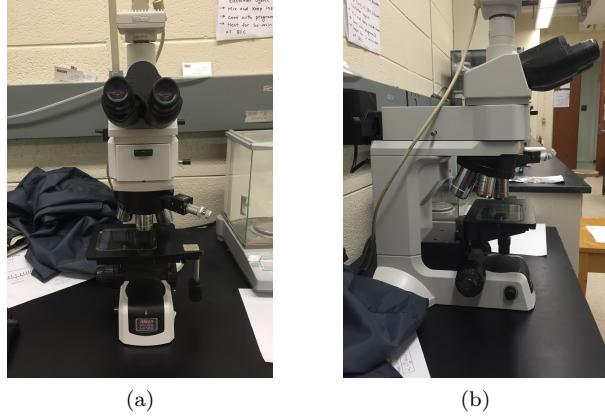


Figure 2.7: (a) Optical microscope front view. (b) Optical microscope side view.

2.4.2 AFM Characterization

In addition to the characterizing samples optically, AFM characterization is another important aspect of the device design and fabrication process. AFM characterization occurs several times throughout the process, after each transfer of a sample onto another, for example. This occurs for two reasons; to verify the thickness of the sample(s) that have been transferred, and also to verify the cleanliness of the surface of the sample (to ensure that any residue has been removed, especially during the course of PC transfer). Additionally, once the electrodes of the device have been fabricated a final AFM characterization is needed to determine the width of the device's channel which is needed to calculate various important electrical properties.

Fig. 2.8(a) shows a front view of the AFM used to characterize. For these purposes, the AFM is operating in “tapping” mode which is less invasive than “contact” mode [78]. In basic terms, an AFM works by measuring the force between the tip of a cantilever (see fig. 2.8(b)) and the sample being imaged.

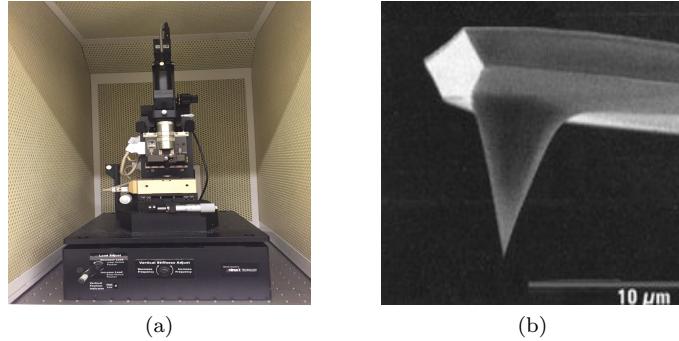


Figure 2.8: (a) Front view of AFM setup. (b) AFM cantilever tip [79].

2.5 Device Fabrication

In order to perform electrical measurements of devices one must fabricate devices with electrodes. The devices are fabricated according to a specific process, though it is worth noting that under certain circumstances some steps of the process may be omitted or altered, however, the main idea remains the same regardless of the device type being fabricated. Once all transfer steps and samples have been placed in their correct locations the fabrication process begins. This process has three main steps: device design (sec. 2.5.1), electron beam lithography (EBL) (sec. 2.5.2), and metal deposition (sec. 2.5.3).

2.5.1 Device Design

The specifics of device electrode design depends largely on the type of measurement that is desired. For example, fig. 2.10(b) demonstrates a Hall bar device pattern. Despite the varying possibilities of patterns, the method for which the designs are generated remains largely the same. In order to generate these patterns a design software, Nanometer Pattern Generation System (NPGS), is used to draw the electrodes which in turn communicates the designed pattern to the SEM [80].

In preparation for EBL the substrate is spin-coated with two layers of polymethyl methacrylate (PMMA). The first layer of PMMA is 495-A4 is added then the substrate is baked on a hot plate for 5 minutes at 180° C. The first layer is followed by another layer of PMMA, 950-A2 (same polymer of different molecular weight). Again, the substrate is spin-coated with this PMMA layer and baked at the same temperature for 5 minutes.

2.5.2 Electron Beam Lithography

To generate the patterns described in sec. 2.5.1 a SEM is used to complete EBL. Fig. 2.9 shows the control panel and electron beam writer of the SEM. The SEM is optimized by adjusting the beam current to the saturation point. Using the alignment marks mentioned in sec. 2.1 the electron beam is aligned to the correct position on the substrate. The NPGS system allows for adjustments in the concentration of the electron beam current at certain areas, for example, whether a line dose or an area dose is necessary. In general, these values are adjusted as needed depending on the device design but are usually around $300 \mu\text{C cm}^{-2}$ for area doses and $15 \mu\text{C cm}^{-1}$ for line doses. Ultimately, the EBL process creates three separate patterns that are joined together. The first pattern is written at 1000x magnification on the SEM (see fig. 2.10(b)). The second and third patterns (written at 300x and 100x, respectively, see fig. 2.10(a)) are connected to the inner 1000x pattern and they connect this inner pattern to the “electrode pads” where the electrodes will eventually be connected for device measurement. After completing the device pattern, the substrate is developed in a solution of methyl isobutyl ketone (MIBK) and methyl ethyl

ketone (MEK) for 70 seconds. The MIBK is the main developer while the MEK acts to enhance the developing process, both fig. 2.10(a) and fig. 2.10(b) have undergone this development process.



Figure 2.9: Control panel and electron beam writer of scanning electron microscope.

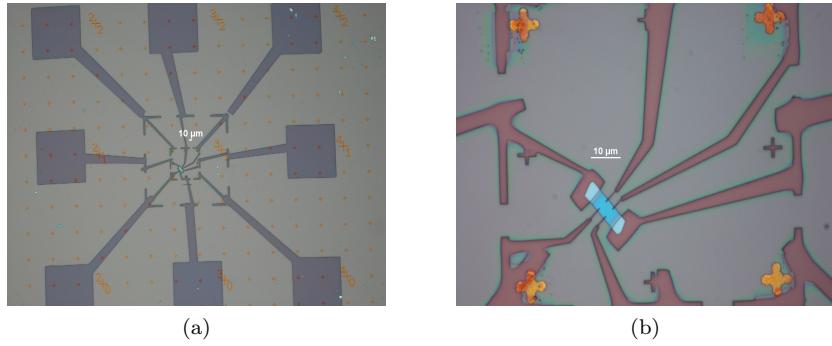


Figure 2.10: (a) Developed pattern at 10x magnification, (b) developed pattern at 100x magnification. Both developed using MIBK and MEK.

2.5.3 Metal Deposition

In order to make proper electrical contacts metal must be deposited on the pattern made by EBL. This process of metal deposition is done using a Bell Jar deposition (BJD) system which evaporates 10 nm of titanium (Ti) followed by 40 nm of Au on the substrate's surface at ultrahigh vacuum ($\sim 10^{-7}$ torr) at a rate of 1 \AA s^{-1} . After the metal deposition process is complete, a process called "lift-off" is performed. In this process the substrate is placed in acetone for approximately 5-10 minutes, until the Au has "lifted-off." Once this process is complete all that remains on the substrate is Au where the EBL was performed. Figs. 2.11(a) and 2.11(b) illustrates a substrate that has undergone the lift-off process, all that remains is the portion of the pattern that is necessary to perform electrical measurements on the device.

2.6 Electrical Measurements and Characterization

Upon completion of the fabrication process and physical characterization processes, the remaining process is electrical characterization. Many of the options available in electrical characterization are put to use, at least in some capacity regardless of the device. Then, depending on the device's quality, further measurements can be made in which a more comprehensive electrical data profile can be obtained.



Figure 2.11: (a) Au/Ti deposited on developed sample after electron beam lithography at 10x. (b) Au/Ti deposited on developed sample after electron beam lithography at 100x.

2.6.1 Measurement Devices

Pictured in fig. 2.12(a) is a measurement device that allows for automated electrical data collection through pre-made programs. The user adjusts parameters and the desired device properties to be measured. Initially, the device is usually measured in non-vacuum conditions at room temperature in order to determine the device's quality. If it is determined that the device's quality is worth continuing with low temperature measurements then the substrate is placed in the vacuum measurement chamber pictured in fig. 2.12(b). This apparatus is used in conjunction with the measurement setup in fig. 2.12(a) to continue measurements. However, in this configuration the measurements take place under ultrahigh vacuum ($\sim 10^{-6}$ to 10^{-7} torr) and temperature control via liquid nitrogen (with the ability to cool to 70 K). In addition, there is another measurement device that allows for both temperature control and the application of a magnetic field. This device, known as a physical property measurement system (PPMS), is shown in fig. 2.12(c) and is used in situations when it is necessary to apply a magnetic field such as measuring a Hall device.

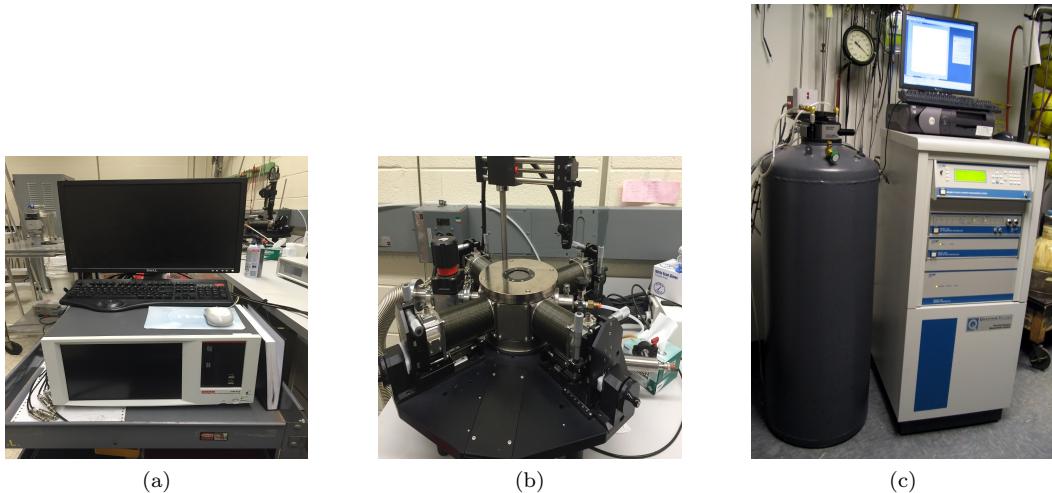


Figure 2.12: (a) Keithley semiconductor measurement system. (b) Low temperature, vacuum measurement chamber. (c) Physical property measurement system.

Chapter 3

Intrinsic Properties and Scattering Mechanisms

Intro...

3.1 Approach to Low-Resistance Contacts

Developing low-resistance contacts is important two enable the study of intrinsic transport properties of devices, but also it is vital to applications of TMDs. Large contact resistance at room temperature is not ideal for applications. At the metal/semiconductor contact interface a barrier develops, the SB [81]. The device in question must be able to supply the necessary current, and the voltage drop across the contacts should be small compared to the voltage drop across the device's active channel region. In most cases, the contacts should be ohmic, the current-voltage characteristic should be linear and not degrade the device's performance to any significant extent [82]. In the ideal, theoretical case (Schottky-Mott model) the SBH is given by

$$\Phi_{Bp} = \frac{E_g}{e} - (\Phi_m - \chi_s), \quad (3.1)$$

where Φ_{Bp} is the hole barrier height, e is the charge of an electron, E_g is the semiconductor bandgap energy, Φ_m is the metal workfunction, χ_s is the semiconductor electron affinity, note that these properties are intrinsic to the material before forming the junction [83]. In reality the description is not this simple and is largely dependent on other factors, such as imperfections, Fermi level pinning, and Fermi level mismatch [84]. For a metal/*p*-type semiconductor interface the magnitude of the SBH is reflective of the mismatch in Fermi level of the metal and the valence band maximum (VBM) of the semiconductor. Conversely, for the case of a metal/*n*-type interface it is the mismatch in the Fermi level of the metal and the conduction band minimum (CBM) of the semiconductor [85]. Therefore, to address the issue of contact resistance one must find ways to effectively “tune” the SB.

There have been several approaches employed in order to reduce the contact resistance. One method is to attempt to tune the SBH by using different common metals to find a desirable work function. Eq. 3.1 implies that the SBH is linearly dependent on the work function Φ_m of the metal. However, in reality, this is usually not the case because, one, finding metals with the proper work function that minimizes the SBH while still maintaining high conductivity has proven to be difficult, and, two, the lowering that would potentially be achieved by the use of the proper work function would most likely be diminished due to Fermi level pinning [61, 62, 86]. Fermi level pinning occurs when there are surface states that develop in the bandgap and pin the Fermi level position of the semiconductor [85]. Another method is the use of graphene contacts [87, 88, 89]. Barrier-free contacts have been achieved using this method in combination

with MoS₂ using a gate potential to tune band alignment [90]. However, this method has not been shown to be extendable down to low enough contact resistances in some other TMDs, most notably WSe₂, but has been shown to be tunable down to ($< 2 \text{ k}\Omega \mu\text{m}$) [91, 87]. The method to that is enacted here to reduce the contact resistance is using degenerately doped contact regions. By degenerately doping the contact region one can thin the SB width. However, this method is not without its challenges as well. Several doping techniques that can be used have limited spatial resolution [68]. Despite the challenges posed, this method has produced promising results that are transferrable to TMDs including WSe₂, MoS₂, and MoSe₂ resulting in high-performance, low contact resistance devices.

To determine the contact resistance of fabricated devices a method known as transmission line model (TLM) is used. In general, resistance is given by

$$R = \frac{\rho}{A} l, \quad (3.2)$$

where, in this case, it is assumed that the resistivity ρ and the area A of the electrodes are constant throughout the device [92]. The resistance R is then proportional to the length of the channel l . By determining the resistance as a function of length one can deduce the contact resistance. The total contact resistance is given by

$$R = R_{\text{ch}} + 2R_c, \quad (3.3)$$

where R_c and R_{ch} are the contact and channel resistances, respectively [92]. A typical device for a TLM measurement has drain and source electrodes with varying lengths between them. By finding the resistance from the gradient of an *IV* characteristic curve, one can apply the logic from eqs. 3.2 and 3.3 to find the contact resistance. The contact resistance is ultimately extracted from the *y*-intercept of a linear fit of resistance as a function of length for the device. In general, this method is done at several temperatures to further characterize the quality of the contacts as one would expect that at low temperatures, for low-resistance contacts, they would behave in similar fashion as they did at higher temperatures. To determine the effect that varying doping schemes has on contact resistance devices that were lightly doped (Nb_{0.0005}W_{0.9995}Se₂) were measured using TLM and compared to degenerately doped devices (Nb_{0.005}W_{0.995}Se₂).

3.1.1 Transmission Line Method: Nb_{0.0005}W_{0.9995}Se₂

As stated in sec. 3.1, the TLM measurement involves designing a device that has varying drain source channel lengths in order to determine the resistance as a function of length. Fig. 3.1(a) shows an optical micrograph consisting of a lightly doped WSe₂ (Nb_{0.0005}W_{0.9995}Se₂) channel. Figs. 3.1(b)-3.1(d) show the total resistance as a function of length for both $V_{bg} = 0 \text{ V}$ and $V_{bg} = -60 \text{ V}$ at room temperature. The contact resistances are then determined from the linear fit and the *y*-intercept. These figures show ohmic contacts with a minimum contact resistance of $R_c = 2.35 \text{ k}\Omega \mu\text{m}$ achieved with application of $V_{bg} = -60 \text{ V}$. In addition, the contact resistances are lower for the higher values of V_{bg} . This is due, in part, to the fact that the higher V_{bg} works to reduce the width of the SB and allow for more transmission across the barrier that has developed between the metal/semiconductor interface. Moreover, when there is no V_{bg} applied, the reported contact resistances are an order of magnitude higher. The fact that the channel material in use here is only lightly doped means that there is a larger mismatch between the Fermi level of the metal and the VBM causing a larger SBH than one would expect with a channel that was more heavily doped.

3.1.2 Transmission Line Method: Nb_{0.005}W_{0.995}Se₂

The lightly doped WSe₂ device showed reasonably low contact resistances at room temperature, but lower-resistance contacts are desired. Using TLM degenerately doped WSe₂ (Nb_{0.005}W_{0.995}Se₂) devices were measured. Fig. 3.2(a) shows an optical micrograph of the device design which is identical to that in sec. 3.1.1. The contact resistances as a function of length are shown in figs. 3.2(b) and 3.2(c) at room

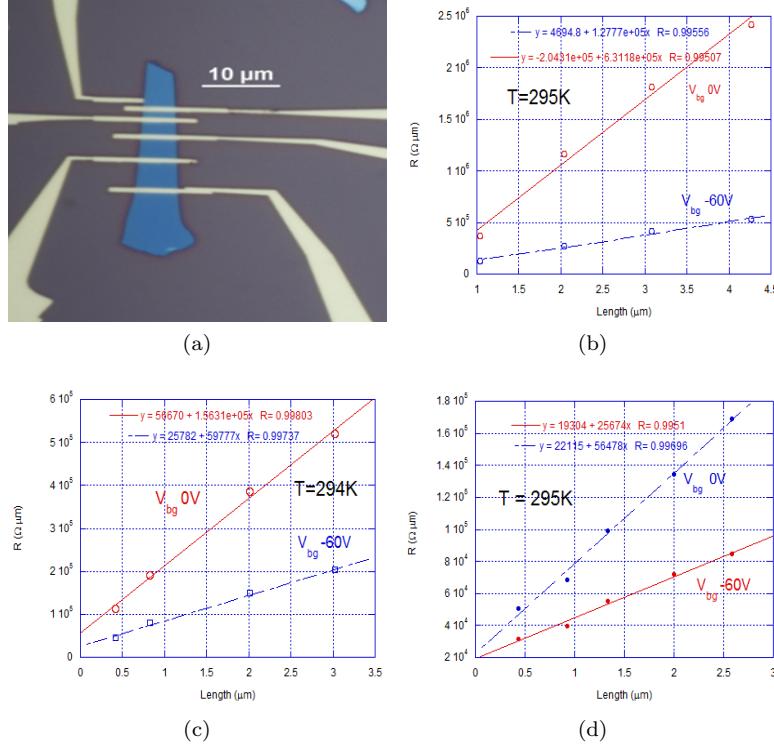


Figure 3.1: (a) Optical micrograph of a device structure for TLM measurement consisting of lightly *p*-doped WSe₂ (Nb_{0.0005}W_{0.9995}Se₂) with Ti/Au metal contacts. (b)-(d) Normalized total resistance as a function of channel length measured at room temperature.

temperature and 5 K, respectively. At both temperatures they exhibit linear ohmic behavior. Even more promising is that the values for contact resistance are essentially the same at high and low temperature, which indicates significant reduction of the SB. The low temperature performance means that the contacts are of high quality as the contacts tend to degrade as temperature decreases mainly due to the lack of thermionic emmission of carriers [85].

3.1.3 Discussion of Results for Light and Degenerately Doped Contacts

The results for lightly (Nb_{0.0005}W_{0.9995}Se₂) and degenerately (Nb_{0.005}W_{0.995}Se₂) doped WSe₂ contacts are summarized in table 3.1. The degenerately doped contacts have resistances of at least an order of magnitude lower at room temperature due to the lowered SBH from the higher doping scheme. The lightly doped contacts, though still relatively high, demonstrate the effect that applying a higher V_{bg} can have on the SB. An effective thinning of the barrier is observed for higher backgate voltage and thus this can also be used to further tune the SB and lower contact resistances. The results from the lightly doped WSe₂ channel are on the same order of magnitude as what has been previously shown using graphene/WSe₂ contacts ($\sim 2 \text{ k}\Omega \mu\text{m}$) [87]. The results shown obtained for the degenerately doped WSe₂ are significantly lower than graphene/WSe₂ method and are in line with the best results that have been achieved for TMDs ($\sim 0.2 - 0.7 \text{ k}\Omega \mu\text{m}$) [93, 67, 94]. With these results in mind, this 2D/2D contact method using degenerately doped WSe₂ (Nb_{0.005}W_{0.995}Se₂) looks to be a viable and effective way to engineer low-resistance contacts which will be essential to explore the intrinsic channel properties of TMDs, the performance limits, and also when it comes to applications.

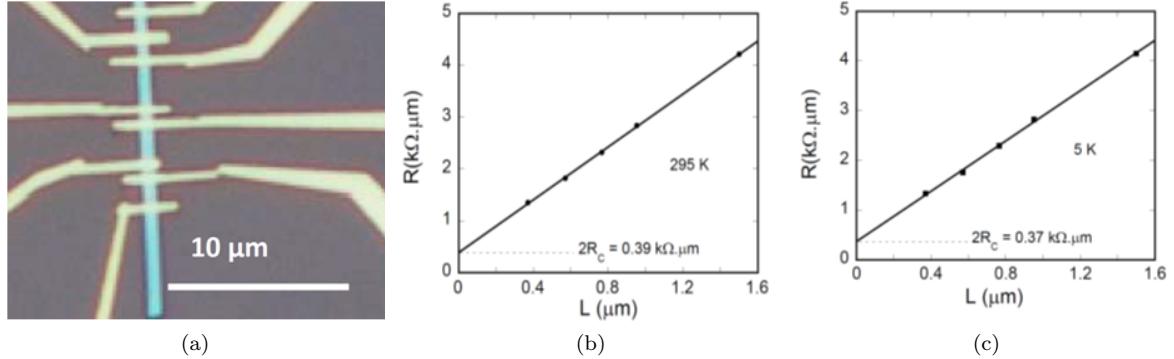


Figure 3.2: (a) Optical micrograph of a device structure for TLM measurement consisting of degenerately *p*-doped WSe₂ (Nb_{0.005}W_{0.995}Se₂) with Ti/Au metal contacts. (b) Normalized total resistance as a function of channel length measured at room temperature $T = 295\text{ K}$ and (c) low temperature $T = 5\text{ K}$. Figures appeared in ref. [91].

Doping Content	Temperature (K)	$R_c(\text{k}\Omega \cdot \mu\text{m})^*$
(0.05%) Nb _{0.0005} W _{0.9995} Se ₂	295	2.35 [†]
(0.05%) Nb _{0.0005} W _{0.9995} Se ₂	294	12.9 [†]
(0.05%) Nb _{0.0005} W _{0.9995} Se ₂	295	9.65 [†]
(0.5%) Nb _{0.005} W _{0.995} Se ₂	295	0.195 [‡]
(0.5%) Nb _{0.005} W _{0.995} Se ₂	5	0.185 [‡]

* The contact resistances R_c are reported as per electrode by taking the intercept and dividing by 2. In some other references this may not be the case.

[†] Resistance values from figs. 3.1(b), 3.1(c), and 3.1(d).

[‡] Resistance values from figs. 3.2(b) and 3.2(c).

Table 3.1: Summary of contact resistances for lightly *p*-doped WSe₂ (Nb_{0.0005}W_{0.9995}Se₂) and degenerately *p*-doped WSe₂ (Nb_{0.005}W_{0.995}Se₂) found using linear fit data from figs. 3.1(b)-3.1(d) and 3.2(b)-3.2(c).

3.2 Field-Effect Mobility and Scattering Mechanisms

There are several properties to electrically characterize and quantify the performance of a device. One such property is the two-probe and four-probe field-effect mobility μ_{FE} . The two-probe field-effect mobility is given by

$$\mu_{\text{FE}} = \frac{L}{w} \frac{1}{C} \frac{1}{V_{ds}} \frac{dI_{ds}}{V_{bg}}, \quad (3.4)$$

where L is the length of the channel (the distance between the source and drain), w is the width of the channel, I_{ds} is the drain current, V_{bg} is the backgate voltage, V_{ds} is the drain voltage, and C is the geometric capacitance [95]. To measure the field-effect mobility there are two main approaches used, either the two-probe method or the four-probe method. The two-probe method is shown in fig. 3.3(a). In this configuration measurement takes place between the drain and source only. The main drawback of this measurement is that it is subject to resistance that can make data difficult to interpret because of this [92]. Alternatively, there is the four-point probe configuration which is shown in fig. 3.3(b) [96]. The main advantage of this configuration is that the voltage drop is measured across V_3 and V_2 and therefore allows

the resistance to be subtracted. The field-effect mobility is important to characterizing a device because, it can reveal information about scattering mechanisms present and how they affect the mobility. Also, depending on the device's channel and whether it is doped or not, the mobility shows how the doping can be tuned to perform in a desired manner for device applications, especially at room temperature. To begin to study these issues devices with varying doping schemes and fabrication methods were measured to address where improvements can be made and where unknowns still exist.

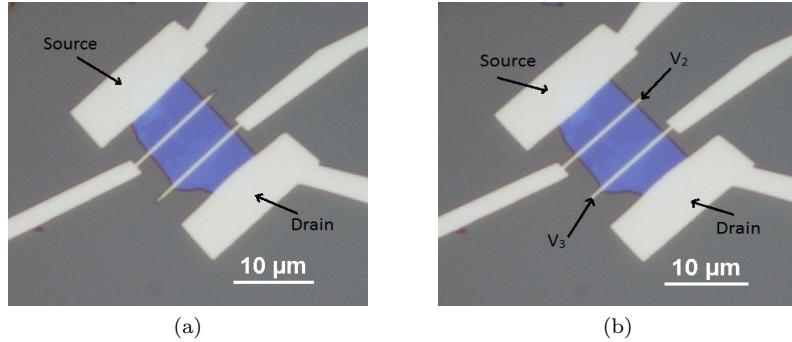


Figure 3.3: Examples of (a) two-point probe measurement configuration for field-effect mobility measurements and (b) four-point probe configuration.

3.2.1 Applying Low-Resistance Contacts: Doped Channel

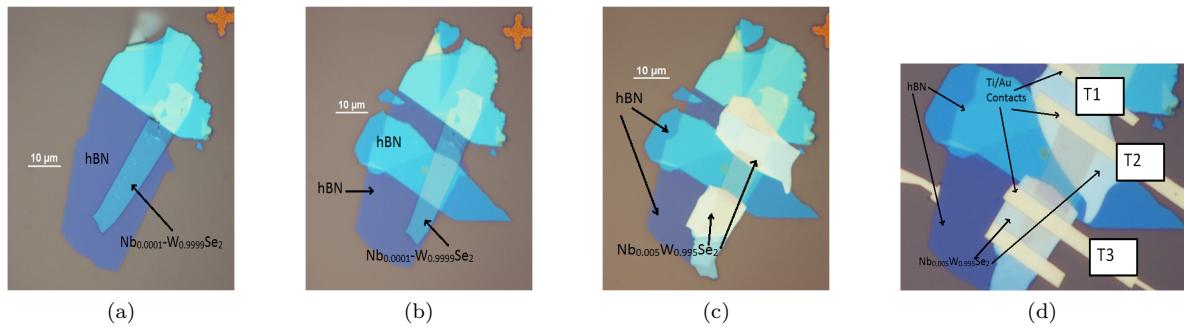


Figure 3.4: (a) $\text{Nb}_{0.0001}\text{W}_{0.9999}\text{Se}_2$ transferred to hBN substrate, (b) top hBN transferred onto channel, (c) degenerately doped ($\text{Nb}_{0.005}\text{W}_{0.995}\text{Se}_2$) contacts transferred onto device, and (d) device after fabrication steps with Ti/Au metal electrodes consisting of a 5.6 nm thick channel.

3.2.2 Applying Low-Resistance Contacts: Undoped Channel

3.3 Hall Effect and Applying Low-Resistance Contacts

3.3.1 Hall Effect: $\text{Nb}_{0.0005}\text{W}_{0.9995}\text{Se}_2$

3.3.2 Hall Effect: Extended to Contact Method

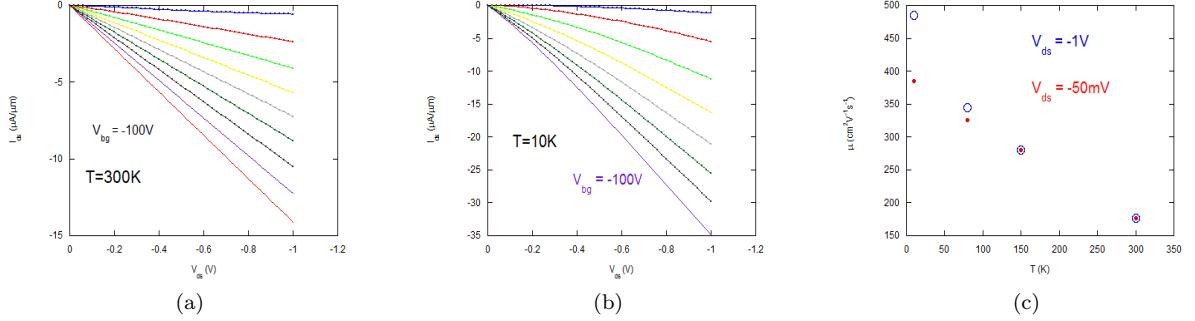


Figure 3.5: (a) IV chacteristics of device at $T = 300\text{ K}$ and (b) at $T = 10\text{ K}$. (c) Two-terminal field-effect mobility as a function of temperature for $V_{ds} = -50\text{ mV}$ and -1 V . Note: figures correspond to device shown in fig. 3.4(d). Measurements shown were made before the device was annealed.

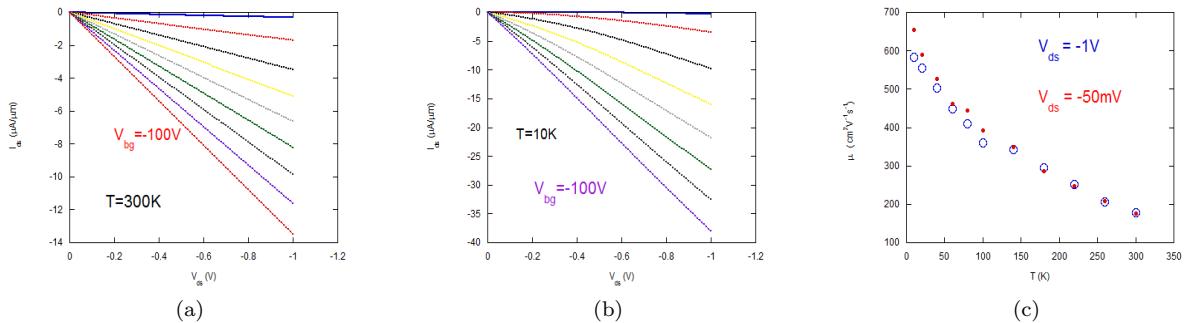


Figure 3.6: (a) IV chacteristics of device at $T = 300\text{ K}$ and (b) at $T = 10\text{ K}$. (c) Two-terminal field-effect mobility as a function of temperature for $V_{ds} = -50\text{ mV}$ and -1 V . Note: figures correspond to device shown in fig. 3.4(d). Measurements shown wereee made after the device was annealed for 30 minutes at 250° C .

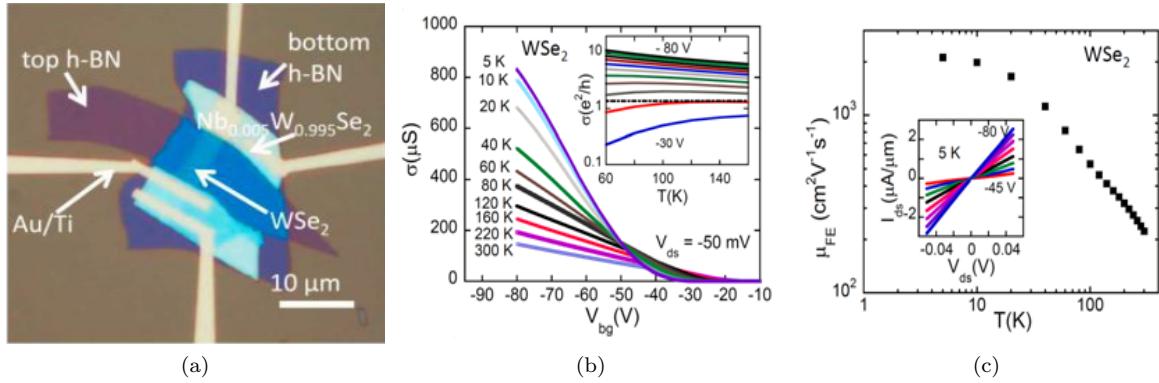


Figure 3.7: (a) Optical micrograph of WSe₂ FET with degenerately *p*-doped WSe₂ ($\text{Nb}_{0.005}\text{W}_{0.995}\text{Se}_2$) contacts with channel region on hBN substrate and covered with a top hBN piece. (b) Temperature dependent two-terminal conductivity as a function of V_{bg} at $V_{ds} = -50 \text{ mV}$ for device shown in (a). (c) Two-terminal field-effect mobility. Figures appeared in ref. [91].

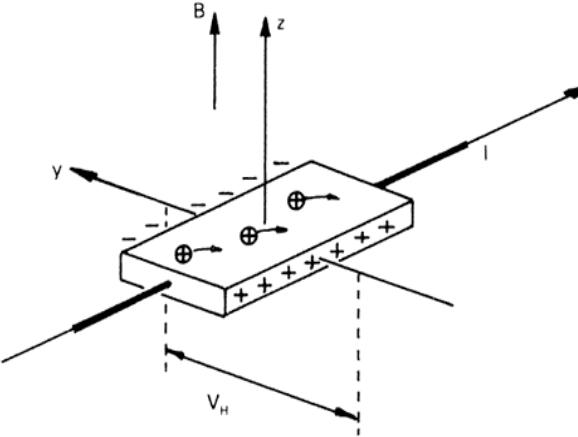


Figure 3.8: Geometry of Hall effect measurement. Current flows in the positive *x*-direction and magnetic field is applied in the positive *z* direction generating a Hall voltage [97]. Diagram originally appeared in ref. [98].

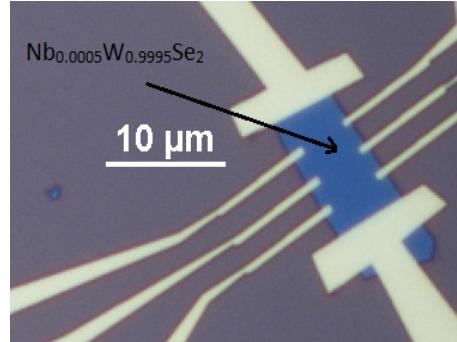


Figure 3.9: Optical micrograph of device structure consisting of lightly *p*-doped WSe₂ ($\text{Nb}_{0.0005}\text{W}_{0.9995}\text{Se}_2$) with device thickness 7.7 nm and Ti/Au metal contacts.

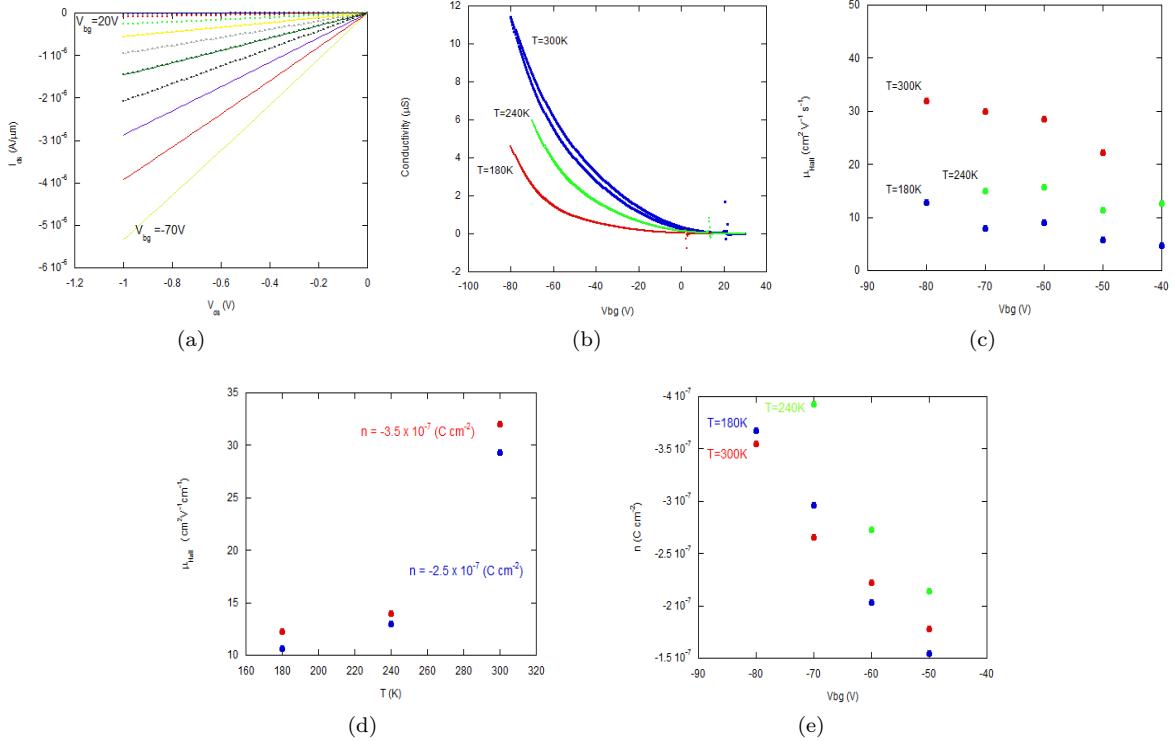


Figure 3.10: (a) IV characteristic curve at $T = 300\text{ K}$ as a function of V_{ds} for V_{bg} ranging from -70 V to 20 V . (b) Temperature-dependence of conductivity and (c) Hall mobility as a function of V_{bg} . (d) Charge carrier density dependence of Hall mobility as a function of temperature and (e) temperature dependence of charge carrier density as a function of V_{bg} . Note: the data here corresponds to device shown in fig. 3.9.

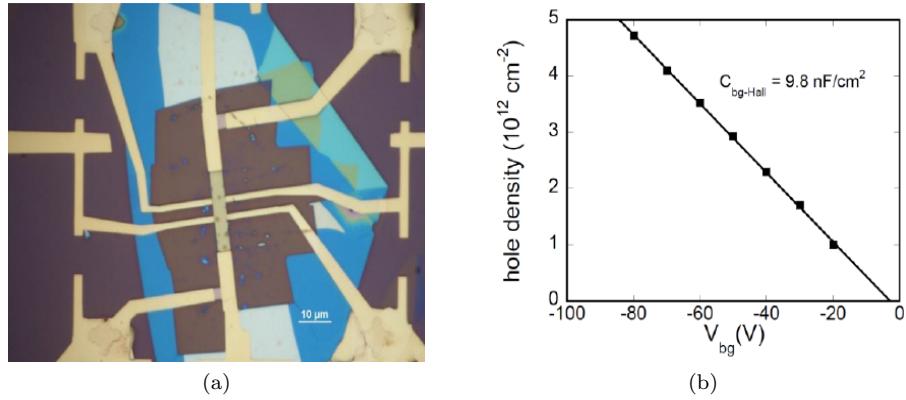


Figure 3.11: (a) Optical micrograph of WSe₂ Hall bar device encapsulated in hBN with degenerate 2D/2D contacts. (b) Hole density as a function of V_{bg} at $T = 300\text{ K}$ extracted from Hall effect measurement. Figures appeared in ref. [91].

Chapter 4

Future Works and Conclusion

Certain measurable quantities are valued because of the information they reveal about the geometry of the Fermi surface. Additionally, these quantities are attractive because they depend only on universal constants, experimentally controlled variables, and information about the electronic band structure which is entirely determined by the shape of the Fermi surface [99]. These measurable quantities commonly arise in the presence of a strong magnetic field and low temperature system. Determining the Fermi surface geometry provides insight into the transport and scattering properties of the material.

4.1 Integer Quantum Hall Effects

In a two-dimensional electron system (2DES) there are a number of interesting phenomena that occurs at low temperatures in the presence of strong magnetic fields. One such effect is the integer quantum Hall effect (IQHE). The IQHE was discovered in 1980 by Klitzing *et al.* [100]. They showed that under a quantum regime of temperature and magnetic field there is a quantization of the Hall resistance, which deviates from its linearity in the magnetic field seen in the classical Hall effect, displaying plateaus at particular values of the magnetic field where the Hall resistance is given purely in terms of universal constants. In addition, the plateaus observed in the Hall resistance are accompanied by a vanishing longitudinal resistance [100, 101, 102, 103].

In order to fully mathematically describe the theory behind the IQHE one must first introduce the concept of Landau levels. Here we assume a quantum regime in which there is a low temperature and high magnetic field such that $\hbar\omega \gg k_B T$. The Hamiltonian of a particle in a uniform magnetic field is given by

$$\hat{H} = \frac{1}{2m} (\hat{p}_x + eBy/c)^2 + \frac{\hat{p}_y^2}{2m} + \frac{\hat{p}_z^2}{2m} - (\mu/s) \hat{s}_z B, \quad (4.1)$$

where \hat{p}_i is the momentum operator in the specified coordinate direction, B is the magnetic field, e is the charge of an electron, $(\mu/s) \hat{s}_z$ is the intrinsic magnetic moment operator [104]. It is worth noting that the vector potential chosen in eq. 4.1 is known as the Landau gauge, $\vec{A} = (-By, 0, 0)$, which implies the magnetic field B is directed in the positive z -direction [105, 106]. In this case the eigenfunctions of the Hamiltonian must take the form,

$$\psi(\vec{r}) = e^{(i/\hbar)(p_x x + p_z z)} \chi(y), \quad (4.2)$$

where $\chi(y)$ is defined by solutions to

$$\frac{\partial^2 \chi}{\partial y^2} + \frac{2m}{\hbar^2} \left[E + (\mu/s) \sigma B - \frac{p_z^2}{2m} - \frac{1}{2} m \left(\frac{eB}{mc} \right)^2 (y - y_0)^2 \right] \chi = 0, \quad (4.3)$$

where $y_0 = -cp_x/eB$ and $\omega = |e|B/mc$. Additionally, since the Hamiltonian does not explicitly depend on x and z this implies that both the x and z components of the generalized momentum are conserved. Eq. 4.3 is formally identical to that of the linear oscillator, thus the expression for the energy levels of a particle in a uniform magnetic field is

$$E = \left(n + \frac{1}{2} \right) \frac{|e|\hbar B}{mc} + \frac{p_z^2}{2m} - (\mu/s) \sigma B, \quad (4.4)$$

where n is any integer [104]. These quantum numbers n specify states known as Landau levels. For the case in which the motion of particles is restricted to a rectangular geometry of $L_x \times L_y$, also let $p_z = 0$ as the motion of particles is restricted in this case to only the $x - y$ plane. In this case the energy of each Landau level is given by

$$E = \left(n + \frac{1}{2} \right) \frac{|e|\hbar B}{mc} - (\mu/s) \sigma B. \quad (4.5)$$

Due to the restriction that $\hbar\omega \gg k_B T$, thermal excitations can be neglected because the interval between Landau levels is much greater than thermal excitation energy. As a result, the probability that electrons will be thermally excited to higher energy levels can be neglected. In order to fill higher energy levels the density of states must be increased. When the Landau level is fully occupied from the lowest to the i th energy level the transverse resistivity becomes

$$\rho_{xy} = \frac{h}{ie^2}, \quad (4.6)$$

where i is any integer corresponding to a specific filled Landau level, e is the charge of an electron, and h is Planck's constant [100, 102]. Eq. 4.6 shows that at critical values of the field, the Hall resistivity (or conductivity) is quantized in units of h/e^2 [78, 103]. Fig. 4.1 demonstrates an example of the quantized

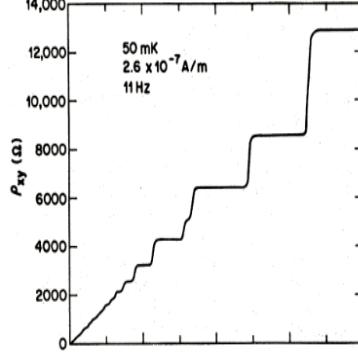


Figure 4.1: ρ_{xy} as a function of magnetic field B at low temperature ($T = 50\text{ mK}$). Figure originally appeared in ref. [107].

nature of the transverse resistivity. The distance between each plateau (step height) is given by h/e^2 divided by an integer i . These steplike increases with plateaus in the magnetic field region where the longitudinal resistivity ρ_{xx} vanished [108]. Thus, when $\rho_{xx} = 0$ then $\rho_{xy} = h/ie^2$ and is at a plateau. Note that the temperatures needed to observe the IQHE ($\lesssim 4\text{ K}$) is a likely reason why it was not discovered until 1980. It is also important to note that the value of resistivity only depends on fundamental constants of physics and can be used as a primary resistance standard known as the von Klitzing constant, $R_{K-90} = 25812.807\Omega$ [100, 109, 110]. Observation of the IQHE confirms the high-quality nature of the device in question as it is necessary to obtain high mobilities at very low temperatures. Furthermore, this would offer a more complete picture of the quantum structure of under the high-field limit and allow for the measurement of further quantum properties that reveal important information about the underlying structure of the device.

4.2 Shubnikov-de Haas Oscillations

There are several techniques and measurements that can determine the geometry of the Fermi surface, many of these are closely related to one another and are based on the same underlying mechanism. One such effect is the SdH effect [111]. The SdH effect is an oscillatory dependence of the resistivity on the magnetic field, there it is related to the quantum hall effect (QHE) [112]. This effect is produced by the oscillation of the density of states at the Fermi level which is caused by the quantization of electron energy levels in the presence of a magnetic field (see sec. 4.1, Landau levels) [113, 114]. The oscillations occur with a periodicity of B^{-1} [115].

SdH oscillations can provide a wealth of information about the effective 2DEG (2DHG). For exam-

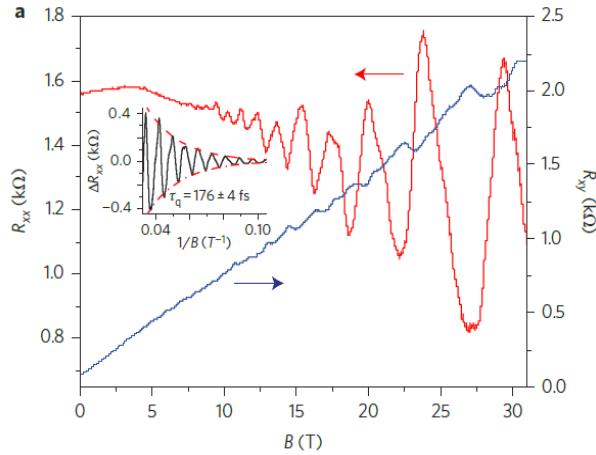


Figure 4.2: main

ple, one can extract the carrier lifetimes, effective cyclotron mass, information about the Fermi surface [75]. In order to observe the QHE and therefore observe SdH oscillations, high device mobility is required [116, 117]. Recently the Cui *et al.* observed the first SdH oscillations in MoS₂, Li *et al.* and Gillgren *et al.* observed this same effect in black phosphorus (and phosphorene) [118, 75, 119]. Cui *et al.* were able to determine geometry of the Fermi surface from the oscillation frequency and prove the two-dimensional nature of their system. Furthermore, from the analysis of the oscillation amplitude the cyclotron effective masses of both electrons and holes could be determined. From this method the carrier lifetime could also be determined, they reported lifetimes of $\tau = 0.11$ ps and $\tau = 0.12$ ps for holes and electrons, respectively [75, 115]. Cui *et al.* was able to provide insight about the quantum lifetimes and the underlying interactions between short-range and long-range scattering limits [118]. The results provide promise that with the implementations of improvements in contact resistance reduction and further mobility enhancement that the world of TMDs is closer to the routine study of novel quantum physics in two-dimensional systems.

4.3 Performance Limits in TMDs

The ultimate performance limit of TMDs is of interest, especially at room temperature as this is most relevant to device applications. First principles calculations show mobility in monolayer MoS₂ to be $\sim 320 - 410 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ at room temperature depending on initial parameters [120, 121]. Previously the experimental values reported differed by an order of magnitude compared to first principles calculations, however, the improvements made in the area of reducing contact resistance has improved mobility measurements [122, 123]. Experimentally, room temperature mobility measurements of both *p* and *n*

type semiconductors still lag behind the theoretical calculations. For example, WSe₂ room temperature mobilities have been reported as $\sim 200 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ with perfect subthreshold swings of $\sim 60 \text{ mV/dec}$, a $I_{\text{on}}/I_{\text{off}}$ of $> 10^6$ at room temperature (others have shown $I_{\text{on}}/I_{\text{off}}$ of $> 10^7$ in WSe₂ and MoS₂), and high $I_{\text{on}} \sim 300 \mu\text{A}/\mu\text{m}$ [59, 124, 67, 88]. Undoped samples have shown to have room temperature mobility of an order of magnitude less than the doped counterparts [125, 88]. Note that these values are not the theoretical limits, but rather represent a current state of where measurements can achieve. To further improve the mobilities measured at room temperature a further understanding of scattering mechanisms is needed. At room temperature phonon scattering limits the mobility, the mobility can be enhanced by doping, however, this introduces impurities and can have an adverse effect on the mobility. Understanding the performance limit at room temperature in monolayers (and few layers) is key to applications in which several TMDs are already being implemented, such as thin film transistor (TFT) and components of ICs like analog amplifiers, digital inverters, and memory transistors [126, 24, 127].

4.4 Conclusion

Overall, TMDs offer a wealth of opportunities in applications. In order to realize these proposed applications several challenges must be overcome, namely achieving low-resistance contacts and high mobility at room temperature. The approach of using degenerately doped contacts and hBN encapsulated devices to lower the SBH and promote increased mobility has shown potential. In addition, the increased mobility that the success of this method would allow one to study quantum transport properties which will reveal many fundamental properties, such as quantum scattering times and effective masses.

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Appendices

2DEG two-dimensional electron gas

2DES two-dimensional electron system

2DHG two-dimensional hole gas

AFM atomic force microscopy

Au gold

BJD Bell Jar deposition

BP black phosphorus

CBM conduction band minimum

DI deionized water

DFT density functional theory

EBL electron beam lithography

FET field effect transistor

IC integrated circuit

IPA isopropanol

IQHE integer quantum Hall effect

MEK methyl ethyl ketone

MFM magnetic force microscopy

MIBK methyl isobutyl ketone

Mo molybdenum

MoS₂ molybdenum disulfide

N₂ nitrogen

Nb niobium

Ni nickel

NPGS Nanometer Pattern Generation System

PC polycarbonate

PDMS polydimethylsiloxane

PMMA polymethyl methacrylate

PPMS physical property measurement system

QHE quantum hall effect

Re rhenium

S sulfur

SB Schottky barrier

SBH Schottky barrier height

Se selenium

SEM scanning electron microscope

SdH Shubnikov-de Haas

SiO₂ silicon dioxide

STM scanning tunneling microscopy

Te tellurium

TEM transmission electron microscopy

TFT thin film transistor

Ti titanium

TLM transmission line model

TMD transition metal dichalcogenides

V vanadium

VBM valence band maximum

W tungsten

WS₂ tungsten disulfide

WSe₂ tungsten diselenide

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