

Principle of operation and environment  
of the AVR Boot-loader  
optiboot

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# Preface

My interest for the AVR boot-loaders begun, as some users had told me their interest to run the transistor tester software at some boards of the Arduino family. Of course the transistor tester software does not run as Arduino Sketch. The Arduino development environment Sketch is only used to show the output of the serial interface. The transistor tester software do not use the Arduino library. This is not necessary to use the boot-loader.

The boot-loader is a little program, which can receive program data from a serial interface from a host (PC) and can put this data in the instruction storage (flash) of the micro-controller. Because the transistor tester software use very much program storage, the boot-loader should use as less program memory as possible for his program. The boot-loader should also be able to write data to the nonvolatile data storage of the AVR, the EEprom. So the target was specified. I search a boot-loader, which support the writing of flash and EEprom, but use only little space in the flash memory for it's own code.

# Chapter 1

## Principle function of a boot-loader

A boot-loader is a little program, which can receive program data from a interface and store this data in the instruction memory of a processor. Typically the received program is also started at the end of transmission. With this method a computer with writable instruction memory is able to run any application program.

In principle the BIOS of a PC is also a boot-loader, but the BIOS is extended for the function to select a interface to fetch the program data. You can select a chain of peripheral equipment, which is tested for existence of program data. Often is a second stage of loader started, which can choose more selections like different operating systems or boot options.

For the micro-controllers the function of a boot-loader is designed more simple. Only one interface is preselected and there are no further options selectable during operation. A characteristic for the mode of operation of a boot-loader is the type of instruction memory. If the instruction memory of the computer is build with RAM (Random Access Memory), the boot-loader must be sure to start any application program only, if it is loaded just before.

For a micro-controller with non-volatile instruction memory (flash), the boot-loader can assume, that a application program has been loaded some time ago to the instruction memory. Therefore the boot-loader try to start a application program every time after waiting for new program data a appropriate time. It doesn't matter, if new program data are received before or not. Even if there was never loaded any application program, the result is not fatal. The facility to load a application program later is still available. The lack of any application program let the boot-loader resume with the next try to get program data from the serial interface.

The figure 1.1 shows the principle function of boot-loaders, which receive their data from a serial interface.

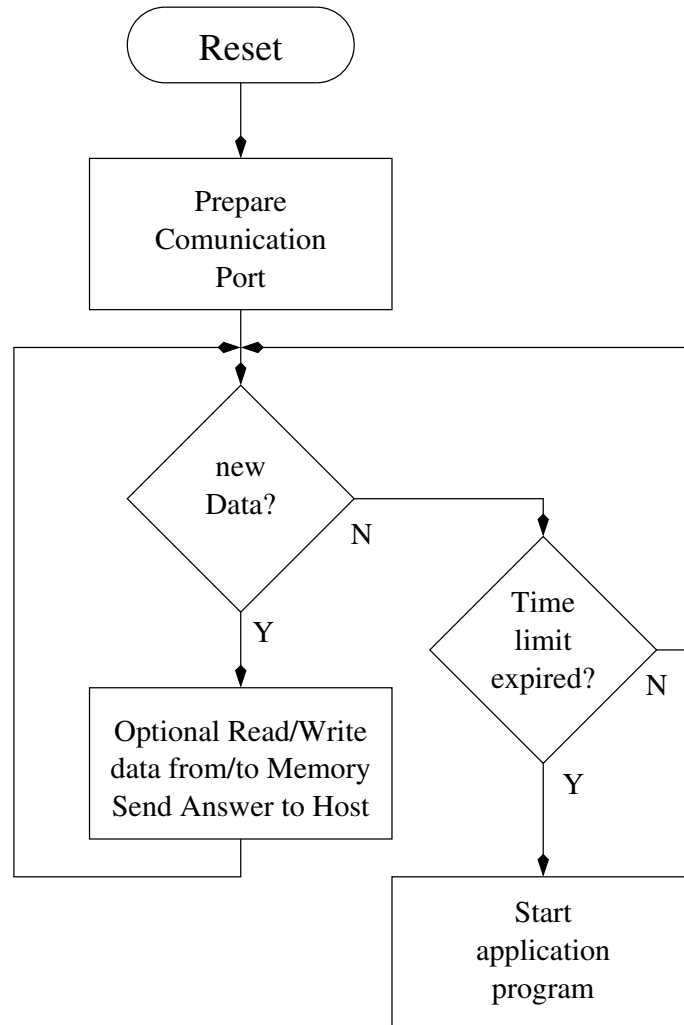


Figure 1.1. Principle function of a boot-loader

The transmitter process at the PC will reset the AVR target processor at the beginning of transmission. If the reset is not done automatically, you must reset the AVR processor manually. The PC tries to start the communication with the AVR processor by sending a data byte to the serial output and wait for any serial response of the AVR processor. If the answer is not received in a appropriate time, the procedure is repeated some times. The boot-loader program at the AVR processor wait only a limited time for new data. If the wait time is exceeded, the boot-loader ties to start a application program in the flash memory.

# Chapter 2

## The Hardware of the AVR 8-bit micro controllers

### 2.1 CPU and memory access

You can find any thing at the chip of a AVR 8-bit micro-controller, what is needed to run a digital computer. You find a clock generator, registers, data storage (RAM), program storage (flash), input registers and output registers. The content of registers and data storage is loosed with every restart. The content of the instruction memory (flash) and the often available additional nonvolatile data storage (EEProm) is preserved for long time. The figure 2.1 shows a simplified block diagram of a 8-bit AVR micro-controller.

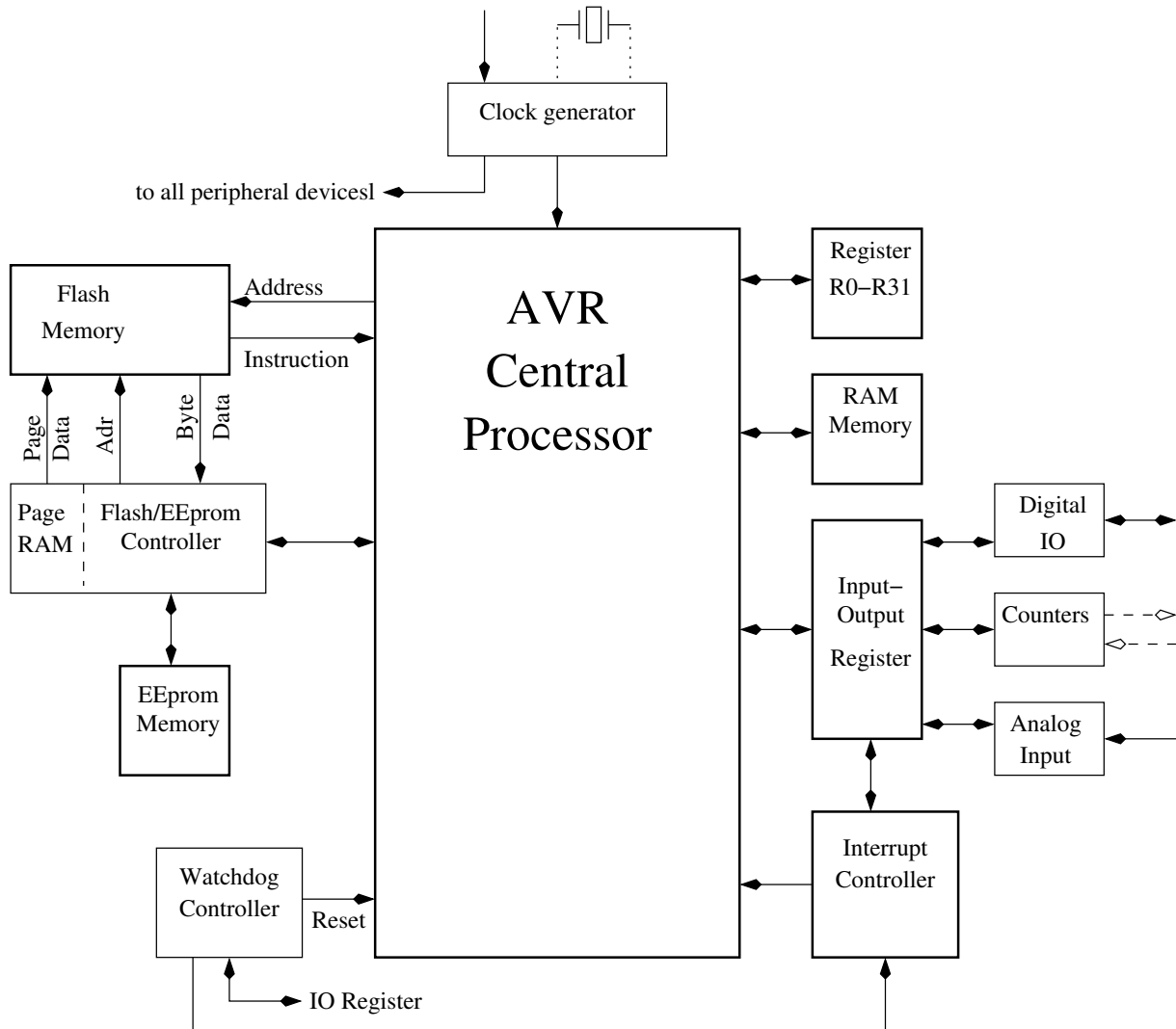


Figure 2.1. Simplified block diagram of a AVR mikrocontroller

You can see at the diagram, that the CPU (Central Processor Unit) can access easy the registers R0-R31 and the RAM memory. Also the access to the input and output registers is easy possible. But the access to the instruction memory (flash) is only possible with a special controller and more complex.

Only the instruction engine can easy access the flash data for the selected program address. With the Load Immediate (LDI) instruction you can transfer parts of the instruction word to the upper registers (R16-R31). Also with the instructions ADIW, ANDI, CPI, ORI, SBCI, SBIW and SUBI parts of the 16-bit instruction word are processed.

Usually after every instruction the program counter will be increased by one word or two words, depending on the instruction length. A exception to this rule for the normal operation is only caused by the conditional or unconditional jump instructions (RJMP, JMP, IJMP, RCALL, CALL, ICALL, RET, RETI).

Also a reset event or interrupt event can be the reason for a discontinuity of the program counter increase. A Reset will reset the whole processor and the program counter will be set to a previous selected address. A interrupt will set the program counter to a associated address. Normally the start address for the reset event is set to 0. For starting the boot-loader many AVR processors have special configuration bits is fuses to select a different start address.

A random address to the instructing memory content is only possible with the flash-controller. For that access you must tell the controller the requested byte address. Afterward the requested byte can be read with a special instruction.





## 2.3 The start of AVR micro-controllers

With the factory set configuration of the AVR micro-controller a first pass over of the minimal operating voltage will cause a reset of the processor. All IO-register are set to predefined values and after waiting some time to stabilize the operating voltage the instruction unit is started with the flash address 0. Normally all pins are set to input mode. Beside this reason for a reset event there exist three other reasons for a reset of the processor. The reason for the reset event is saved in the MCU status register (MCUSR) with four bits.

Name of Flag	Reason for the Reset
PORF	Power-on Reset This Reset is caused by switching on the operating voltage. This reason can not be deactivated.
BORF	Brown-out Reset This reason can only occur, if the function is selected with the BODLEVEL bits of a Fuse and no Brown-out Interrupt is selected.
EXTRF	External Reset is caused by a 0 level at the Reset Pin, if the fuse RSTDISBL is not activated.
WDRF	Watchdog Reset can only be set, if the corresponding Interrupt is not enabled.

Table 2.1. Different Reset reasons in the MCUSR register

By setting the right configuration bits in the fuses of the AVR micro-controller you can select another start address as the usual 0. The figure 2.3 shows the options for a ATmega168. This processor has a total instruction memory (flash) capacity of 16384 Byte. The instruction interpreter of the micro-controller can access a 16-bit parallel instruction code of the flash memory. So the largest program counter is only 8190 for optiboot! It can not be 8192 because the counting begin with 0, but it is one word less because the last word of the flash memory is used to hold the version number of optiboot.

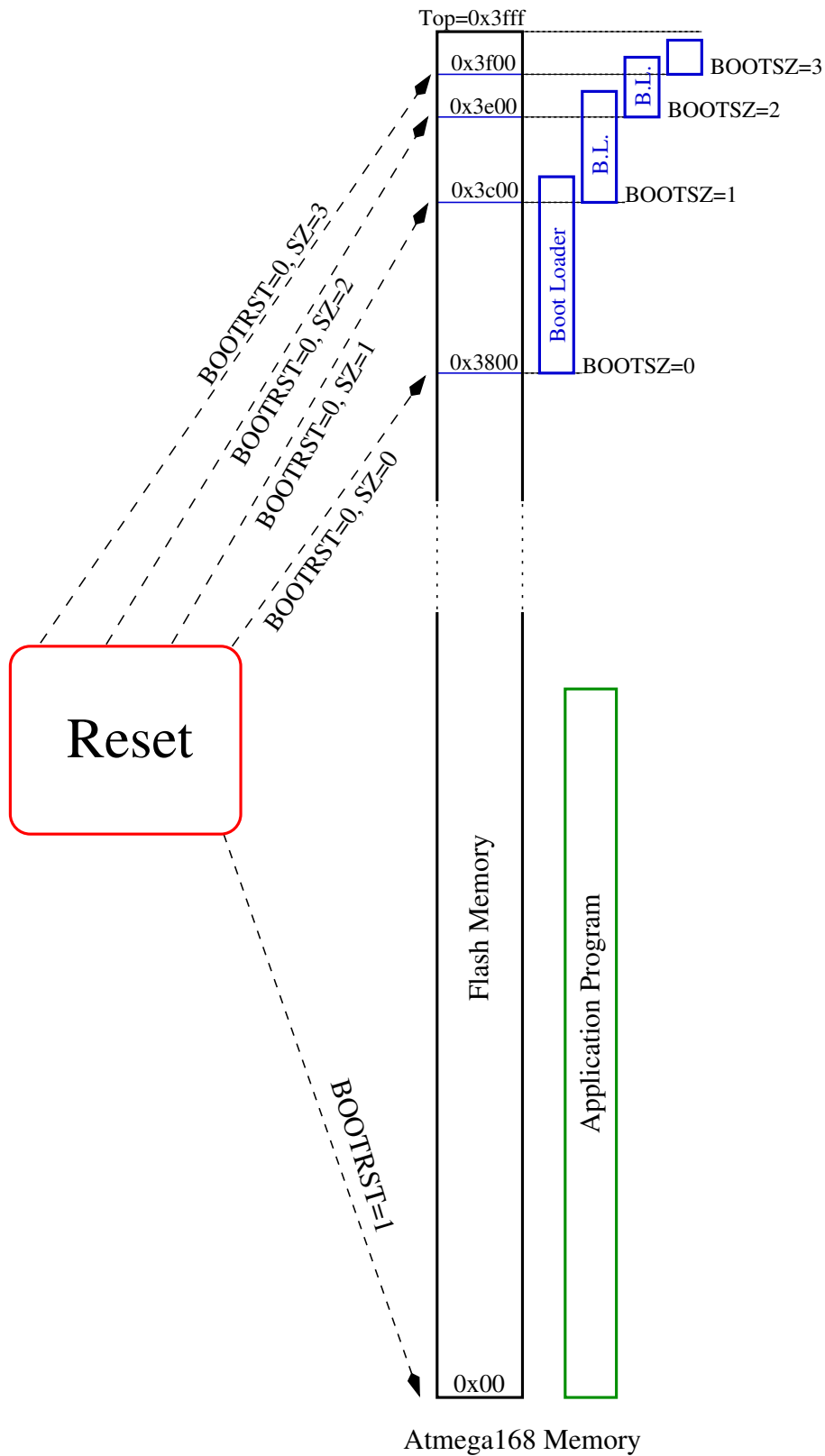


Figure 2.3. The different Start-Options for the ATmega168

The ATmega168 can select a boot-loader size of 256 bytes (BOOTSZ=3), 512 Bytes (BOOTSZ=2), 1024 Bytes (BOOTSZ=1) and 2048 Bytes (BOOTSZ=0). The application program would like to use as many program space as possible, so the boot-loader space should be as low as possible. The boot-loader code is placed at the highest starting address possible. The activating of Lock-bits of the AVR micro-controller can protect the boot-loader area against overwrite. Once activated Lock-bits can only be reset with a total erase of the AVR memories.

For this processor, also for the Mega48 and Mega88, the control bits for the boot-loader start are located in the extended fuse (efuse). This is also true for the BOOTRST fuse, which can be used to switch the start address from 0 to the boot-loader start. For most other AVR micro-controller, also for the ATmega328, the same control bits are located in the high fuse (hfuse). The table 2.2 shows the memory sizes of different AVR-micro-controllers and additionally the options for the Boot-loader area. The boot-loader options are located in the same bit numbers, whatever fuse is selected, the high or extended fuse.

Processor Type	Flash size	EEProm size	RAM size	UART	Boot Config Fuse	BOOTSZ			
						=3	=2	=1	=0
ATmega48	4K	256	512	1	Ext.	256	512	1K	2K
ATtiny84	8K	512	512	-	-	(N x 64)			
ATmega8	8K	512	1K	1	High	256	512	1K	2K
ATmega88	8K	512	1K	1	Ext.	256	512	1K	2K
ATmega16	16K	512	1K	1	High	256	512	1K	2K
ATmega168	16K	512	1K	1	Ext.	256	512	1K	2K
ATmega164	16K	512	1K	1	High	256	512	1K	2K
ATmega32	32K	1K	2K	1	High	512	1K	2K	4K
ATmega328	32K	1K	2K	1	High	512	1K	2K	4K
ATmega324	32K	1K	2K	2	High	512	1K	2K	4K
ATmega644	64K	2K	4K	2	High	1K	2K	4K	8K
ATmega640	64K	4K	8K	4	High	1K	2K	4K	8K
ATmega1284	128K	4K	16K	2	High	1K	2K	4K	8K
ATmega1280	128K	4K	8K	4	High	1K	2K	4K	8K
ATmega2560	262K	4K	8K	4	High	1K	2K	4K	8K

Table 2.2. Boot-loader configurations for different micro-controllers

By the way the boot-loader will work for the first time, even if the BOOTRST fuse bit is not activated. In this case the reset vector is still set to address 0, where usually the application program is located. Because for the first time no application program is loaded, the CPU execute the instructions in the cleared flash memory until it reach the boot-loader code. For the ATmega168 this are less than 8000 instructions, which executes the CPU in less than 1 ms with a 8 MHz clock. But if any application program was loaded, the Reset will start the application program, if the BOOTRST bit is not activated (still set). The boot-loader program can no longer work, because it is not addressed by the reset.

## 2.4 Writing to the AVR memories

The AVR micro-controllers know three different nonvolatile memories. The most important is the instruction memory, the so called Flash memory.

In addition there are some configuration bits, which can be used to select some features of the processor. This configuration bits are organized in some bytes, the lfuse (low fuse), the hfuse (high fuse), the efuse (extended fuse), the lock byte and the calibration byte. The calibration byte is used to calibrate the frequency of the internal RC oscillator. The lock byte can be used to restrict the access to the memories. Once activated lock bits can not be reset by rewriting the lock byte. The only way to deactivate the lock bits is a complete clear of all memories. Note, that the lock function will

be activated by clearing the appropriate bits (write to 0). With the complete clear of all Memories the lock bits will be set to 1 (full access). The layout of the configuration bits to the different fuse bytes differ for the several AVR processor models and should be read in the specific data sheet. You can select the way of clock generation, the delay of start and a monitoring of operating voltage with the fuses.

Most AVR micro-controllers are also equipped with a nonvolatile data memory, the EEPROM. This memory type has no special function for the processor. It is just a way for a application program so save data for the next program start.

### 2.4.1 Parallel programming

All three nonvolatile memory types can be written or read with different technique. Usually the parallel programming method is rare used for writing the nonvolatile memories. Sometimes this method is the only way to reactivate processors, which can not accessed with other methods. For example you can not use the serial programming, if the fuse bit for the Reset pin usage is deactivated (RSTDISBL=0). The voltage at the reset pit is raised to higher voltage level (12V) for this parallel programming method. Therefore this method is also called HV-programming.

### 2.4.2 serial download with ISP

The normal way to program any non volatile memory is the serial programming. The Atmel documentation call this method also serial download. For that way a SPI (Serial Parallel Interface) interface is used. The SPI interface is build with three signals, MOSI, MISO and SCK. Additionally the Reset pin of the AVR processor must hold to 0V to force this special download mode. Together with two additional power signals GND and VCC (about 2.7 to 5V) this four signals build a ISP (In System Programming) interface, which is often integrated at many boards. The figure 2.4 shows the layout of two usual plugs, which are often integrated at boards with AVR micro-controllers.

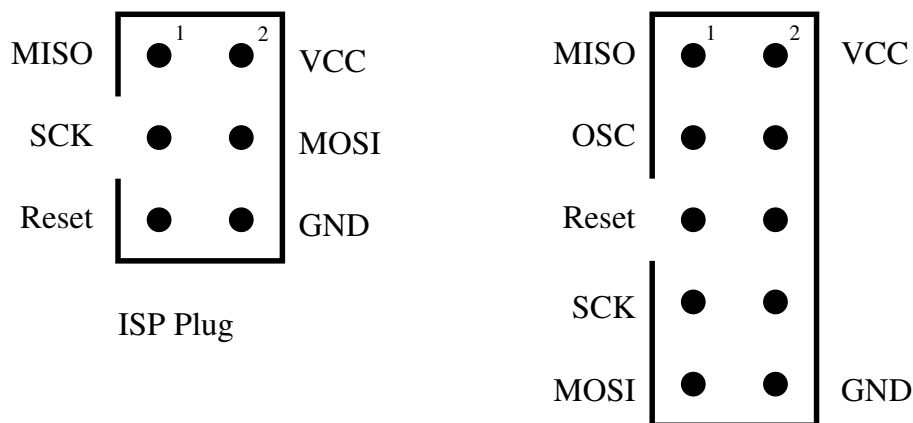


Figure 2.4. Two different types of ISP Plugs

The 10-pin version of the ISP-plug can additionally support a clock signal OSC for feed-in a clock signal to the AVR micro-controller. One of this two plug versions are usually required to program a boot-loader in the flash memory of a AVR micro-controller. The program data for the flash memory are usually created with a PC. To transfer the program data to the AVR micro-controller a ISP programmer is required, which use often a USB interface to the host computer side. But the host computer can also use a serial or parallel interface to connect a ISP programmer. The USB interface has the advantage, that the power (5V or 3.3V) for the micro-controller can be taken easy from the interface. You can choose some types of specific ISP programmers at the electronic market,

the manufacturer of the controllers offer the Atmel AVR-ISP MK2 programmer for example. But you can also use a Arduino UNO or a similar Arduino with a special program for the connected ISP interface. I use a DIAMAX ALL-AVR, which is equipped with both plug types and has some additional features.

### 2.4.3 Self programming with serial interface

Because the AVR processor can write flash and EEPROM memories with special instructions, you can write a little program to the flash memory with one of the two programming methods, which receive data from a serial interface and can write this data to the flash or EEPROM memory. Exactly this is the feature of the boot-loader optiboot. Setting of fuses or lock bytes is often not possible with this method and is not supported by the boot-loader. You must set the fuses and the lock byte with one of the other methods. The STK500 Communication Protocol from Atmel is used for the serial data transfer. Because up-to-date computers often have no more any serial interfaces, a USB - serial converter like the FTDI chip of Future Technology Devices International Ltd is used. A module with this chip is for example a UM232R.

The Chips PL2303 from Prolific Technology Inc. and CP2102 from Silicon Laboratories Inc. satisfy the same purpose. Also a suitable programmed ATmega16U2 can be used for the same function. All of these chips have a selectable Baud-rate and a TTL level for the serial signals. You have to add level converter to get real RS232 signals. But the AVR micro-controllers don't need RS232 signal level. One of these chips is integrated at any Arduino board with USB interface. For a fast answer the serial interface should also connect the DTR signal of the converter with a serial 100nF capacitor to the Reset input pin of the AVR processor. The figure 2.5 shows a typical way of connection.

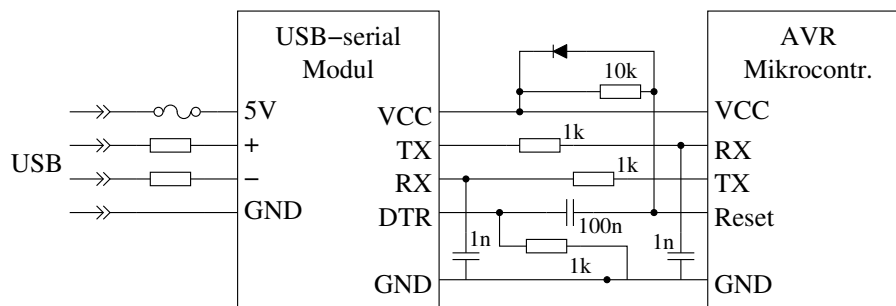


Figure 2.5. Connection of a USB-serial converter to the micro-controller

You should select the right power voltage for the USB - serial converter. Most modules can select a 3.3V or a 5V signal level with a jumper. If you have a Arduino UNO with a ATmega328p at a socket, you can remove the ATmega328p and use the board as USB - serial converter. So you can transfer program data to another AVR processor with a already installed boot-loader. If you frequently use this serial interface, a separate USB - serial interface make sense.

You can select with the Arduino development tool Sketch with the menu entry "Tools - serial Port" a detected serial port. Then you can open a monitor window with the menu entry "Tools - Serial Monitor", which can show you the serial output of your AVR micro-controller at the screen. The Baud rate of the serial interface can be selected at the monitor window. Both 1 nF capacitors at the RX-inputs removes spikes from the serial signals. The test of the software UART program was only successfull with a little capacitor at the RX input of the AVR processor. The probe of a scope was sufficient as "filter" for the spikes. The hardware UART tolerates the spikes without any filter and runs proper with or without the capacitor.

The running Serial Monitor of the Arduino Sketch can disturb the program download with the serial interface, if the same USB - serial module is used for download and the monitor program. But

you can insert a additional USB - serial module to the host computer and connect only the RX-Signal to the TX-Port of the AVR micro-controller. This second serial input listen to the output of the AVR without any problems for the serial communication of the program download, if you select this second interface with the Serial Monitor tool.

## 2.4.4 Diagnostic Tools

At the Linux operating system you can install a tool with the strange name `jpnevulator`, which can monitor two serial inputs at the same time. Any received data are shown in a hexadecimal format and with the option `-a` also as ASCII characters. With the option `--timing-print` the system time of the serial data packets are shown. To prevent any affect to the data communication, you should select two separate USB - serial modules for this monitoring. You should connect the serial input (RX) of one module to the TX signal and the serial input of the other module to the RX signal of the AVR micro-controller. Together with the module for the program download there are three USB - serial modules connected to the PC. Of course all three modules must be set to the same baud rate (`stty ... -F /dev/ttyUSB1`). Without the speed parameter (`stty -F /dev/ttyUSB1`) the current settings of the specified device are shown by `stty`. Some applications like `avrdude` can set the baud rate itself. The full command line with the start of the protocol can be look like:

```
jpnevulator -a --timing-print --read --tty "/dev/ttyUSB1" --tty "/dev/ttyUSB2"
2016-05-29 11:05:06.589614: /dev/ttyUSB0
30 20                                0
2016-05-29 11:05:06.589722: /dev/ttyUSB1
14 10                                ..
2016-05-29 11:05:06.593593: /dev/ttyUSB0
41 81 20                            A.
2016-05-29 11:05:06.594581: /dev/ttyUSB1
14 74 10                            .t.
2016-05-29 11:05:06.597583: /dev/ttyUSB0
41 82 20                            A.
2016-05-29 11:05:06.598574: /dev/ttyUSB1
14 02 10                            ...
2016-05-29 11:05:06.601586: /dev/ttyUSB0
42 86 00 00 01 01 01 01 03 FF FF FF FF 00 80 04 B.....
00 00 00 80 00 20                    .....
2016-05-29 11:05:06.603608: /dev/ttyUSB1
14 10                                ..
2016-05-29 11:05:06.605639: /dev/ttyUSB0
45 05 04 D7 C2 00 20                E.....
2016-05-29 11:05:06.606576: /dev/ttyUSB1
14 10                                ..
...
```

# Chapter 3

## The optiboot boot-loader for AVR Micro-controllers

The optiboot Boot-loader has been created with C language by Peter Knight and Bill Westfield. I have used the version 6.2 as base for the here described revised Assembler version. I would like to underline, that I did not reinvent the optiboot boot-loader. I have just done some optimizing. Many adaptations to several target processors and special board level systems are present with the version 6.2. The program use parts of the STK500 communication protocol, which is released with AVR061 [21] from Atmel.

### 3.1 Changes and enhancements to the version 6.2

Basically I have translated the total program in the assembler language and have adapted the Makefile, that the program length will be processed automatically to select the start address of the boot-loader and set the right fuses for the program length. The selected solution generates some small files during some interim steps, which are required to solve the following steps to select the right start address and the right fuses. The start address of the boot-loader for any target processor depends on the present flash size, the flash requirement of the boot-loader code and the tile size, which is supported by the target processor for bootlace. The tile size is the smallest boot-loader size, which can be supported by the selected target processor.

For processors like the ATtiny84, which don't support the boot-loader start function, the page size of the flash memory is used for this calculation. For the ATtiny84 this are 64 Bytes. Therefore the start address of the boot-loader is always located at the begin of a flash page.

For all other supported target processors the boot-loader area can be selected with the fuse bits BOOTSZ1 and BOOTSZ0 (each with the values 0 and 1). If you put together the both bits, you get a coded boot-loader size with values between 0 and 3. Always the value of 3 select the smallest possible boot-loader area. A value of 2 select a double size, the value 1 the quadruple size and the value 0 select a size of eight times the smallest size. The table 2.2 at page 10 shows a overview for the several target processors.

### 3.2 Automatic size adaption in the optiboot Makefile

The boot-loader start address and the required boot-loader size will be adapted automatically with the Makefile. For the calculation some interim files are created, which is only possible together with some Linux tools:

**bc** a simple calculator, which can operate with input and output- values in decimal and hexadecimal values.

**cat** put the file content to the standard output.

**cut** can select part of lines of a text.

**echo** shows the specified text at standard output.

**grep** shows only lines of a text file which contain the specified string.

**tr** can replace or erase characters.

Until now this function of the Makefile is only tested with a Linux system. Probably a use with the Windows system is only possible, if you install the Cygwin package.

You don't handle the different interim files in normal case. Here I would like to refer the names and the meaning:

**BootPages.dat** hold the count of required pages by the boot-loader. For processors which support the boot-loader start feature, the value can be only 1, 2, 4, or 8 and specifies how many times the minimum size of the boot-loader area (tile) is used. With the virtual boot-loader support the number can be any value and specifies the count of required flash pages.

**BOOTSZ.dat** hold a number between 0 and 3 for selection of the BOOTSZ0 and BOOTSZ1 bits.

**BL\_StartAdr.dat** hold the start address of the boot-loaders with hexadecimal format. The start address is computed with the flash size of the selected target processor and the count of required page or tile size.

**EFUSE.dat** hold the value for the efuse in hexadecimal format. The Makefile determine depending of the target processor type, if this file is used or not.

**HFUSE.dat** hold the value for the hfuse in hexadecimal format. The Makefile determine depending of the target processor type, if this file is used or not.

### 3.3 target selection for the optiboot Makefile

The control of steps for generating the program data from the source code is defined in the Makefile. Except the main Makefile there are three additional extension Makefiles, which are included by the main Makefile: Makefile.1284, Makefile.atmel, and Makefile.extras . There can exist different configurations for the same processor type. The table 3.1 shows different basic configuration for several target processors. In principle this list can be extended. You can select some parameters also with the make call or by setting a environment variable of the shell.



Name	MCU	AVR_ FREQ	total Flash size	Flash page size	BP_ LEN	LFUSE	HFUSE	EFUSE
attiny84	t84	16M?	8K	64	(64)	62	DF	FE
atmega8	m8	16M	8K	64	256	BF	CC	-
atmega88	m88	16M	8K	64	256	FF	DD	04
atmega16	m16	16M	16K	128	256	FF	9C	-
atmega168	m168	16M	16K	128	256	FC	DD	04
atmega168p	m168p	16M	16K	128	256	FC	DD	04
atmega32	m32	16M	16K	128	256	BF	CE	-
atmega328	m328	16M	32K	128	512	FF	DE	05
atmega328p	m328p	16M	32K	128	512	FF	DE	05
atmega644p	m644p	16M	64K	256	512	F7	DE	05
atmega1284	m1284	16M	128K	256	512	F7	DE	05
atmega1284p	m1284p	16M	128K	256	512	F7	DE	05
atmega1280	m1280	16M	128K	256	1K	FF	DE	05

Table 3.1. Processor targets for optiboot Makefile

All size values are shown in byte units, the values for fuses are shown with hexadecimal values. The frequency values must be specified in Hz units, 16M is the same as 16000000 Hz. The standard baud rate of the serial interface is always 115200.

Additional to the universal processor configurations you can also select configurations for special boards or operational environment. The table 3.2 shows the different adjustments.

Name	MCU	AVR_ FREQ	BP_ LEN	L FUSE	H FUSE	E FUSE	BAUD_ RATE	LED	SOFT_ UART
luminet	t84	1M	64v	F7	DD	04	9600	0x	-
virboot8	m8	16M	64v						
diecimila	m168	(16M)		F7	DD	04		3x	-
lilypad	m168	8M		E2	DD	04	-	3x	-
pro8	m168	16M		F7	C6	04	-	3x	-
pro16	m168	16M		F7	DD	04	-	3x	-
pro20	m168	16M		F7	DC	04	-	3x	-
atmega168p_lp	m168	16M		FF	DD	04	-		-
xplained168pb	m168	(16M)					57600		
virboot328	m328p	16M	128v						-
atmega328_pro8	m328p	8M		FF	DE	05	-	3x	-
xplained328pb	m168	(16M)					57600		
xplained328p	m168	(16M)					57600		
wildfire	m1284p	16M					-	3xB5	
mega1280	m1280	16M		FF	DE	05	-		-

Table 3.2. configured targets for the optiboot Makefile

## 3.4 The Options for the optiboot Makefile

With the options you can select the feature of the optiboot boot-loader. For example you can select with the option `SOFT_UART`, that a software solution is used for the serial communication. Without this option a integrated hardware UART is used for serial communication. The pin TX (Transmit) is used for serial output and the pin RX (Receive) is used for serial input. If more than one UART is present at the target processor, the first interface with the number 0 is used. But you can also select every other present UART by specify the number with the option `UART` (`UART=1` for the second present UART). For the hardware UART interfaces the pins for transmit and receive are fixed to the specific pins. For the serial communication with software you can select any pins, which are able to do digital input and output. More details for the available options you can find in the tables 3.3 and 3.4

Name of the Option	Example	Function
F_CPU	F_CPU=8000000	Tell the program the clock frequency of the processor. The value is specified in Hz units (cycles per second). The example specifies a frequency of 8 MHz.
BAUD_RATE	BAUD_RATE=9600	Specifies the baud-rate for the serial communication. Always 8 data bits without parity is used.
SOFT_UART	SOFT_UART=1	Select a software solution for the serial communication.
UART_RX	UART_RX=D0	Specifies the port and bit number used for the serial input. The example select bit 0 of PIND as serial input. You can use this option only with the software UART.
UART_TX	UART_TX=D1	Specifies the port and bit number used for the serial output. The example select bit 1 of PORTD as serial output. You can use this option only with the software UART.
UART	UART=1	Select a hardware UART used for the serial communication. You can only select a UART if more than one is present.
LED_START_FLASHES	LED_START_FLASHES=3	Select a repetition count of flashing cycles for the control LED. A count of 1 or -1 will only flash once without a loop. Negative values will force a additional check of the RX pin of the serial interface. The loop is interrupted immediately, if any incoming serial data is detected. Please note, that the start of application program is delayed with the blink cycles.
LED	LED=B3	Select a port and bit number for the control LED. The example would select the bit number 3 of the port B for the LED connection. With the option LED_START_FLASHES this LED will flash the specified count before the communication start. With the option LED_DATA_FLASH the LED will glow during wait for serial input.
LED_DATA_FLASH	LED_DATA_FLASH=1	The control LED will glow during waiting for serial input data.
TIMEOUT_MS	TIMEOUT_MS=2000	This option specifies a time limit in ms units for receiving boot data. After this time without data the boot process is aborted and the processor tries to start the user program. Possible values for TIMEOUT_MS are 500, 1000, 2000, 4000 and 8000. The effective value can be limited to 2s because of processor limits for the watchdog. If no TIMEOUT_MS is specified, the time limit is set to 1 second.

Table 3.3. Important options for the optiboot Makefile

When operating with the internal RC generator, it is quite possible that a serial data transfer not immediately succeed. This is principle independent of whether the hardware UART interface or a software solution (SOFT\_UART) is used. Without additional measurement you can only try with estimated OSCCAL\_CORR values. Probably the data sheet of the AVR processor can help a little bit. Here is described at which operating voltage and at what temperature the RC oscillator

was calibrated. In addition here is also described the gradient of frequency change with operating voltage, temperature and OSCCAL modification.

More options are listed in table 3.4 . Some of these options are only interesting for software checks and for processors without the boot-loader support.

Name of the Option	Example	Function
SUPPORT_EEPROM	SUPPORT_EEPROM=1	Select the EEPROM read and write function for the boot-loader. If the assembly language is selected as source, the EEPROM support is enabled without this option, but can be switched off by setting the SUPPORT_EEPROM Option to 0. For the C-source the function must be switched on (default = off).
C_SOURCE	C_SOURCE=1	Select the C language as source instead of the assembly language (option 0 = assembly). The assembly version requires less program space.
BIGBOOT	BIGBOOT=512	Select additional space usage for the compiled program. This is used only for tests of the automatic adaption to the program size.
VIRTUAL_BOOT_PARTITION	VIRTUAL_BOOT_PARTITION	Changes the interrupt vector table of a user program, that the boot-loader is called with a Reset. For the start of the user program another interrupt vector is used.
save_vect_num	save_vect_num=4	Choose a interrupt vector number for the VIRTUAL_BOOT_PARTITION method.
OSCCAL_CORR	OSCCAL_CORR=5	With the option OSCCAL_CORR you can adjust the internal 8 MHz RC-generator of the AVR. Is effectless with crystal-operation or external clock! The correction value will be subtracted from the actual OSCCAL byte. The frequency will be lower with a positive correction value. Because the produced Baud rate is directly derived from the processor clock, a correct selected processor clock is important for a successful serial communication. The value must be between -15 and +15.

Table 3.4. More options for the optiboot Makefile

### 3.5 Usage of optiboot without a boot-loader area

For processors without a special boot-loader area in the flash memory, for example the ATtiny84, a solution is selectable to use the optiboot anyway. This function can be selected with the VIRTUAL\_BOOT\_PARTITION option. To start the boot-loader first with every Reset of the processor, the interrupt vector table of the application program is changed. At the reset vector location a jump to the optiboot program is registered. The original start address of the application program will be moved to another interrupt vector the "replacement reset vector". This interrupt vector should not be used by the application program. If the boot-loader does not receive any data from the serial interface within a appropriate time, the boot-loader jump to the location of the replacement reset vector and start the application program. The figure 3.1 should illustrate these changes.

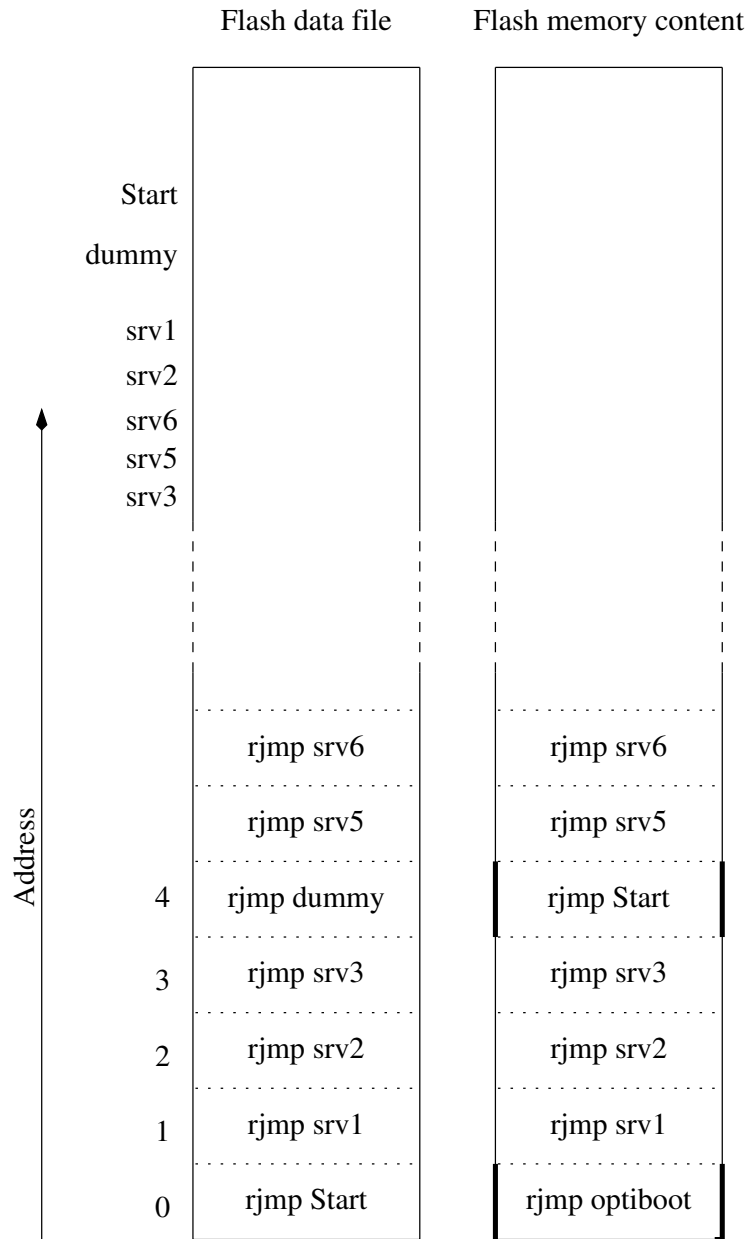


Figure 3.1. Changes of program data by optiboot

At the left side the content of the program data file (.hex) is shown. Just to the right the content of the flash memory is shown, as it is modified by the optiboot boot-loader. At two interrupt vector addresses the content is changed. At the reset vector address 0 the jump is modified to select the optiboot start address as jump target. At the "replacement vector address" 4 the original jump target address of the application program's reset vector is used as new jump target address of this vector. One of the problems with this modification is, that usually the program data is verified by the host after write is finished. To provide any error message by verify the program data, the optiboot return the program data without its own modification, not the real content of the interrupt vector table. The jump target address of the reset vector can be reconstructed with the content of the replacement vector address. But the original content of the replacement vector would be lost because there is no place to save the original content in the flash memory. Therefore optiboot use the last two places of the EEprom memory to save this original content of the replacement vector. So the verify of the program data is possible without errors, as long as the application program do not use one of the last two EEprom locations. Even if the application program use one of the last two EEprom locations, the boot-loader will be unaffected. Only the program verify by the host is no longer possible without

a error message. An error message will occur at the location of the replacement interrupt vector.

For processors with more than 8 kByte flash memory two instruction words are used for every interrupt vector. Normally every of this double words hold one JMP instruction with the proper jump target address. The optiboot program can respect these JMP vector table too. But if you use the linker avr-ld with the option `-relax`, all JMP instructions are replaced by a RJMP, if this is possible for the target address. This replacement of JMP instruction in the vector table by RJMP is not respected by the optiboot program. The optiboot program assume, that all interrupt vector numbers of a processor with more than 8 kByte flash hold a JMP instruction. For that reason a optiboot program with the `VIRTUAL_BOOT_Partition` option will not work with a application program, which is linked with the `-relax` option. The same problem exist, if the application program itself use a RJMP instruction in one of the two critical interrupt vector positions.

Further you should notice, that you don't activate the BOOTRST fuse together with with the usage of the `VIRTUAL_BOOT_PARTITION` option. The reason is, that the start address of the boot-loader can be located to other addresses with the `VIRTUAL_BOOT_PARTITION` option than without this option. With the `VIRTUAL_BOOT_PARTITION` the start address can be placed to every begin of a flash page. For the normal boot-loader support of the AVR the start address can only respect the single, double, quadruple or octuple size of a minimum boot-loader size as shown in figure 2.3 at page 9.

## 3.6 Capabilities of the serial interface with the applied software

Das Programm für die Erzeugung und Verarbeitung der elektrischen Signale ist in AVR-Assembler geschrieben. The way of operation is taken over from the Application Note AVR305 of the ATmel Corporation. However here are some special features build in. For example it is respected, that we can not use the special bit-instructions SBI, CBI and SBIC for any port address. You can use this instructions only up to the address 31 (0x1f). For some higher port addresses up to 63 (0x3f) you can use special input (IN) and output (OUT) instructions. If the addresses of the port are higher than this value, you must use the instructions LDS and STS to access this ports. This instructions need 2 processor clocks for execution and use the double flash memory (2 words or 4 byte) of the other instructions. The changed cycle number of one loop pass without any additional delay will be automatically determined by the program. This number of cycles is then taken into account for the calculation of the delay loop, to achieve a correct time for the transmission of a bit. The diagrams 3.2 and 3.3 should be used to explain the work of the C-processor.

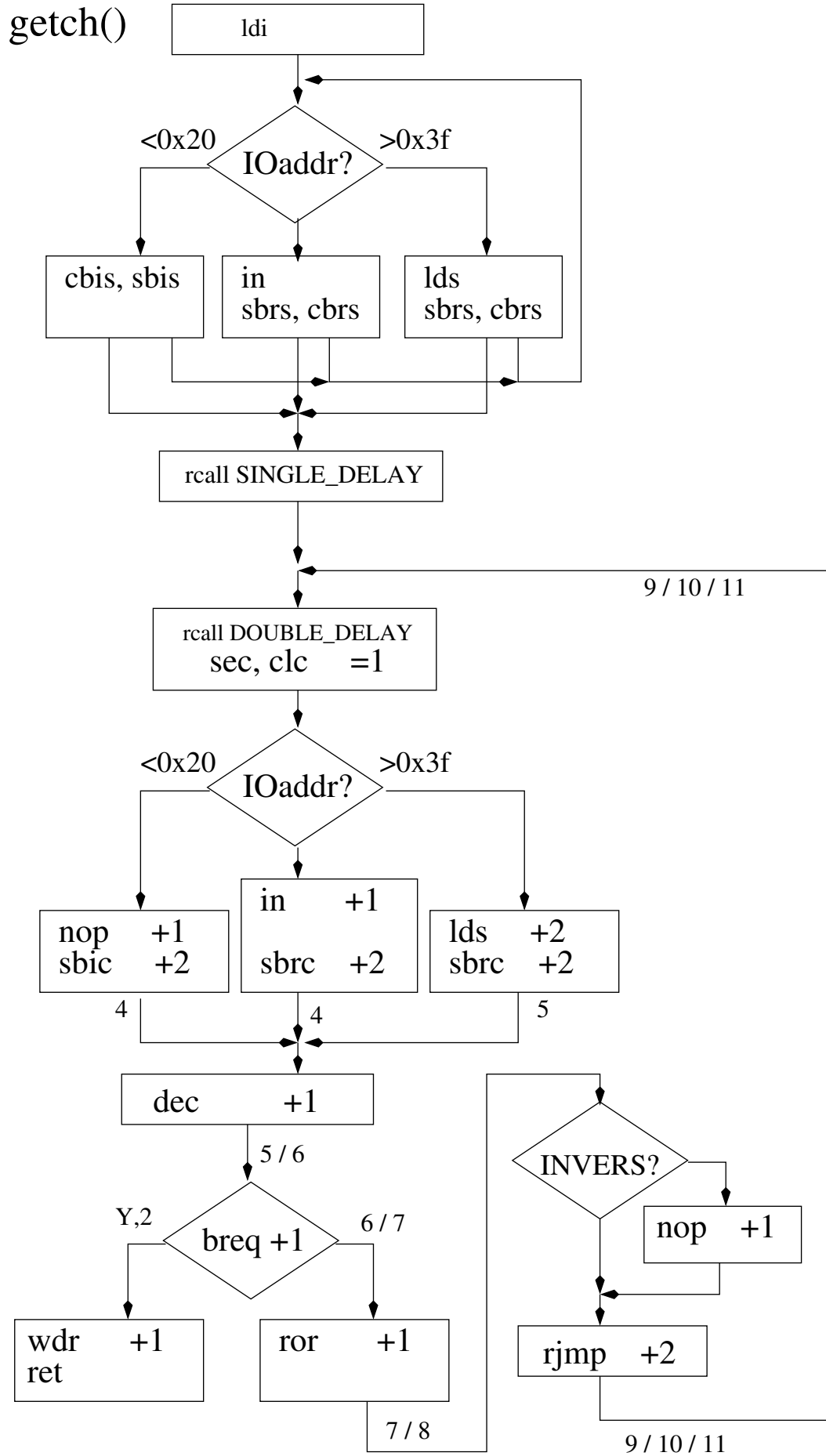


Figure 3.2. Possible variants of the getch function

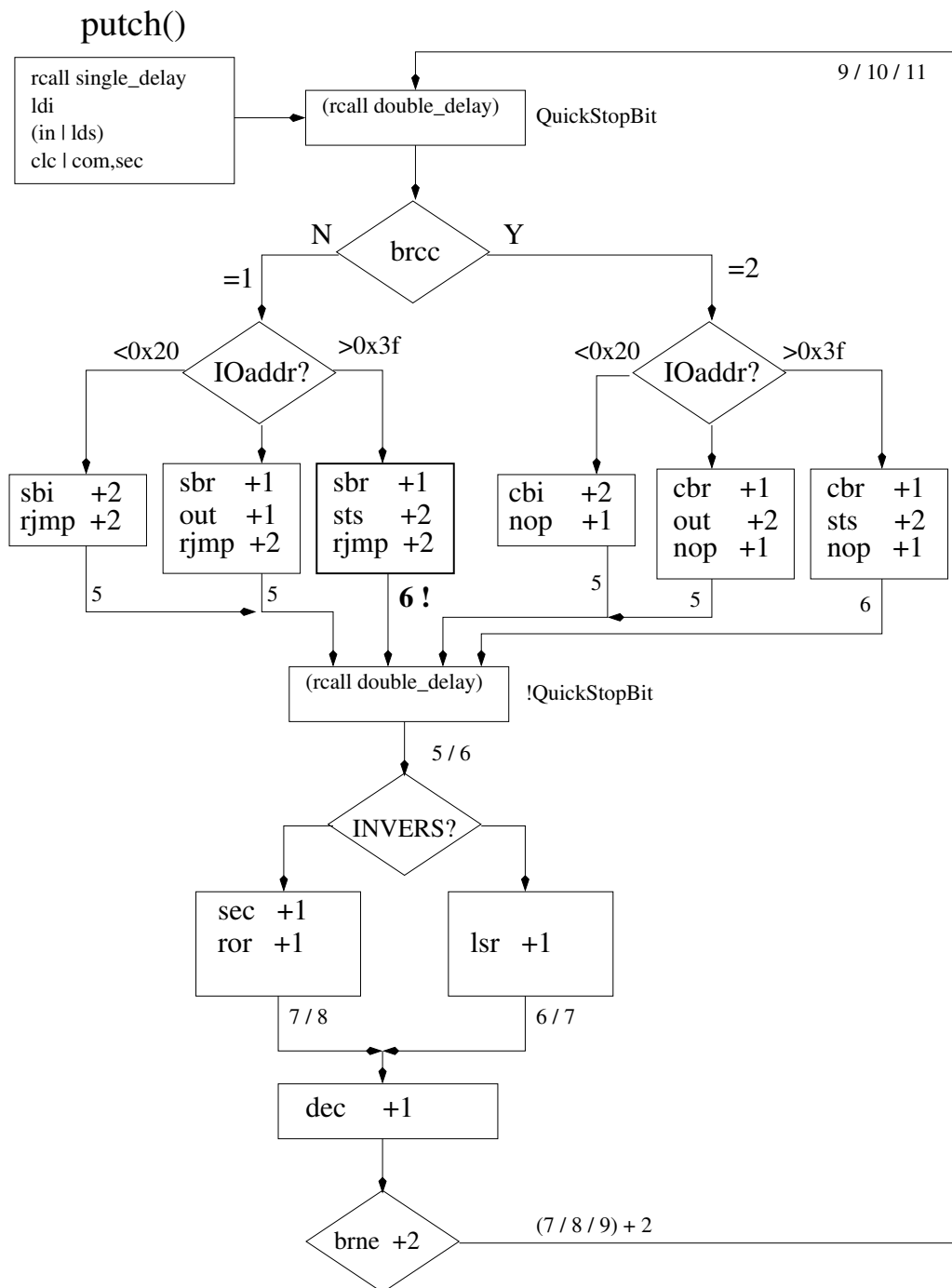


Figure 3.3. Possible variants of the putch function

Both loops are generated so that one cycle with the same conditions of **INVERS** option and address range of the used ports use the same tic count. So both functions can use the same function for generating the necessary delay.

### 3.6.1 Computing of the delay time

For the read-in function `getch()` is the half baud time needed. From the detection of the start bit a total time of 1.5 times of the baud-time is delayed to read the first data bit. Therefore the base loop is designed for the half duration of a bit transmission. This base loop is called twice in a special way, so that exactly twice the time is get. Should one clock have been lost by the building of half the time and subsequent doubling, this clock is compensated by adding a additional NOP command, so that the total time is exactly correct for the transmission of one bit. Because of the limited



time resolution of the counter loop of 3 tics, a remainder of up to 2 clock tics is compensated by adding a additional instruction with the right tic count (RJMP or NOP). Of course, all this happens automatically, because only the loop time of the input function (getch) and the output function (putch), the clock frequency of the processor and the desired baud rate must be known. All other parameters like the number of clocks for a subroutine call (RCALL, RET) are known for the target processor. A disadvantage of the base delay loop is the limited number of clocks for the delay. With the used 8-bit counter only a maximum of  $256 \cdot 3$  clocks is possible for the loop delay. In addition there is the subroutine call of 7 tics, resulting in a half delay time of 775 tics. This value must be doubled (delay for a whole bit time) and the loop-time of the input or output function must be added to get the total time possible. Thus the highest achievable delay time is 1559 clocks. With a  $16\text{MHz}$  clock frequency you can not get a baud rate of 9600 Baud  $104.17\mu\text{s}$ , because the limit is only  $97.4\mu\text{s}$ . If a 16-bit counter is used by the delay loop, you would get an even worse resolution of time because one loop cycle would take more time. In addition, the 16-bit loop probably need to use the carry bit. The 8-bit counter don't use the carry bit. This problem is solved by gradually doubling the delay times by doubling the delay loop call. The C-preprocessor checks, if the initial value of the loop counter would match the 8-bit limit (255) at the selected clock frequency and the desired baud rate. In this case the calculation is repeated for a double call of the base delay loop. If the resulting initial value for the counting loop is still too high, the double call is doubled again. Currently this procedure is repeated up to a factor 64 of the base time with the 8-bit counter. At a clock frequency of  $16\text{MHz}$  or  $20\text{MHz}$  it is now possible to set the serial interface to 300 baud. For every doubling of the delay time, a additional instruction (2 bytes) is required. With the maximum count of doubling 6 additional instructions (12 byte) are required in the flash memory. There is no attempt to add additional instructions to compensate the missing tics caused by the prescaler for saving flash memory. The baud time error remains clearly below 1%, because the scaler is used only if necessary. So the base loop has at least 127 passes with approximately 381 tics, The double delay time makes no error because of the "NOP" compensation. Thus the error stays below  $1:762$  0.13%. The higher baud rates tend to get higher error for the transmission time, because the time frame of the CPU clock does not match to the desired baud time. The hardware UART has then the same problem, if it use the same CPU-clock. If you wish to generate a baud rate of 230400 with a CPU clock rate of  $8\text{MHz}$ , you can use either 34 tics with a baud time of  $4.25\mu\text{s}$  or 35 tics with a baud time of  $4.375\mu\text{s}$ . For the first case your baud time is 2.08% too short, for the second case the baud time is 0.8% too long.

### 3.6.2 Using more than one serial interface

The assembler file `soft_uart.S` is designed to be included by a different file which hold a normal assembler source for the AVR family. For the optiboot application this is done by the `optiboot.S` file. The included file `soft_uart.S` use many instructions of the GNU C-preprocessor and includes another file `uart_delay.S` for producing a delay loop for the desired baud rate. Because this include can be repeated with other parameters, you can produce up to 4 different delay loops for 4 different baud rates. This feature use the file `soft_uart.S` for generatung a getch and a putch function. For both functions the file `uart_delay.S` is included. But for the second call is usually no new code generated because the calling parameters are the same. Only if the parameters differ, a new delay loop would be generated. Please note, that the callings for the delay loop are named with C-preprocessor macros. This macros are set to a matching delay loop named `DOUBLE_DELAY_CALL` and `SINGLE_DELAY_CALL`, if you include the `uart_delay.S` file before the code of the serial input or output function.

Three constants must be set before any include of `uart_delay.S`, named `F_CPU`, `BAUD_RATE` and `LOOP_TICS`. The `LOOP_TICS` must be set to the count of tics of the serial input or output loop for one cycle without any additional delay (usually 9 tics). For every generated delay loop,

the total count of delay tics are saved in one of four different constant names of the C-preprocessor `BIT_CLOCKS_0`, `BIT_CLOCKS_1`, `BIT_CLOCKS_2` and `BIT_CLOCKS_3` . Before a new delay loop is generated, the C-preprocessor checks, if any of the already generated code for a delay match the new requirement. Because also the file `soft_uart.S` must be included to generate the code for the serial input and serial output function, you can repeat this include for another serial interface. But you must set a additional constant for differing the name in the functions. If you set the `SOFT_UART_NUMBER` to 1 (`#define SOFT_UART_NUMBER 1`) before the `#include`, the serial input function is named `getch_1` and the serial output function is named `putch_1`. If you define a constant named `NO_SOFT_UART_TX` before the `#include` of `soft_uart.S`, no serial output function is generated by this include. The same is done with the serial input function, if you specify the constant `NO_SOFT_UART_RX`.

### 3.6.3 Serial Input and Output with only one AVR Pin

Sometimes it makes sense to operate the serial communication only with one pin, to unlock one of the few IO pins of small AVR's for other use. With a special circuit technology can be achieved that you can read in data in the output pauses. The software solution of optiboot can only use the half-duplex operation in any case. Thus, at one time, only either data can be send or data can be received. Normally the output pin with the TX function becomes high in the transmission pauses, which prevent a data reading on the same pin. But if the TX output pin is switched to input mode instead of the high level, a external pull-up resistor can provide the required high level. In contrast to the fixed high level now a externally connected TX signal can pull down the level and let the input function read the low level. A serial resistor in the connection between the common TX/RX pin of the AVR with the external TX output can serve as pull-up resistor, because the idle state if the interface is a high signal. In addition, this serial resistor provides current limiting, if both TX interfaces send at the same time. The external RX interface must be connected directly to the common TX/RX pin to enable the reading of the external RX interface. The figure 3.4 should illustrate this simplest connection.

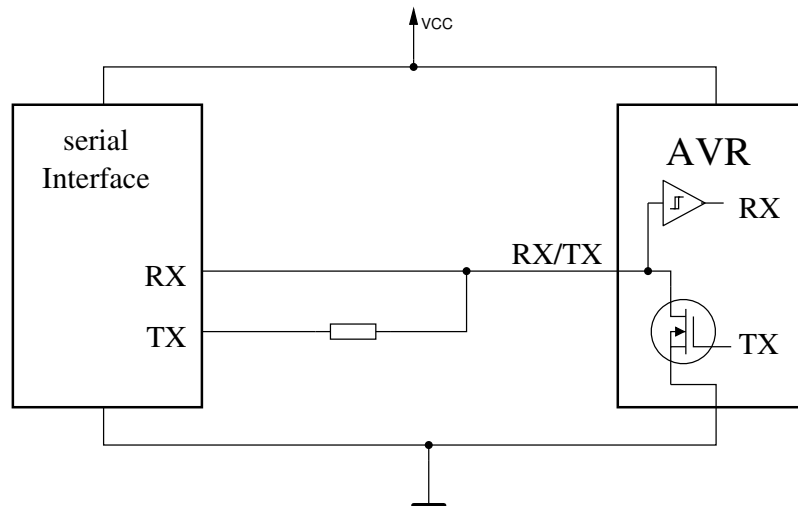


Figure 3.4. Possible serialconnection to a AVR with one Pin

Now is the problem, that the mostly full-duplex capable external interface will read back the own output. The communication program at the external side is usually unprepared for this condition. One solution for this problem is to adapt the program at the external side to handle this read back. But I believe, that this is not a good idea, because this special version will have no maintenance or you must repeat this adaption for new versions constantly. That's why I prefer a hardware solution.

CH340 or FTDI

Special Bootloader required!

74HC132

Can be used instead of HCF4093 with other pin layout!

With the first two NAND gates of the HCF4093 a flip-flop is build, which is set or reset by the two other NAND gates of this chip. The switching signals are get from from signals of a chain of inverting buffers with Schmitt-trigger inputs (HC7414). For one of this signals a additional C-R circuit ( $120pF$  and  $3.3k\Omega$ ) is required to prevent switching at the wrong edge. The flip-flop is switched with the 1-0 edge of the two transmission sides. This changeover is only required at the edge of the start bit. But additional switching with data bits will not hurt, if the flip-flop is already in the right state. When the external interface sends, the reception of the own data with the external receiver is prevented. The external RX signal remains at high level. With this additional circuit no software adaption is necessary. You can use avrdude for example for the bootloader. The circuit is largely independent of the selected baud rate. I expect only problems with very high baud rates. At 115200 baud the circuit operates well. Much higher baud rates can not be used in most cases with the software serial interface.

The first example is the building of a bootloader for the popular ATmega328P:

26

```
-----  
BAUD RATE CHECK: Desired: 115200, Real: 117647, UBRR1 = 16, Error=2.12%  
-----
```

```
#####  
Boot Loader start address: 0x7E00  
#####
```

16000000 Hz operation with Baudrate 115200 configured.

avr-size optiboot.elf

text	data	bss	dec	hex	filename
474	0	0	474	1da	optiboot.elf

Requires 1 Boot Pages, 512 Bytes each

BOOTSZ=3

avr-objdump -h -S optiboot.elf > optiboot\_atmega328p.lst

avr-objcopy -j .text -j .data -j .version --set-section-flags .version=alloc,load \  
-O ihex optiboot.elf optiboot\_atmega328p.hex

With no additional option a baudrate of 115200 with a clock frequency of 16MHz is selected. For serial output the hardware interface is selected. You should notice, that the systematic baud rate error is above 2% with the hardware UART. The second example with the same processor is done with a software solution for the serial interface.

optiboot \$ make atmega328p SOFT\_UART=1

avr-gcc -g -Wall -Os -fno-split-wide-types -mrelax -mmcu=atmega328p \  
-fno-diagnostics-show-caret \  
-DBAUD\_RATE=115200 -DLED\_START\_FLASHES=3 -DSOFT\_UART=1 -DSUPPORT\_EEPROM=1 \  
-DLED=p -DUART\_RX=p -DUART\_TX=p -DF\_CPU=16000000 -c -o optiboot.o optiboot.S

In file included from optiboot.S:254:0:

pin\_defs.h:183:4: warning: #warning "LED bit is set to default B5" [-Wcpp]

pin\_defs.h:192:4: warning: #warning use default RX PD0 for Soft UART [-Wcpp]

pin\_defs.h:200:4: warning: #warning use default TX PD1 for Soft UART [-Wcpp]

```
-----  
BAUD RATE CHECK: Desired: 115200, SoftUART_Real: 115107, Error=-.08%  
-----
```

```
#####  
Boot Loader start address: 0x7E00  
#####
```

16000000 Hz operation with Baudrate 115200 configured.

avr-size optiboot.elf

text	data	bss	dec	hex	filename
494	0	0	494	1ee	optiboot.elf

Requires 1 Boot Pages, 512 Bytes each

BOOTSZ=3

avr-objdump -h -S optiboot.elf > optiboot\_atmega328p.lst

avr-objcopy -j .text -j .data -j .version --set-section-flags .version=alloc,load \  
-O ihex optiboot.elf optiboot\_atmega328p.hex

Please note, that the software solution for the serial interface requires a little more flash memory, but take use of only 1 boot page too. The systematic baud rate error is much smaller than the error with the hardware UART. But the hardware UART has the advantage, that the input and output

could be done simultaneous and is more tolerant against short disturbance of the input signal. For the software serial interface you can specify every digital IO-pin for input (UART\_RX) and output (UART\_TX). In this example the feature is used to automatically select the RX and TX of the hardware UART. Please ignore the three warning messages, which tell you about the automatic selection. The automatic IO-pin selection depends on the selected processor type and the selected UART number, if more than one UART is available.

# Chapter 4

## Various USB to serial converter with Linux

The classic serial interface is less and less used today. On older computers this interface with RS232 standard is more common. However, the classic serial interface is not very practical anyway, because the voltage levels used (about -12V and +12V) can not be used directly. This voltage levels must be first converted back to +5V or +3.3V common with microcontrollers. For purpose of programming microcontrollers the USB to serial converter are more practical, because these provide the proper signal level and can also provide the +5V or +3.3V supply for the microcontroller. With the Linux operating system these USB devives are most detected without problems. But problems can occur to access this devices with the normal user access rights. Mostly the access nodes like `/dev/ttyUSB1` are assigned to the group dialout. Then you (the user) should belong to this dialout group. You can be member of the group dialout with the command `"usermod -a -G dialout %USER"`.

### 4.1 The CH340G and the CP2102 converter

Checked have I a board with the label BTE13-005A, at which a CH340G converter from QinHeng Elektronik is mounted. The board has a mini switch to switch the VCC voltage to 3.3V or 5V and a 12 MHz crystal. At one side there is a USB-A plug and on the other side a 6-pin strip with signals GND, CTS, VCC, TXD, RXD and DTR. One LED connected to VCC and another LED is also mounted at the board. You can find a list of supported baud rates in the chinese datasheet of the CH340G chip. The other board with the CP2102 converter from Silicon Laboratories Inc. has no label. At one side of the board you will find also a USB-A plug and at the opposite side there is also a 6-pin strip with the signals 3.3V, GND, +5V, TXD, RXD and DTR. At the two other sides of the board you can add a 4-pin strip with the signals DCD, D3R, RTS and CTS as well as RST, R1, /SUS and SUS. All signals required by the bootloader are present already at the mounted strip. But the sequence of the signals is different for both boards. You can find only a few parts additional to the CP2102 converter chip, but a LED for RXD, TXD and power is present. With my Linux-Mint 17.2 both convertes are detected without further ado. You can see the folowing output of the `lsusb` command:

```
Bus 002 Device 093: ID 10c4:ea60 Cygnal Integrated Products, Inc. CP210x UART Bridge / myA
Bus 002 Device 076: ID 0403:6001 Future Technology Devices International, Ltd FT232 Serial
```

Of course, the information on the bus depends on the computer and the USB port used. The automatically created device name after the connection can be find out by the command `"dmesg | tail -20"`. In the following example I have summarized both results.

```

usb 2-4.2: new full-speed USB device number 94 using ohci-pci
usb 2-4.2: New USB device found, idVendor=1a86, idProduct=7523
usb 2-4.2: New USB device strings: Mfr=0, Product=2, SerialNumber=0
usb 2-4.2: Product: USB2.0-Serial
ch341 2-4.2:1.0: ch341-uart converter detected
usb 2-4.2: ch341-uart converter now attached to ttyUSB1
usb 2-4.5: new full-speed USB device number 93 using ohci-pci
usb 2-4.5: New USB device found, idVendor=10c4, idProduct=ea60
usb 2-4.5: New USB device strings: Mfr=1, Product=2, SerialNumber=3
usb 2-4.5: Product: CP2102 USB to UART Bridge Controller
usb 2-4.5: Manufacturer: Silicon Labs
usb 2-4.5: SerialNumber: 0001
cp210x 2-4.5:1.0: cp210x converter detected
usb 2-4.5: reset full-speed USB device number 93 using ohci-pci
usb 2-4.5: cp210x converter now attached to ttyUSB2

```

With this information and my own experiments I have created the tables 4.1 and 4.2. Because the newer operating system Linux Mint 18.3 has given partially better results, I have measured the results with this system.

CH340G supported BaudRate	CH340G stty speed	CH340G measured BaudRate	CP2102 supported BaudRate	CP2102 stty speed	CP2102 measured BaudRate	AVR UBBR @16MHz
50	50	50.00	-	Error		
75	75	75.18	-	Error		
100	Error	-	-	Error		
110	110	109.3	-	Error		
134	134	133.4	-	Error		
150	150	150.4	-	Error		
300	300	300.7	300	300	300.7	
600	600	602.4	600	600	598.8	3332
900	Error	-	(900)	Error	-	2221
1200	1200	1204.8	1200	1200	1198	832
1800	1800	1801.6	1800	1800	1802	555
2400	2400	2409.6	2400	2400	2410	416
3600	Error	-	(3600)	Error	-	277
(4000)	Error	-	4000	Error	-	249
4800	4800	4808	4800	4800	4808	207
(7200)	Error	-	7200	Error	-	138
9600	9600	9616	9600	9600	9616	207
14400	Error	-	14400	Error	-	138
-	Error	-	16000	Error	-	124
19200	19200	19232	19200	19200	19232	103

Table 4.1. Tested baud rates of the CH340 and CP2102 chips at lower baud speed

CH340G supported BaudRate	CH340G stty speed	CH340G measured BaudRate	CP2102 supported BaudRate	CP2102 stty speed	CP2102 measured BaudRate	AVR UBBR @16MHz
28800	Error	-	28800	Error	-	68
33600	Error	-	(33600)	Error	-	59
38400	38400	38.464k	38400	38400	38.464k	51
(51200)	Error	-	51200	Error	-	38, 0.16%
56000	Error	-	56000	Error	-	35, -0.79%
57600	57600	57.8k	57600	57600	57.472k	34, -0.79%
(64000)	Error	-	64000	Error	-	30, 0.80%
76800	Error	-	76800	Error	-	25, 0.16%
115200	115200	115.6k	115200	115200	114.96k	16, 2.12%
128000	Error	-	128000	Error	-	15, -2.34%
153600	Error	-	153600	Error	-	12, 0.16%
230400	230400	229.9k	230400	230400	229.9k	8, -3.54%
(25000)	Error	-	250000	Error	-	7, 0.00%
(25600)	Error	-	256000	Error	-	7, -2.34%
460800	460800	460.8k	460800	460800	458.7k	-, >5%
(500000)	500000	500.0k	500000	500000	500.0k	3, 0.00%
(576000)	576000	<b>543.4k</b>	576000	576000	571.4k	-, >5%
921600	921600	<b>851.2k</b>	921600	921600	921.6k	-, >5%
(1000000)	1000000	1000k	(1000000)	1000000	<b>921.6k</b>	1, 0.00%
(1200000)	Error	-	(1200000)	Error	-	-, >5%
1500000	1500000	1498k	(1500000)	1500000	1498k	-, >5%
2000000	2000000	2000k	(2000000)	2000000	<b>1504k</b>	0, 0.00%
(3000000)	3000000	3007k	(3000000)	2000000	-	-, >5%

Table 4.2. Tested baud rates of the CH340 and CP2102 chips at higher baud speed

In both tables you can see, that not all baud rates specified by the manufacturers are adjustable with the Linux stty command. In most cases an error is reported, but unfortunately not always. With the CP2102 converter the error limit is exceeded at the baud rates 1 MBaud and 2 MBaud. Even at the 576 kBaud rate the deviation is higher than expected. With the CH340G converter there are only two baud rate noticeable, the setting 576000 and 921600. All other baud selections have a uncritical tolerance. I have not searched for the reason of this abnormalities. But something is dubious with the documentation of the CH340G chip. We can select the baud rate 500 kBaud and 1 MBaud, which should be impossible according to the documentation.

## 4.2 The PL-2303 and the FT232R converter

This time I have tested a board with the label "SBT5329" and the PL-2303RX converter from Proflic Technology and a board "FTDI Basic 1" with a FT232RL converter from Future Technology Devices.

The SBT5329 board has a USB-A plug at one side and a 5-pin strip with the signals +5V, GND, RXD, TXD, and 3.3V at the opposite side. Additionally you can find a 12 MHz crystal and three LEDs Tx, Rx and power. The control signals of the serial interface are not routed to the strip at this board. But the PL-2303 chip provide the handshake signals of the serial interface.

The FTDI Basis 1 board has a USB-B plug at one side and at the opposite side a 6-pin strip with the signals GND, CTS, 5V, TXD, RXD and DTR. Only a few parts can be found at the



board additional to the FT232RL chip. But two LEDs for Tx and Rx are also present.

As with the other two boards, the devices are properly recognized by Linux Mint 17.1:

```
Bus 002 Device 095: ID 067b:2303 Prolific Technology, Inc. PL2303 Serial Port
```

```
Bus 002 Device 076: ID 0403:6001 Future Technology Devices International, Ltd FT232 Serial
```

So the devices are shown with the command `lsusb`. With the command `"dmesg | tail -20"` you can get directly after plug in a similar result as:

```
usb 2-4.5: new full-speed USB device number 95 using ohci-pci
usb 2-4.5: New USB device found, idVendor=067b, idProduct=2303
usb 2-4.5: New USB device strings: Mfr=1, Product=2, SerialNumber=0
usb 2-4.5: Product: USB-Serial Controller
usb 2-4.5: Manufacturer: Prolific Technology Inc.
pl2303 2-4.5:1.0: pl2303 converter detected
usb 2-4.5: pl2303 converter now attached to ttyUSB1
```

or rather

```
usb 2-4.3: new full-speed USB device number 96 using ohci-pci
usb 2-4.3: New USB device found, idVendor=0403, idProduct=6001
usb 2-4.3: New USB device strings: Mfr=1, Product=2, SerialNumber=3
usb 2-4.3: Product: FT232R USB UART
usb 2-4.3: Manufacturer: FTDI
usb 2-4.3: SerialNumber: A50285BI
ftdi_sio 2-4.3:1.0: FTDI USB Serial Device converter detected
usb 2-4.3: Detected FT232RL
usb 2-4.3: Number of endpoints 2
usb 2-4.3: Endpoint 1 MaxPacketSize 64
usb 2-4.3: Endpoint 2 MaxPacketSize 64
usb 2-4.3: Setting MaxPacketSize 64
usb 2-4.3: FTDI USB Serial Device converter now attached to ttyUSB0
```

In the table 4.3 the baud setting for the FT232R converter is tested below 300 baud, which can not be solved by the chip. But the `stty` command accept these settings without an error message. Of course the resulting baud rate is incorrect for these settings.

PL2303 supported BaudRate	PL2303 stty speed	PL2303 measured BaudRate	FT232R supported BaudRate	FT232R stty speed	FT232R measured BaudRate	AVR UBBR @16MHz
75	75	75.18	(75)	75	<b>415</b>	
(110)	110	109.9	(110)	110	<b>278</b>	
(134)	134	135.1	(134)	134	<b>502</b>	
150	150	149.8	(150)	150	<b>832</b>	
300	300	300.7	300	300	300.72	
600	600	602.4	600	600	602.4	3332
(900)	Error	-	900	Error	-	2221
1200	1200	1204.8	1200	1200	1212	832
1800	1800	1801.6	1800	1800	1809.6	555
2400	2400	2409.6	2400	2400	2424	416
3600	Error	-	3600	Error	-	277
4800	4800	4808	4800	4800	4831	207
7200	Error	-	7200	Error	-	138
9600	9600	9616	9600	9600	9664	207
14400	Error	-	14400	Error	-	138
19200	19200	19232	19200	19200	19320	103

Table 4.3. Tested baud rates of the PL-2303 and FT232R chips at lower baud speed

In the table 4.4 the baud setting for the FT232R converter are done correctly, when the stty command report no error. I don't know the reason, why some baud rates are not accepted by the stty command for the FT232R chip. Only the 576000 setting can be solved more exactly by the chip than done here.

PL2303 supported BaudRate	PL2303 stty speed	PL2303 measured BaudRate	FT232R supported BaudRate	FT232R stty speed	FT232R measured BaudRate	AVR UBBR @16MHz
28800	Error	-	28800	Error	-	68
(33600)	Error	-	33600	Error	-	59
38400	38400	38.464k	38400	38400	38.6k	51
(51200)	Error	-	51200	Error	-	38, 0.16%
(56000)	Error	-	56000	Error	-	35, -0.79%
57600	57600	57.8k	57600	57600	57.8k	34, -0.79%
(64000)	Error	-	64000	Error	-	30, 0.80%
(76800)	Error	-	76800	Error	-	25, 0.16%
115200	115200	115.6k	115200	115200	115.6k	16, 2.12%
(128000)	Error	-	128000	Error	-	15, -2.34%
(153600)	Error	-	153600	Error	-	12, 0.16%
230400	230400	231.2k	230400	230400	231.2k	8, -3.54%
(250000)	Error	-	250000	Error	-	7, 0.00%
(256000)	Error	-	256000	Error	-	7, -2.34%
460800	460800	460.8k	460800	460800	465.1k	-, >5%
(500000)	500000	500.0k	500000	500000	500.0k	3, 0.00%
(576000)	Error	-	576000	576000	<b>588.24k</b>	-, >5%
921600	921600	925.6k	921600	921600	930.4k	-, >5%
(1000000)	1000000	1000k	1000000	1000000	1005k	1, 0.00%
(1200000)	Error	-	1200000	Error	-	-, >5%
(1500000)	Error	1482k	1500000	1500000	1509k	-, >5%
(2000000)	2000000	2010k	2000000	2000000	2020k	0, 0.00%
(3000000)	3000000	3007k	3000000	3000000	3007k	-, >5%

Table 4.4. Tested baud rates of the PL-2303 and FT232R chips at higher baud speed

### 4.3 The USB-serial converter with the ATmega16X2 software

At some Arduino UNO boards a ATmega16X2 is used as USB-serial converter. Therefore I would like to test this board for selectable baud rates. At the first table 4.5 for the lower baud speeds is remarkable, that baud rates below 600 are accepted by the stty command without error messages. But all baud rates above 600 are implemented correctly.

Mega16X2 supported BaudRate	Mega16X2 stty speed	Mega16X2 measured BaudRate	AVR UBBR @16MHz
75	75	<b>956</b>	
110	110	<b>1120</b>	
134	134	<b>757.6</b>	
150	150	<b>1914</b>	
300	300	<b>778</b>	
600	600	599	3332
900	Error	-	2221
1200	1200	1198	832
1800	1800	1802	555
2400	2400	2395	416
3600	Error	-	277
4800	4800	4808	207
7200	Error	-	138
9600	9600	9616	207
14400	Error	-	138
19200	19200	19232	103

Table 4.5. Tested baud rates of the ATmega16X2 at lower baud speed

At the table 4.6 for the upper baud speeds you can see, that not all settings without error message are implemented correctly. Of course a better feedback of the stty command would be desirable to let us know, if a baud rate is selectable or not.

Mega16X2 supported BaudRate	Mega16X2 stty speed	Mega16X2 measured BaudRate	AVR UBBR @16MHz
28800	Error	-	68
33600	Error	-	59
38400	38400	38.321k	51
51200	Error	-	38, 0.16%
56000	Error	-	35, -0.79%
57600	57600	58.82k	34, -0.79%
64000	Error	-	30, 0.80%
76800	Error	-	25, 0.16%
115200	115200	116.9k	16, 2.12%
128000	Error	-	15, -2.34%
153600	Error	-	12, 0.16%
230400	230400	221.0k	8, -3.54%
250000	Error	-	7, 0.00%
256000	Error	-	7, -2.34%
(460800)	460800	<b>500.0k</b>	-, >5%
500000	500000	500.0k	3, 0.00%
(576000)	576000	<b>667k</b>	-, >5%
(921600)	921600	<b>995.0k</b>	-, >5%
(1000000)	1000000	1000k	1, 0.00%
(1200000)	Error	-	-, >5%
(1500000)	Error	<b>2000k</b>	-, >5%
2000000	2000000	2000k	0, 0.00%
(3000000)	3000000	<b>2000k</b>	-, >5%

Table 4.6. Tested baud rates of the ATmega16X2 at higher baud speed

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