EE-313 Lab Preliminary Report 4

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1. **Introduction:**

Aim of this lab is designing a Wide-Band Amplifier with Feedback circuit. It consist of two amplification stage and it gives a flat gain with low output-impedance. Specifications are as follows:

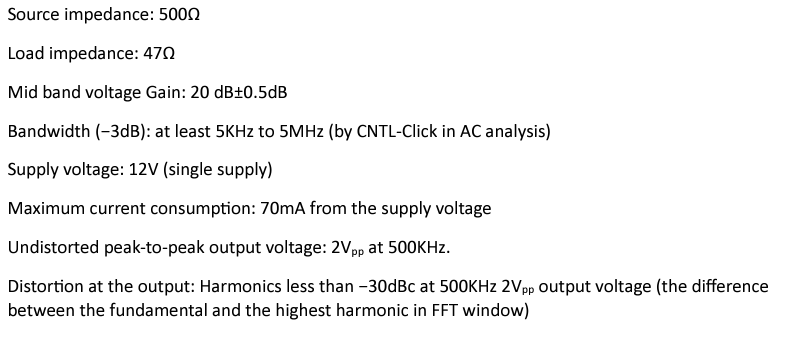


Fig. 1: Specifications

1. **LTspice Implementation:**

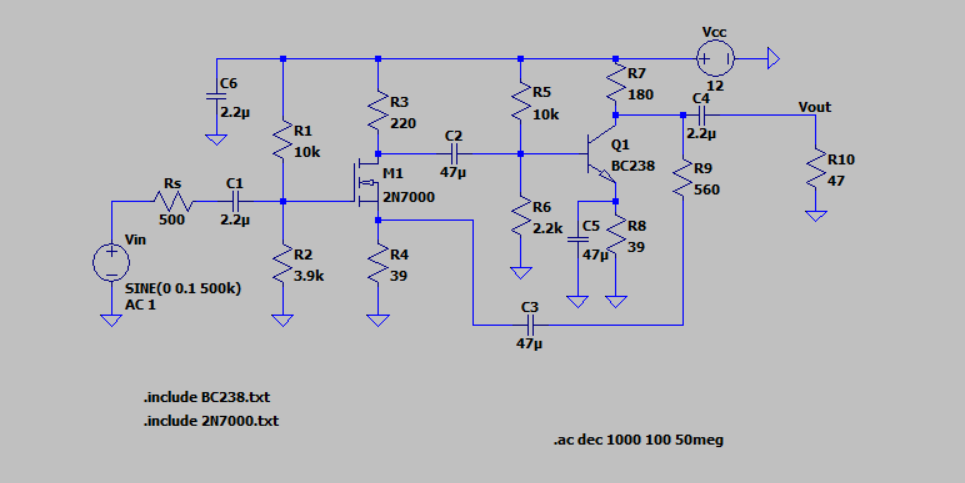
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Fig. 2: Implemented circuit

In order to achieve low output-impedance, I used voltage feedback circuitry. I used an NMOS transistor in series with BJT. Since output impedance is lower than the initial value seen by the circuit, I allocated more current to the Q1. Current of M1 is 30mA and Q1 is 35mA. I adjusted the values so that the source and emitter voltages are about 1V as suggested. I adjusted values so that which gives the 30mA current through the drain. I used the following formula with the datasheet of 2N7000 to calculate the ratio:

A similar procedure applied to Q1 to achieve necessary biasing conditions. adjusted so current through it is times smaller (1.01 mA obtained) than the 31.15 mA which flows through the . I choose to obtain 20dB gain. are calculated as below to obtain DC block capacitor which are nearly have no effect after and about 5kHz frequency range. I have calculated the threshold value of from . As seen in Fig. 2, my circuit has 500Ω source impedance, 47Ω load impedance, and has the 12V supply voltage.

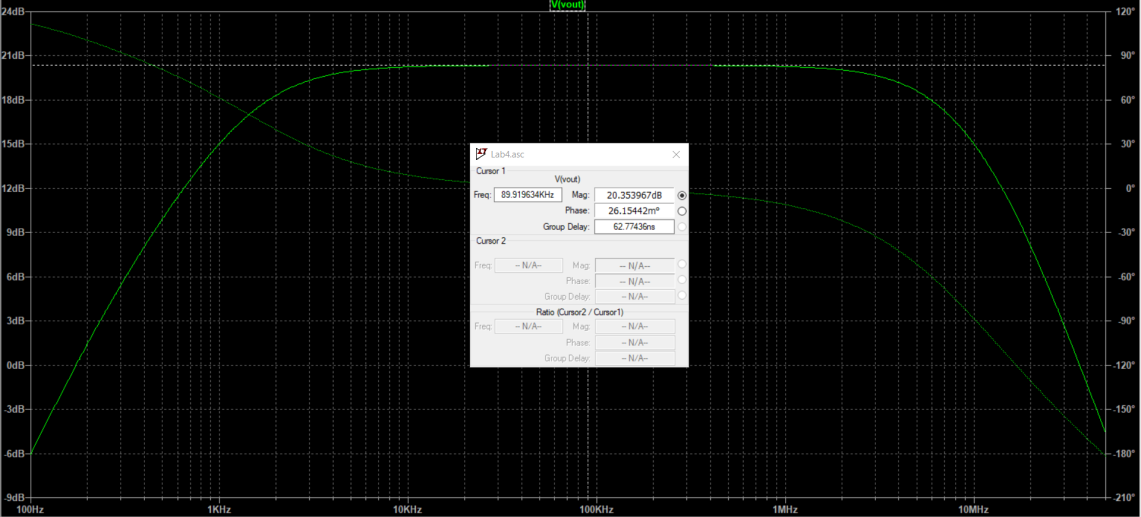


Fig. 3: Gain for different frequencies

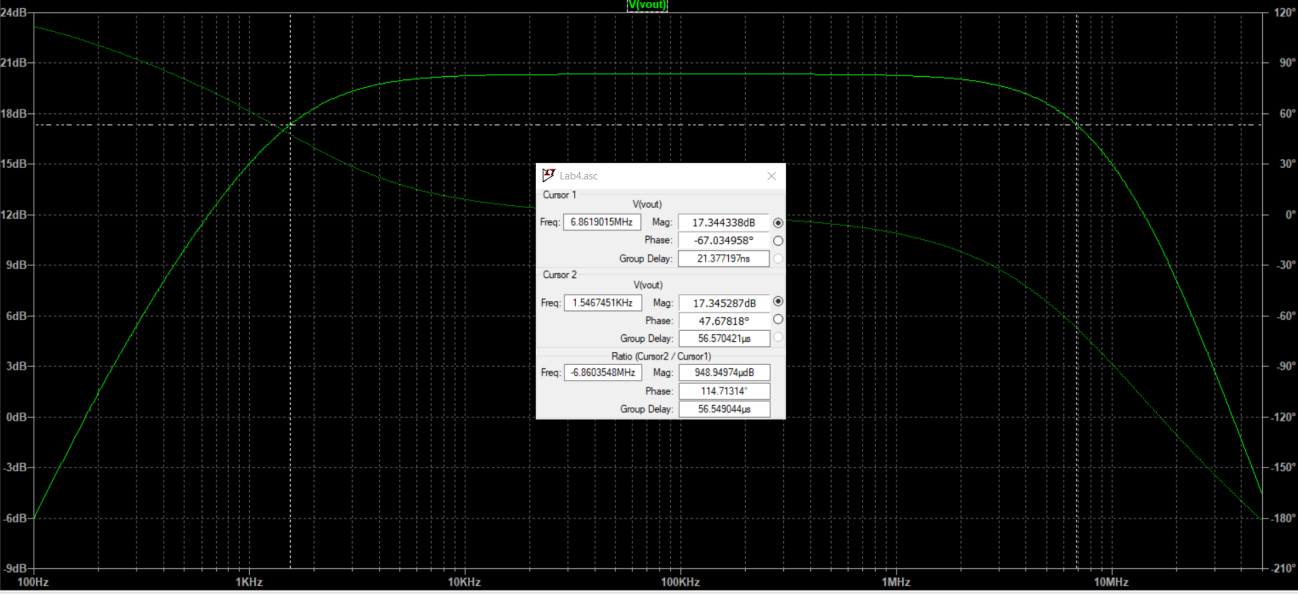


Fig. 4: Band-with of the gain

As seen in Fig. 3, the voltage gain of the circuit is 20.35dB. Corner frequencies are at 1.55kHz and 6.86 MHz which are less than 5kHz and greater than 5MHz, which can be seen in Fig1 4. Hence band-with specification is achieved.

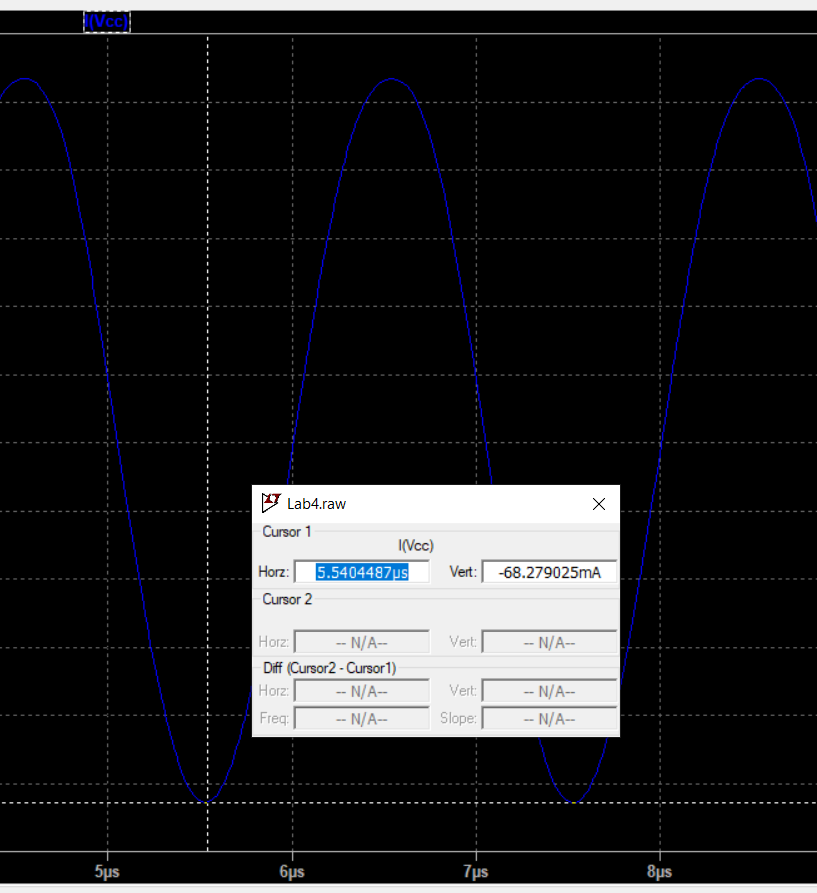


Fig. 5: Current consumption at 500kHz frequency

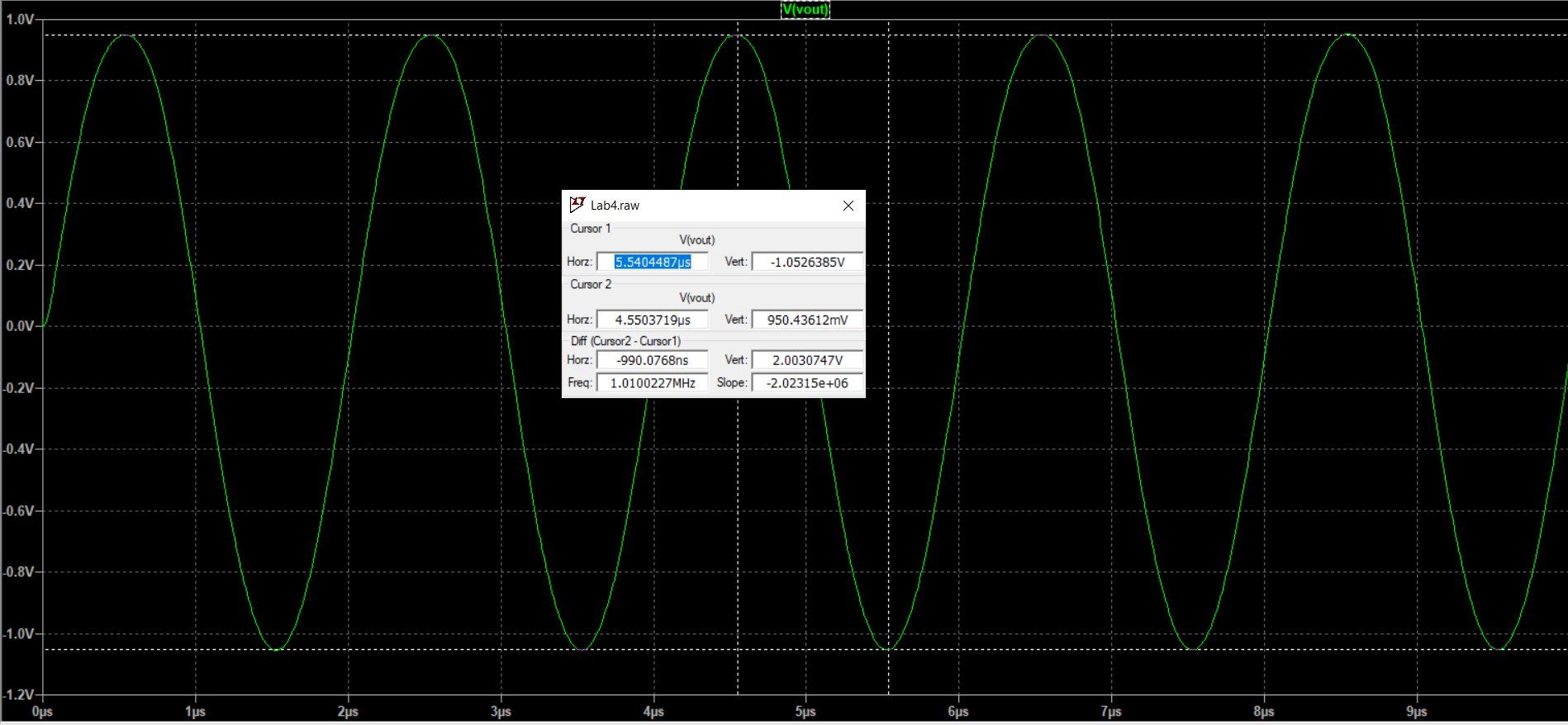


Fig. 6: at the 500kHz

As seen in Fig. 5 and 6, maximum current consumption is 68.27mA which is less than 70mA and which satisfies the corresponding specifications..

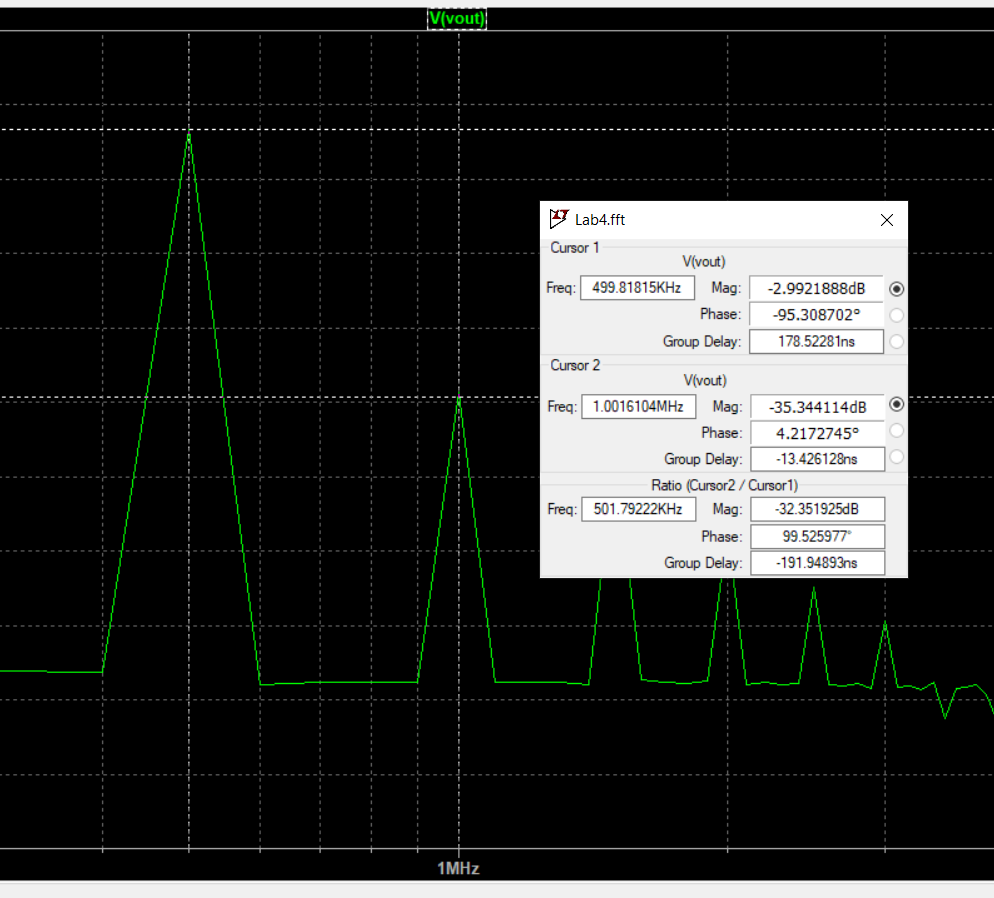
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Fig. 7: FFT analysis

Fig. 7 shows that the difference between fundamental component of the output voltage and second highest harmonic is which meets the specification as well.

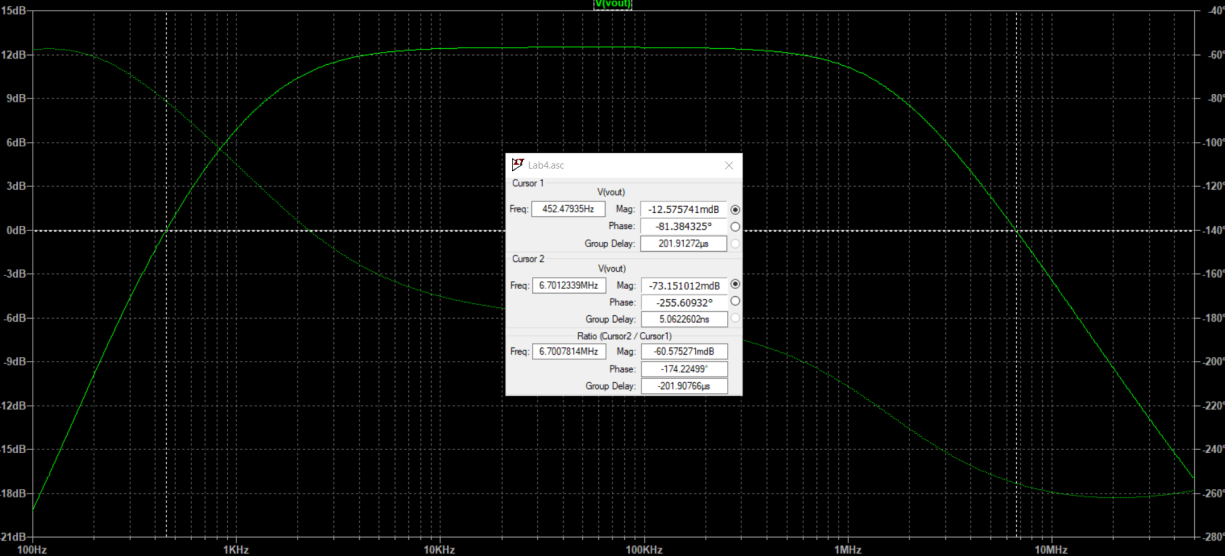


Fig. 8: The phase margin of the open-loop system

Fig. 8 presents that phase margin for 6.7MHz, which is the unity gain point, is .

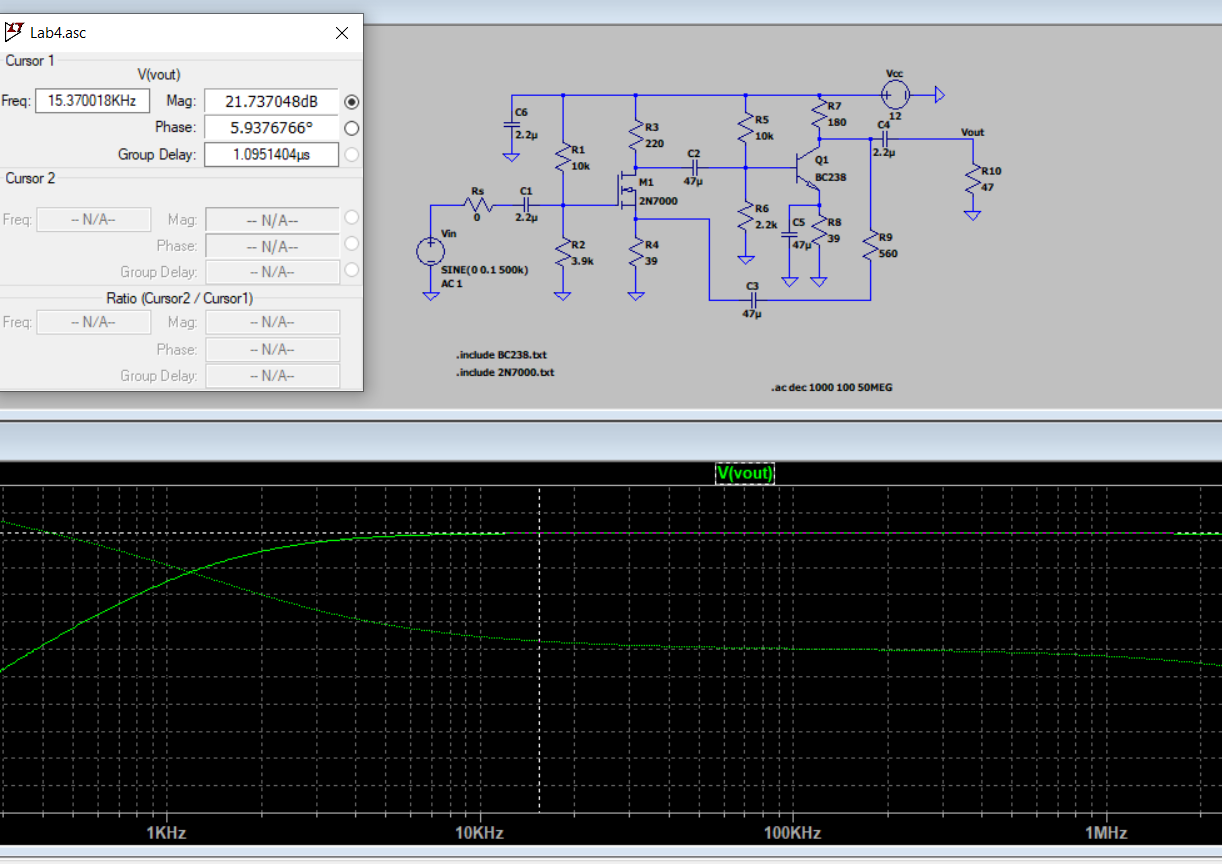


Fig. 9: Gain with

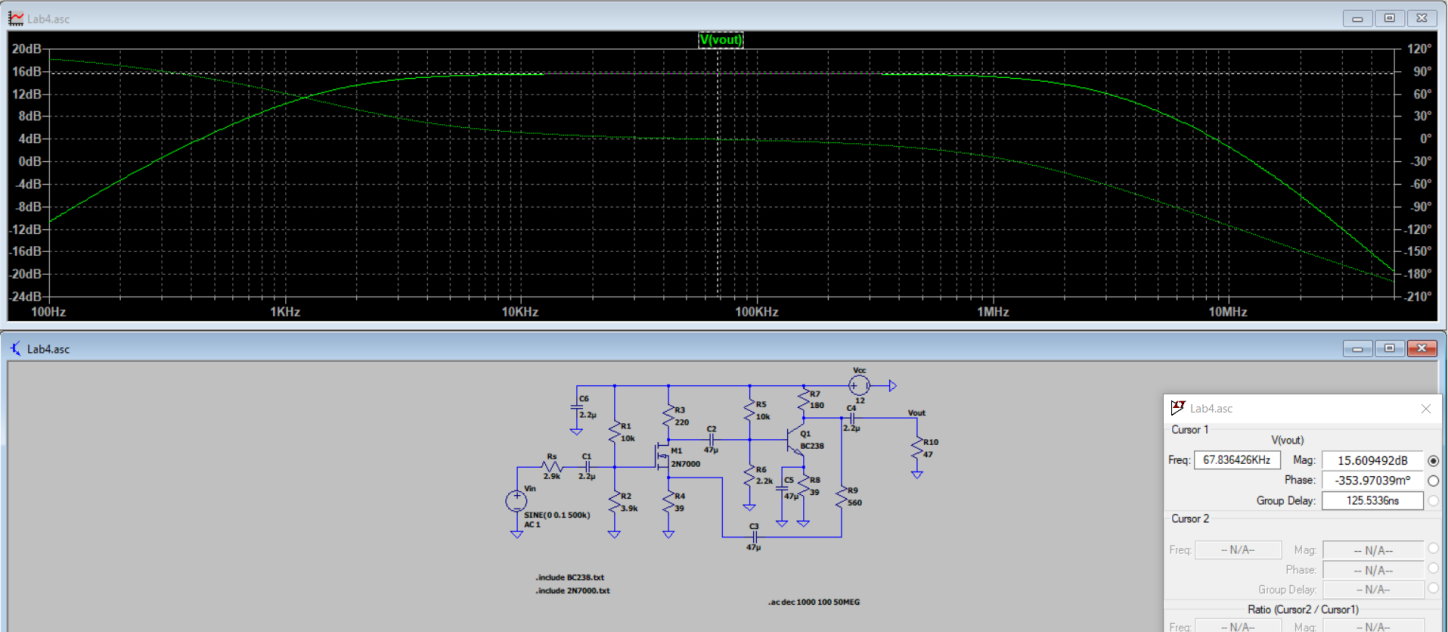


Fig. 10: 6dB lower gain with

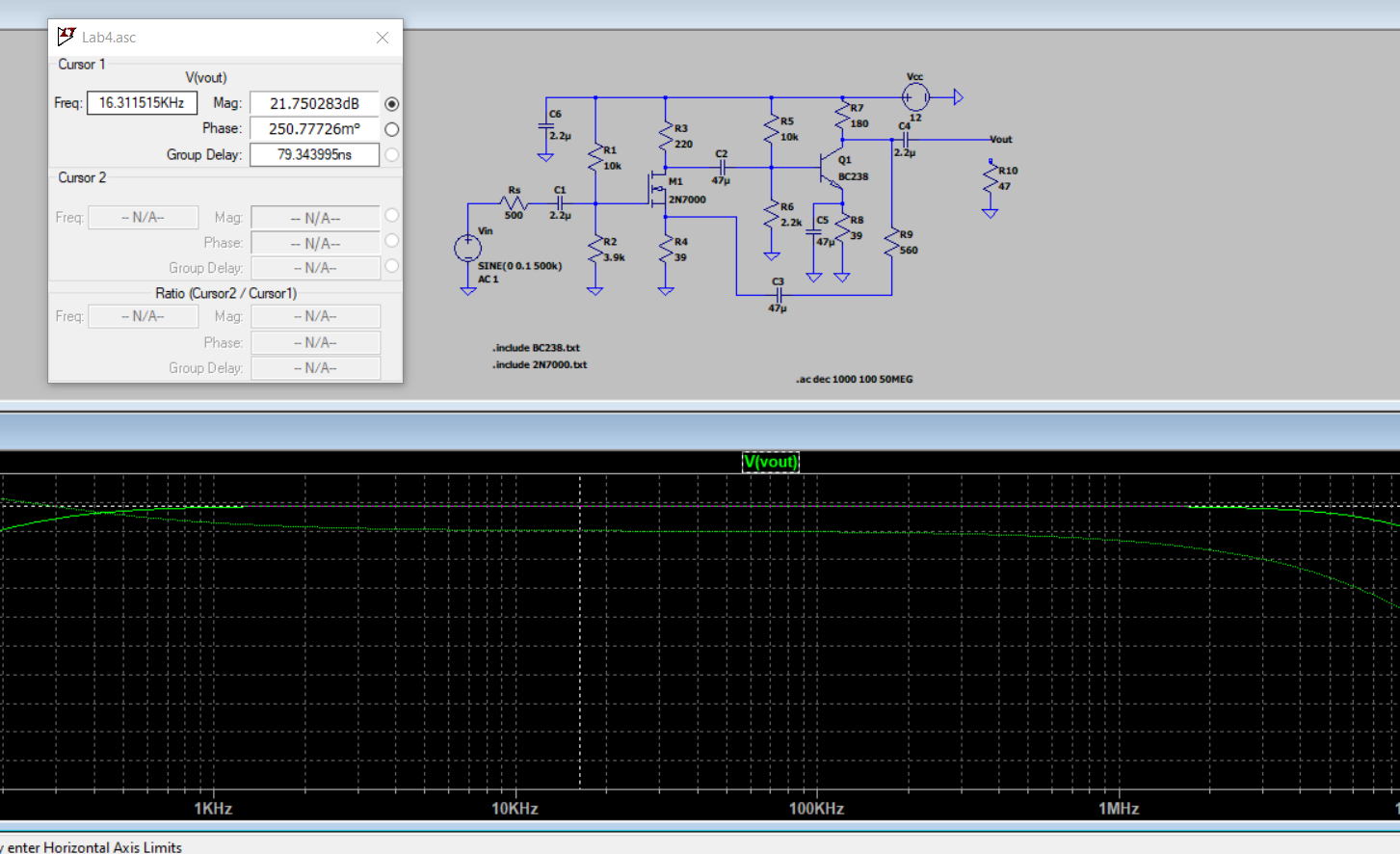


Fig. 11: Gain with

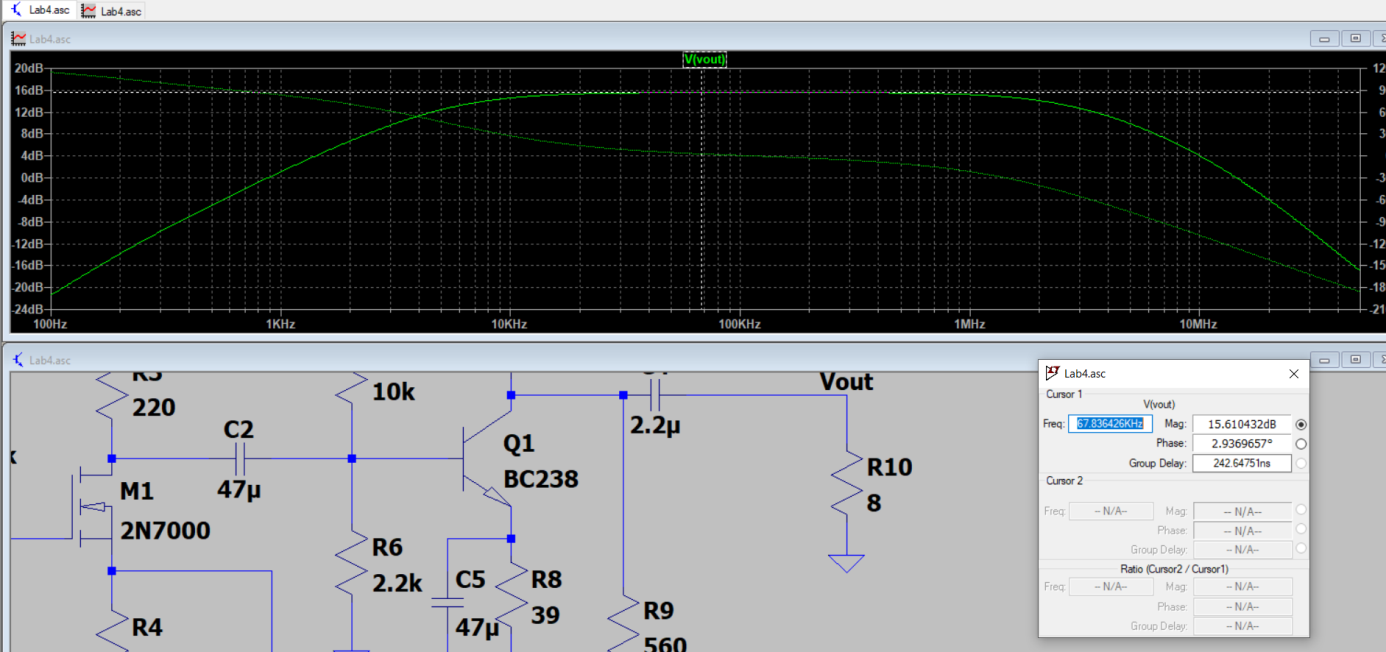


Fig. 12: Gain with

In Fig. 9 and 10, input impedance is found as 2.9kΩ and in Fig. 11 and Fig. 12, output impedance found as 8Ω. Impedance is seen 6 times higher than the actual value and output impedance is 6 times smaller than the actual value. You can see the Diptrace schematic in following page. All specifications achieved and calculations are done.

* 1. **Diptrace Schematic:**

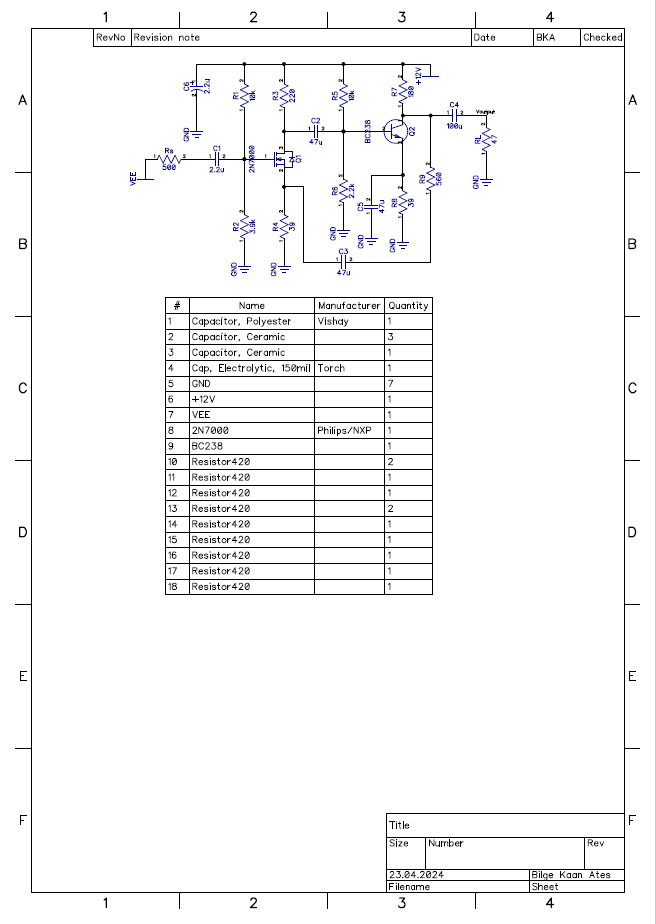
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Fig. 10: Diptrace Schematic