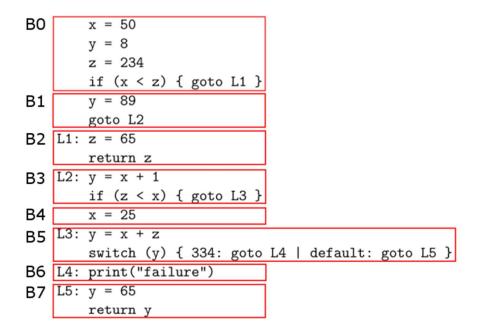
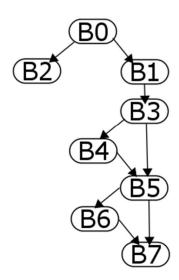
Assignment 1 Write-Up

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3.1





ВВ	Gen	Kill	In	Out
1	b+c	b+c	Empty	c+d
	c+d			a*b
	a*b			
2	i+d	c+d	c+d	i+d
	c+d	a*b	a*b	c+d
3	b+d	a+d	i+d	i+d
			c+d	c+d
				b+d
4	b*b	Empty	i+d	b*b
	b+d		c+d	b+d
				c+d
				i+d
5	Empty	i+2	i+d	i+d
			c+d	c+d
			b+d	b+d

3.3

- 1. Variables
- 2. Backwards analysis
- Out[B] = U In[s], s ∋ Succ[B]
 In[B] = Out[B] (Control[B] + Relevant[B])
 Relevant[B] = variables used to define LHS ∉ Out[B] | Control[B]
- 4. Union
- 5. ENTRY is initialized to the bottom of the call graph, and EXIT is initialized to the top.
- 6. OUT is initialized to a bit vector of all zeros, IN is uninitialized.
- 7. Block traversal will not impact correctness, but post-order traversal will reduce the number of iterations to find a fixed-point solution because predecessors will not need to be analyzed again after their successors, since faint variables in their successors will be determined first.
- 8. The analysis will converge because once variables are removed from the faint set, they are never returned. Without returning variables to the faint set, there is only ever a finite number of variables to analyze, so at some point the analysis will converge on faint/not faint values for every expression.
- 9. The following pseudo code assumes that a bit vector the length of the total number of variables in the program is initialized to all zeros, where zero indicates that the variable is faint. Further, "is control instruction" refers to all control flow instructions as well as function calls and function returns. For each instruction, the LHS (left hand side) of the instruction, the variable being defined, is checked and if it is not faint, then the variables used to define the LHS are also set to NOT FAINT in the bit vector.