523.01 초기 initialization 에서 setting해주어야 하는 register 및 Sequence!!(SPI)

- **CLKCTRL(0x01)** ➔ 외부 clock사용하지 않을경우 don't care!! (제일 먼저 setting해주어야함!!)
- **WDCTRL(0x10)** ➔ Watchdog setting (page3)
- **VREGCTRL(0x07)** ➔ 3.3V & VG/VCC on = **0x03** (page 4)
- **BRIDGEMODE(0x20)** ➔ BLDC motor 구동 (Inverter switching) & MCU deadtime = **0x3F** (page 5)
- **GATECFG1/2/3(0x21/22/23)** ➔ MCU 에서 직접 H-side/L-side switch 제어하려면 **0x12**로 setting해주면 됨! (page 6)
- **DEADTIME_LH/HL(0x24/25)** ➔ MCU에서 deadtime 사용할 경우 0으로 setting하면 됨!! (page 7)
- **SCTH(0x26)** ➔ Drain –Source short circuit detection threshold & Mask time 설정!! (page 8,9)
- **SCPCTRL(0x0B)** ➔ VDS short circuit detection 이 되었들때의 Fault reaction 설정 !! (9)
- **AMUX(0x17)/CMUX(0x18)/ DMUX(0x19)** ➔ (page 10,11)
- **IOCOMPTHR(0x16)** ➔ Comparator threshold!! (page 12)
- **IOCFG(0x06)** ➔ LIN안쓰고, PWM duty measurement 안쓰고, interrupt pin 사용할 경우 ➔ **0x03**(interrupt pin = VSEL) or **0x01**(interrupt pin = SO pin) (page 13)
- **CHIPCTRL(0x02)** ➔ Sleep mode에서 Wake-up 을 위한 configuration(page 14)
- **IRQMSK1/2(0x12/14)** ➔ Interrupt Mask register!! Interrupt 발생 원하는 function enable해줌!! (page 15)
- **SAFECTRL(0x05)** ➔ safety 관련 function 설정 (table 6.24,25 참조!!) (page 16)
- **SECURCTRL(0x04)** ➔ 이 register의 ESECURE(0bit)가 set 되기 전에 restricted register의 값을 먼저 define 해주어야 함!! (이후에는 register값 변경 안됨!!)
  이 register 자체도 ESECURE(0bit) 을 enable 하기 전에 setting 해주고 이후에 ESECURE(0bit) 을 set 한후 한번더 써주어야 함 (page 17,18)
- **IRQSTAT1/2(0x13/15)** ➔ Sequence 마지막에 interrupt status register clear(0xff)해주는 것을 recommend함!!

<그외 register>
SLEEPCTRL(0x03) ➔ sleep mode 진입시 사용
PWM_LH/HL(0x09/0A) ➔ PWM interface 사용시 duty 값을 나타내는 register (PWM Interface 사용을 위해서는 external clock 필요, mcu의 input capture 기능 사용하는것 추천함!!)

<Example in real code>

StartSpi1Tx(Address , target value);

```
StartSpi1Tx(0x01,0x77); //CLKCTRL
StartSpi1Tx(0x10,0x00); //WDCTRL
StartSpi1Tx(0x07,0x03); //VREGCTRL
StartSpi1Tx(0x20,0x3F); //BRIDGEMODE
StartSpi1Tx(0x21,0x12); //GATECFG1
StartSpi1Tx(0x22,0x12); //GATECFG2
StartSpi1Tx(0x23,0x12); //GATECFG3
StartSpi1Tx(0x24,0x00); //DEADTIME_LH
StartSpi1Tx(0x25,0x00); //DEADTIME_HL
StartSpi1Tx(0x26,0x32); //SCTH
StartSpi1Tx(0x0B,0x11); //SCPCTRL
StartSpi1Tx(0x17,0x00); //AMUX
StartSpi1Tx(0x18,0x00); //CMUX
StartSpi1Tx(0x19,0x00); //DMUX
StartSpi1Tx(0x16,0x3F); //IOCOMPTHR
StartSpi1Tx(0x06,0x03); //IOCFG
StartSpi1Tx(0x02,0x07); //CHIPCTRL
StartSpi1Tx(0x12,0xFF); //IRQMSK1
StartSpi1Tx(0x14,0x0F); //IRQMSK2
StartSpi1Tx(0x05,0x00); //SAFECTRL
StartSpi1Tx(0x04,0x14); //SECURCTRL (ESECURE(0bit) = 0)
StartSpi1Tx(0x04,0x15); //SECURCTRL (ESECURE(0bit) = 1)
StartSpi1Tx(0x13,0xFF); //IRQSTAT1
StartSpi1Tx(0x15,0xFF); //IRQSTAT2
```

6.5.2 Watchdog

There are two watchdogs available:

- Register watchdog: standard or window watchdog for monitoring of the external microcontroller
- CLK watchdog: monitoring of the CLK input clock signal

*Table 6.30: Register **WDCTRL** (0x10), watchdog control*

	MSB							LSB
Content	WDUSECW	PINTRIG	WDTOW1	WDTOW0	WDFOW	WDTEST	REG-WDEN	CLKWDEN
Reset value	1	0	1	1	-	-	1	1
Internal access	R	R	R	R	W	W	R	R
External access	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Bit Description	**WDUSECW:** Use closed window for register watchdog ($WD_{T,CW}$) **PINTRIG:** 1: Register watchdog is triggered on PWML3 rising edge, 0: Register watchdog is triggered via WDTRIG register (SPI access) **WDTOW[1:0]:** Register watchdog open window time ($WD_{T,OW}$) **WDFOW:** Register watchdog is in first open window **WDTEST:** 1: Register watchdog is stopped (T pin = 'H'), 0: Register watchdog is running **REGWDEN:** Enable register watchdog **CLKWDEN:** Enable CLK watchdog							

For debugging purposes and software upload only, the watchdog can be stopped by setting T pin to VCC level.

6.5.2.1 Register Watchdog

The register watchdog can be configured in WDCTRL register within the first open window. It can be triggered by SPI access to WDTRIG register or a rising edge at PWML3 input pin.

Standard watchdog (WDUSECW = 0): The next trigger command has to be sent within $WD_{T,OW}$.

Window watchdog (WDUSECW = 1): The next trigger command has to be sent after $WD_{T,CW}$ and before $WD_{T,CW}$ + $WD_{T,OW}$.

*Table 6.31: Register **WDTRIG** (0x11), watchdog trigger*

	MSB							LSB
Content	-	-	-	-	-	-	-	TRIG
Reset value	0	0	0	0	0	0	0	0
Internal access	-	-	-	-	-	-	-	R
External access	R	R	R	R	R	R	R	R/W
Bit Description	**TRIG:** Value has to be toggled on each write access in order to trigger the watchdog							

Watchdog 이 enable 되었을 경우 SPI를 통해서 WDTRIG.TRIG data를 toggle시켜가면 Writing해주면 됨!!!

Table 4.17: Watchdog parameters [1)]

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Register watchdog first open window time		$WD_{T,FOW}$	230	256	282	ms
Register watchdog closed window time	WDCTRL[7] = 1	$WD_{T,CW}$	5.4	8	8.8	ms
Register watchdog open window time	WDCTRL[5:4] = 3	$WD_{T,OW}$	115	128	143	ms
	WDCTRL[5:4] = 2		57	64	73	ms
	WDCTRL[5:4] = 1		28	32	38	ms
	WDCTRL[5:4] = 0		14	16	20	ms
CLK watchdog detection time		$WD_{T,d,CLK}$	2	4	10	µs
Watchdog reset activation duration		$WD_{T,RES}$	200	400	1000	µs

[1)] *Watchdog parameters ATPG tested*

CLK input을 이용한 방법 or Watchdog register를 이용한 방법 2가지 선택가능
Watchdog register 방식인 경우
1. standard watchdog 방식 (Watchdog 주기 안에 아무때나 register clear해주면 됨!! ➔ WDUSECW = 0
2. window watchdog 방식 (한주기가 open window + close window로 이루어 졌으며, close window에서만 register clear해주어야 함!!) ➔ WDUSECW = 1

****초기 S/W 개발 단계에서 Watchdog이 구현이 안되어 있으면, VCC가 주기적으로 reset되면서 MCU에 원활한 전원공급이 되지 않음(downloading 안될수 있음)**
따라서 S/W 개발 단계에서는 T pin을 high level로 만들어 줘서 test mode(watchdog 무시) 로 구동되도록 해주어야 함!!

*Table 6.1: Register **VREGCTRL** (0x07), VCC and VG supply control*

	MSB							LSB
Content	-	-	-	-	VCC_SON	VSEL	VGON	VCCON
Reset value	0	0	0	0	0	0	0	1
Internal access	-	-	-	-	R	R	R	R
External access	R	R	R	R	R/W	R/W	R/W	R/W
Bit Description	**VCC_SON:** 1: VCC is connected to VDD in sleep mode internally, if VSEL = 'L' 0: VCC is off in sleep mode **VSEL:** Confirmation of VSEL level: 1: µC supply VCC is 5V, 0: µC supply VCC is 3.3V **VGON:** 1: Enable VG supply **VCCON:** 1: Enable VCC supply							

VDD 전압이 3.3V 이기 때문에 VCC가 3.3V 일때만 이 Function 적용 가능함!!

In sleep mode, the VCC regulator is switched off. If setting VCC_SON bit in VREGCTRL register, VCC pin is connected to the internal 3.3V supply VDD (VCC in 3.3V mode only). Then the output current is limited to 300µA. An overload leads to IC and microcontroller reset and restart.

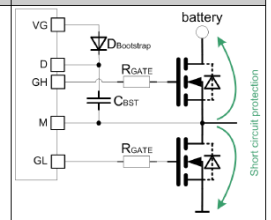
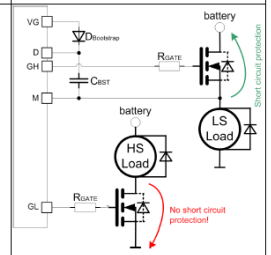
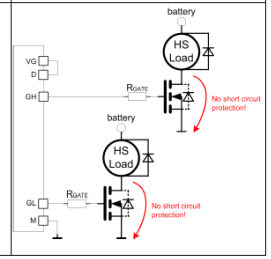
***Note:** If VCC is supplied in sleep mode, all input pins should have pull resistances externally to avoid increased current consumption.*

*Table 6.18: Register **BRIDGEMODE** (0x20), bridge mode configuration*

	MSB							LSB
Content	-	ASYNC	DM31	DM30	DM21	DM20	DM11	DM10
Reset value	0	0	0	0	0	0	0	0
Internal access	-	R	R	R	R	R	R	R
External access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**ASYNC:** 1: PWMH1-3 and PWML1-3 are not synchronized (CLK input clock does not have to be applied), cross current protection disabled 0: PWMH1-3 and PWML1-3 are synchronized, CLK input clock must be applied for internal dead time generation **DM3[1:0]:** Phase 3 driver mode, see below for coding **DM2[1:0]:** Phase 2 driver mode, see below for coding **DM1[1:0]:** Phase 1 driver mode, see below for coding							

ASYNC = 0일 경우 CLK입력이 꼭 필요하며, IC가 자체적으로 Low side switch를 high side와 반대로 on/off 함. 이때 dead time도 자체적으로 생성 가능!!!
ASYNC = 1 일 경우, 외부 MCU에서 모터 구동을 위한 PWM 및 deadtime 생성해서 주면 됨!!

Table 6.20: Gate driver applications

Divergent usage of half bridge	Application	DM (BRIDGE-MODE register) requirement	GATECFG register recom-mendation	Depiction
Half bridge (stand-ard) ***Note:** recharge of bootstrap capacitor necessary*	BLDC, EC, DC motors	3	"0-0--0--"	
1 NMOS high side and 1 NMOS low side FET ***Note:** recharge of bootstrap capacitor necessary*	DC motors, other loads	2	"000xx0xx"	
2 NMOS low side FETs	DC motors, other loads	1	"000xx0xx"	

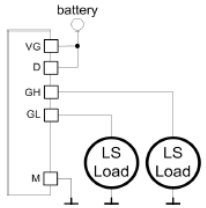
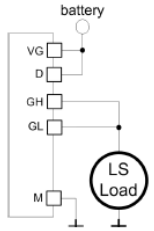
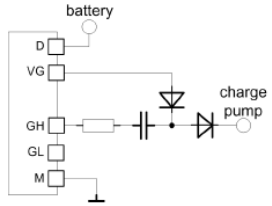
Divergent usage of half bridge	Application	DM (BRIDGE-MODE register) requirement	GATECFG register recom-mendation	Depiction
2 direct loads	Small motors, other loads	1	"00xxxxxx"	
1 direct load, reduced on-resist-ance	Small motors, other loads	1	"10xxxx--"	
Driving of external charge pump	Active high side reverse polarity pro-tection	1	"00010000"	
-	-	0	-	Disabled, GH and GL switched to ground

*Table 6.19: Register **GATECFG1-3** (0x21, 0x22, 0x23), motor phase gate driver control configuration*

	MSB							LSB
Content	GLSYNC	GLINV	GHHZ	GHPWM	GHLEVEL	GLHZ	GLPWM	GLLEVEL
Reset value	0	0	0	1	0	0	1	0
Internal access	R	R	R	R	R	R	R	R
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**GLSYNC:** Low side driver is controlled synchronous (non inverted) to high side driver (ignored if DM = 3) **GLINV:** Low side driver is controlled inverted to HS driver (ignored if DM != 3) **GHHZ:** Switch GH to high impedance **GHPWM:** Use PWMH input pin to control high side driver (ignored if GHHZ = 1) **GHLEVEL:** High side driver output level, if GHHZ = 0 and GHPWM = 0 (control via SPI possible) **GLHZ:** Switch GL to high impedance **GLPWM:** Use internal high side driver control to control low side driver (ignored if GLHZ = 1, depending on GLHZ, GLSYNC and GLINV), refer to **GLLEVEL:** Low side driver output level, if GLHZ = 0 and GLPWM = 0 (control via SPI possible) ***Note:** GLINV = 1 and GLSYNC = 1: driver off due to security reasons*							

BLDC 구동일때는 don't care

MCU를 이용해서 HS 직접 PWM 제어할 경우 1로 set!!

MCU를 이용해서 LS 직접 PWM 제어할 경우 1로 set!!

6.3.2.2 Dead Time Generation

The dead time between off-switching of the activated and on-switching of the opposite FET is programmable in DEADTIME_LH and DEADTIME_HL registers.

The dead time clock base is defined in CLKCTRL register:

$$T_{CLK,dead} = T_{CLK} \cdot (8 - CLKCTRL[6:4])$$

The dead time value calculation is:

case CLKCTRL[7] = 0: $t_{dead} = DEADTIME\_xx[5:0] \cdot T_{CLK,dead}$

case CLKCTRL[7] = 1: $t_{dead} = 0.5 \cdot DEADTIME\_xx[5:0] \cdot T_{CLK,dead}$

*Table 6.10: Register **DEADTIME_LH** (0x24), low to high transition dead time*

	MSB							LSB
Content	NEG	PARITY	D5	D4	D3	D2	D1	D0
Reset value	0	0	1	1	1	1	1	1
Internal access	R	R	R	R	R	R	R	R
External access	R/W	W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**NEG:** On-switching before off-switching of the correspondent power FET (negative dead time with D[5:0] value) ***Security warning:*** *Using small or negative dead times is on own risk due to the possibility of driver damage.* **PARITY:** Even register parity (write only, read as 0) **D[5:0]:** Dead time value.							

*Table 6.11: Register **DEADTIME_HL** (0x25), high to low transition dead time*

	MSB							LSB
Content	NEG	PARITY	D5	D4	D3	D2	D1	D0
Reset value	0	0	1	1	1	1	1	1
Internal access	R	R	R	R	R	R	R	R
External access	R/W	W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**NEG:** On-switching before off-switching of the correspondent power FET (negative dead time with D[5:0] value) ***Security warning:*** *Using small or negative dead times is on own risk due to the possibility of driver damage.* **PARITY:** Even register parity (write only, read as 0) **D[5:0]:** Dead time value.							

6.3.3 Short Circuit Protection

The drain source voltage of the external low side and high side power FETs in on-state are monitored by the IC. If the motor phase voltage M exceeds a programmable threshold, the gate driver switches the power FETs off immediately. Reference for the high side FETs is VBATS sense voltage, for the low side FETs ground.

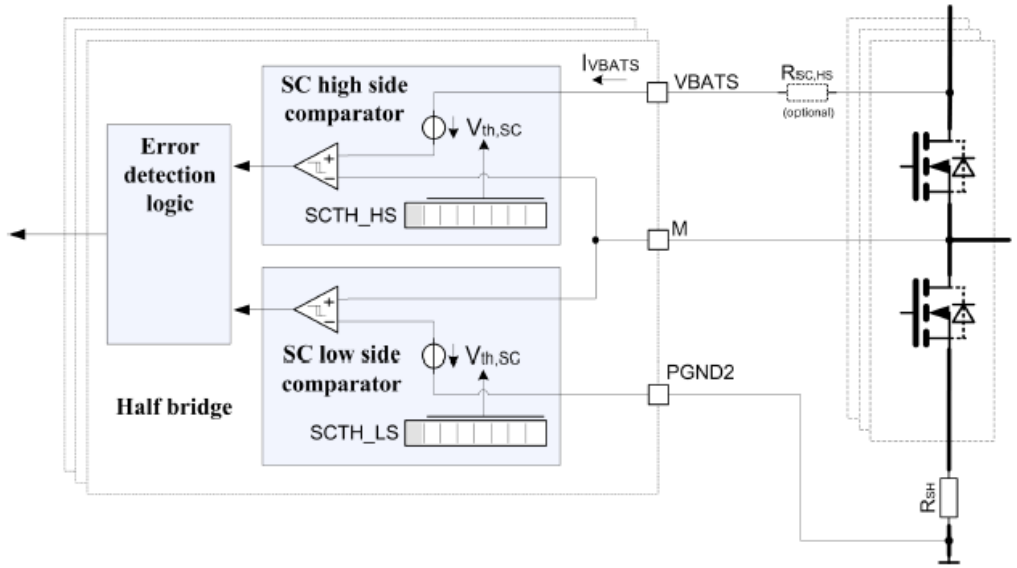
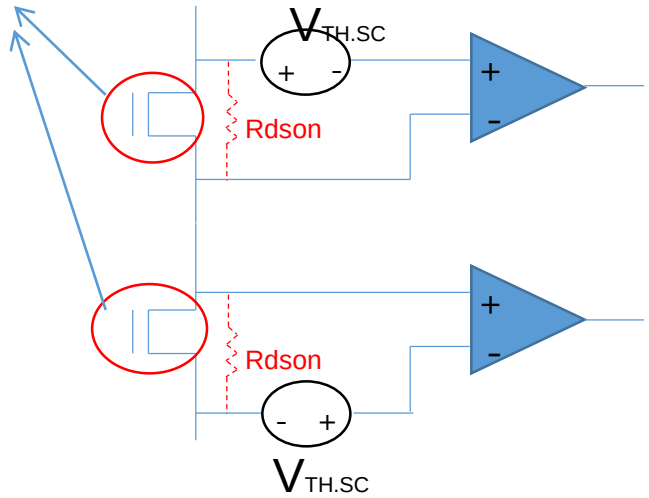


Figure 25: Short circuit protection block diagram

The thresholds of high side and low side power FETs are programmable in SCTH register in low resolution mode. If higher resolution is needed, registers SCTH_HS and SCTH_LS provide 80 equidistant steps derived from VDD voltage for both high side and low side independently. If one of these registers is written, SCTH[2:0] will be ignored for the corresponding side. The calculation of the threshold values is given in the following table.

Note: *It is mandatory to write SCTH register, since the short circuit masking time has to be adjusted. SCTH_HS and SCTH_LS registers have to be written after SCTH register access.*

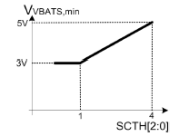
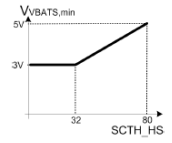
When FETs turn on, it could be Rdson.



Short circuit으로 over current 가 발생하여 Vds 전압이 Short circuit threshold voltage 이상으로 발생될 경우 Short circuit error detection.
Short circuit threshold voltage level은 외부 MCU에서 설정 가능함!

- Short circuit protection사용을 위해 유의할 점
  - VBATS 와 모터에 인가되는 전압이 같은 line이어야 함! (ex. VBATs 에는 battery 전압 연결하고 Motor 에는 diode를 지난 Vin 전압을 인가할 경우 두 전압간의 전압차로 인해 short circuit detection이 제대로 동작안할 수 있음!!!!)
  - PGND2 와 motor ground가 같은 line이어야 함!!(위와 같은 이유!!)
  - SCTH_HS/LS 에 값을 써 넣을 경우 기존에 써 넣었던 SCTH값은 무시됨!!!

Table 6.12: Short circuit threshold calculation

Mode	Mean value	Tolerance (+/-)	Minimum Battery Voltage
Low resolution	$\frac{SCTH[2:0]+1}{8}\cdot 3.3\text{V}$	$\frac{SCTH[2:0]+1}{8}\cdot 275\text{mV}+24\text{mV}$	
High resolution	$\frac{SCTH\_xS}{127}\cdot 3.3\text{V}$	$\frac{SCTH\_xS}{127}\cdot 275\text{mV}+24\text{mV}$	

Warning: *The short circuit threshold must be set carefully corresponding to power FET parameters and short circuit impedance. If the threshold is chosen too high, the short circuit protection may not work properly.*

After on-switching of the power FET the error detection is masked for a programmable time. The masking time is derived from the internal 1MHz oscillator:

$$t_{MT\_SC} = SCTH[6:4]\cdot 2\mu\text{s}$$

*Table 6.13: Register **SCTH** (0x26), short circuit threshold selection (low resolution mode) and masking time*

	MSB							LSB
Content	-	MT2	MT1	MT0	-	TH2	TH1	TH0
Reset value	0	0	0	0	0	0	0	0
Internal access	-	R	R	R	-	R	R	R
External access	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit Description	**MT[2:0]:** Short circuit initial masking time value **TH[2:0]:** Short circuit threshold value (0 … 4) Value 7 disables the short circuit detection (only for Ordering no. E52301Cxxx401)							

*Table 6.14: Register **SCTH_HS** (0x28), high side short circuit threshold selection (high resolution mode)*

	MSB							LSB
Content	-	D6	D5	D4	D3	D2	D1	D0
Reset value	0	0	0	0	1	1	1	1
Internal access	-	R	R	R	R	R	R	R
External access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**D[6:0]:** Short circuit threshold value (3 … 80). Write access to SCTH register resets this register. Value 127 disables the highside short circuit detection (only for ordering no. E52301Cxxx401)							

*Table 6.15:Register **SCTH_LS** (0x29), low side short circuit threshold selection (high resolution mode)*

	MSB							LSB
Content	-	D6	D5	D4	D3	D2	D1	D0
Reset value	0	0	0	0	1	1	1	1
Internal access	-	R	R	R	R	R	R	R
External access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**D[6:0]:** Short circuit threshold value (3 … 80). Write access to SCTH register resets this register. Value 127 disables the lowside short circuit detection (only for ordering no. E52301Cxxx401)							

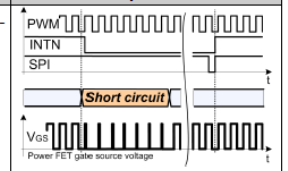
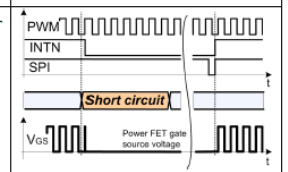
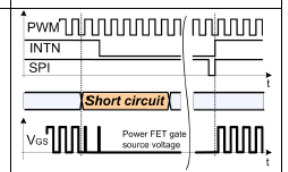
6.3.3.1 Superior Short Circuit Failure Reaction

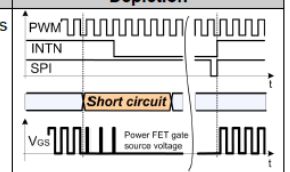
A superior reaction to a short circuit failure can be configured in SCPCTRL register.

*Table 6.16: Register **SCPCTRL** (0x0B), superior short circuit protection control*

	MSB							LSB
Content	-	-	-	SCALL	-	-	SCFCT1	SCFCT0
Reset value	0	0	0	0	0	0	0	0
Internal access	-	-	-	R	-	-	R	R
External access	R	R	R	R/W	R	R	R/W	R/W
Bit Description	**SCALL:** 1: Switch off all power FETs on short circuit, 0: Switch off only correspondent FET on short circuit **SCFCT[1:0]:** See following tabl							

Table 6.17: Superior short circuit protection behaviour

SCFCT[1:0]	Description	Depiction
0	Re-try of power FET switching at every rising edge of the correspondent input control. Interrupt is thrown after first short circuit failure detection	
1	Drivers remain off until interrupt is cleared by the microcontroller	
2	One re-try of power FET switching allowed, after that all drivers remain off until interrupt is cleared by the microcontroller	

SCFCT[1:0]	Description	Depiction
3	Two re-tries of power FET switching allowed, after that all drivers remain off until interrupt is cleared by the microcontroller	

INTN: low-active interrupt

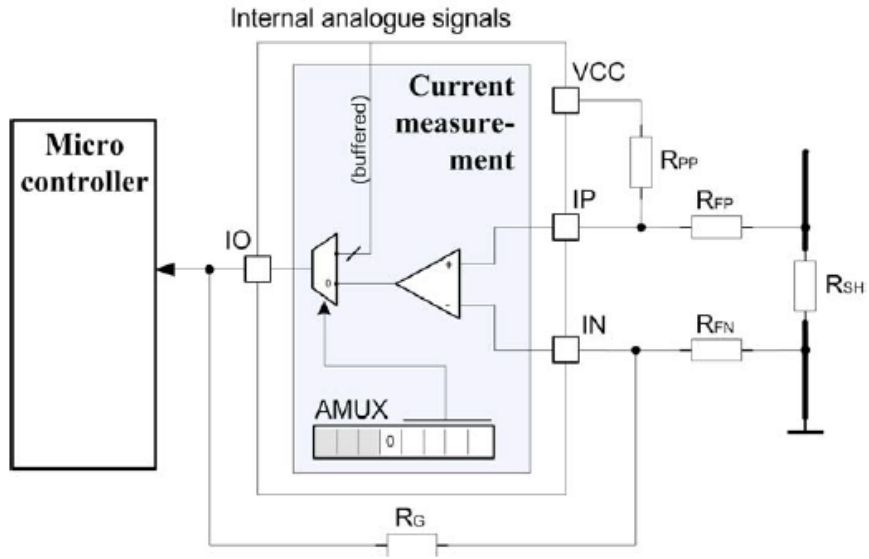


Figure 28: Motor current measurement amplifier circuitry

IO Pin으로 나가는 Analog 출력값을 AMUX register를 이용해서 선택할 수 있음!!
0~ 10까지 선택 가능!!

6.4.2 Analogue Signal Measurement

The IC is able to provide divided pin potentials and internal analogue signals to the microcontroller. The analogue signals can be switched to IO pin via AMUX register. The observable voltage range at IO pin is limited from 0V to V_{VDD}.

*Table 6.22: Register **AMUX** (0x17), analogue signal measurement selection*

	MSB							LSB
Content	-	-	-	S4	S3	S2	S1	S0
Reset value	0	0	0	0	0	0	0	0
Internal access	-	-	-	R	R	R	R	R
External access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit Description	**S[4]:** Reserved, bit must be 0 **S[3:0]:** Analogue signal selection. See below for coding.							

Table 6.23: Analogue signals measurement code table

AMUX	Analogue signal to IO pin
0	Current amplifier mode (standard)
1	V_{VIN}
2	V_{IP}
3	V_{TEMP}
4	V_{VBAT} / 12
5	V_{VG} / 5
6	Over current comparator threshold (IOCOMPTHR)
7	Low side power FET short circuit threshold (SCTH, SCTH_LS)
8	V_{GL1}
9	V_{GL2}
10	V_{GL3}

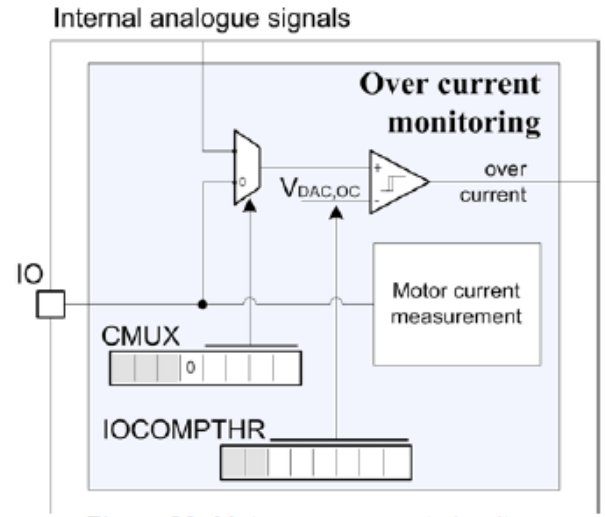


Figure 29: Motor over current circuitry

내부 comparator로 들어가는 Analog 입력을 CMUX를 이용해서 선택할 수 있음.
Default로는 Motor current(IO) 의 Analog 값이 comparator출력으로 들어가도록 되어 있음 (Over current detection)
하지만 CMUX값을 변경해서 다른 Analog값이 comparator에 들어가도록 설정 할 수 있음!!
단, 여기서 comparator의 threshold값은 IOCOMPTHR register에 의해 결정됨!!!

*Table 6.28: Register **CMUX** (0x18), motor over current comparator input signal selection*

	MSB							LSB
Content	-	-	-	S4	S3	S2	S1	S0
Reset value	0	0	0	0	0	0	0	0
Internal access	-	-	-	R	R	R	R	R
External access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit Description	**S4:** Reserved, bit must be 0 **S3:** Motor over current comparator configuration. See below for coding.							

Table 6.29: Switch analogue signals to motor over current comparator code table

CMUX	Analogue signals
0	Motor over current comparator (standard)
1	V_{VIN}
2	V_{IP}
3	V_{TEMP}
4	V_{VBAT} / 12
5	V_{VG} / 5
6	Over current comparator threshold (IOCOMPTHR)
7	Low side power FET short circuit threshold (SCTH, SCTH_LS)

CMUX	Analogue signals
8	V_{GL1}
9	V_{GL2}
10	V_{GL3}

내부 digital signal 의 status를 monitoring 할 수 있음!!
어떻게 monitoring 하냐?

1. SO Pin을 내부 digital signal pin과 mapping 해서 상태를 SO pin을 통해 바로 읽어 볼 수 있음!!! DMUX register를 이용해서 mapping 가능!!

2. SPI를 통해서 내부 digital signal의 status를 읽어 볼 수 있음
DMON1 또는 DMON2 Register를 읽으면 됨!!!!

6.5.4 Internal Digital Signal Monitoring

Internal digital signals, e. g. monitoring comparator outputs or digital input pin levels, can be monitored by the micro controller. They can be switched to SO pin transparently via DMUX register or read via SPI in DMON1-2 register. DMUX register write access is locked, if EDMUX bit in SECURCTRL register is 0.

*Table 6.37: Register **DMUX** (0x19), digital value output SO selection*

	MSB							LSB
Content	-	-	-	-	S3	S2	S1	S0
Reset value	0	0	0	0	0	0	0	0
Internal access	-	-	-	-	R	R	R	R
External access	R	R	R	R	R/W	R/W	R/W	R/W
Bit Description	**S3:0** : SO pin digital signal output selection. See below for coding.							

Table 6.38: Digital signal output code table

DMUX	Signal at SO pin [1]
0	No internal digital signal output
1	VSEL pin level
2	S pin level
3	T pin level
4	Motor over current comparator level
5	Over temperature comparator level
6	On-state of low side gate driver output GL1
7	On-state of low side gate driver output GL2
8	On-state of low side gate driver output GL3
9	VG under voltage comparator level

[1] *Shared functionality with SO pin: If CSB = 'L', SO is used as SPI data output in any configuration.*

*Table 6.39: Register **DMON1** (0x1A), digital value monitoring*

	MSB							LSB
Content	OT	OC	SC_HS3	SC_HS2	SC_HS1	SC_LS3	SC_LS2	SC_LS1
Reset value	-	-	-	-	-	-	-	-
Internal access	W	W	W	W	W	W	W	W
External access	R	R	R	R	R	R	R	R
Bit Description	**OT:** Over temperature comparator level **OC:** Motor over current comparator level **SC_HS3:** High side 3 short circuit comparator level **SC_HS2:** High side 2 short circuit comparator level **SC_HS1:** High side 1 short circuit comparator level **SC_LS3:** Low side 3 short circuit comparator level **SC_LS2:** Low side 2 short circuit comparator level **SC_LS1:** Low side 1 short circuit comparator level							

*Table 6.40: Register **DMON2** (0x1B), digital value monitoring*

	MSB							LSB
Content	S	VTHONLS3	VTHONLS2	VTHONLS1	VBAT_OV	VG_OV	VG_UV	-
Reset value	-	-	-	-	-	-	-	0
Internal access	W	W	W	W	W	W	W	W
External access	R	R	R	R	R	R	R	R
Bit Description	**S:** Pin S input comparator level **VTHONLS3:** Low side 3 on threshold comparator level **VTHONLS2:** Low side 2 on threshold comparator level **VTHONLS1:** Low side 1 on threshold comparator level **VBAT_OV:** VBAT over voltage comparator level **VG_OV:** VG over voltage comparator level **VG_UV:** VG under voltage comparator level							

6.5.1 Motor Over Current

The motor current measurement amplifier output at IO pin is monitored by the IC. If the voltage exceeds a programmable threshold, a motor over current is detected. The threshold value is calculated to:

$$V_{th,OC} = \frac{IOCOMPTHR \pm 8}{64} \cdot V_{VDD}$$

*Table 6.27: Register **IOCOMPTHR** (0x16), motor over current threshold*

	MSB							LSB
Content	-	-	D5	D4	D3	D2	D1	D0
Reset value	0	0	0	0	0	0	0	0
Internal access	-	-	R	R	R	R	R	R
External access	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**D[5:0]:** Motor over current threshold value							

*Table 6.41: Register **IOCFG** (0x06), interface configuration*

	MSB							LSB
Content	TXDTO_EN	LIN_FLASH	PWM-FREQ	BUSIF	PWMIF	-	VSELDIR	EINT
Reset value	1	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	-	R	R
External access	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Bit Description	**TXDTO_EN:** Enable TXD dominant clamping time-out **LIN_FLASH:** Enable LIN flash mode **PWMFREQ:** 1: 2 kHz mode (500 kHz sampling frequency), 0: 1 kHz mode (250 kHz sampling frequency) **BUSIF:** Enable dedicated hardware for duty cycle measurement **PWMIF:** 1: Apply dedicated hardware for duty cycle measurement on S pin, 0: Apply dedicated hardware for duty cycle measurement on BUS pin **VSELDIR:** 1 VSEL is interrupt output, 0: SO is interrupt output **EINT:** Enable shared functionality at VSEL or SO pin (interrupt output)							

*Table 6.4: Register **CHIPCTRL** (0x02), wake-up configuration*

	MSB							LSB
Content	-	-	-	-	-	SSENS	BUSWA-KEEDGE	BUSWA-KEEN
Reset value	0	0	0	0	0	0	1	1
Internal access	-	-	-	-	-	R	R	R
External access	R	R	R	R	R	R/W	R/W	R/W
Bit Description	**SSENS:** 1: Wake up at S is level sensitive (high level leads to wake up), 0: Wake up at S is edge sensitive (rising edge) **BUSWAKEEDGE:** 1: BUS wake up at rising edge, 0: BUS wake up at falling edge **BUSWAKEEN:** BUS wake up enable							

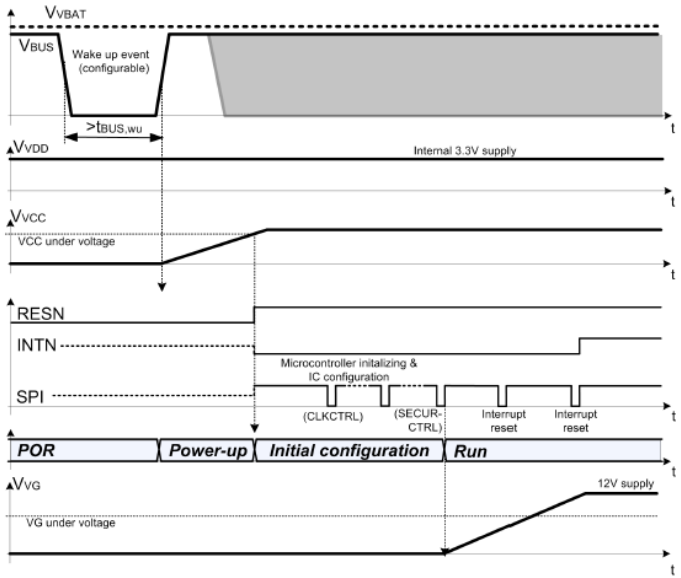


Figure 19: Wake-up via BUS pin, typical scenario with BUSWAKEEDGE = 1

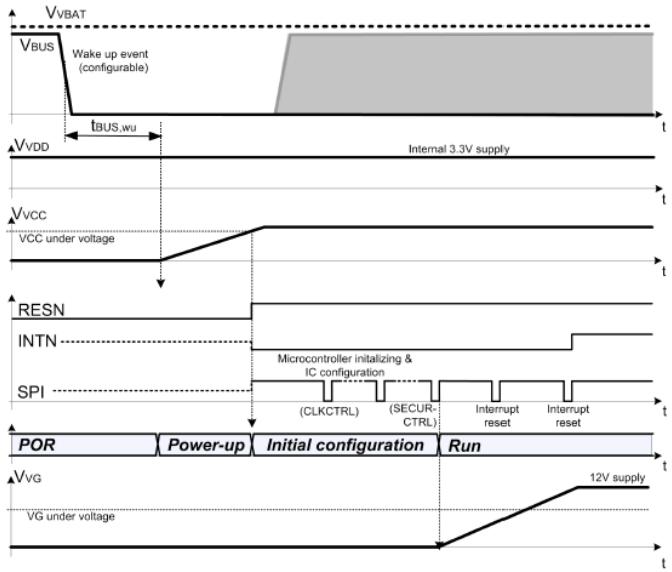


Figure 20: Wake-up via BUS pin, typical scenario with BUSWAKEEDGE = 0

*Table 6.33: Register **IRQMSK1** (0x12), interrupt mask register*

	MSB							LSB
Content	EN_OT	EN_OC	EN_SC_HS3	EN_SC_HS2	EN_SC_HS1	EN_SC_LS3	EN_SC_LS2	EN_SC_LS1
Reset value	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**EN_OT:** Enable over temperature interrupt **EN_OC:** Enable motor over current interrupt / CMUX multiplexer interrupt **EN_SC_HS3:** Enable HS 3 short circuit interrupt **EN_SC_HS2:** Enable HS 2 short circuit interrupt **EN_SC_HS1:** Enable HS 1 short circuit interrupt **EN_SC_LS3:** Enable LS 3 short circuit interrupt **EN_SC_LS2:** Enable LS 2 short circuit interrupt **EN_SC_LS1:** Enable LS 1 short circuit interrupt							

*Table 6.34: Register **IRQSTAT1** (0x13), interrupt status register*

	MSB							LSB
Content	OT	OC	SC_HS3	SC_HS2	SC_HS1	SC_LS3	SC_LS2	SC_LS1
Reset value	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**OT:** Over temperature interrupt flag **OC:**Motor over current interrupt flag / CMUX multiplexer interrupt flag **SC_HS3:** HS 3 short circuit interrupt flag **SC_HS2:** HS 2 short circuit interrupt flag **SC_HS1:** HS 1 short circuit interrupt flag **SC_LS3:** LS 3 short circuit interrupt flag **SC_LS2:** LS 2 short circuit interrupt flag **SC_LS1:** LS 1 short circuit interrupt flag							

*Table 6.35: Register **IRQMSK2** (0x14), interrupt mask register*

	MSB							LSB
Content	-	EN_CLK_WD	EN_REG_WD	EN_PWM	EN_VBAT_OV	EN_VG_OV	EN_VG_UV	EN_VCC_UV
Reset value	0	0	0	0	0	0	0	0
Internal access	-	R	R	R	R	R	R	R
External access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**EN_CLK_WD:** Enable clock watchdog interrupt **EN_REG_WD:** Enable register watchdog interrupt **EN_PWM:** Enable dedicated hardware at BUS pin (PWM mode) interrupt **EN_VBAT_OV:** Enable VBAT over voltage interrupt **EN_VG_OV:** Enable VG over voltage interrupt **EN_VG_UV:** Enable VG under voltage interrupt **EN_VCC_UV:** Enable VCC under voltage interrupt							

*Table 6.36: Register **IRQSTAT2** (0x15), interrupt status register*

	MSB							LSB
Content	-	CLK_WD	REG_WD	PWM	VBAT_OV	VG_OV	VG_UV	VCC_UV
Reset value	0	0	0	0	0	0	0	0
Internal access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**CLK_WD:** Clock watchdog interrupt flag **REG_WD:** Register watchdog interrupt flag **PWM:** Dedicated hardware at BUS pin (PWM mode) interrupt flag **VBAT_OV:** VBAT over voltage interrupt flag **VG_OV:** VG over voltage interrupt flag **VG_UV:** VG under voltage interrupt flag **VCC_UV:** VCC under voltage interrupt flag							

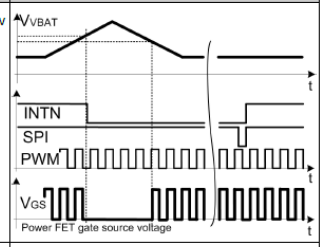
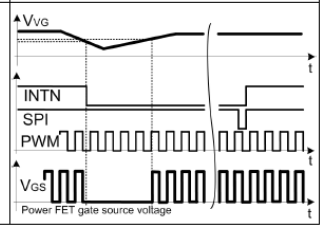
*Table 6.25: Register **SAFECTRL** (0x05), safety function configuration*

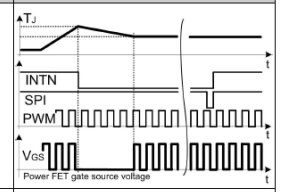
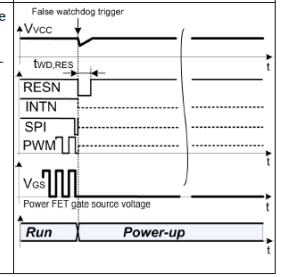
	MSB							LSB
Content	VBATOV_FR1	VBATOV_FR0	VGUV6V	SOC	SVBATO	SVG	OTVC-COFF	OTSLEEP
Reset value	0	0	0	1	1	1	1	0
Internal access	R	R	R	R	R	R	R	R
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**VBATOV_FR[1:0]:** Refer to following table **VGUV6V:** V_{VG} under voltage threshold select for V_{VBAT} > 7V (0) or V_{VBAT} > 6V (1) **SOC:** Safety function on over current **SVBATO:** Safety function on VBAT over voltage **SVG:** Safety function on VG over or under voltage **OTVCCOFF:** Disable VCC supply on over temperature. This bit has no effect when OTSLEEP is 1 (VCC is always off in sleep mode). **OTSLEEP:** IC shut down on over temperature							

Table 6.26: VBAT over voltage failure reaction code table

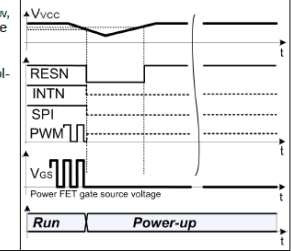
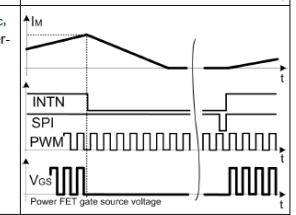
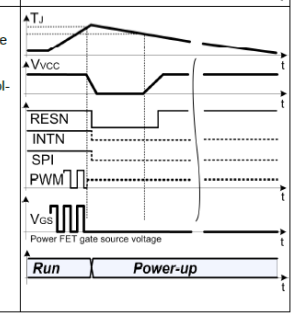
SAFECTRL[7:6]	VBAT over voltage failure reaction
0	All LS-FETs are switched on, all HS-FETs are switched off automatically
1	All FETs are switched off automatically
2	All HS-FETs are switched off automatically, switching of LS-FETs allowed

Table 6.24: Monitoring functions

Function	Failure condition	Failure actions	Reset condition	Depiction
VBAT over voltage	V_{VBAT} > $V_{VBAT,OV}$, SAFECTRL[3] = 1	Switch all high side power FETs off cases SAFECTRL[7:6]: 0: Switch all low side power FETs on 1: Switch all low side power FETs off 2: allow switching of low side power FETs	V_{VBAT} < $V_{VBAT,OV}$	
VG under voltage	V_{VG} < $V_{VG,UV}$, SAFECTRL[2] = 1	Switch all power FETs off	V_{VG} > $V_{VG,UV}$	

Function	Failure condition	Failure actions	Reset condition	Depiction
Over temperature with SAFECTRL[1] = 0	T_J > T_{otemp}	Switch all power FETs off, disable BUS, ***Safety warning:** The microcontroller has to switch into low power mode immediately, else the IC might be damaged.*	T_J < T_{otemp}	
Watchdog event	No watchdog trigger or false trigger, WDCTRL[1] = 1	Switch all power FETs off, reset of external microcontroller, reset of internal registers except IRQSTATx	Restart of the IC and external microcontroller	

INTN: low-active interrupt

Function	Failure condition	Failure actions	Reset condition	Depiction
VCC under voltage	V_{VCC} < $V_{VCC,UV}$	Switch all power FETs off, reset of external microcontroller, reset of internal registers except IRQSTATx	V_{VCC} >$V_{VCC,UV}$, restart of the IC and external microcontroller	
Motor over current	V_{IO} > $V_{DAC,OC}$, SAFECTRL[4] = 1	Switch all power FETs off	V_{IO} < $V_{DAC,OC}$, cleared interrupt	
Over temperature with SAFECTRL[1] = 1	T_J > T_{otemp}	Switch all power FETs, VCC and VG regulator off, disable BUS, reset of external microcontroller, reset of internal registers except IRQSTATx	T_J < T_{otemp}, restart of the IC and external microcontroller	

6.2 Initial Configuration and Security

Some registers of the IC are only writeable within the initial configuration state (refer to restricted register table).

After power-up or wake-up an initial IC configuration via SPI needs to be done. The initial configuration:

- starts with the writing of CLKCTRL clock divider register. Before writing CLKCTRL register, any writing of restricted registers is ignored.
- ends with setting ESECURE bit in SECURCTRL register. Once ESECURE bit is set, any writing of restricted registers is ignored.

Register setting 순서 유의해야함!!

The ESECURE bit can only be set, if all other bits in SECURCTRL register are left unchanged. So the register has to be written twice, if special IC features want to be selected.

Example 1: *SECURCTRL = 0x01, only 1 SPI access to the register necessary (no special features selected)*

Example 2: *SECURCTRL = 0x18 (1st SPI access), SECURCTRL = 0x19 (2nd SPI access), analogue signal multiplexing and emergency shut-off selected*

이 register는 2번 writin해주어야함!!
두번재 writing 에서는 0bit를 1로 해서 writing 해줌!!

Reset conditions of ESECURE bit are:

- Watchdog event (register watchdog or CLK watchdog)
- Under voltage at VDD or VCC (at low battery voltage or short circuit)
- Sleep state

The restriction of the dead time registers (section "Power FET Gate Driver") and analogue / digital signal multiplexing registers can be released by writing SECURCTRL register accordingly.

*Table 6.5: Register **SECURCTRL** (0x04), security configuration*

	MSB							LSB
Content	-	-	EDMUX	EACMUX	EMER-GENCY	EDEAD-MULT	EDEAD-NEG	ESECURE
Reset value	0	0	0	0	0	0	0	0
Internal access	-	-	R	R	R	R	R	R
External access	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**EDMUX:** Enable write access to DMUX register in run mode **EACMUX:** Enable write access to AMUX and CMUX registers in run mode **EMERGENCY:** Enable emergency shut-off functionality of power FET gate driver at VIN pin **EDEADMULT:** Enable write access to DEADTIME_LH and DEADTIME_HL registers in run mode **EDEADNEG:** Allow negative dead times in DEADTIME_LH and DEADTIME_HL registers ***Security warning:*** *Setting this bis is at own risk. The customer has to guarantee that no cross currents occur at the half bridge. Damage of IC and external components are possible.* **ESECURE:** 1: Disables write access to all restricted registers (including ESECURE bit itself)							

Motor 구동 전에는 반드시 status register clear해줄것!! ➔ 해당 bit에 1을 쓰면 clear됨!!
(0x13 : IRQSTAT1, 0x15 : IRQSTAT2)

6.5.3 Interrupt

Previous Next

The interrupt bits in IRQSTAT1 and IRQSTAT2 registers are set in case of the accordant failure event. Although there is no dedicated interrupt pin, an interrupt can be signalized to the microcontroller.

Table 6.32: Interrupt output configuration possibilities

Output Pin	Mode	Configuration	Signal direction	Shared functionality with
VSEL [1)]	V_{VCC} = 3.3V	IOCFG[1] = 1, IOCFG[0] = 1	High active	VCC regulator voltage selection
VSEL [1)]	V_{VCC} = 5V	IOCFG[1] = 1, IOCFG[0] = 1	Low active	VCC regulator voltage selection
SO [2)]	-	IOCFG[1] = 0, IOCFG[0] = 1	Low active	SPI interface

[1)] Shared functionality with VSEL pin: Only available in run mode, since VSEL is used for VCC regulator voltage selection in power-up mode.

[2)] Shared functionality with SO pin: If CSB = 'L', SO is used as SPI data output in any configuration.

An interrupt can only be cleared, when the failure situation is over. The interrupt bit is cleared by writing 1 to the interrupt bit in IRQSTAT registers or after power-up (applying battery voltage). It is not cleared during sleep mode.
The interrupt mask bits in IRQMSK1 and IRQMSK2 registers mask the effect of the interrupt bits in IRQSTAT registers on the selected interrupt output pin (VSEL or SO).