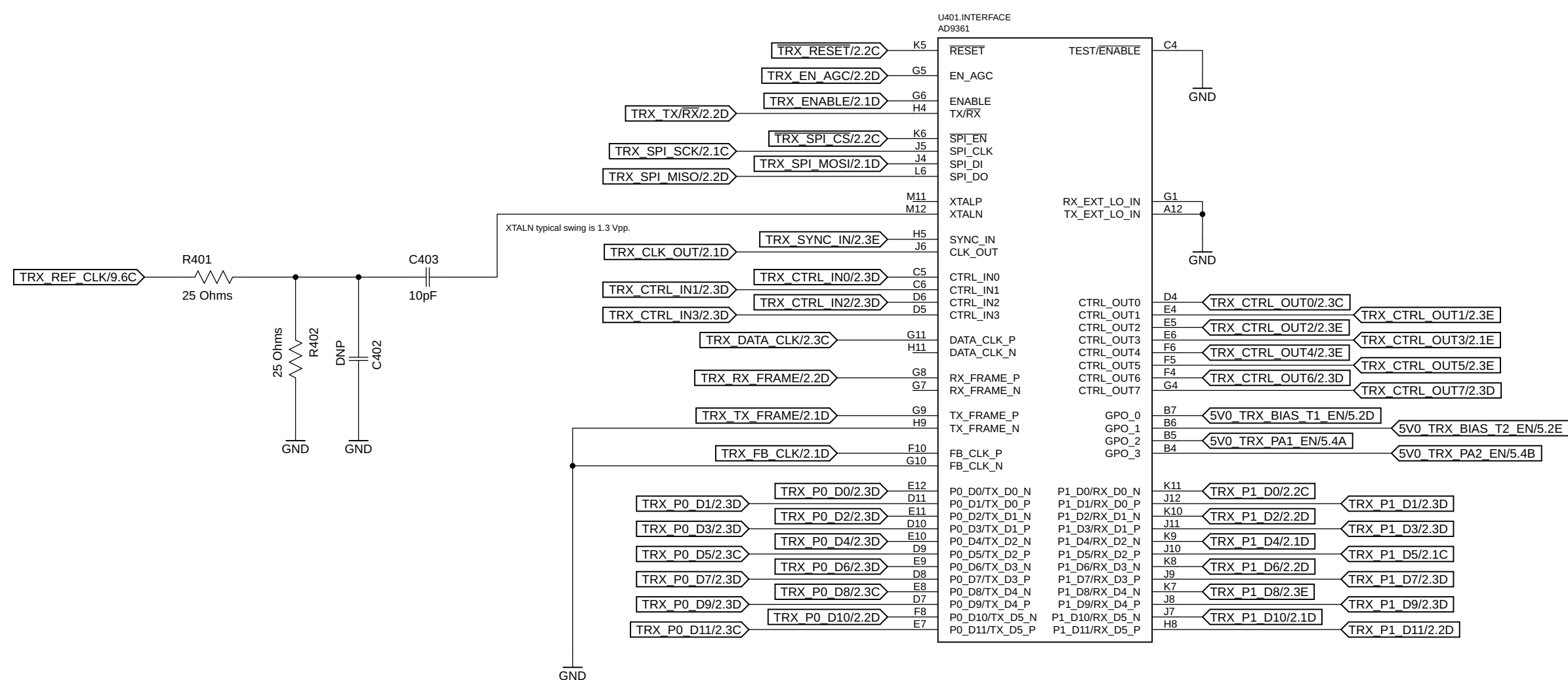
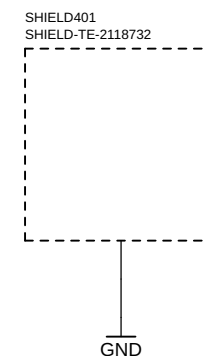


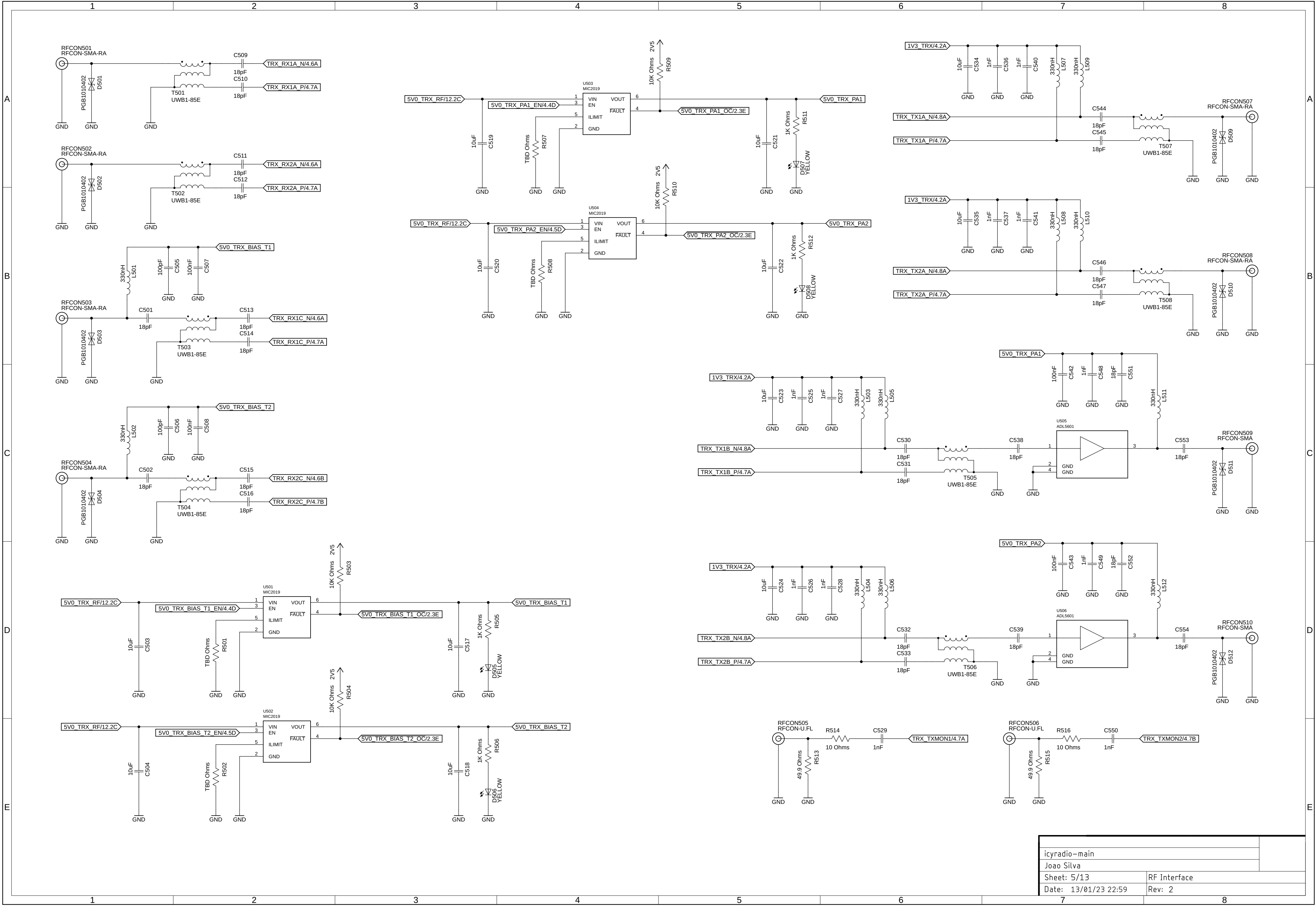
TODO:
 - AUXDAC
 - AUXADC
 - Add keepout on RF components

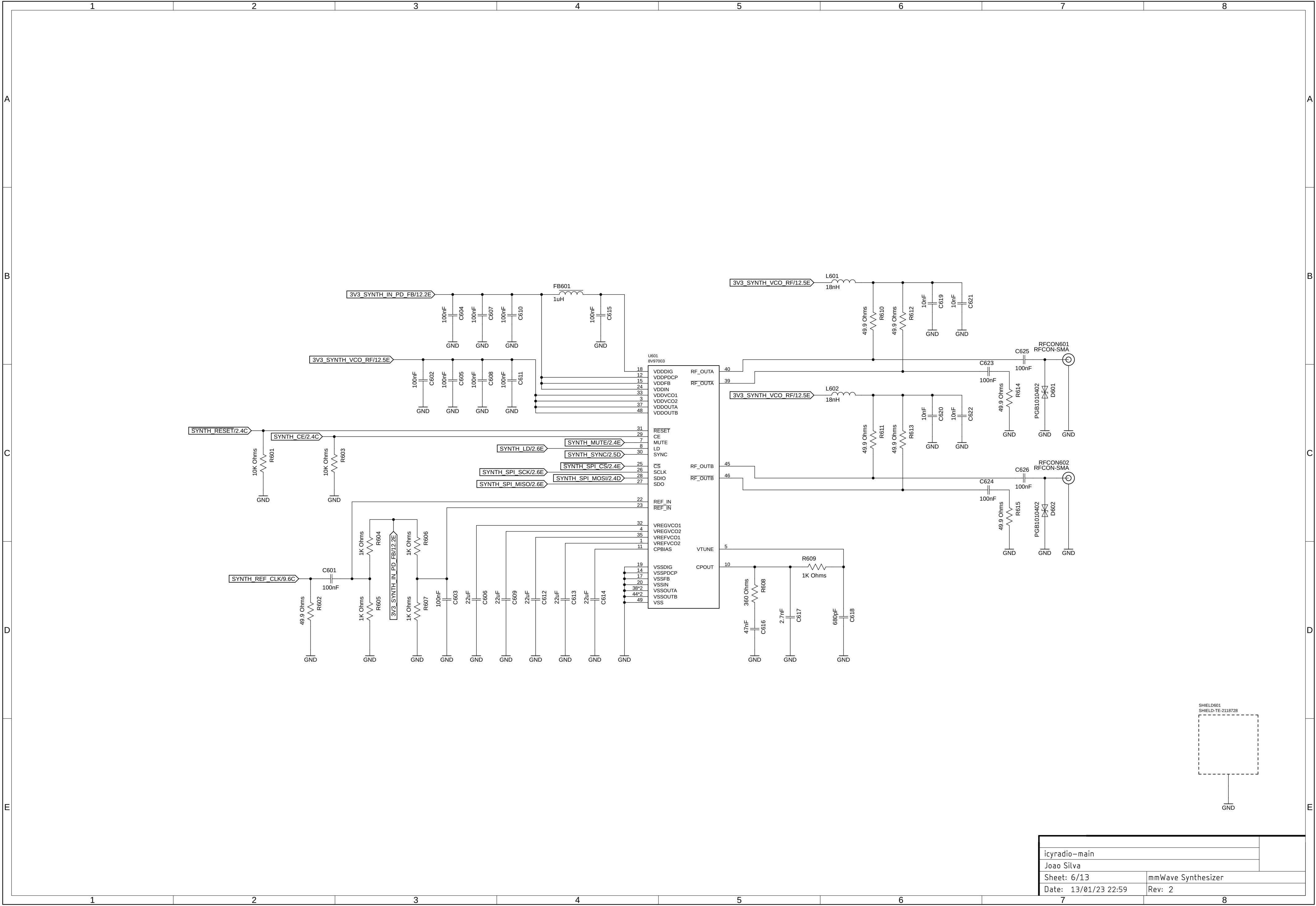


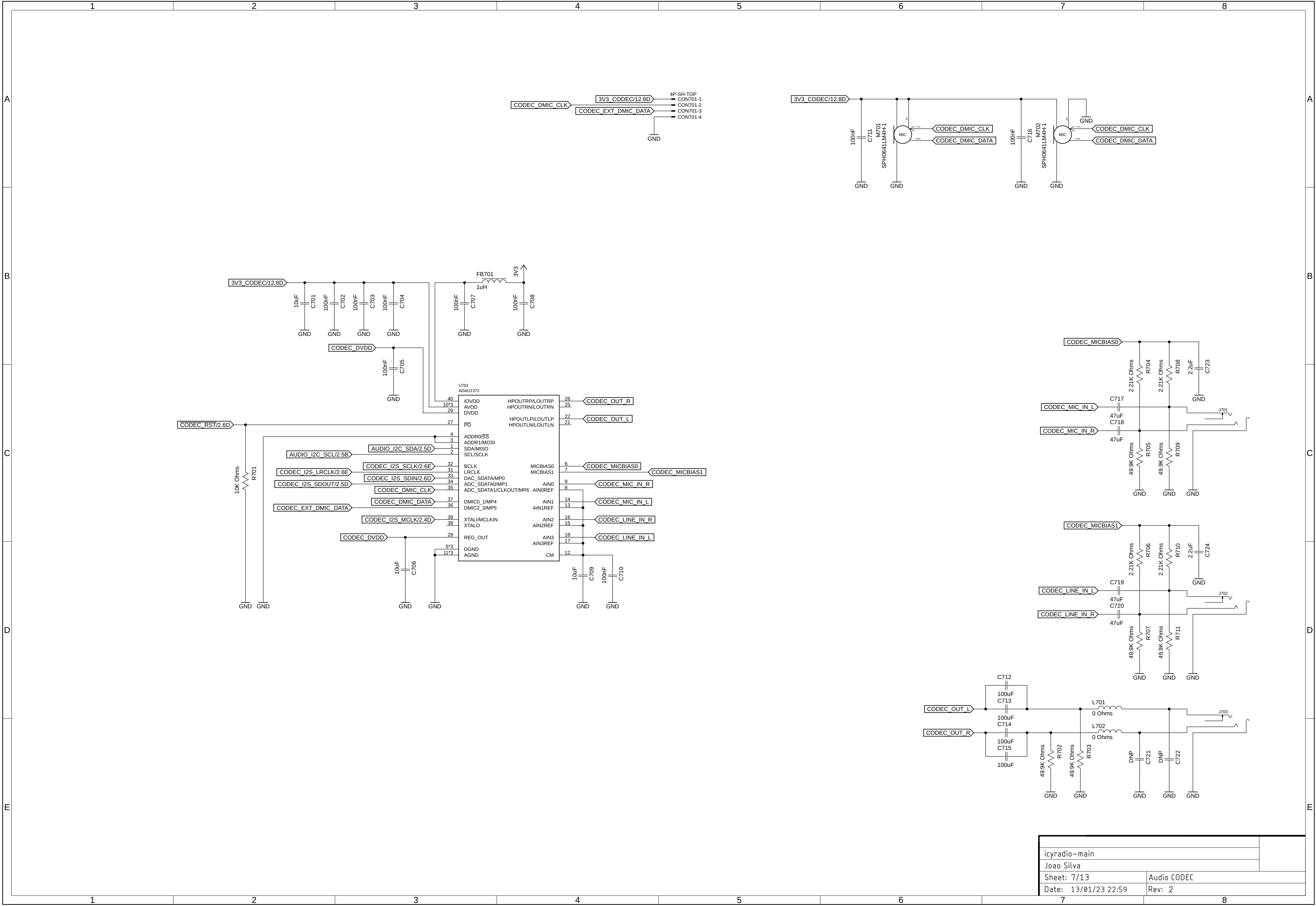
GPOs are used to control the power switches to the Bias-Ts and PAAs. GPO0 should be used for RX Bias-T on channel 1. GPO1 should be used for RX Bias-T on channel 2. This is because those are able to be mapped to gain table bits, facilitating the use of external LNAs. There is no specific GPO assignment required for PA bias.

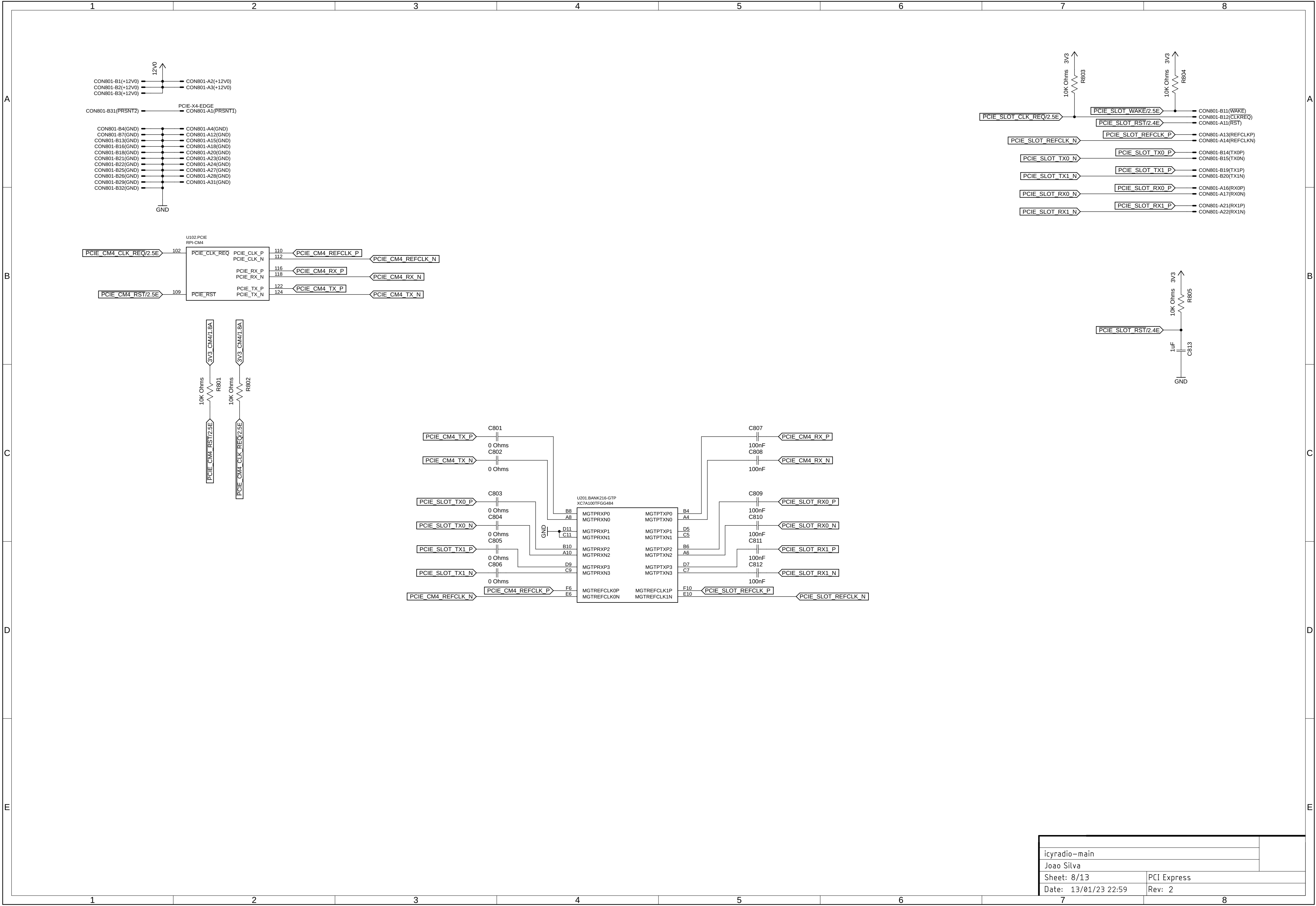
Warning: Always use DC blocks when connecting to the RX inputs with Bias-Ts, if the equipment cannot tolerate a DC voltage. This is because, by default, the Bias-Ts are enabled on transceiver reset!

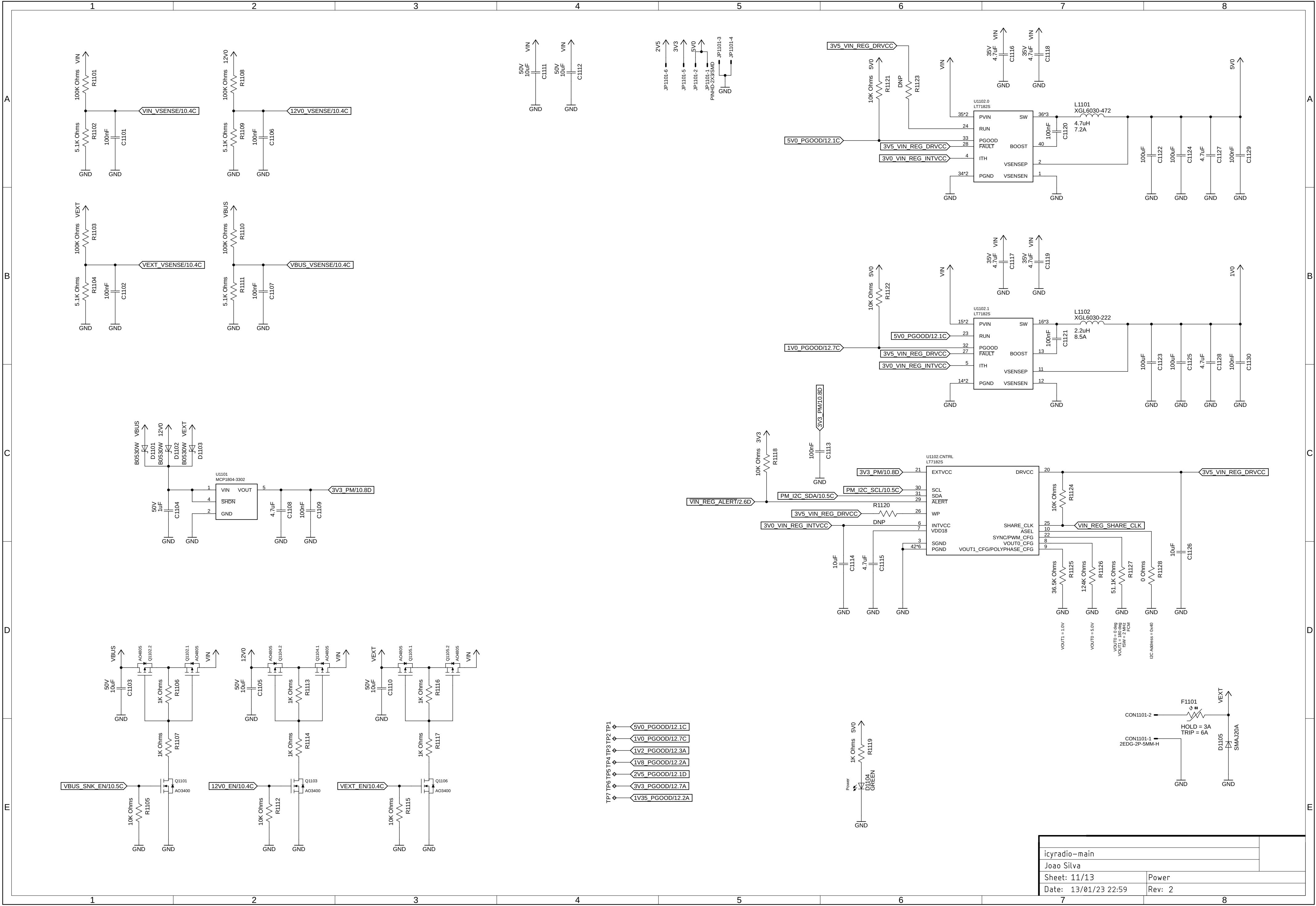


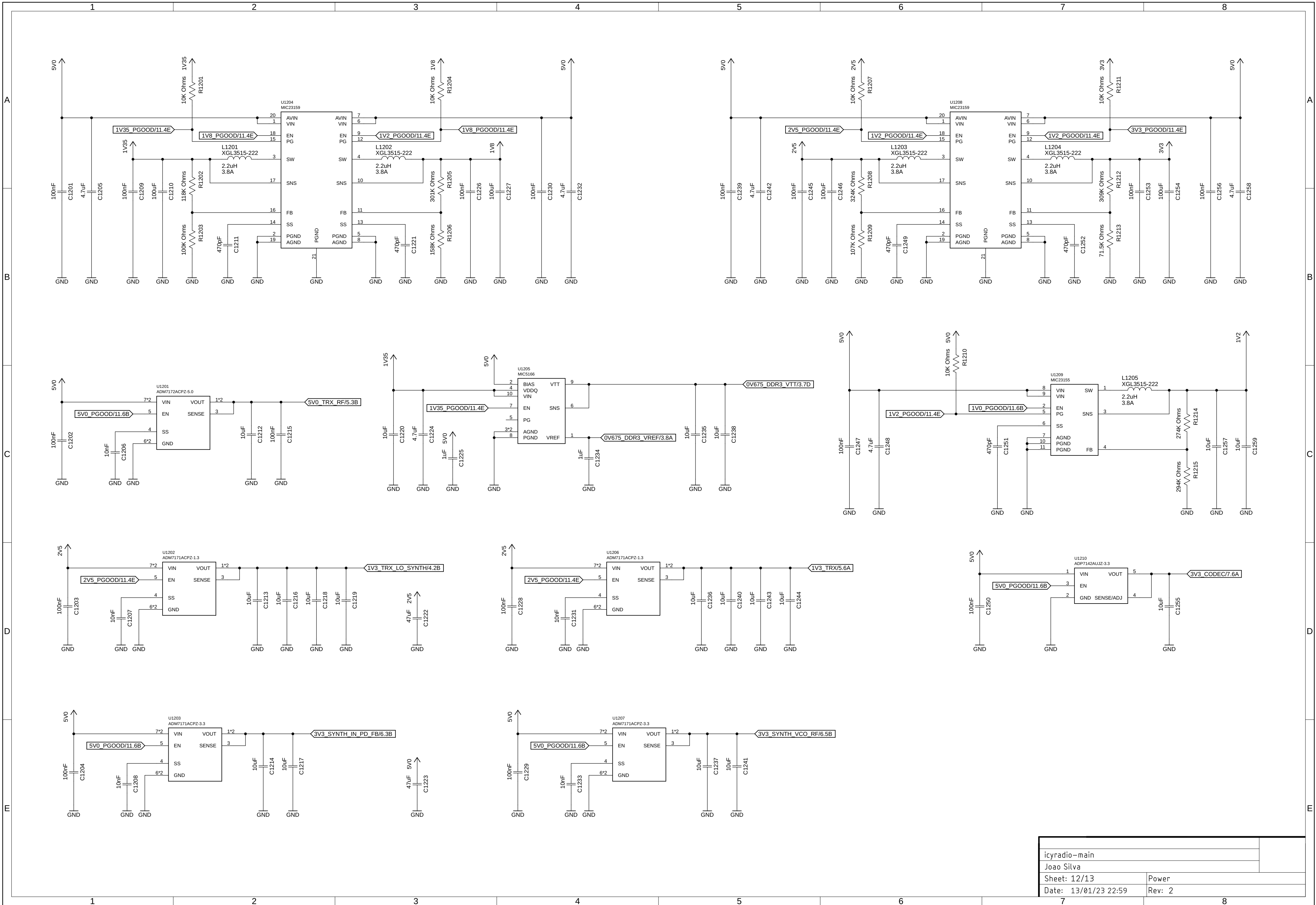








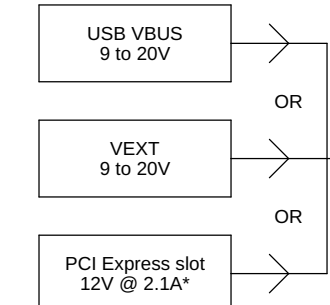




TODO:

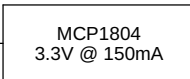
- Review current requirements
- Check if the parts can supply the requested current

If the Compute Module 4 is installed, the only possible power sources are USB or the external 9 to 20V adapter (which makes sense, since the data will be processed in the Compute Module 4, with no external connections required to offload FPGA data, only power)



Power from PCI Express slot is to be used ONLY when the data also goes through PCI Express (i.e. the Compute Module 4 should NOT be installed)

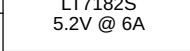
* x4 cards may draw up to 25W as per PCIe spec. May be able to draw up to 75W.



Digital Rail
Power Management & TCPC MCU



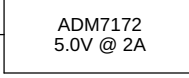
Digital Rail
FPGA Core, FPGA GTP VCC



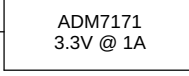
Digital Rail
Compute Module 4



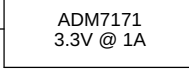
Analog Rail
Audio CODEC



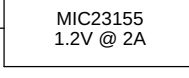
Analog Rail
TX RF Amplifiers, RX RF Bias Ts



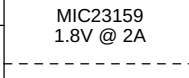
Analog Rail
mmWave Synth VDDPDCP, VDDFB, VDDIN



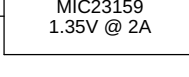
Analog Rail
mmWave Synth VDDVCOx, VDDOUTx



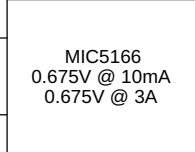
Digital Rail
FPGA GTP VTT



Digital Rail
FPGA Auxiliary, FPGA Bank 3

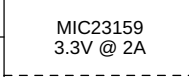


Digital Rail
FPGA IO Banks 34/35, DDR3 VDDQ

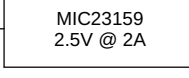


Digital Rail
DDR3 VREF

Digital Rail
DDR3 VTT



Digital Rail
FPGA IO Banks 0/13/14, Misc



Digital Rail
FPGA Banks 15/16, AD9361 Interface

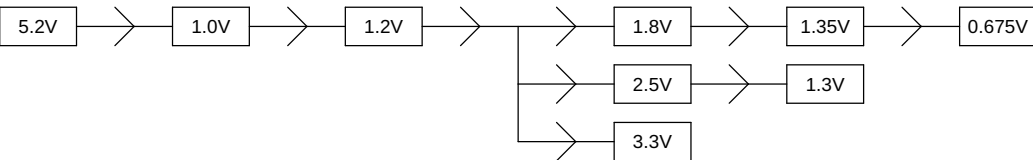


Analog Rail
AD9361 LOs and Synthesizers



Analog Rail
AD9361 Baseband, Core, TX bias

Power Sequence



icyradio-main	
Joao Silva	
Sheet: 13/13	Power tree
Date: 13/01/23 22:59	Rev: 2