txpll.pll analysed at 03/27/20 13:36:56

PLL Chip is ADF4351
Notes:
VCO is ADF4351
Reference is custom

Advanced Design - VCO Divider is Outside loop and set as follows:

Start Freq	Stop Freq	VCO Divider	Channel Spacing
60.0MHz	68.75MHz	64	95.391 Hz
68.75MHz	137.5MHz	32	190.78 Hz
137.5MHz	275MHz	16	381.56 Hz
275MHz	550MHz	8	763.13 Hz
550MHz	1.10GHz	4	1.5263kHz
1.10GHz	2.20GHz	2	3.0525kHz
2.20GHz	4.40GHz	1	6.105kHz

Frequency Domain Analysis of PLL
Analysis at PLL output frequency of 60MHz
VCO divider set to 64

Phase Noise Table

Freq	Total	VCO	Ref	Chip	SDM	Filter
100	-57.56	-140.0	-57.56	-120.4	-288.6	-193.0
1.00k	-77.55	-137.0	-77.55	-129.8	-248.9	-173.1
10.0k	-97.05	-135.8	-97.05	-135.8	-208.4	-155.0
100k	-114.7	-140.0	-114.7	-135.3	-166.1	-148.3
1.00M	-163.0	-163.2	-187.4	-188.4	-179.0	-188.3

Reference Spurious
Noise and Jitter Calculations include the first 10 ref spurs
First three spurs: -300 dBc -300 dBc -300 dBc

Fractional-N Spur Estimate (worst case)
Phase Detector mode is Dither OFF

Freq (Hz)	Spur Level (dBc)
2.04k	-237
4.07k	-237
6.11k	-237

Phase jitter using brick wall filter
from 60.0MHz to 4.40GHz
Phase Jitter **1.38ps rms**

---- End of Frequency Domain Results ----

Transient Analysis of PLL
Frequency change from 60MHz to 4.4GHz
Simulation run for 250us Final Tuning voltage = 1.6370 V

Frequency Locking
Time to lock to 1.00kHz is 132us
Time to lock to 10.0 Hz is 189us

Phase Locking (VCO Output Phase)
Time to lock to 10.0 deg is 122us
Time to lock to 1.00 deg is 151us

Lock Detect Threshold
Time to lock detect exceeds 2.50 V is 30.8us

---- End of Time Domain Results ----