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MX6 Quad Plus SABRE AI CPU3 Card with AVB

MX6 Quad CPU2 Card

Schematic SCH-27925
Part No. MCIMX6QAICPU2

Qualcomm (Atheros)
Ethernet PHY Card - RGMII

Schematic SCH-27953
Part No. IMXAI2ETH-ATH

Broadcom
Ethernet PHY Card - RGMII

Schematic SCH-27954
Part No. IMXAI2ETH-BRC

MX6 DualLite CPU2 Card

Schematic SCH-28605
Part No. MCIMX6DLAICPU2

MX6 QuadPlus CPU3 Card

Schematic SCH-28615
Part No. MCIMX6QPAICPU3

Automotive Base Board

Schematic SCH-26662
Part No. MCIMXABASEV1

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass production design. For an added resource, refer to Hardware Development Guide document number IMX6DQ6SDLHDG.

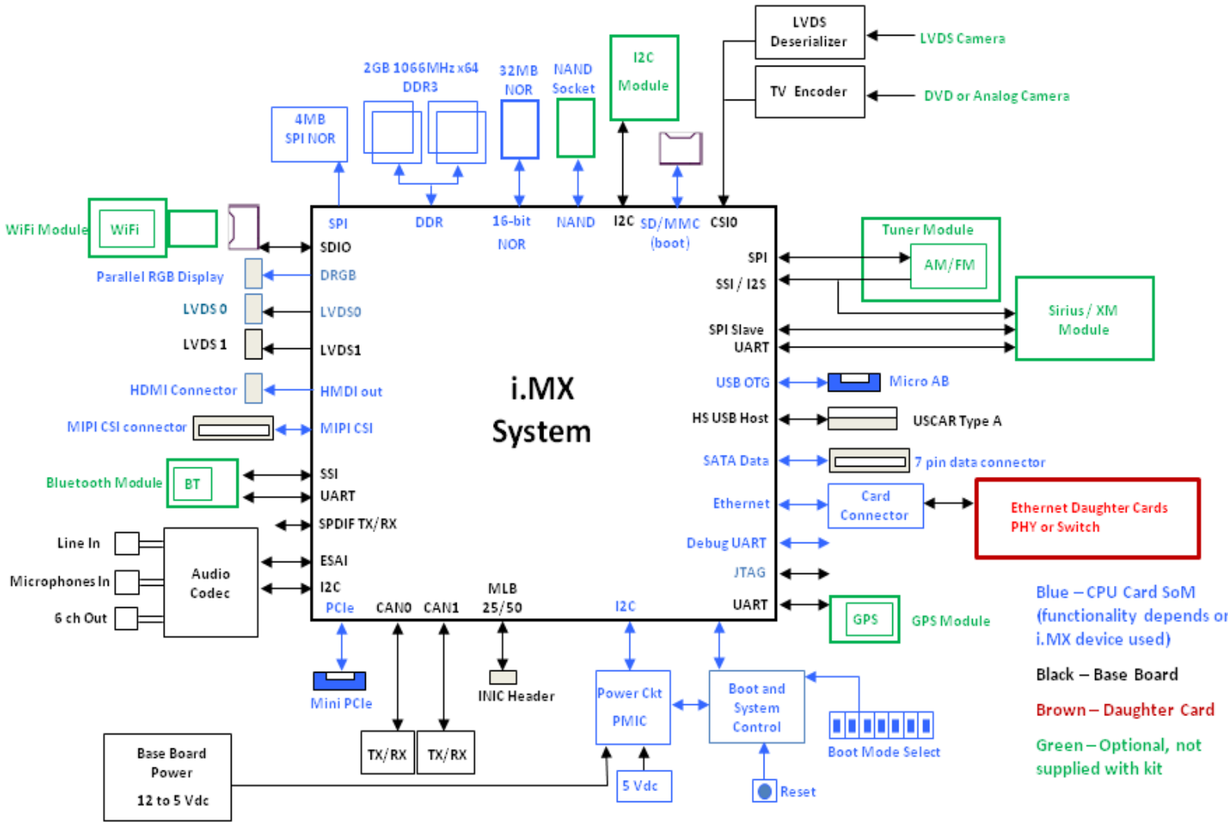
Consumer devices were utilized in this design when lead time for equivalent automotive-grade devices conflicted with production schedules. Freescale suggests consulting component suppliers for equivalent automotive-grade device information.

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: ___ IUO: ___ PUBI: _X_

Designer: David B	Drawing Title: MCIMX6QPAICPU3	
Drawn by: David B	Page Title: Cover	
Approved: Ross M	Size C / Document Number SCH-28615 PDF: SPF-28615	Rev A3
	Date: Friday, February 26, 2016	Sheet 1 of 25

Block Diagram



ICAP Classification:	CP: ___ IUO: ___ PUBI: _X_	
Drawing Title:	MCIMX6QPAICPU3	
Page Title:	Block Diagram	
Size C	Document Number SCH-28615 PDF: SPF-28615	Rev A3
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I2C2 – 50 kbps Max Bus Speed
I2C2_SDA = KEY_ROW3
I2C2_SCL = EIM_EB2

Peripheral	Location	Speed (kbps)	8-Bit Write Addresses	Default Write Address
PM IC	CPU Card	400	0x10 to 0x1E	0x10
I2C Module	Base Board	50	0x20	0x20
Terrestrial Radio AM-FM	Base Board	400	0xC0, 0xC2, 0xC4, 0xC6	0xC6
ESAI Audio CODEC	Base Board	100	0x90, 0x92, 0x94, 0x96	0x90
LVDS0 Capacitive Touch	CPU Card	100	0x82	0x82
HDMI EDID	CPU Card option	100	0xA0	Option not installed
MIPI ADI Video Card	CPU Card	400	0x40, 0x42	0x42
Ethernet Card ID "ROM" *	Daughter Card	400	16 combinations	0xD0
CS2000 (Cirrus Device)	CPU Card	100	0x9C, 0x9E	0x9C

I2C3 – 400 kbps Max Bus Speed
I2C3_SDA = EIM_D18
I2C3_SCL = GPIO_3

Peripheral	Location	Speed (kbps)	8-Bit Write Addresses	Default Write Address
MOST (MLB)	Base Board	400	0x40	0x40
Port Expander A	CPU Card	400	56 combinations	0x60
Port Expander B	CPU Card	400	56 combinations	0x64
Port Expander C	CPU Card	400	56 combinations	0x68
Analog In via Video ADC	Base Board	400	0x40, 0x42	0x42
Ambient Light Sensor	Base Board	400	0x88	0x88
Compass	Base Board	400	0x1C	0x1C
Accelerometer	Base Board	400	0x3A, 0x38	0x38
RGB LCD Resistive Touch	CPU Card option	3400	0x90	Option not installed

* Ethernet Daughter Card Identification

0000 = Atheros (Qualcomm) PHY – RGMII
0001 = Broadcom PHY – RGMII
0010 = Broadcom PHY – MII (not compatible with MX6 CPU2 or CPU3)
0011 = reserved
0100 = SMSC PHY – RMII (not compatible with MX6 CPU2 or CPU3)

--- WARNING---
This CPU Card must be plugged into the Base Board and cannot be run standalone under heavy conditions such as simultaneous requirements of:

- Intense graphics
- ARM heavy load
- Heavy DRAM activity
- OTG = host supplying 500 mA
- 2 displays active
- Broadcom Switch Daughter Card plugged into J21

Standalone CPU3 operation is restricted to functional testing and light-to-medium running.

The reason is that the 5 V brick commonly used (25 W) and 5-V jack J8 are rated up to 5A.

ICAP Classification: CP: ___ IUO: ___ PUBI: X_
Drawing Title: MCIMX6QPAICPU3
Page Title: Notes - I2C
Size C | Document Number SCH-28615 PDF: SPF-28615 | Rev A3
Date: Friday, February 26, 2016 | Sheet 3 of 25

Boot Config	NAND Flash 64Gb	NAND Flash 16Gb	Parallel NOR Flash	SD on CPU Card	MMC on CPU Card	SATA HDD	Serial NOR Flash
S2-1	*	*	0	*	*	0	1
S2-2	0	0	0	0	1	1	1
S2-3	X	X	0	1	1	0	0
S2-4	1	1	0	0	0	0	0
S1-1	0	0	X	*	*	*	X
S1-2	0	0	X	1	*	*	X
S1-3	0	0	X	X	*	*	X
S1-4	1	1	X	0	0	*	X
S1-5	0	0	X	1	1	*	X
S1-6	X	X	1	*	*	X	X
S1-7	X	X	0	*	*	X	X
S1-8	0	0	X	*	X	X	X
S1-9	0	0	X	*	X	X	X
S1-10	0	0	0	*	*	X	X

Notes:
1 = High Level.
0 = Low Level.
X = Don't Care.
* = Switch needs to be configured for high or low depending on the application needs. Please check reference manual for boot configuration options.

Default boot configuration = SD on CPU Card

[redacted]

See switch interconnection on sheet 10.
See the two Boot Mode switches on sheet 8.

CPU Card Identification for Software

MX6 fuses OCOTP_GP1[15:8] = 0xB1
for SABRE-AI CPU3 rev A

Controlling document = Agile DOC-01878

SD Speed Selection

S1-10	S1-9	S2-1	Data Rate
0	0	0	SDR12
0	1	0	SDR25
1	0	0	SDR50
1	1	0	SDR104

ICAP Classification: CP: ___ IUO: ___ PUBI: _X_
Drawing Title: MCIMX6QPAICPU3
Page Title: Notes - Boot Config & Board ID
Size C | Document Number SCH-28615 PDF: SPF-28615 | Rev A3
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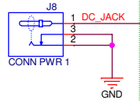
Main Power

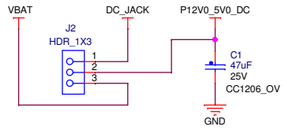
When CPU Card is run standalone, all power is sourced from P5V0 (Q505 pad 5).

5 Vdc +/-5%
Up to 5 A

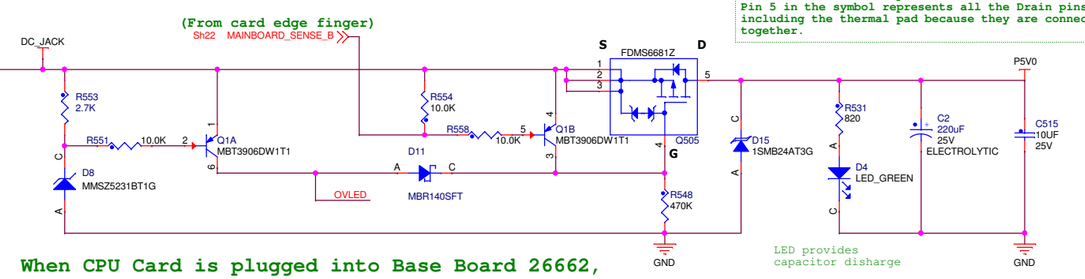


IMPORTANT!
No fuse protection.
Use current-limited supply.

J2 Jumper Position:
Stand-alone CPU card operation = 1-2
CPU card plugged into Base Board = 2-3 (default)

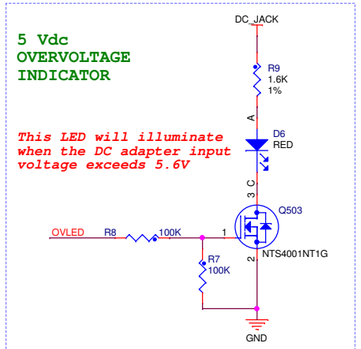


WARNING
When CPU Card is plugged into Base Board, J2 must be in position 2-3 to avoid damage to Q505 drain-source diode and P5V0 overload under processor heavy-current draw conditions.

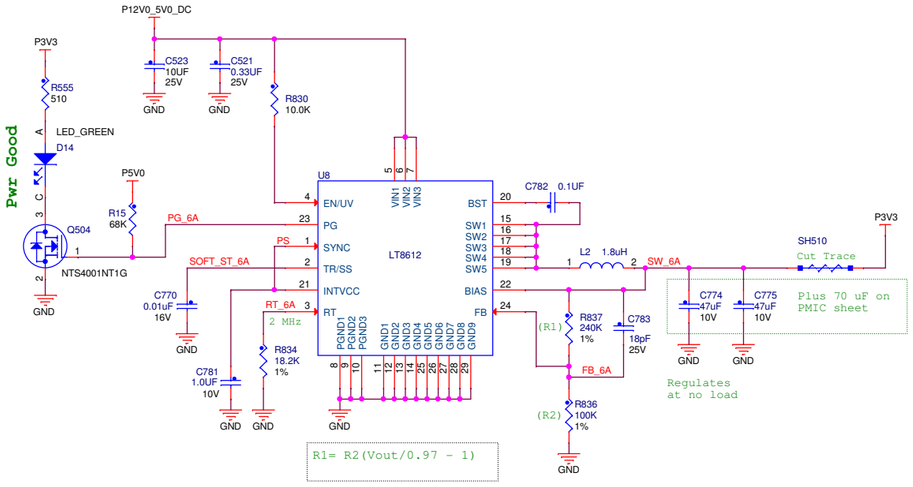


Symbol Q502 & Q505:
Base on the datasheet, FDMS6681Z is a 8-pin package with an extra thermal pad on the bottom.
Pin 5 in the symbol represents all the Drain pins including the thermal pad because they are connected together.

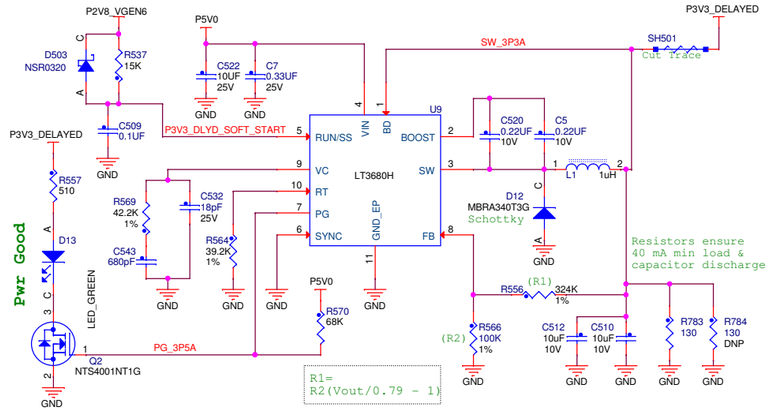
When CPU Card is plugged into Base Board 26662, part of the power is sourced from P5V0 and part is supplied by VBAT to avoid overloading the 5-V regulator on 26662.



PMIC Power Feed 4.3 A Max Load

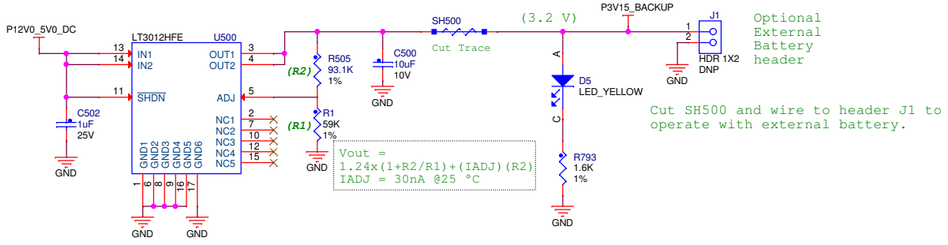


Peripheral Power Supply 2.4 A Max Load



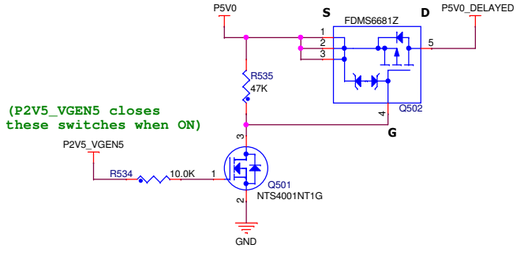
P3V3_DELAYED voltage is actually 3.35 V nominal for compatibilty with Base Board 26662. For customer production product, Freescale recommends R1 = 317k 1% for 3.3 V nominal.

Backup Supply for Real-Time Clock, etc.



3.2 V @ 3 mA max load

5 V delay FET



ICAP Classification:	CP: ___ IUO: ___ PUBI: _X_	
Drawing Title:	MCIMX6QPAICPU3	
Page Title:	Main PWR	
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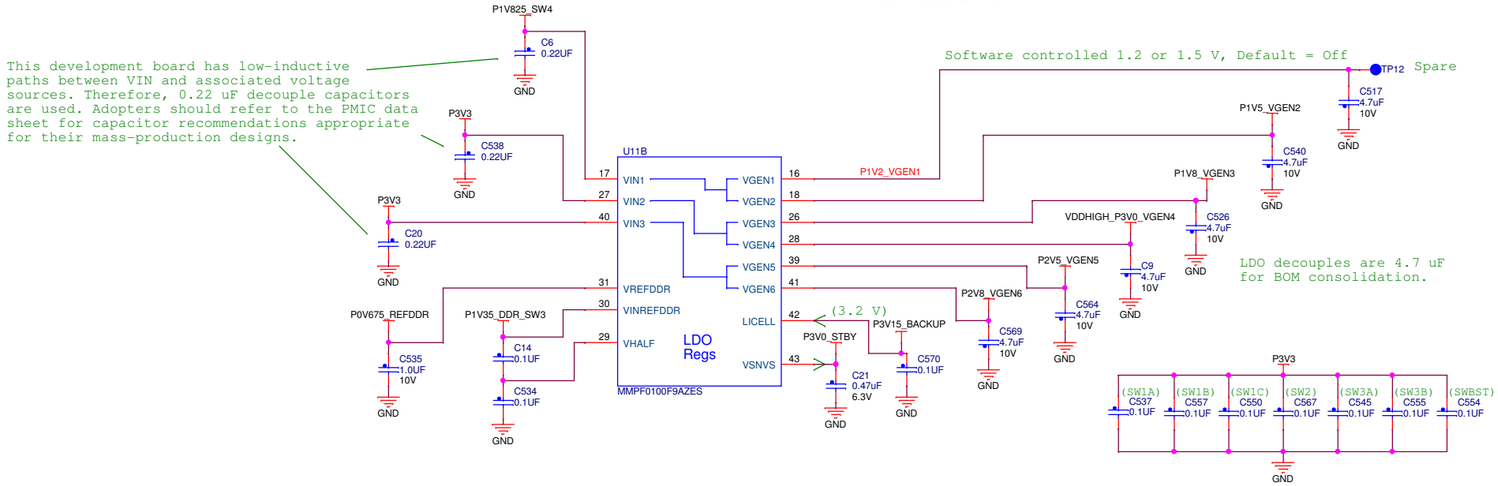
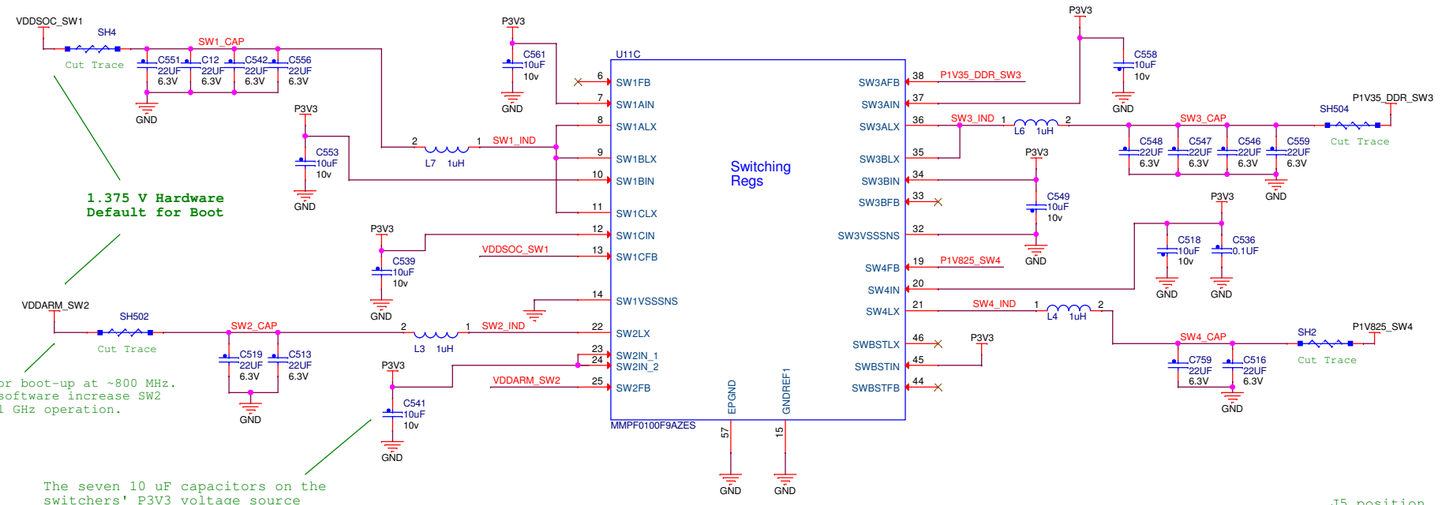
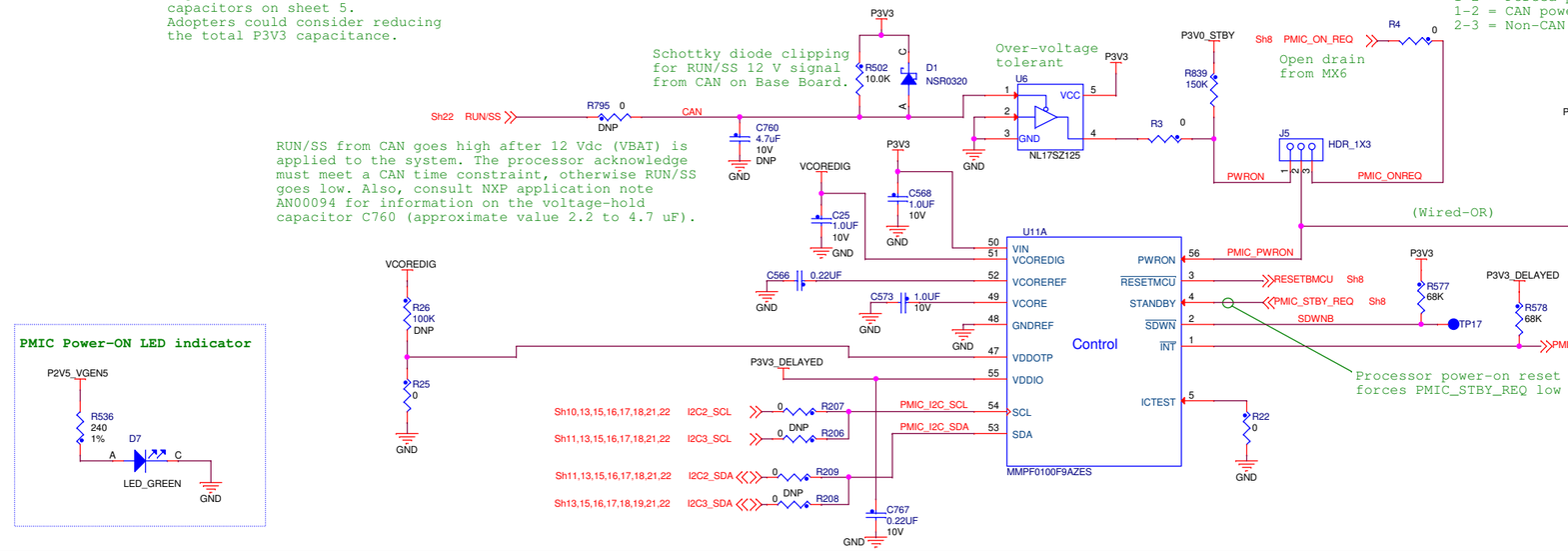
PMIC

1.825 V setpoint ensures compliance with VIN1 min voltage spec

This development board has low-inductive paths between VIN and associated voltage sources. Therefore, 0.22 uF decouple capacitors are used. Adopters should refer to the PMIC data sheet for capacitor recommendations appropriate for their mass-production designs.







PMIC Power-ON LED indicator

Peripheral Power Rails

Voltage (V)	Rail Name	Block	Power Source	Generated By	Max Current (A)
5	P5V0_DELAYED	RGB LCD	Main Power	Base Board or Jack (Note 2)	3 or 5
		LVDS LCD			
		HDMI			
		MIPI			
	P5V0_OTG_VBUS	USB			0.5
	P5V0_H1_VBUS	USB		Base Board	0.8
3.3	P3V3_DELAYED	NAND Flash	VOUT1	LT3680	2.4
		SD Slot			
		NOR Flash			
		HDMI			
		LVDS LCD			
		Ethernet			
		UART			
		MIPI			
		Mini PCIE			
3.0	P3V0_VDD_USB	USB	VDDUSB_CAP	iMX	-
2.8	P2V8_VGEN6	MIPI	VGEN6	PMIC	0.2
2.5	P2V5_VGEN5	Note 1	VGEN5	PMIC	0.1
1.825	P1V825_SW4	MIPI	SW4	PMIC	1.0
1.8	P1V8_VGEN3	SD Slot	VGEN3	PMIC	0.1
1.5,1.8,2.5	P_ENET_VDDIO	ENET	ENET Card	Card Reg	0.15/0.5
1.5	P1V5_VGEN2	Mini PCIE	VGEN2	PMIC	0.25
1.35	P1V35_DDR_SW3	DDR	SW3A/B	PMIC	2.5
0.675	P0V675_REFDDR	DDR	VREFDDR	PMIC	0.01

Note 1	Powers AUDIO_REF_24MHZ level converter, PMIC power LED, & turns on P5V0_DELAYED FET
Note 2	Use of CPU Card SD port in full-speed SDXC mode simultaneous with ethernet
	in Gbit mode may exceed the 5V supply current rating sourced from the Base Board.

See sheet 25 for additional information.

ICAP Classification:	CP: ___	IUO: ___	PUBI: X_
Drawing Title:	MCIMX6QPAICPU3		
Page Title:	PMIC		
Size C	Document Number SCH-28615 PDF: SPF-28615		Rev A3
Date: Friday, February 26, 2016		Sheet 6 of 25	

MX6 Power

U1E

i.MX6Q - POWER

VDDARM_SW2

1.375 V default for boot

C613 0.22UF, C617 0.22UF, C615 0.22UF, C614 0.22UF, C616 0.22UF, C620 22UF 6.3V, C653 22UF 6.3V → GND

VDDARM_IN_1 H14, VDDARM_IN_2 J14, VDDARM_IN_3 K14, VDDARM_IN_4 L14, VDDARM_IN_5 M14, VDDARM_IN_6 N14, VDDARM_IN_7 P14, VDDARM_IN_8 R14

C662 0.22UF, C666 0.22UF, C665 0.22UF, C664 0.22UF, C663 0.22UF, C661 0.22UF, C62 22UF 6.3V → GND

VDDARM23_IN_1 K9, VDDARM23_IN_2 L9, VDDARM23_IN_3 M9, VDDARM23_IN_4 N9, VDDARM23_IN_5 P9, VDDARM23_IN_6 R9, VDDARM23_IN_7 T9, VDDARM23_IN_8 U9

Diode ensures VDD_SNVS_IN is always powered whenever VDDHIGH_IN is powered to meet data sheet spec even if P3V0_STBY faults to 0 V. See Hardware Development Guide doc IMX6DQ6SDLHDG.

VDDSOC_SW1

1.375 V default for boot

C679 0.22UF, C70 22UF 6.3V, C691 22UF 6.3V → GND

VDDSOC_IN_1 H16, VDDSOC_IN_2 J16, VDDSOC_IN_3 K16, VDDSOC_IN_4 L16, VDDSOC_IN_5 M16, VDDSOC_IN_6 N16, VDDSOC_IN_7 P16, VDDSOC_IN_8 R16, VDDSOC_IN_9 T16, VDDSOC_IN_10 U16

VDDHIGH_P3V0_VGEN4

C619 0.22UF, C60 10uF 10V → GND

D17 NSR0320

P3V0_STBY → R43 0 → VDD_SNVS_IN

C784 0.22UF → GND

VDDHIGH_IN_1 H9, VDDHIGH_IN_2 J9

VDD_SNVS_IN G11

GND_1 A13, GND_2 A25, GND_3 A4, GND_4 A8, GND_5 AA10, GND_6 AA13, GND_7 AA16, GND_8 AA19, GND_9 AA22, GND_10 AA7, GND_11 AB24, GND_12 AB3, GND_13 AD10, GND_14 AD13, GND_15 AD16, GND_16 AD19, GND_17 AD22, GND_18 AD4, GND_19 AD7, GND_20 AE1, GND_21 AE25, GND_22 B4, GND_23 C1, GND_24 C10, GND_25 C4, GND_26 C6, GND_27 D3, GND_28 D6, GND_29 D8, GND_30 E5, GND_31 E6, GND_32 E7, GND_33 F5, GND_34 F6, GND_35 F7, GND_36 F8, GND_37 G10, GND_38 G19, GND_39 G3, GND_40 H12, GND_41 H15, GND_42 H18, GND_43 H8, GND_44 J12, GND_45 J15, GND_46 J18, GND_47 J2, GND_48 J8, GND_49 K10, GND_50 K12, GND_51 K15, GND_52 K18, GND_53 K8, GND_54 L10, GND_55 L12, GND_56 L15, GND_57 L18, GND_58 L2, GND_59 L5, GND_60 L8, GND_61 M10, GND_62 M12, GND_63 M15, GND_64 M18, GND_65 M8, GND_66 N10, GND_67 N15, GND_68 N18, GND_69 N8, GND_70 P10, GND_71 P12, GND_72 P15, GND_73 P18, GND_74 P8, GND_75 R12, GND_76 R15, GND_77 R17, GND_78 R8, GND_79 T11 → GND

MCIMX6QP6AVT1AA

VDDARM_CAP_1 H13, VDDARM_CAP_2 J13, VDDARM_CAP_3 K13, VDDARM_CAP_4 L13, VDDARM_CAP_5 M13, VDDARM_CAP_6 N13, VDDARM_CAP_7 P13, VDDARM_CAP_8 R13

VDDARM_CAP: C649 0.22UF, C642 0.22UF, C643 0.22UF, C644 0.22UF, C652 22UF 6.3V → GND

VDDARM23_CAP_1 H11, VDDARM23_CAP_2 J11, VDDARM23_CAP_3 K11, VDDARM23_CAP_4 L11, VDDARM23_CAP_5 M11, VDDARM23_CAP_6 N11, VDDARM23_CAP_7 P11, VDDARM23_CAP_8 R11

VDDARM_CAP: C630 0.22UF, C628 0.22UF, C629 0.22UF, C633 0.22UF, C640 22UF 6.3V → GND

VDDSOC_CAP

{DVFS not allowed on VDDSOC}

C626 0.22UF, C631 0.22UF, C647 0.22UF, C648 0.22UF, C667 0.22UF, C668 0.22UF, C637 0.22UF, C654 22UF 6.3V → GND

VDDSOC_CAP_1 R10, VDDSOC_CAP_2 T10, VDDSOC_CAP_3 T13, VDDSOC_CAP_4 T14, VDDSOC_CAP_5 U10, VDDSOC_CAP_6 U13, VDDSOC_CAP_7 U14

VDDPU_CAP

C687 0.22UF, C686 0.22UF, C689 0.22UF, C688 0.22UF, C685 0.22UF, C692 22UF 6.3V, C119 22UF 6.3V → GND

VDDPU_CAP_1 H17, VDDPU_CAP_2 J17, VDDPU_CAP_3 K17, VDDPU_CAP_4 L17, VDDPU_CAP_5 M17, VDDPU_CAP_6 N17, VDDPU_CAP_7 P17

VDDHIGH_CAP

C623 0.22UF, C57 10uF 10V → GND

VDD_CACHE_CAP N12

~ 2.5 V

VDDHIGH_CAP_1 H10, VDDHIGH_CAP_2 J10

VDD_SNVS_CAP G9 — VDD_SNVS_CAP — C609 0.22UF → GND

NVCC_LCD P19 — {NVCC_LCD} — C702 0.22UF → GND — P3V3_DELAYED_NVCC

NVCC_CSI N7 — {NVCC_CSI} — C603 0.22UF → GND — P3V3_DELAYED_NVCC

NVCC_MIPI K7 — NVCC_MIPI

NVCC_EIM0 K19

SH506 Cut Trace — VDDHIGH_CAP

C612 0.22UF → GND

NVCC_EIM1 L19

NVCC_EIM2 M19

{NVCC_EIM0} — P3V3_DELAYED_NVCC — C710 10uF 10V, C78 10uF 10V → GND

NVCC_ENET R19

NVCC_GPIO P7

NVCC_PLL_OUT E8

~ 1.1 V

{NVCC_EIM1} {NVCC_EIM2} — P3V3_DELAYED_NVCC — C594 0.22UF, C701 0.22UF, C40 10uF 10V, C583 10uF 10V → GND

NVCC_RGMII G18

NVCC_SD1 G16

NVCC_SD2 G17

NVCC_SD3 G14

NVCC_NANDF G15

NVCC_JTAG J7

{NVCC_ENET} — P3V3_DELAYED_NVCC — C695 0.22UF → GND

{NVCC_GPIO} — P3V3_DELAYED_NVCC — C604 0.22UF → GND

GPANAIO C8 — TP24

FA_ANA A5 — TP23

VDD_FA B5 — TP22

NVCC_PLL_OUT

C608 0.22UF, C778 10uF 10V → GND

SH508 Cut Trace

SH509 Cut Trace

NVCC_RGMII — NVCC_RGMII

C700 0.22UF → GND — Controlled on Ethernet sheet

{NVCC_SD1} {NVCC_SD2} — P3V3_DELAYED_NVCC — C705 0.22UF → GND

NVCC_SD3 — C657 0.22UF → GND

{NVCC_NANDF} — P3V3_DELAYED_NVCC — C673 0.22UF → GND

{NVCC_JTAG} — P3V3_DELAYED_NVCC — C611 0.22UF → GND

DDR module under-BGA decoupling

P1V35_DDR_SW3

C592 0.22UF 10V, C54 22UF 6.3V, C77 22UF 6.3V → GND

These capacitors are part of DDR3 module on sheet 9.

MX6 power domains under-BGA decoupling

P1V35_DDR_SW3

C635 0.22UF, C627 0.22UF, C621 0.22UF, C690 0.22UF, C681 0.22UF, C655 22UF 6.3V, C49 22UF 6.3V → GND

C634 0.22UF, C646 0.22UF, C674 0.22UF, C697 0.22UF, C699 0.22UF, C698 0.22UF → GND

VDDSOC_SW1

C684 0.22UF, C683 0.22UF, C682 0.22UF, C675 0.22UF, C676 0.22UF, C677 0.22UF, C678 0.22UF, C669 22UF 6.3V → GND

SDa (SD3) power source for MX6 I/O.
Required for SDXC UHS-1 I/O logic level change.

P3V3_DELAYED, P1V8_VGEN3 → R640 DNP 0, R631 DNP 0 → NVCC_SD3

P3V3_DELAYED → C625 0.1UF → GND

U508 ADG849 (VDD, S2, S1, IN, D, GND)

Sh11 SDa_VSELECT(SD3_VSEL_GPIO_18) → R638 4.7K → GND

R633 0

0 = S1 closed
1 = S2 closed

Voltage for the MX6 supplies fed by rail P3V3_DELAYED_NVCC are provided through SH9.

P3V3_DELAYED_NVCC — SH511 Cut Trace — P3V3_DELAYED

ICAP Classification:	CP: ___	IUO: ___	PUBI: X_
Drawing Title:	MCIMX6QPAICPU3		
Page Title:	iMX6 Power		
Size C	Document Number SCH-28615 PDF: SPF-28615		Rev A3
Date: Friday, February 26, 2016	Sheet 7 of 25		

MX6 Control

CPU Warm Reset

Reset sources (wired-OR):
Pushbutton SW1,
JTAG, and PMIC;
WDOG option.

Forces Reboot

22 kohm pull-up resistor on Base Board also

210 ms negative pulse

1.5 ms negative pulse

Open Drain

{2.3V Threshold}
{1.5 ms delay}
{Open Drain}

Wired OR

Effective pull-up resistance on MX_POR_B is approx 60 kohm due to the MX6 on-chip 100 kohm pull-up resistor.

From WDOG option

From PMIC

Level Shifter
(Sink only)

(Over-voltage tolerant)

Four sources (wired-OR):
Pushbutton SW1,
JTAG, PMIC, and WDOG1)

5V powers the Voltage Supervisor initially but does not allow it to reach the threshold. The 3.3V power is the final voltage in the power sequence. This will trip the threshold and begin the time-out for POR release.

When Tamper is used in an end product, instead of a connection to the standby voltage sourced from the vehicle battery, a dedicated coin cell could be employed for security.

Boot Mode
Tamper
SPI NOR Write Protect

BOOT_MODE[1:0] SETTINGS
00 = Fuses
01 = Serial downloader
10 = Internal (development)
11 = Reserved

S3 Pos 4 = SPI NOR Flash
Off = Write protected
On = Not write protected

(These 3 resistors are DNP due to on-chip Pull-down on MX6)

Note 1

R788 = bias resistor.
See Chip Errata doc IMX6DQCE.

HEATSINK

Freescale P/N: 901-76751

Manufacturer: CTS
CTS P/N: APF19-19-13CB/A01
Description:
HW ACCESSORY,
HEATSINK FORGED
W/ADHESIVE TAPE,
0.748"L X 0.748"W X 0.5"H

JTAG Adapter Board Connector

Adapter with cable supplied with kit.
Pull resistors reduce input resistance and ESD suseptability.

{I/O Ref}

J17 notch on pin 1 side

MX6 has on-chip pull-up on TCK.

Platform Clocks

100-ohm differential pair

Input if External Oscillator is used.

100-ohm differential pairs

2.5 V Signal Level

3.3 V Signal Level

Level Shifter
Over-voltage tolerant

Peripheral Reset

For peripherals on CPU Card only
Two sources: Pushbutton SW2 or I/O port expander A.

RC = 68 ms
C761 provided to adjust peripheral power-up reset time out.

1. Designers should calculate the maximum current drawn from the P3V0_STBY rail for their application at hot temperature. For applications exceeding 400 uA, MX6 VDD_SNVS_IN can be directly powered by P3V0_VDDHIGH_SW2 or other 3 V source. The PF100 PMIC is limited to 400 uA. See the data sheets.

ICAP Classification:	CP: ___	IUO: ___	PUBI: X
Drawing Title:	MCIMX6QPAICPU3		
Page Title:	MX6 Control, POR-RST, JTAG		
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Clock terminators: Place at end of route at each DDR pair

GND probe pads

DRAM_SDCLK0 — R56 200 1% — DRAM_SDCLK0_B

DRAM_SDCLK1 — R37 200 1% — DRAM_SDCLK1_B

TP28 GND, TP27 GND

DRAM_D[63:0]

DRAM_A[15:0]

U1J

i.MX6Q - DDR

MCIMX6QP6AVT1AA

R791 minimizes standby current drain in DSM (Deep-Sleep Mode).

P1V35_DDR_SW3

U3

4G_DDR3_SDRAM_256MX16

MT41K256M16HA-125:E

Top right

P0V675_REFDDR

R44 240 1% GND — DRAM0_ZQ

C622 0.22UF 16V, C47 0.22UF 16V

DRAM_DQM0, DRAM_DQM1

NC_J1 J9, NC_J9 L1, NC_L1 L9, NC_L9 M7 DRAM_A15, NC_M7

P1V35_DDR_SW3

U5

4G_DDR3_SDRAM_256MX16

MT41K256M16HA-125:E

Bottom under U3

P0V675_REFDDR

R609 240 1% GND — DRAM1_ZQ

C693 0.22UF 16V, C589 0.22UF 16V

DRAM_DQM3, DRAM_DQM2

NC_J1 J9, NC_J9 L1, NC_L1 L9, NC_L9 M7 DRAM_A15, NC_M7

Clock access points

SH8 DDR_SDCLK0 — Cut Trace — DRAM_SDCLK0

SH7 DDR_SDCLK0_B — Cut Trace — DRAM_SDCLK0_B

SH5 DDR_SDCLK1 — Cut Trace — DRAM_SDCLK1

SH6 DDR_SDCLK1_B — Cut Trace — DRAM_SDCLK1_B

GND probe pad

TP26 GND

P1V35_DDR_SW3

U2

4G_DDR3_SDRAM_256MX16

MT41K256M16HA-125:E

Top left

P0V675_REFDDR

C599 0.1UF GND — DRAM_VREF

R46 240 1% GND — ZQPAD

R59 240 1% GND — DRAM2_ZQ

C81 0.22UF 16V, C66 0.22UF 16V

DRAM_DQM4, DRAM_DQM5

NC_J1 J9, NC_J9 L1, NC_L1 L9, NC_L9 M7 DRAM_A15, NC_M7

P1V35_DDR_SW3

U4

4G_DDR3_SDRAM_256MX16

MT41K256M16HA-125:E

Bottom under U2

P0V675_REFDDR

R45 240 1% GND — DRAM3_ZQ

C714 0.22UF 16V

DRAM_DQM7, DRAM_DQM6

NC_J1 J9, NC_J9 L1, NC_L1 L9, NC_L9 M7 DRAM_A15, NC_M7

P1V35_DDR_SW3

C618 C584 C585 C636 C85 0.22UF 16V

C588 C587 C586 C595 0.22UF 16V

P1V35_DDR_SW3

C716 C715 C713 C712 C711 C694 0.22UF 16V

P1V35_DDR_SW3

C84 C71 C717 C67 C68 C69 C75 0.22UF 16V

P1V35_DDR_SW3

C79 C80 C82 C83 C87 C86 0.22UF 16V, 6.3V

P1V35_DDR_SW3

C39 C61 C44 C46 C37 C34 0.22UF 16V, 6.3V

C45 C42 C41 C59 C43 0.22UF 16V

T32 T62 T12, T43 T69 T19, T30 T55 T5, T44 T63 T13, T41 T67 T17, T28 T53 T3, T39 T65 T15, T26 T51 T1, T38 T64 T14, T29 T54 T4, T35 T59 T9, T42 T68 T18, T31 T56 T6, T27 T52 T2, T40 T66 T16, T33 T57 T7

DRAM_A0, DRAM_A1, DRAM_A2, DRAM_A3, DRAM_A4, DRAM_A5, DRAM_A6, DRAM_A7, DRAM_A8, DRAM_A9, DRAM_A10, DRAM_A11, DRAM_A12, DRAM_A13, DRAM_A14, DRAM_A15

T34 T58 T8, T45 T70 T20, T46 T71 T21, T36 T60 T10, T37 T61 T11, T49 T74 T24, T47 T72 T22, T48 T73 T23, T50 T75 T25

DRAM_SDBA0, DRAM_SDBA1, DRAM_SDBA2, DRAM_CS0_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_WE_B, DRAM_SDCKE0, DRAM_SDODT0

T-point routing
Components allow pin to pin route length matching

NOTE 1:

Using bit swapping for DATA bus to allow easy pcb routing.

When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.

This design utilizes a consumer device. Freescale suggests consulting the supplier for the equivalent automotive-grade device information.

ICAP Classification: CP: ___ IUO: ___ PUBI: _X_

Drawing Title: **MCIMX6QPAICPU3**

Page Title: **LV DDR3 DRAM 2 GByte Total (256M x 16-bit each)**

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Parallel & Serial NOR FLASH, BOOT Select

U1A

i.MX6Q - EIM

MCIMX6QP6AVT1AA

NVCC_EIM1 / NVCC_EIM0 / NVCC_EIM2

EIM_LBA	K22	EIM_LBA	EIM_LBA
EIM_OE	J24	EIM_OE_B	R688 0 → GPS_INT_B(EIM_LBA_GPIO2_27) Sh22
EIM_RW	K20	EIM_WE_B	
EIM_CS0	H24	NOR_CE_B(EIM_CS0)	
EIM_CS1	J23		→ MLB_PWRDN(EIM_CS1_GPIO2_24) Sh22
EIM_A16	H25	EIM_A16	
EIM_A17	G24	EIM_A17	
EIM_A18	J22	EIM_A18	
EIM_A19	G25	EIM_A19	
EIM_A20	H22	EIM_A20	
EIM_A21	H23	EIM_A21	
EIM_A22	F24	EIM_A22	
EIM_A23	J21	EIM_A23	
EIM_A24	F25	EIM_A24	SH507 Cut Trace → EIMD18_I2C3_STEER(EIM_A24) Sh19
EIM_A25	H19	EIM_A25	R657 0 → HDMI_CEC(EIM_A25) Sh13
EIM_D16	C25	EIM_D16	EIM_D16 → EIM_D16 Sh15 **ENET SPI**
EIM_D17	F21	EIM_D17	EIM_D17 → EIM_D17 Sh15 **ENET SPI**
EIM_D18	D24		EIM_D18 Sh19 — Muxed flash data and I2C3_SDA
EIM_D19	G21	EIM_D19	
EIM_D20	G20	EIM_D20	
EIM_D21	H20	EIM_D21	
EIM_D22	E23	EIM_D22	
EIM_D23	D25	EIM_D23	
EIM_D24	F22	EIM_D24	
EIM_D25	G22	EIM_D25	
EIM_D26	E24	EIM_D26	
EIM_D27	E25	EIM_D27	
EIM_D28	G23	EIM_D28	
EIM_D29	J19	EIM_D29	
EIM_D30	J20	EIM_D30	EIM_D30 Sh19 — Muxed flash data and UART3_CTS
EIM_D31	H21	EIM_D31	
EIM_EB2	E22	EIM_EB2	
EIM_EB3	F23	EIM_EB3	
EIM_BCLK	N22		R674_DNP 0 → ACCEL_INT1_B(EIM_BCLK_GPIO6_31) Sh22; ACCEL_INT2_B(EIM_BCLK_ GPIO6_31) Sh22
EIM_WAIT	M25	EIM_WAIT	
EIM_EB0	K21	EIM_EB0	
EIM_EB1	K23	EIM_EB1	
EIM_DA0	L20	EIM_DA0	
EIM_DA1	J25	EIM_DA1	
EIM_DA2	L21	EIM_DA2	
EIM_DA3	K24	EIM_DA3	
EIM_DA4	L22	EIM_DA4	
EIM_DA5	L23	EIM_DA5	
EIM_DA6	K25	EIM_DA6	
EIM_DA7	L25	EIM_DA7	
EIM_DA8	L24	EIM_DA8	
EIM_DA9	M21	EIM_DA9	
EIM_DA10	M22	EIM_DA10	
EIM_DA11	M20	EIM_DA11	
EIM_DA12	M24	EIM_DA12	
EIM_DA13	M23	EIM_DA13	
EIM_DA14	N23	EIM_DA14	
EIM_DA15	N24	EIM_DA15	

I2C2 Clock

P3V3_DELAYED — R53 4.7K (Associated data on sheet 11) → I2C2_SCL Sh6,13,15,16,17,18,21,22

EIM_WAIT R684 0 → USB_HOST1_OC_B(EIM_WAIT_GPIO5_0) Sh22

EIM_EB0 R63 0 → TOUCH_INT_B(EIM_EB0_ GPIO2_GPIO[28]) Sh16

EIM_EB1 R668 0 → COMPASS_INT(EIM_EB1_GPIO2_29) Sh22

P3V3_DELAYED — U516 NC7SP126 — R703 0 — R107 68K — GND

Hi-Z_FOR_BOOT_B Sh8,16,22

UART3_RTS(EIM_EB3) Sh22 — Bluetooth

Ensures high-Z at boot-up to allow development boot configuration.

Boot Configuration Select

Switch mapping with the configuration options is described on the Notes page of the schematics.

R517 can be 0 ohms.

P3V3_DELAYED NVCC_EIM2 — R517 120, R525–R528 DNP 0

P3V3_DELAYED NVCC_EIM1 — S1 SW_DIP-10/SM, R529–R534 DNP 0

P3V3_DELAYED NVCC_EIM0 — S2 SW DIP-4, R535–R540 DNP 0, R523 0

RN501 10K, RN500 10K, RN502 10K, RN503 10K

BT_CFG1_0	R667	4.7K	EIM_DA0
BT_CFG1_1	R78	4.7K	EIM_DA1
BT_CFG1_2	R683	4.7K	EIM_DA2
BT_CFG1_3	R686	4.7K	EIM_DA3
BT_CFG1_4	R662	4.7K	EIM_DA4
BT_CFG1_5	R691	4.7K	EIM_DA5
BT_CFG1_6	R687	4.7K	EIM_DA6
BT_CFG1_7	R55	4.7K	EIM_DA7
BT_CFG2_0	R66	4.7K	EIM_DA8
BT_CFG2_1	R673	4.7K	EIM_DA9
BT_CFG2_2	R663	4.7K	EIM_DA10
BT_CFG2_3	R682	4.7K	EIM_DA11
BT_CFG2_4	R62	4.7K	EIM_DA12
BT_CFG2_5	R52	4.7K	EIM_DA13
BT_CFG2_6	R685	4.7K	EIM_DA14
BT_CFG2_7	R61	4.7K	EIM_DA15
BT_CFG3_0	R74	4.7K	EIM_A16
BT_CFG3_1	R68	4.7K	EIM_A17
BT_CFG3_2	R669	4.7K	EIM_A18
BT_CFG3_3	R71	4.7K	EIM_A19
BT_CFG3_4	R692	4.7K	EIM_A20
BT_CFG3_5	R670	4.7K	EIM_A21
BT_CFG3_6	R58	4.7K	EIM_A22
BT_CFG3_7	R694	4.7K	EIM_A23
BT_CFG4_0	R60	4.7K	EIM_A24
BT_CFG4_1	R57	4.7K	EIM_WAIT
BT_CFG4_2	R65	4.7K	EIM_LBA
BT_CFG4_3	R690	4.7K	EIM_EB0
BT_CFG4_4	R54	4.7K	EIM_EB1
BT_CFG4_5	R679	4.7K	EIM_WE_B
BT_CFG4_6	R666	4.7K	EIM_EB2
BT_CFG4_7	R699	4.7K	EIM_EB3

Bus Isolation Resistors — DNP

To avoid resistor divider with R53 I2C pull-up, R666 is DNP.

32 MB Parallel NOR Flash

NOR Flash is bottom boot-block uniform (32Kword).
NOR Flash is sized for bootloaders, kernel images, and/or nonvolatile configuration/data storage.

P3V3_DELAYED — C725 0.1UF, C733 0.1UF — R721 10.0K, R719 10.0K DNP — NOR_WP_B/ACC

U510 FLASH TSOP56 14X20MM

EIM_DA0	31	A0	DQ0 35 EIM_D16
EIM_DA1	26	A1	DQ1 37 EIM_D17
EIM_DA2	25	A2	DQ2 39 EIM_D18_STEERED Sh15,19
EIM_DA3	24	A3	DQ3 41 EIM_D19
EIM_DA4	23	A4	DQ4 44 EIM_D20
EIM_DA5	22	A5	DQ5 46 EIM_D21
EIM_DA6	21	A6	DQ6 48 EIM_D22
EIM_DA7	20	A7	DQ7 50 EIM_D23
EIM_DA8	10	A8	DQ8 36 EIM_D24
EIM_DA9	9	A9	DQ9 38 EIM_D25
EIM_DA10	8	A10	DQ10 40 EIM_D26
EIM_DA11	7	A11	DQ11 42 EIM_D27
EIM_DA12	6	A12	DQ12 45 EIM_D28
EIM_DA13	5	A13	DQ13 47 EIM_D29
EIM_DA14	4	A14	DQ14 49
EIM_DA15	3	A15	DQ15/A-1 51 EIM_D31
EIM_A16	54	A16	EIM_D30_STEERED Sh19
EIM_A17	19	A17	
EIM_A18	18	A18	
EIM_A19	11	A19	
EIM_A20	12	A20	NC30 30, NC28 28, NC27 27, NC55 55, NC56 56
EIM_A21	15	A21	
EIM_A22	2	A22	
EIM_A23	1	A23	
EIM_OE_B	34	G	
EIM_WE_B	13	W	
NOR_BYTE_B/WORD	53	BYTE	
	14	RP	R/B 17 NOR_RDY_BSY_B → TP36
	32	E	
	33, 52	VSS1, VSS2	M29W256GL7AN6E

VCCQ 29, VCC 43, VPP-WP 16

P3V3_DELAYED — R739 10.0K — BYTE_B/WORD: 1 = 16-bit mode, 0 = 8-bit mode

Sh8 POR_3V3_B

P3V3_DELAYED — R104 150K — NOR_CE_B(EIM_CS0)

Effective pull-up resistance on NOR_CE_B(EIM_CS0) is approx 60 kohm due to the MX6 on-chip 100 kohm pull-up resistor.

Adopters should consider that U16 M25P32 is EOL (end of life) in 2016. Consider N25Q032A13ESCAOF.

4 MB SPI NOR Flash

Port = eCSPI1

Kernal and/or Boot Loader Storage

P3V3_DELAYED — C720 4.7uF 10V, C722 0.1UF

P3V3_DELAYED — R702 10.0K

ENET SPI — EIM_D18_STEERED — R715 0 — SPI_NOR_DIN

EIM_D16 — R711 0 — SPI_NOR_CLK

SPI_NOR_CS_B

SPI_NOR_WP_B

U16 M25P32-VMW3TGB: VCC, D, C, S, W/VPP, HOLD, VSS, Q

SPI_NOR_DOUT — R709 0 — ENET SPI EIM_D17

SPI_NOR_RST_B — R708 10.0K — P3V3_DELAYED

EIM_D19 — 74LCX125 U512B — NOR_CS_B — R697 33 — SS1

(Vih = 2.0 V)

Sh11,22 BOOT_COMPLETE(SD2_DAT1_GPIO1_14) — J3 HDR_1X3 — P3V3_DELAYED — R736 4.7K — GND

Sh8 SPI_NOR_WP_B

See Control sheet for write protect switch info

Jumper Boot Selection
1 - 2 Do not boot from SPI NOR (default)
2 - 3 Boot from SPI NOR

If SPI NOR is not utilized, BOOT_COMPLETE can be used as a GPIO on either the CPU Card or Main board by installing the jumper 1 - 2 and wiring to jumper pin 3. The signal is also routed to a card edge finger.

To allow SPI NOR boot when plugged into Base Board 26662:
Base Board rev B (green): Remove R193 on Base Board
Base Board rev E (orange): No changes

ICAP Classification:	CP: ___ IUO: ___ PUBI: X_
Drawing Title:	MCIMX6QPAICPU3
Page Title:	NOR FLASH, BOOT_SEL
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NAND FLASH, MLB, SD-MMC, CAN, WDOG

U1B

i.MX6Q

MCIMX6QP6AVT1AA

NVCC_SD1
SD1_CMD B21
SD1_CLK D20
SD1_DAT0 A21
SD1_DAT1 C20
SD1_DAT2 E19
SD1_DAT3 F18

Sh22 SDb_CMD
Sh22 SDb_CLK
Sh22 SDb_DAT0
Sh22 SDb_DAT1
Sh22 SDb_DAT2
Sh22 SDb_DAT3

NVCC_SD2
SD2_CMD F19
SD2_CLK C21
SD2_DAT0 A22
SD2_DAT1 E20
SD2_DAT2 A23
SD2_DAT3 B22

Sh22 HOME_(SD2_CMD_ GPIO1_11)
Sh22 ESAI_INT(SD2_CLK_ GPIO1_10)
Sh18 I2CPORTEXP_RST_B(SD2_DAT0_GPIO1_15)
Sh10,22 BOOT_COMPLETE(SD2_DAT1_GPIO1_14)
SDa_WP(SD2_DAT2_GPIO1_13)
Sh22 BACK_(SD2_DAT3_ GPIO1_12)

NVCC_SD3
SD3_CMD B13
SD3_CLK D14
SD3_DAT0 E14
SD3_DAT1 F14
SD3_DAT2 A15
SD3_DAT3 B15
SD3_DAT4 D13
SD3_DAT5 C13
SD3_DAT6 E13
SD3_DAT7 F13
SD3_RST D15

SDa_CMD(SD3_CMD)
SDa_CLK(SD3_CLK)
SDa_DAT0(SD3_DAT0)
SDa_DAT1(SD3_DAT1)
SDa_DAT2(SD3_DAT2)
SDa_DAT3(SD3_DAT3)
SDa_DAT4(SD3_DAT4)
SDa_DAT5(SD3_DAT5)
SDa_DAT6(SD3_DAT6)
SDa_DAT7(SD3_DAT7)
Sh20 SDa_RST_B(SD3_RST)

Reset is active low.

VDDHIGH_CAP
MLB_CP B11
MLB_CN A11
MLB_SP B9
MLB_SN A9
MLB_DP A10
MLB_DN B10

NVCC_ENET
ENET_MDC V20
ENET_MDIO V23
ENET_CRS_DV U21
ENET_REF_CLK V22
ENET_RX_ER W23
ENET_TX_EN V21
ENET_RXD0 W21
ENET_RXD1 W22
ENET_TXD0 U20
ENET_TXD1 W20

ESAI_TX5_RX0(ENET_MDC) Sh22
ESAI_SCKR(ENET_MDIO) Sh22
ESAI_SCKT(ENET_CRS_DIV) Sh22
TP510 Spare GPIO See Note 1
USB_OTG_ID(ENET_RX_ER) Sh12,21 AVB Signal, sh 21
ESAI_TX3_RX2(ENET_TX_EN) Sh22
VIDEO_ADC_INT_B(ENET_RXD0_GPIO1_27) Sh22
ESAI_FST(ENET_RXD1) Sh22
ESAI_TX4_RX1(ENET_TXD0) Sh22
AVB_MLBCLK(ENET_TXD1) Sh21 AVB Signal, sh 21

P3V3_DELAYED
R91 1.6K 1%
ENET_MDIO(KEY_COL1) Sh15

NVCC_GPIO
KEY_COL0 W5
KEY_ROW0 V6
KEY_COL1 U7
KEY_ROW1 U6
KEY_COL2 W6
KEY_ROW2 W4
KEY_COL3 U5
KEY_ROW3 T7
KEY_COL4 T6
KEY_ROW4 V5

UART4_TXD(KEY_COL0) Sh20
UART4_RXD(KEY_ROW0) Sh20
MLB_INT_B(KEY_ROW1) Sh15,22 ENET SPI
ENET_CAN1_IO(KEY_COL2) Sh19
CAN1_RXCAN(KEY_ROW2) Sh22
MAINBOARD_SPDIF_IN(KEY_COL3) Sh22
CAN2_TXCAN(KEY_COL4) Sh22
CAN2_RXCAN(KEY_ROW4) Sh22

P3V3_DELAYED
R19 4.7K
(Associated clk on sheet 10)
I2C2_SDA Sh6,13,15,16,17,18,21,22
I2C2 Data

P3V3_DELAYED
R23 4.7K
(Associated data on sheet 19)
I2C3_SCL Sh6,13,15,16,17,18,21,22
I2C3 Clock

GPIO_0 T5
GPIO_1 T4
GPIO_2 T1
GPIO_3 R7
GPIO_4 R6
GPIO_5 R4
GPIO_6 T3
GPIO_7 R3
GPIO_8 R5
GPIO_9 T2
GPIO_16 R2
GPIO_17 R1
GPIO_18 P6
GPIO_19 P5

GPS_32_kHz(CLKO_GPIO_0) Sh22
SDb_CD(GPIO_1) Sh22
GPIO_2 Sh21
CAN1_NERR_B(GPIO_4_GPIO1_4) Sh22
ESAI_TX2_RX3(GPIO_5) Sh22
GPIO_6 Sh21
UART2_TXD(GPIO_7) Sh19
UART2_RXD(GPIO_8) Sh19
GPIO_9
SPARE(GPIO_16) TP509 Spare GPIO See note 1
ESAI_TX0(GPIO_17) Sh22
SDa_VSELECT(SD3_VSEL_GPIO_18) Sh7
GPIO_19 Sh21 AVB Signal, sh 21

NVCC_NANDF
NANDF_CS0 F15
NANDF_CS1 C16
NANDF_CS2 A17
NANDF_CS3 D16
NANDF_ALE A16
NANDF_CLE C15
NANDF_WP E15
NANDF_RB0 B16
NANDF_D0 A18
NANDF_D1 C17
NANDF_D2 F16
NANDF_D3 D17
NANDF_D4 A19
NANDF_D5 B18
NANDF_D6 E17
NANDF_D7 C18

NANDF_CE0_B R680 0 SDa_CD_B(GPIO6_15)
NANDF_CE1_B
NANDF_CS2_B
NANDF_CE3_B R49 0 ESAI_TX1(NANDF_CS3) Sh22
NANDF_ALE
NANDF_CLE
NANDF_WP_B
NANDF_RB0
NANDF_D0 R649 0 SDb_DAT4 Sh22
NANDF_D1 R48 0 SDb_DAT5 Sh22
NANDF_D2 R647 0 SDb_DAT6 Sh22
NANDF_D3 R648 0 SDb_DAT7 Sh22

SD4_CLK E16 NAND_BT_WIFI_IO(SD4_CLK) Sh19
SD4_CMD B17 CMD R201 0 NAND_BT_WIFI_OUT(SD4_CMD) Sh19
Steering logic on Sheet 19

SD4_DAT0 D18
SD4_DAT1 B19 USB_OTG_OC_B(SD4_DAT0_GPIO2_8) Sh12
SD4_DAT2 F17 LVDS0_PARADISP_PWM3(SD4_DAT1) Sh16,17
SD4_DAT3 A20 LVDS1_PWM4(SD4_DAT2) Sh22
SD4_DAT4 E18 CAN2_NERR_B(SD4_DAT3_GPIO2_11) Sh22
SD4_DAT5 C19 PROG_(SD4_DAT4_ GPIO2_12) Sh22
SD4_DAT6 B20 UART2_RTS(SD4_DAT5) Sh22
SD4_DAT7 D19 UART2_CTS(SD4_DAT6) Sh22
VOL+_(SD4_DAT7_ GPIO2_15) Sh22

NAND Flash Socket
(TSOP48)

U19
980020-48-P2

P3V3_DELAYED
C737 10uF 10V
C736 0.1UF
C738 0.1UF
GND

NANDF_D0 29
NANDF_D1 30
NANDF_D2 31
NANDF_D3 32
NANDF_D4 41
NANDF_D5 42
NANDF_D6 43
NANDF_D7 44
NANDF_CLE 16
NANDF_ALE 17
NANDF_CE0_B 9
NANDF_RE_B(SD4_CMD) Sh19
NANDF_WE_B(SD4_CLK) Sh19
NANDF_WP_B 19
NANDF_RB0 7
NANDF_NC48 48
NANDF_NC39 39

NANDF_RB0
NANDF_RB3 R758 0
NANDF_RB2 R754 0
NANDF_RB1 R750 0
NANDF_CE1_B
NANDF_CE3N
NANDF_CE4N
R738 DNP 0 NANDF_CE0_B
R755 DNP 0 NANDF_CS2_B
R729 DNP 0 NANDF_CE1_B
R727 DNP 0 NANDF_CE3_B
NANDF_NC25 R724 0
NANDF_NC34 R728 0
DQS TP511

P3V3_DELAYED
R762 10.0K
R760 0
GND

P3V3_DELAYED
R740 0
R752 10.0K DNP
GND

Compatible 64 Gb NAND Flash: MT29F64G08AFAAAWP.
Freescale suggests consulting supplier for automotive grade device information and/or lower density memory.
NAND FLASH is not included with shipped boards.

P3V3_DELAYED
R840 0
R602 10K
P3V3_DELAYED
R841 0
C742 0.1UF
GND

Sh17 DISP0_DAT8
LCD or WDOG1_B
R838 Ra 0
Rb
C780 2.2UF 10V
DOG1CAP_B
U21 NC7SP125P5X
Wired-OR
Rd
PMIC_PWRON Sh6
MX_POR_B Sh8
R211
Re
ESAI_FSR into processor or WDOG1_B out of processor
Sh22 ESAI_FSR(GPIO_9)
R32 Rc 0

--- WDOG1 ZERO-OHM OPTIONS TO BE INSTALLED BY USER ---

INFOTAINMENT
Install Ra, remove Rb, install Rc
System with audio; no parallel LCD bit 8

CLUSTER
Remove Ra, install Rb, remove Rc
System with parallel LCD, parallel NOR flash; no audio

SYSTEM POWER CYCLE
Install Rd, remove Re (default)

RESET PROCESSOR
Remove Rd, install Re

Reserved for WDOG Experiment
Mounted on Bottom
TP95
R300 DNP
TP96
TP97
R301 DNP
TP98
U100
TP104
TP103
TP102
STM6315RDW13F
210 ms negative pulse

WATCHDOG TIMING:
C780 is utilized as a blocking capacitor.

Experiment: Remove R840 and R841.
Wire R840 and R841 pad 2 to SH500 which is P3V15_BACKUP.

U100 is for different WDOG experiment.

Freescale recommends utilizing a fixed-supply for CD and WP pull-up voltage. Pull-ups should be on the same supply rail as the associated i.MX inputs, in this case NVCC_NANDF and NVCC_SD2.

SD UHS-1 & MMC

P3V3_DELAYED
NVCC_SD3
R642 10.0K DNP
R695 10.0K
R701 10.0K

SDa_DAT0(SD3_DAT0) 7
SDa_DAT1(SD3_DAT1) 8
SDa_DAT2(SD3_DAT2) 9
SDa_DAT3(SD3_DAT3) 1
SDa_DAT4(SD3_DAT4) R636 0 SDa_4 10
SDa_DAT5(SD3_DAT5) R641 0 SDa_5 11
SDa_DAT6(SD3_DAT6) R650 0 SDa_6 12
SDa_DAT7(SD3_DAT7) R678 0 SDa_7 13
SDa_CLK(SD3_CLK) 5
SDa_CMD(SD3_CMD) 2
SDa_CD_B(GPIO6_15) 14
SDa_WP(SD2_DAT2_GPIO1_13) 15

J14
CONN CRD 19
SDC013-A0-501F

DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
CLK
CMD
CD
WP
VDD
VSS1
VSS2
GND1
GND2
GND3
GND4

P3V3_SDa_SWITCHED
TP29
C696 10uF 10V
GND

SD, SDXC - Remove CMD pull-up resistor (default)
MMC, eMMC - Install CMD pull-up resistor

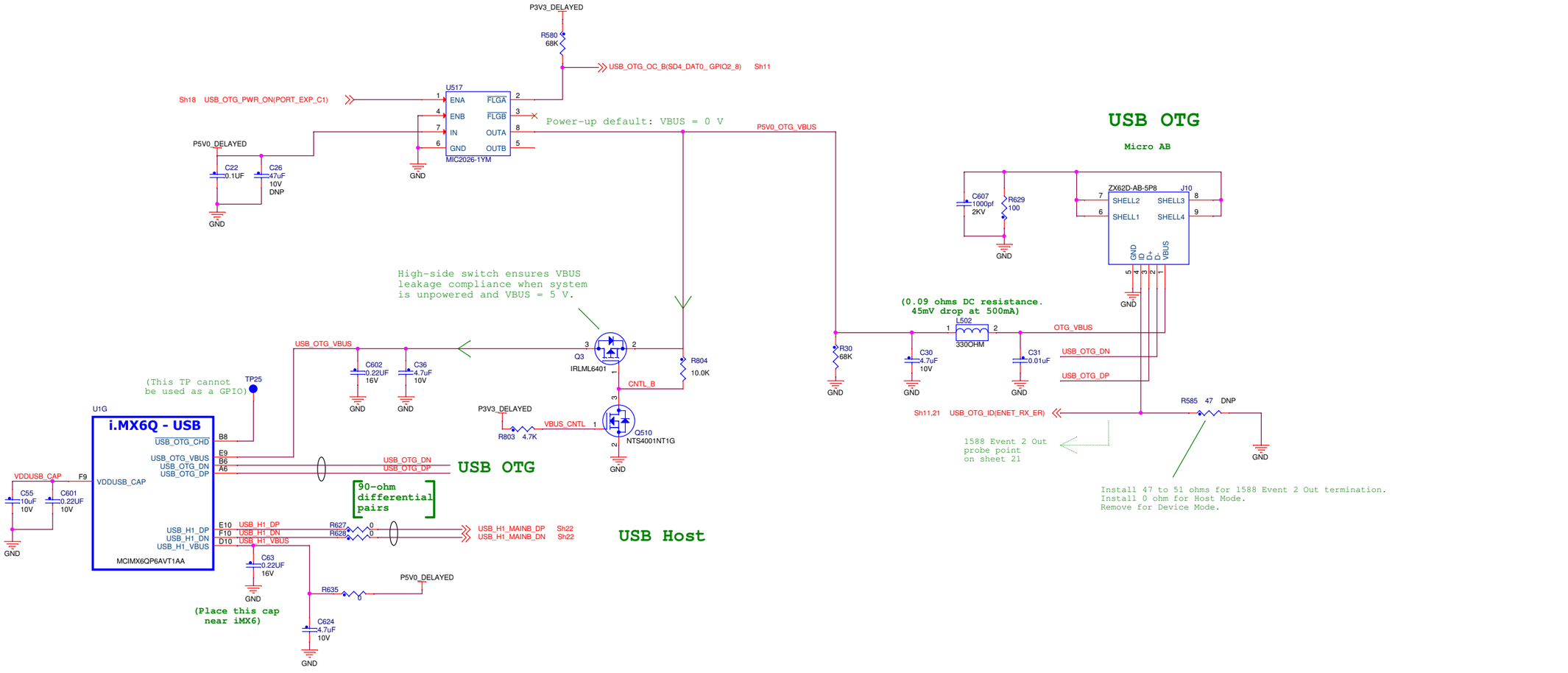
Socket handles 500 mA
SDXC = 800 mA max

SD Slot Pin Order
9
1
10
2
11
3
4
5
12
6
13
7
8
14
15

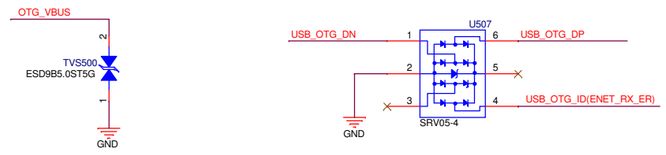
Note 1
Use of GPIO_16 as a ENET reference clock source is not required with MX6QR2.
The 125 MHz reference is routed on-chip.

ICAP Classification:	CP: ___ IUO: ___ PUBI: X_
Drawing Title:	MCIMX6QPAICPU3
Page Title:	NAND FLASH, SD-MMC, MLB, WDOG
Size C	Document Number SCH-28615 PDF: SPF-28615 Rev A3
Date: Friday, February 26, 2016	Sheet 11 of 25

USB OTG and Host



ESD Protection



USB_OTG_ID could cause backfeed through U507 when P3V3_DELAYED is not powered up. Therefore, pin 5 is not connected to a positive supply.

ICAP Classification: CP: ___ IUO: PUBI: X_

Drawing Title: **MCIMX6QPAICPU3**

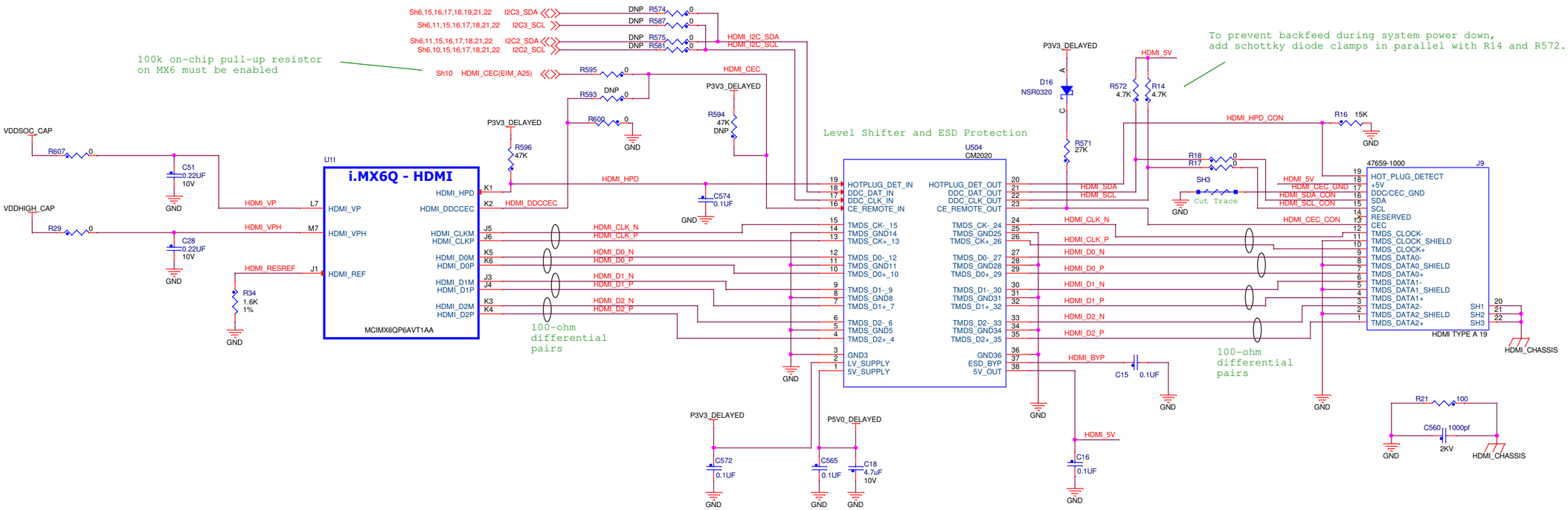
Page Title: **USB**

Size	Document Number	Rev
C	SCH-28615 PDF: SPF-28615	A3

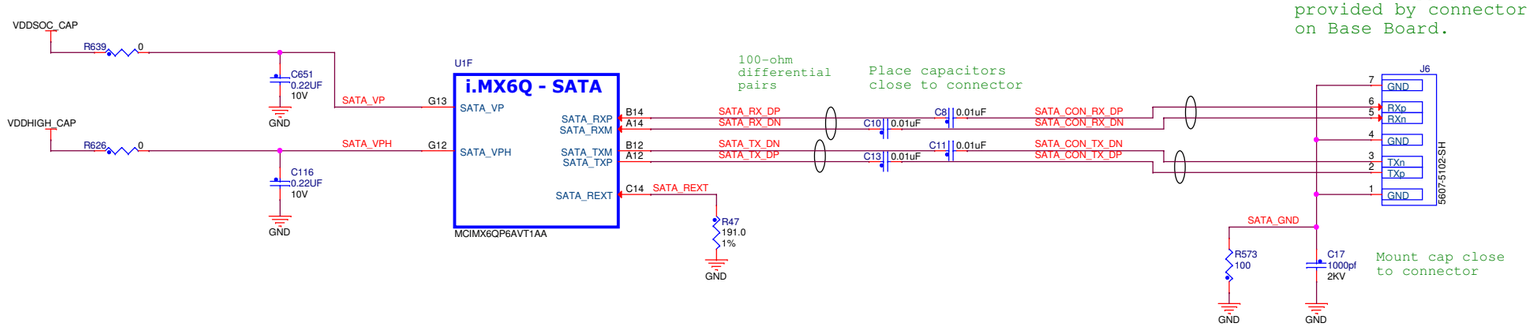
Date: Friday, February 26, 2016 Sheet 12 of 25

HDMI

HDMI for demonstration and prototyping; not used in vehicle.
Connecting I2C to DDC conflicts with audio.



SATA



ICAP Classification:	CP: ___ IUO:	PUBI: _X_
Drawing Title:	MCIMX6QPAICPU3	
Page Title:	HDMI, SATA	
Size: C	Document Number: SCH-28615 PDF: SPF-28615	Rev: A3
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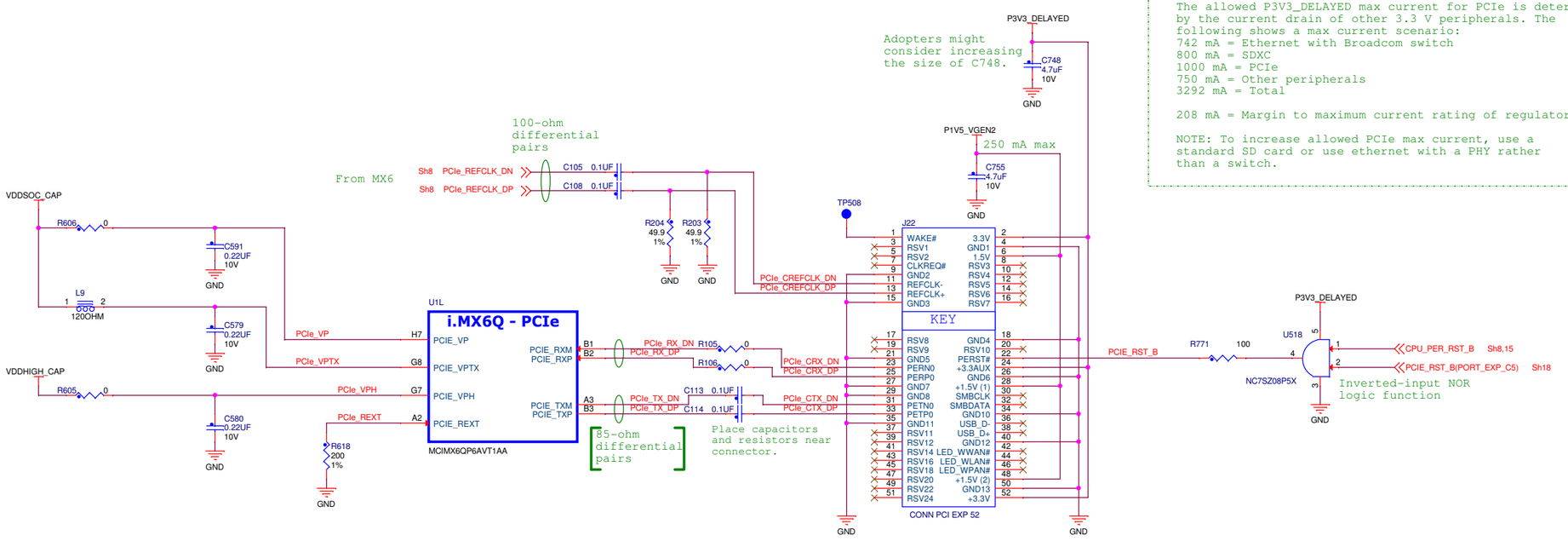
PCIE Connector

Facilitates both Mini and Half-Mini Form Factor

PCIe provided to support USB3.0.
See application note AN4784 for TX conformance test results.

Circuit board not tested for Reference Clock compliance.
See application note AN5158 for reference clock design.



The allowed P3V3_DELAYED max current for PCIe is determined by the current drain of other 3.3 V peripherals. The following shows a max current scenario:
742 mA = Ethernet with Broadcom switch
800 mA = SDXC
1000 mA = PCIe
750 mA = Other peripherals
3292 mA = Total

208 mA = Margin to maximum current rating of regulator

NOTE: To increase allowed PCIe max current, use a standard SD card or use ethernet with a PHY rather than a switch.

Layout considerations

TX pairs are usually routed on top layer

Length/skew compensation (trace serpentines) are not required for this Bus

Please remove ref plane under edgefinger pads

Use wide pair-to-pair spacing
(At least 5H TX vs TX and RX vs RX
use at least 7H for RX vs RX

If a mini PCIe extender is needed, adopters might consider M-Factors Storage JB-E0F0-8KNH or equivalent.

ICAP Classification: CP: ___ IUO: PUBI: X

Drawing Title: **MCIMX6QPAICPU3**

Page Title: **Mini PCI Express**

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Ethernet

U1K

i.MX6Q - RGMII

RGMII_TXC	D21	RGMII_TXC
RGMII_TD0	C22	RGMII_TXD0
RGMII_TD1	F20	RGMII_TXD1
RGMII_TD2	E21	RGMII_TXD2
RGMII_TD3	A24	RGMII_TXD3
RGMII_TX_CTL	C23	RGMII_TX_CTL
RGMII_RXC	B25	RGMII_RXC
RGMII_RD0	C24	RGMII_RXD0
RGMII_RD1	B23	RGMII_RXD1
RGMII_RD2	B24	RGMII_RXD2
RGMII_RD3	D23	RGMII_RXD3
RGMII_RX_CTL	D22	RGMII_RX_CTL

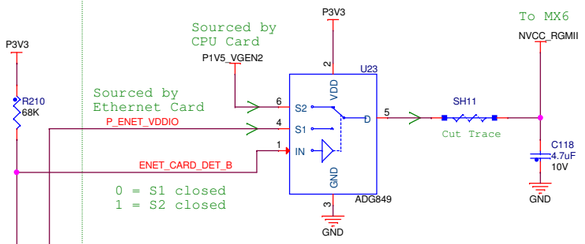
MCIMX6QP6AVT1AA

NVCC_RGMII Power Control

Ensures that NVCC_RGMII does not float if ethernet daughter card is not installed.

P3V3 powers up before other supplies

Bulk capacitor included due to remote I/O supply on Daughter Card.
Adopters with i.MX and PHY on same board do not need bulk capacitor.



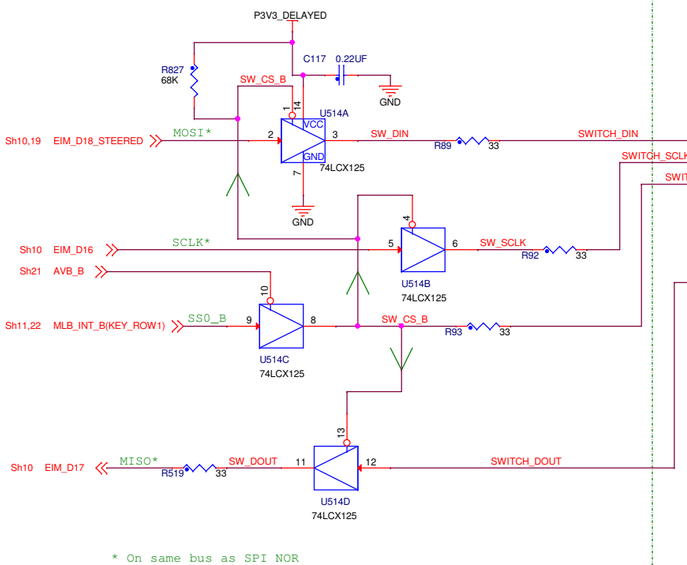
P_ETH_VDDIO_PWR Chart per Daughter Card

Atheros PHY RGMII: 1.5 or 1.8 V (default = 1.5 V)
Broadcom PHY RGMII: 2.5 V
Broadcom Switch: 2.5 V
Broadcom PHY MII: 3.3 V <-- Not used with MX6 CPU2

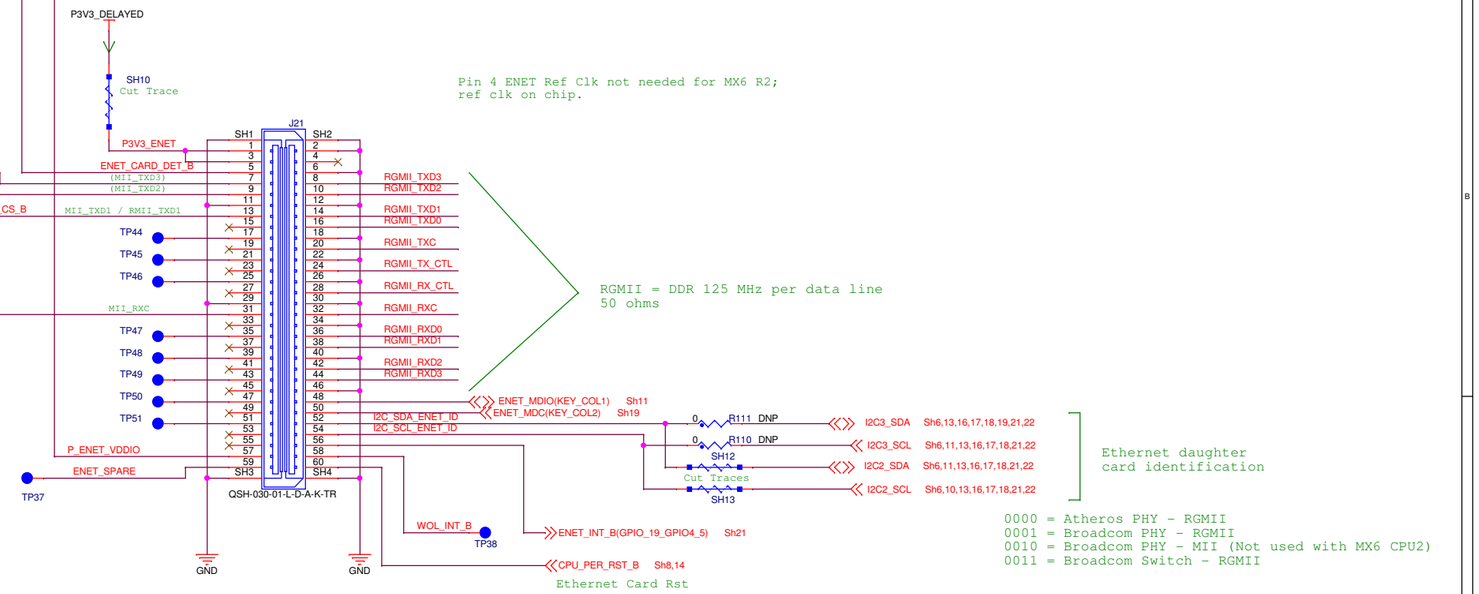
SPI for Switch Card Only

Resistor termination on switch card.
SS0-B also has clipping diode on switch card.

Avoid MLB_INT_B(KEY_ROW1) contention: do not plug card into Base Board MLB connector during ENET Switch use.



* On same bus as SPI NOR



0000 = Atheros PHY - RGMII
0001 = Broadcom PHY - RGMII
0010 = Broadcom PHY - MII (Not used with MX6 CPU2)
0011 = Broadcom Switch - RGMII

Mating conn = Samtec QTH series

Compatible Ethernet Daughter Cards

27953 = Atheros PHY - RGMII
27954 = Broadcom PHY - RGMII
27955 = Broadcom Switch - RGMII

Connector pin assignment per Agile DOC-01898.

ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: **MCIMX6QPAICPU3**

Page Title: **Ethernet**

Size	Document Number	Rev
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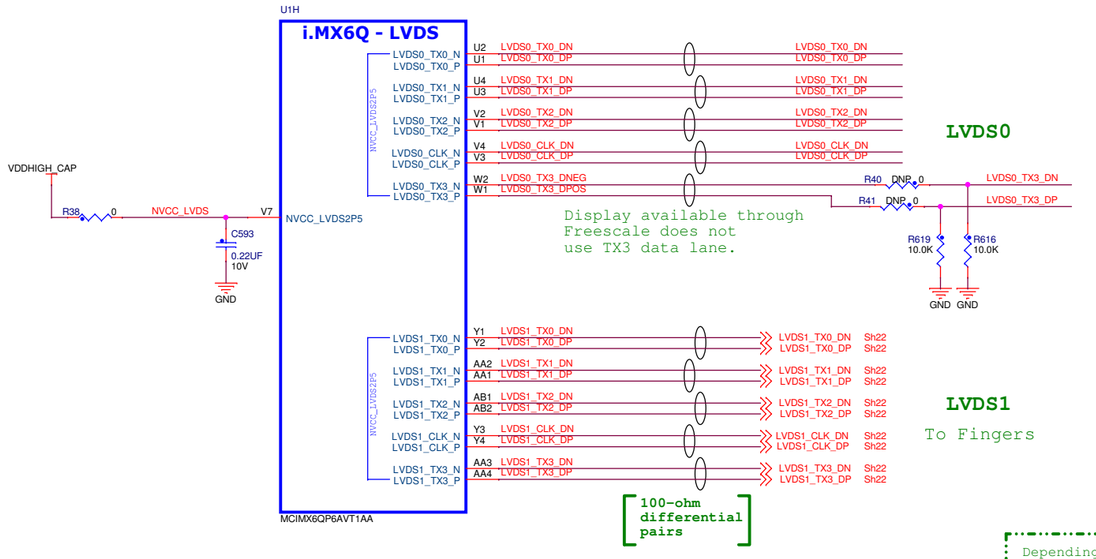
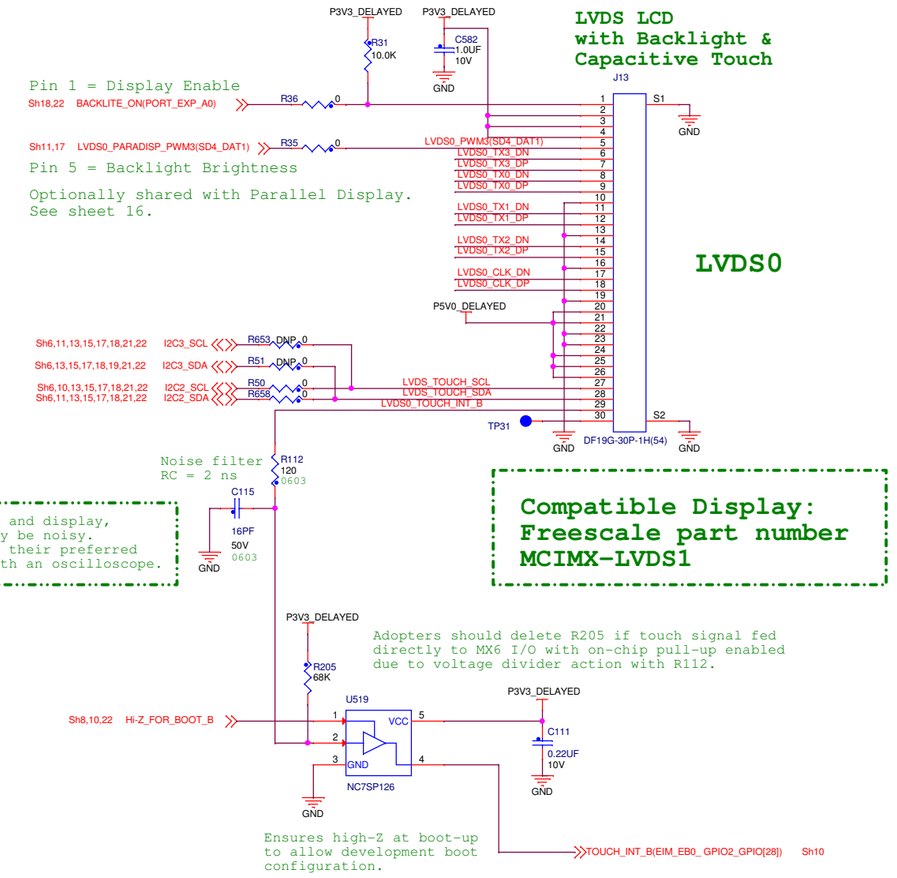
LVDS Displays



NVCC_LVDS2P5 also powers on-chip DDR I/O predrivers, and must be powered whether LVDS is used or not.

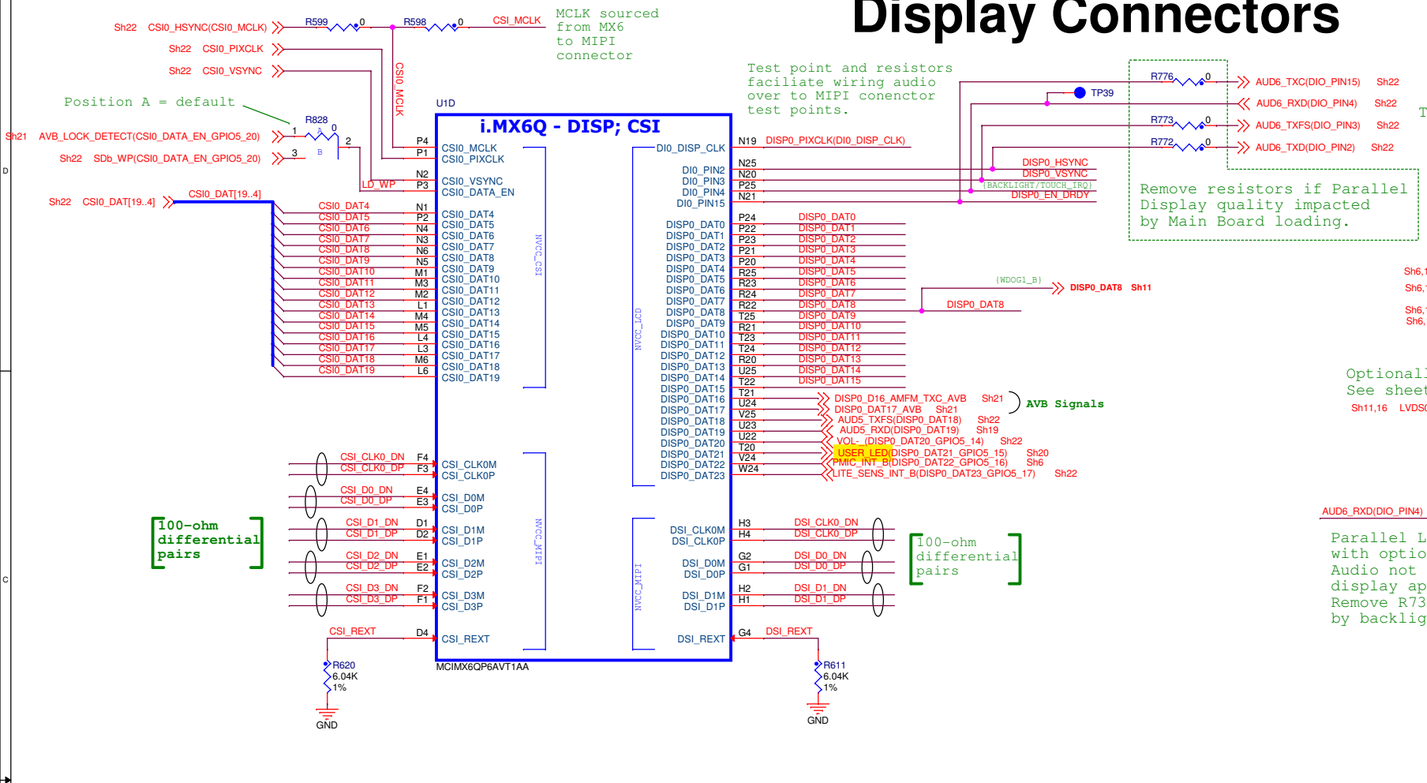


The MCIMX-LVDS1 display with touch can be placed in Sleep through the I2C port. However, INT_B must be driven with a falling edge to wake up the display, which is not allowed due to U1514.

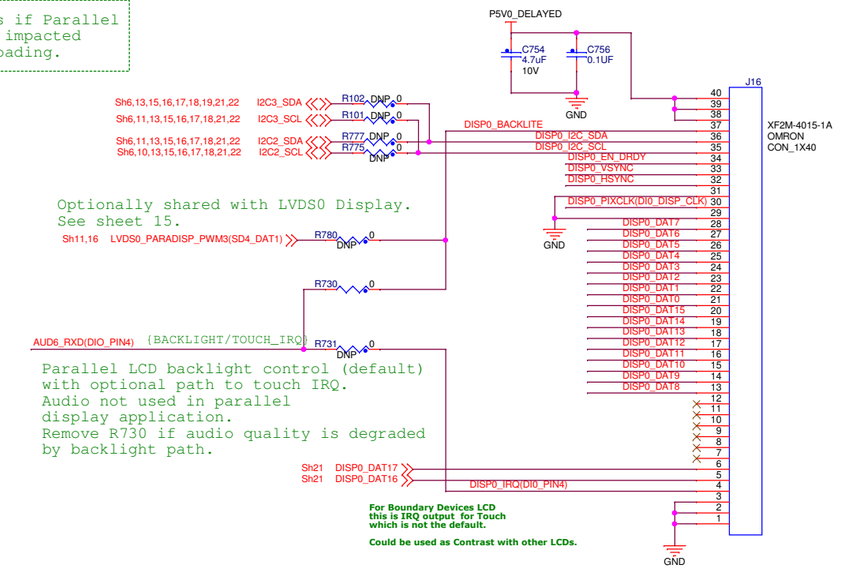
The MCIMX-LVDS1 is not an automotive-grade display. For an automotive system, most likely the display with be placed in sleep and awakened through the I2C port. Adopters should consider their preferred display's requirements.

ICAP Classification:	CP: ___	IUO: ___	PUBI: _X_
Drawing Title:	MCIMX6QPAICPU3		
Page Title:	LVDS Displays		
Size: C	Document Number: SCH-28615 PDF: SPF-28615		Rev: A3
Date: Friday, February 26, 2016	Sheet 16 of 25		

Display Connectors



Parallel Display Connector

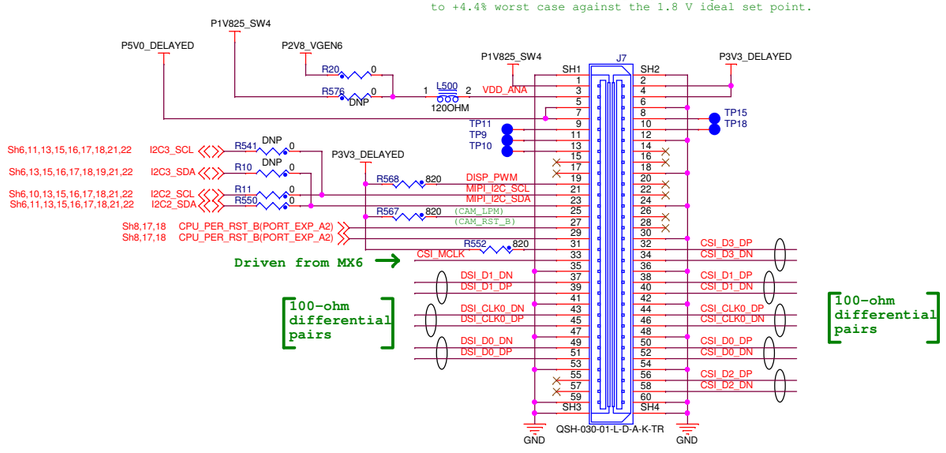


Compatible 7" 800 x 480 LCD and software driver available from Boundary Devices.
If touch is desired, order the LCD with I2C pull-ups removed.

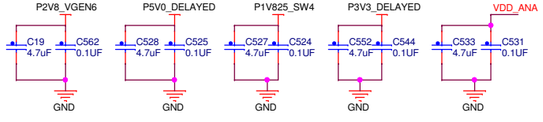
Email: info@boundarydevices.com

MIPI Connector

1.825 V accommodates feed to VIN1 on PMIC.
With the PF0100 tolerance of 3%, this equates to +4.4% worst case against the 1.8 V ideal set point.



Compatible SAMTEC cable HQCD-030-01.72-TTR-TTR-1-N

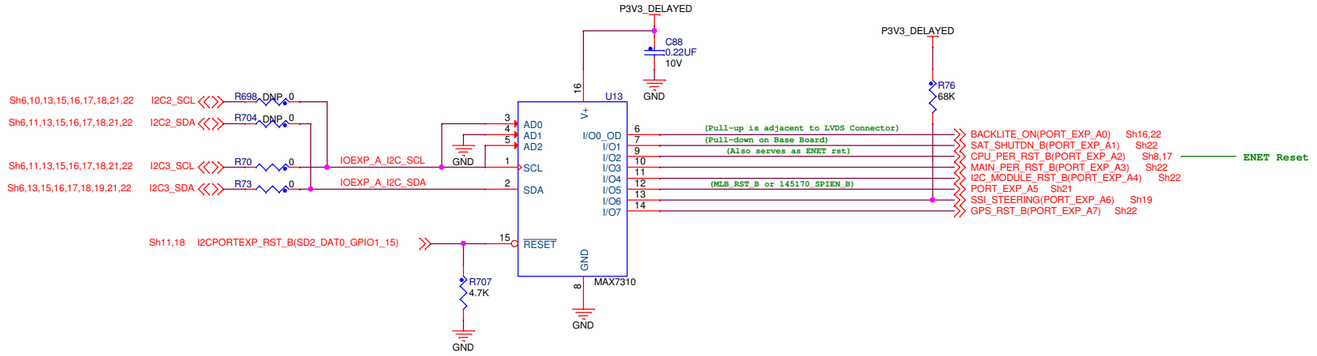


ICAP Classification:	CP: ___	IUO: ___	PUBI: X_
Drawing Title:	MCIMX6QPAICPU3		
Page Title:	Parallel Display, MIPI port		
Size: C	Document Number: SCH-28615 PDF: SPF-28615		Rev: A3
Date: Friday, February 26, 2016	Sheet 17 of 25		

I2C I/O Expanders

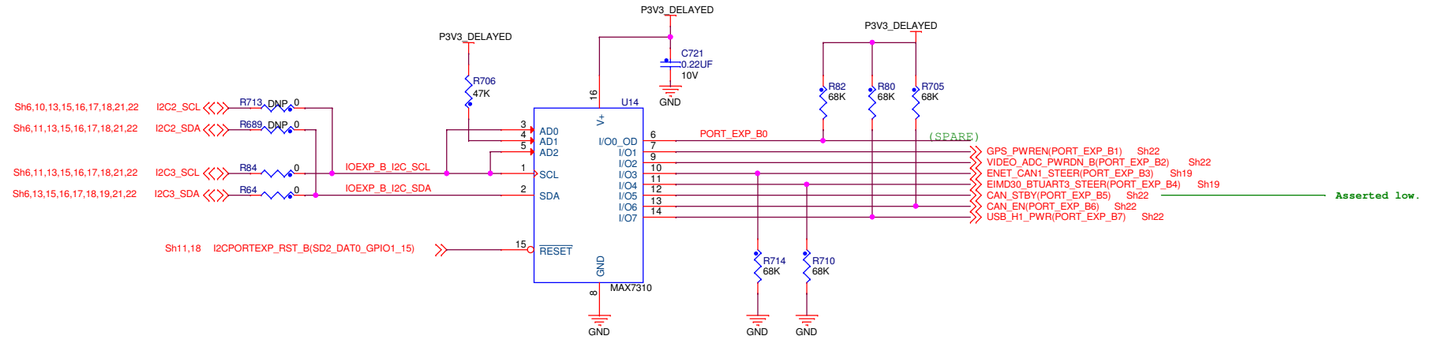
Port Expander A

7-bit Slave Addr(6:0): "0110000"



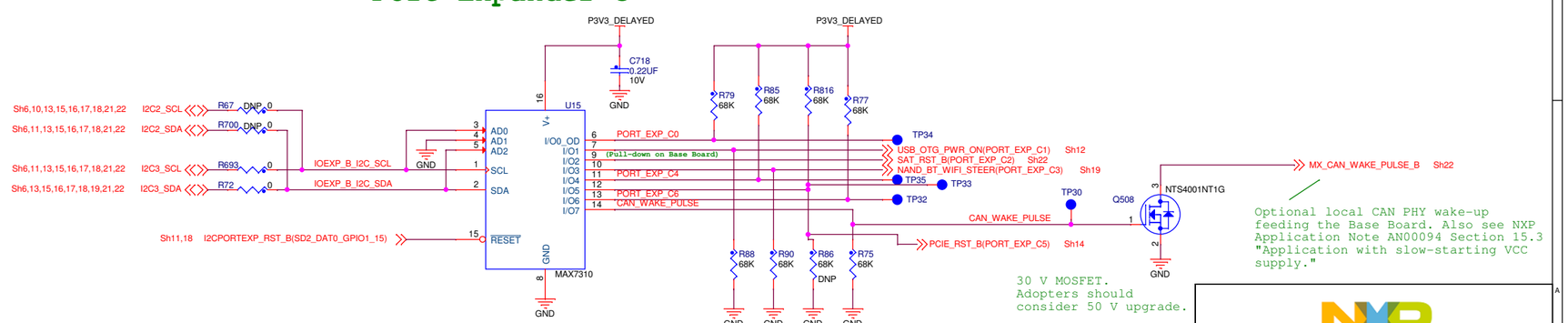
Port Expander B

7-bit Slave Addr(6:0): "0110010"



Port Expander C

7-bit Slave Addr(6:0): "0110100"



ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: **MCIMX6QPAICPU3**

Page Title: **I2C - I/O Expanders**

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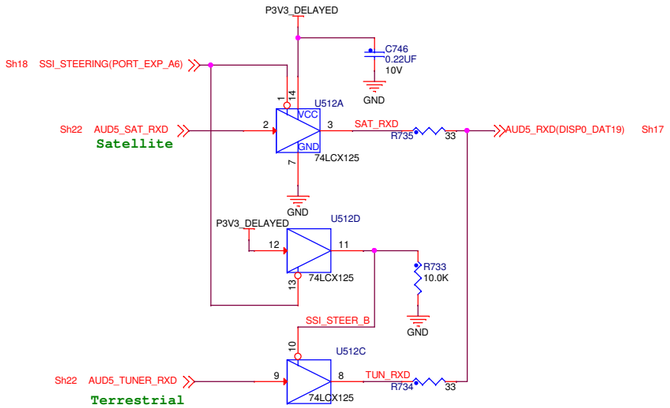
Date: Friday, February 26, 2016 Sheet 18 of 25

Steering Logic

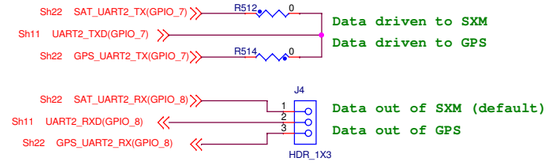
SATELLITE AND TERRESTRIAL TUNER AUDIO DATA STEERING



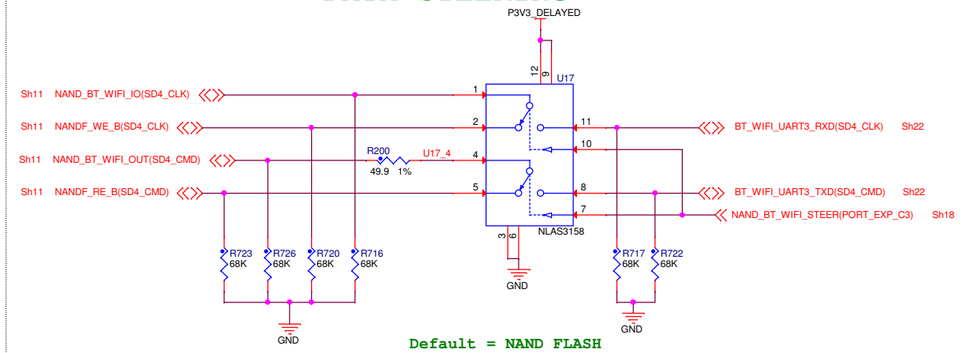
Default = Terrestrial Tuner

Steering logic required due to accommodating a superset of peripherals. For a more robust implementation, Freescale recommends adopters eliminate steering logic especially on the fast signals, since a subset of peripherals will be used in an actual application.

UART2 SHARED BETWEEN GPS AND SATELLITE



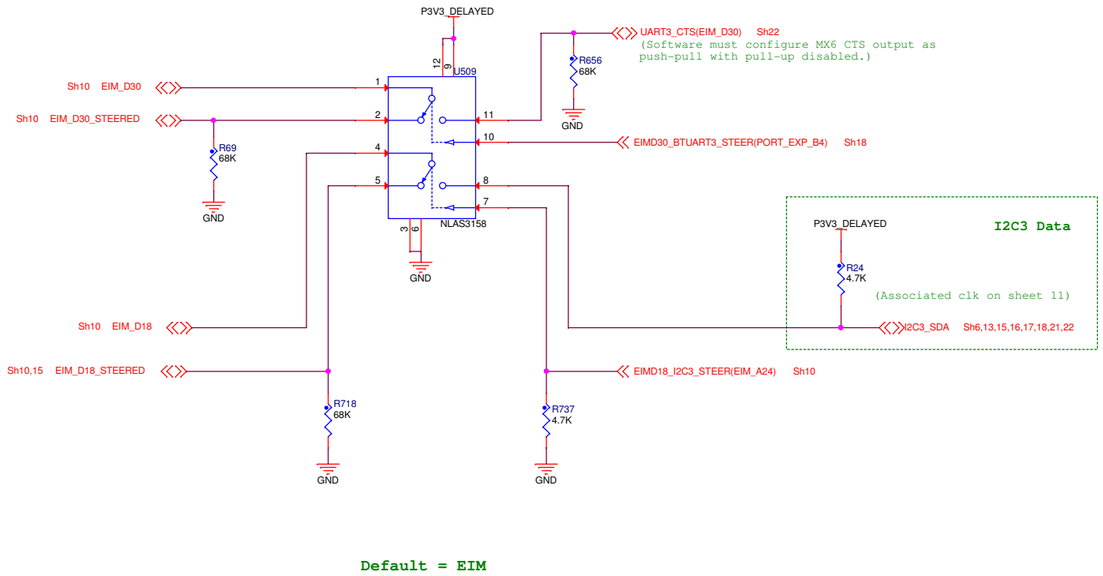
NAND FLASH AND BT_WIFI DATA STEERING



Default = NAND FLASH

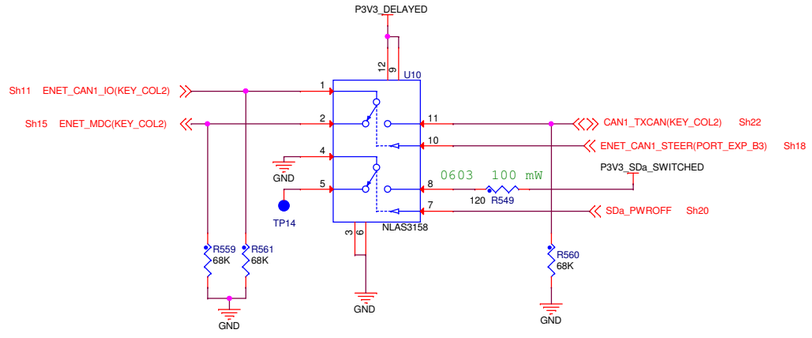
R200 controls reflection on RE_B signal back to processor.

EIM, UART3, and I2C STEERING



Default = EIM

ETHERNET AND CAN DATA STEERING SDa SLOT POWER DISCHARGE FOR RESET



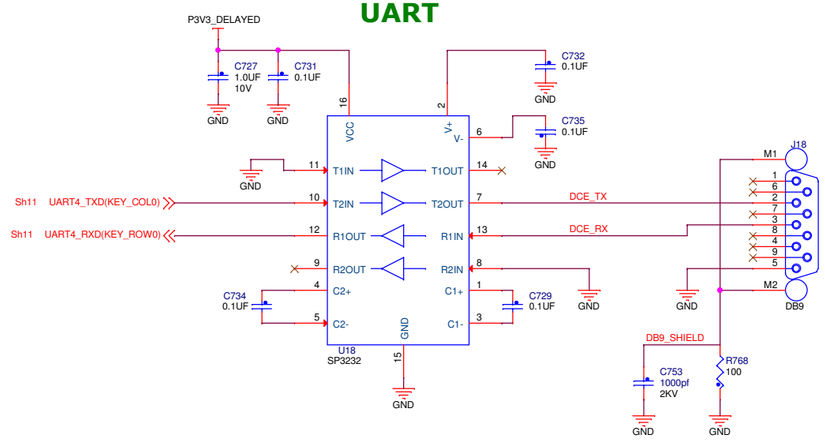
Default = Ethernet

R549 is for discharge current-limiting for SDXC support. Adopters might consider 0805 for operation at temperature extremes, if their available 0603 is not rated to 100 mW.

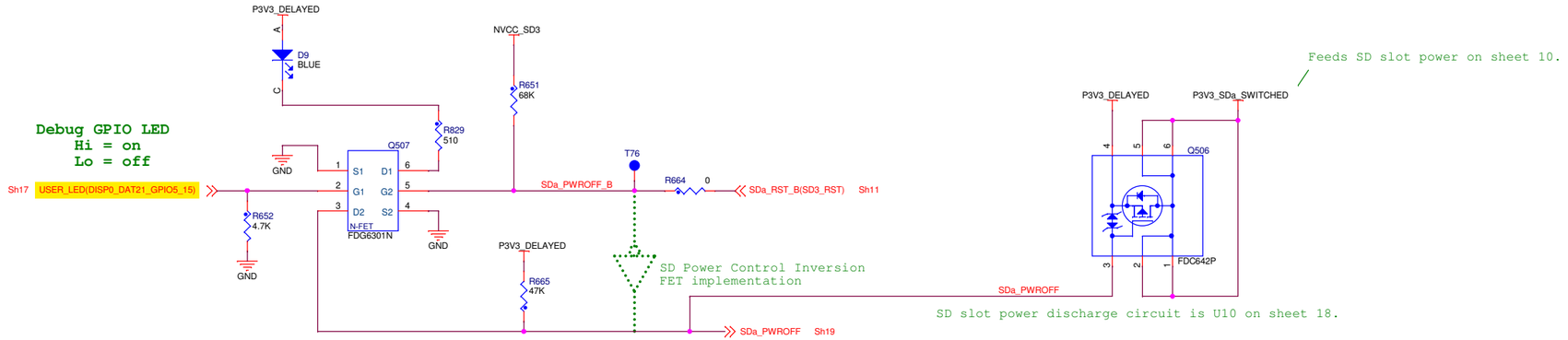
ICAP Classification: CP: ___ IUO: ___ PUBI: X_		
Drawing Title: MCIMX6QPAICPU3		
Page Title: Steering logic		
Size C	Document Number SCH-28615 PDF: SPF-28615	Rev A3
Date: Friday, February 26, 2016	Sheet 19 of 25	

Debug

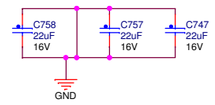
UART



Debug LED and SDXC Power Control Inverter

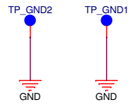


Capacitors as Mechanical Spacers



Place on bottom of board

Ground Test Points



ICAP Classification: CP: ___ IUO: ___ PUBI: _X_		
Drawing Title: MCIMX6QPAICPU3		
Page Title: Debug UART, LED, Test Points		
Size C	Document Number SCH-28615 PDF: SPF-28615	Rev A3
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AVB

SPDT switches accommodate AVB or legacy (MLB) mode for development purposes. Freescale recommends adopters eliminate these switches and unused signals, since use of both AVB and legacy modes is unlikely in an actual application.

Control Low AVB / Control High Legacy — 7X

Sh11,12 USB_OTG_ID(ENET_RX_ER) — 1588 Event 2 Out — TP41

1. USB OTG cable must be disconnected to monitor TP41.
2. Install R585 on sheet 12 to terminate long OTG ID trace for better 1588 Event 2 signal quality.

Local Oscillator, CS2000 Clock Synthesizer, & MLE145170 Configured as Programmable Divider

Sh6,11,13,15,16,17,18,22 I2C2_SDA — R33 0
Sh6,10,13,15,16,17,18,22 I2C2_SCL — R5 0
Sh6,13,15,16,17,18,19,22 I2C3_SDA — R42 0 DNP
Sh6,11,13,15,16,17,18,22 I2C3_SCL — R39 0 DNP
SYNTH_SCL, SYNTH_SDA

U505 CS2000CP: SDA/CDIN, SCL/CCLK, AD0/CS, CLK_IN, XTI/REF_CLK, XTO, VD, CLK_OUT, AUX_OUT, GND

R202 0 — SYNTH_AD0 — GND
TP40 — SDMA Event 1 In, 1588 Event 0 Out

P3V3_DELAYED — C32 0.1UF, C27 1.0UF 10V — SYNTH_VDD — L501 120OHM

P3V3_DELAYED — C766 0.22UF 10V — GND

U521 NC7SZ125L6X: OE, A, GND, VCC, Y, NC — LISTENER_B — SYNTH_24MHZ_BUF — R826 0

SYNTH_24MHZ

P3V3_DELAYED — R2 820 — D20 BLUE — LD_B — R506 68K — Q500 NTS4001NT1G — Lock Detect

AVB_LOCK_DETECT(CSI0_DATA_EN_GPIO5_20) Sh17

24.576 MHz Audio Ref — TP42

TP43 SDMA Event 0 In, 1588 Event 0 In

P3V3_DELAYED — C38 0.22UF — GND

P3V3_DELAYED — R94 68K

U7 MLE145170: D_IN, CLK, ENB, D_OUT, F_IN, OSC_IN, OSC_OUT, VDD, PHI_V, PHI_R, PD_OUT, LD, F_R, REF_OUT, VSS

145170_SPIDATIN
145170_SPICLK
145170_SPIEN_B

Software must configure GPIO function to emulate SPI interface (Bit Bang).

U7 CLK must be stable on power up; see data sheet. R96 value ensures logic low.

R97 4.7K — R96 4.7K

AUDIO_REF_24MHZ — 5170_OSCI — R95 10.0K

MLE145170 divides Audio Ref Clk to achieve frequencies of 8, 4, 1.5, 1.333, 1, 0.75 kHz etc.

This design utilizes a commercial-grade -40 to 85 C device. Freescale suggests consulting the supplier for equivalent automotive-grade device information.

P3V3_DELAYED — R83 L10 120OHM — AUDOSC_VCC — C33 0.1UF — Y1 24.576MHZ (EN, GND, OUT, VCC) — LOC_OSC — R81 0 — LOCAL_AUDIO_24MHZ

Low-jitter timing ref

U502 NLAS3158: Sh11 GPIO_19 — ENET_INT_B(GPIO_19_GPIO4_5) Sh15
AVB_SDMA_IN1_1588_OUT0 — R500 68K — GND
Sh11 GPIO_2 — 145170_SPIDATIN — MLBDAT(GPIO_2) Sh22 — R501 68K — GND
R818 68K — P3V3_DELAYED — AVB_B

U503 NLAS3158: Sh18 PORT_EXP_A5 — MLB_RST_B(PORT_EXP_A5) Sh22
145170_SPIEN_B
Sh11 GPIO_6 — MLBSIG(GPIO_6) Sh22 — R510 68K — GND
145170_SPICLK
Termination on Base Board

U511 NLAS3158: Sh17 DISP0_DAT17_AVB — DISP0_DAT17 Sh17 — R513 68K — GND
AVB_SDMA_IN1_1588_OUT0
Sh17 DISP0_D16_AMFM_TXC_AVB — DISP0_D16 — R515 0 — AMFM_AUD_DISP Sh22 — R516 68K — GND
AVB_SDMA_IN0_1588_IN0

U506 NLAS3158: Sh11 AVB_MLBCLK(ENET_TXD1) — DISP0_DAT16 Sh17 — R518 0
AVB_SDMA_IN0_1588_IN0 — MLBCLK(ENET_TXD1) Sh22 — R511 68K — GND
Sh8,22 AUDIO_REF_24MHZ
SYNCED_AUDIO_24MHZ

Control Low Listener / Control High Head Unit

LISTENER_B — AVB_B — LOCAL_AUDIO_24MHZ

P3V3_DELAYED — R87 68K — AVB_B Sh15 — To ENET SPI Control

SW3 97C02ST

Position 1: Board Config - On = AVB, Off = Legacy
Position 2: Audio Master Clock - On = Listener (Sync'd), Off = Head Unit (local)

ICAP Classification: CP: ___ IUO: ___ PUBI: _X_

Drawing Title: **MCIMX6QPAICPU3**

Page Title: **AVB**

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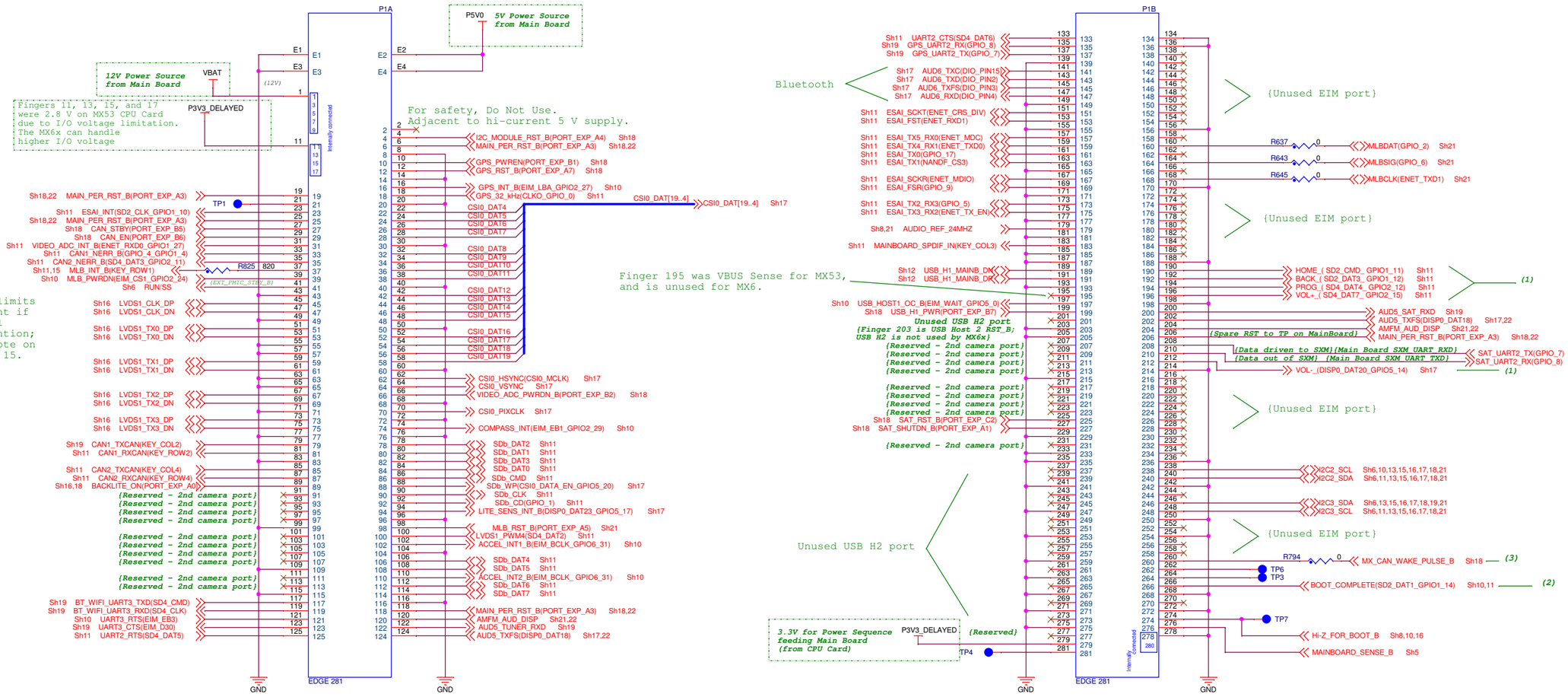
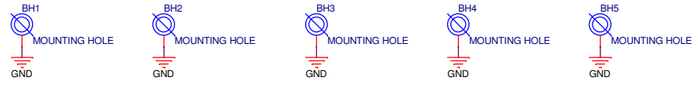
CARD EDGE FINGERS
BOARD-TO-BOARD CONNECTION

Mating connector on Base Board



Plated and Grounded Mounting Holes (130mil hole - 256mil pad)
Label = GND



NOTES:

1 If not Android, can be used as GPIO on Base Board. Base Board schematic cross-reference table does not apply to MX6.

2 Could be used as spare GPIO if SPI NOR is not needed.

3 Could be used as spare open-drain GPIO if not needed for local CAN PHY wake up.

ICAP Classification: CP: ___ IUO: ___ PUBI: X

Drawing Title: **MCIMX6QPAICPU3**

Page Title: **Card Edge Fingers**

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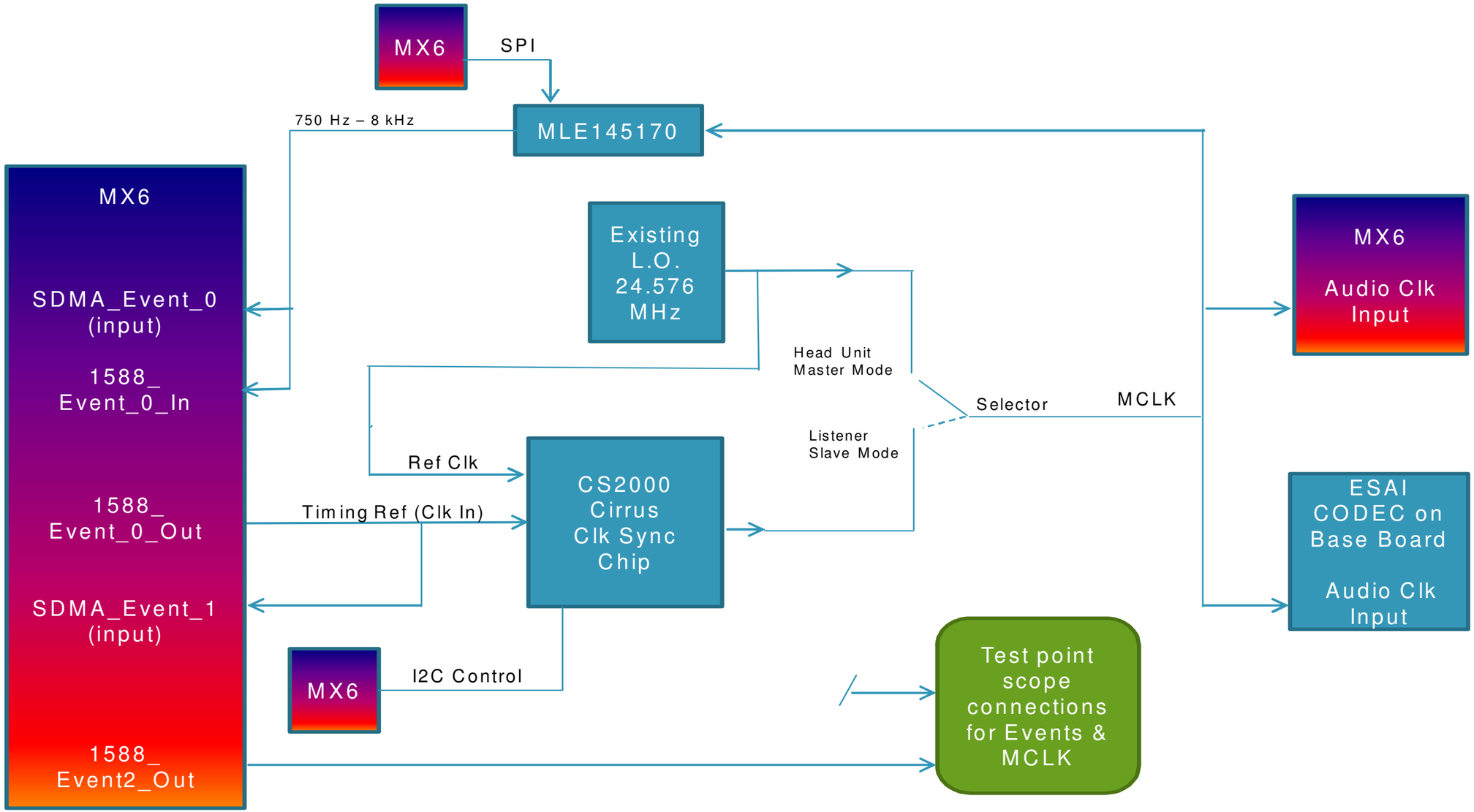
AVB Clock Distribution Block Diagram



AVB/Legacy selector switches not shown for simplicity.

ICAP Classification:	CP: ___ IUO: ___ PUBI: _X_
Drawing Title:	MCIMX6QPAICPU3
Page Title:	AVB Clock Distribution Block Diagram
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A	Sheet 6 - Corrected U524 to U11.	12/09/14

A	Kept as rev A because Agile not signed off yet. File name appended with _Dec10. Sheets 1, 3 - Updated build option note; moved to sh 1. Sheet 6 - Updated U11 to F9 version. Changed net names to facilitate Verilog: SW1, SW2, SW3, SW4 to SW1_IND, etc.	12/10/14

A1	Sheet 1 - Removed prototype build socket note. Sheet 2 - Fixed block diagram by deleting MLB150. Sheet 5 - Increased R505 to 93.1k to increase voltage to 3.2 V. Provides additional margin to allow for U500 and PMIC tolerances, and PMIC drop out per latest data sheet. Sheet 6 - Changed L3, L4, L6, L7 to automotive; these are all same part now. Added note on VGEN1 net due to possible PMIC change. Added power table and note on PMIC_STBY_REQ. Sheet 7 - Upper right note updated. Sheet 8 - Clarified SPI NOR note on S3. Sheet 10 - Modified SPI NOR flash note. Sheet 11 - Changed R838 to DNP to avoid reboot with OBDS. WDOG is now option; updated note. Sheet 25 - Added PMIC info sheet.	2/27/15

A2	Throughout doc - Changed title blocks to NXP. Changed classification to "Public Information". Changed U1 placeholder Quad with QuadPlus. Sheet 1 - Removed "Preliminary", BCM Switch Card, and SX CPU Card. Sheet 12 - Removed VDDUSB_CAP clamp-diode note. Sheet 13 - Added backfeed note. Sheet 14 - Updated PCIe note at top of sheet. Sheet 16 - Updated LVDS connector part number. Sheet 25 - Updated PMIC info (BOOST is ON but not used)	1/29/16

A3	Sheets 7, 15, 21 - Re-sync'd 16 capacitor footprints with legacy layout: 0201_CC_012SM_NSP.	2/26/16

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%.
   All voltages are DC.
   All polarized capacitors are aluminum electrolytic.

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals
   Green text Denotes - Extra Notes to be considered.

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

AVB SIGNAL ASSIGNMENT

v2

Ref	AVB Associated Name	MX6Q Ball & ALT Mode	Comment
TP43	ENET_1588_EVENT0_IN	ENET_TXD1 (ALT4)	Legacy system function = MLB CLK
TP40	ENET_1588_EVENT0_OUT	GPIO_19 (ALT1)	Legacy system function = ENET INT_B
TP41	ENET_1588_EVENT2_OUT	ENET_RX_ER (ALT4)	Legacy system function = USB_OTG_ID
TP43	SDMA Event0	DISP0_DAT16 (ALT4)	Legacy system function = RGB Disp (cluster), AM-FM Aud Clk
TP40	SDMA Event1	DISP0_DAT17(ALT4)	Legacy system function = RGB Disp (cluster)
TP42	MCLK, 24.576 MHz	CLK2_P/N config'd as input	Audio master clock
--	Programmable Divider SPI SS_B	(Port_Exp_A5 for bit bang)	Legacy system function = MLB_RST_B from I2C port exp.
--	Programmable Divider SPI SCLK	GPIO_6 (ALT5) for bit bang	Legacy system function = MLBSIG
--	Programmable Divider SPI MOSI	GPIO_2 (ALT 5) for bit bang	Legacy system function = MLBDAT

ICAP Classification: CP: ___ IUO: ___ PUBI: X_

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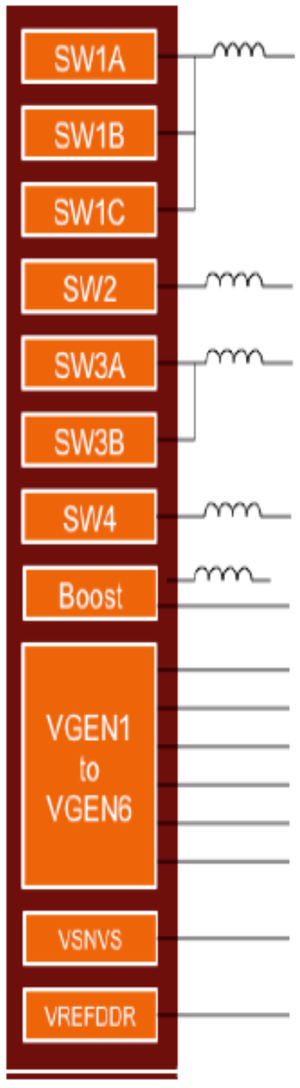
Customized Programming Information

Orderable part number	
SMPF0100F9AZES	Bulk
SMPF0100F9AZESR2	Tape and reel
Automotive AEC100-Grade 3	

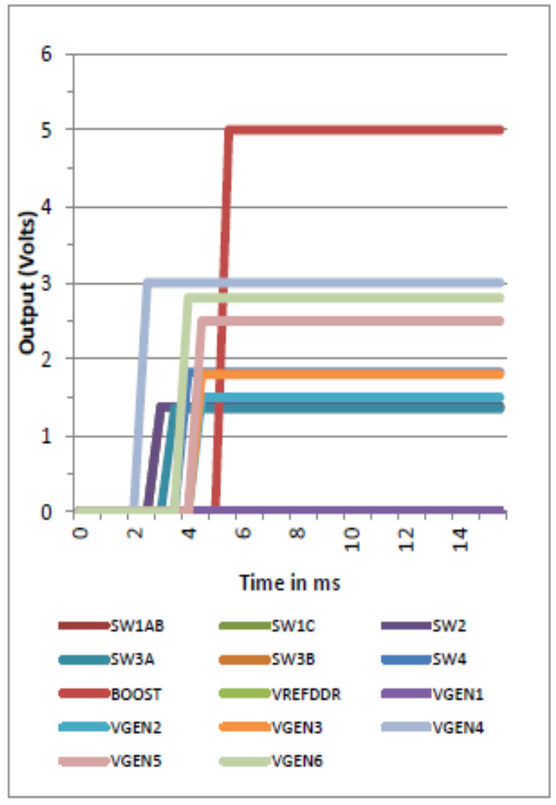
SMPF0100

MPU - ONLY

ES SUFFIX (WF-TYPE)
56 QFN 8x8
0.5MM PITCH



	VOUT (V)	IMAX (mA/A)	Sequence*
SW1A, SW1B, SW1C	1.375V	4.5A	5
SW2	1.375V	2.0A	5
SW3A, SW3B	1.350V	2.5A	6
SW4	1.825V	1.0A	7
Boost	5.00V	600mA	10
VGEN1 to VGEN6	1.20V	100mA	0
	1.50V	250mA	8
	1.8V	100mA	8
	3.0V	350mA	4
	2.5V	100mA	8
	2.8V	200mA	7
VSNVS	3.0V	400uA	
VREFDDR	0.68V	10mA	6



PMIC Regulator	Voltage	Load
VSNVS	3.0	i.MX SNVS, pwr control, rst chips
SW1	1.375	i.MX SoC core
SW2	1.375	i.MX ARM core
SW3	1.35	DRAM
SW4	1.825	MIPI, VGEN1/2
SWBST	0	
VGEN1	0	
VGEN2	1.5	PCIe
VGEN3	1.8	i.MX SD3 I/O
VGEN4	3.0	i.MX VDDHIGH
VGEN5	2.5	Pwr LED, Gate 5 V delay
VGEN6	2.8	MIPI, Gate 3.3 V delay
VREFDDR	0.675	DRAM Vref

I2C address: 0x08
SWDVS_CLK: 25mV step each 4us
PWRON_CNF: Standard (High-ON, Low-Off)
PWRGD_EN: Standard RESETBMCU
SEQ_CLK_SPEED: 0.5ms
SWx_FREQ: 2MHz

* Sequence 0 indicates regulator is off

ICAP Classification: CP: ___ IUO: ___ PUBI: _X_

Drawing Title: **MCIMX6QPAICPU3**

Page Title: **PMIC Voltage & Sequence Notes**

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