**CMPE 200 HW#3**

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Consider a simple single-cycle implementation of MIPS ISA shown on Page 3. The operation times for the major functional components for this processor are as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| **Component** | **Latency (ns)** | **Component** | **Latency (ns)** |
| ALU | 10 | Memory (IM/DM) Read/Write | 15 |
| Adder | 8 | PC Register Read/Write | 2 |
| ALU Control (decoder) | 2 | Register File Read | 7 |
| Shifter | 3 | Register File Write | 5 |
| Main Control (decoder) | 4 | 2-1 MUX | 2 |
| Sign/zero Extender | 3 | Logic (1 or more levels of gates) | 1 |

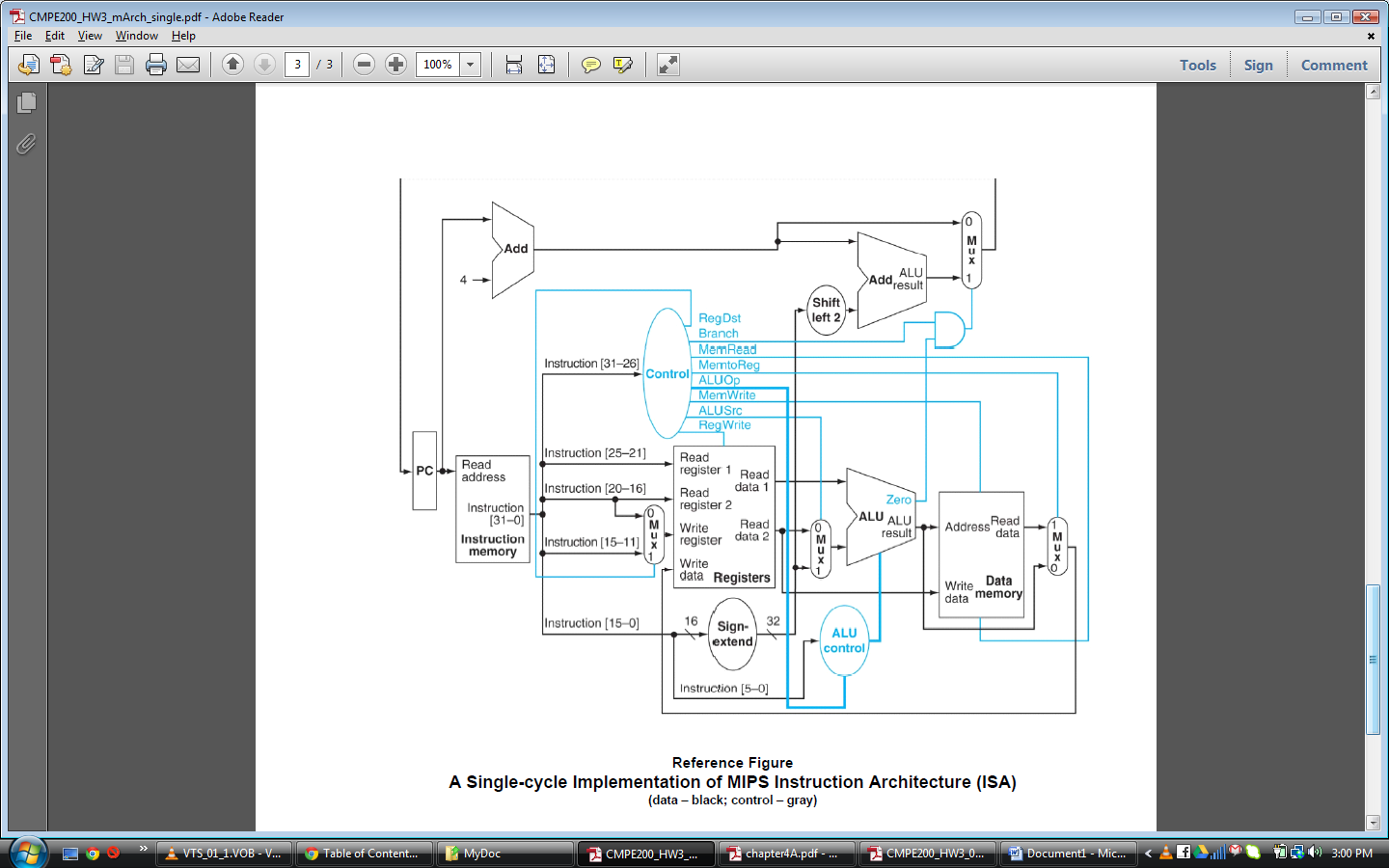
In this design the clock cycle is determined by the longest possible path in the processor. The critical paths for the different instruction types that need to be considered are: R-type, LW (load-word), and SW (store-word). All instructions have the same instruction fetch and decode steps. The basic register-transfer actions of the instructions are:

Fetch/Decode: Instruction IMEM[PC];

R-type: R[rd] R[rs] op R[rt]; PC PC + 4;

LW: R[rt] DMEM[ R[rs] + signext(offset)]; PC PC +4;

SW: DMEM[ R[rs] + signext(offset)] R[rt]; PC PC +4;



1. ***In the table below, indicate the components (names of the functional blocks) that determine the critical path for the respective instruction, in the order that the critical path occurs. If a component is used, but not part of the critical path of the instruction (i.e., it is used in parallel with another slower component), it should not be in the table. The register file is used for reading and writing; it will appear twice for some instructions. All instruction begin by reading the PC register with a latency of 2 ns.***

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction Type** | **Hardware Component Used By The Instruction** | | | | | | | | | |
| R- Type | PC | IM Read | Register File Read | 2-1 Mux | ALU | 2-1 Mux | Register File Write | - | - | - |
| LW | PC | IM Read | Register File Read | 2-1 Mux | ALU | DM Read | 2-1 Mux | Register File Write | - | - |
| SW | PC | IM Read | Register File Read | 2-1 Mux | ALU | DM Write | - | - | - | - |

1. ***Place the latencies of the components that you have decided for the critical path of each instruction in the table below, and compute the total latency for each type if instruction.***

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction Type** | **Hardware Component Used By The Instruction** | | | | | | | | | | **Total (ns)** |
| R- Type | 2 | 15 | 7 | 2 | 10 | 2 | 5 | - | - | - |  |
| LW | 2 | 15 | 7 | 2 | 10 | 15 | 2 | 5 | - | - |  |
| SW | 2 | 15 | 7 | 2 | 10 | 15 | - | - | - | - |  |

1. ***Based on*** ***the results obtained from (2), answer the following questions:***
   1. ***Given the data path latencies above, which instruction determines the overall processor’s critical path?***

***Ans:*** The **LW instruction** determines the overall processor’s critical path as it takes the maximum time(58ns) to complete its execution

* 1. ***What will be the resultant clock cycle time of the processor based on the critical path instruction?***

***Ans:*** The resultant clock cycle time is **58ns**

* 1. ***What clock frequency will the processor run?***

***Ans:*** *Clock**frequency= 1/(clock cycle time) = 1/(58ns) =* ***17.2 MHz***